深圳显旸光电科技有限公司
Shenzhen Xianyang Optoelectronic Technology Co., Ltd

PRODUCT SPECIFICATION

MODULE NO: (模组型号) XY060HD03-01

CUSTOMER：(客户)

APPROVED BY CUSTOMER 客户签署栏	
Approved by 审核	Remark 备注

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	电 子	结 构	

REVISION RECORD

REV NO. 版本	CONTENTS 内容	REV DATE 修改日期	REMARKS 注释
Preliminary	First release	2020-11-25	

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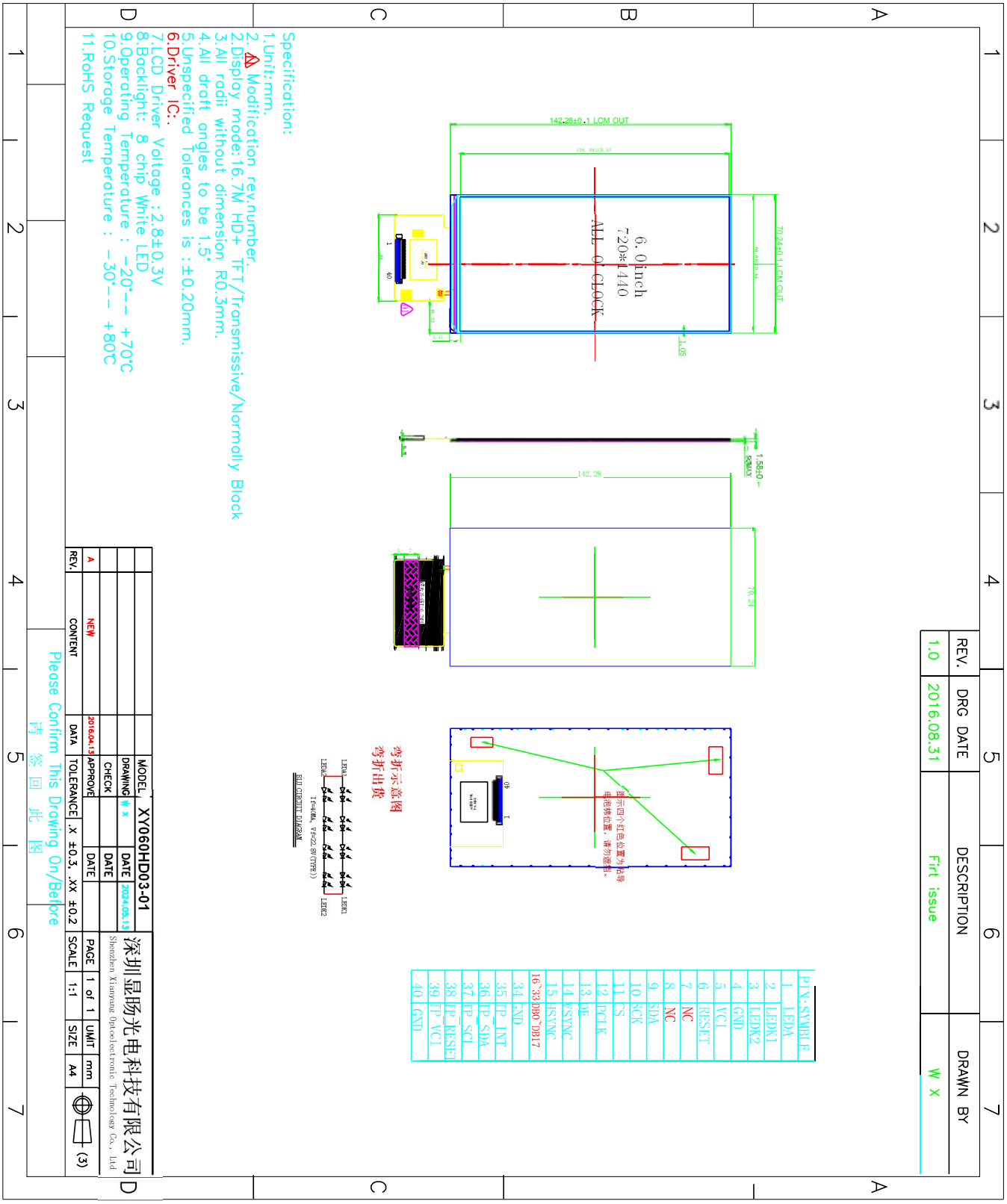
1. GENERAL INFORMATION

基本描述

Item 项目	Contents 内容	Unit 单位
LCD Type LCD 类型	TFT-LCD /TRANSMISSVIE	-
TP Structure TP 结构	--	-
Number of Dots 点阵	720(R.G.B)*1440	Dot
Outline dimensions 外形尺寸	--	mm^3
Active area 有效区域	68.04(W)* 136.08(H)	mm^2
TP Viewing area（宽×高） TP 可视区（W×H）	(有电容 TP 配,可出总成)	mm^2
Pixel pitch 像素	0.0945*0.0945	mm^2
Module size 模组尺寸	6.0	inch
Viewing direction 视角方向	ALL O'CLOCK/IPS MODE	O'clock
Backlight type 背光类型	White LED(16*LED)	-
TP Driver IC TP 驱动 IC	--	-
Interface type 接口类型	SPI+RGB/TTL	-
LCM Input voltage 模组输入电压	2.8~3.3	V
All material of MODULE and process measure up to ROHS Europe		

2. MODULE OUTLINE DRAWING 产品外形图



3. INTERFACE DESCRIPTION

Pin No.	Symbol	Description
1	LEDA	LED Positive
2	LEDK1	LED Positive
3	LEDK2	LED Negative
4	GND	Power ground.
5	VCI	Power Supply 2.8~3.3V
6	RESET	Reset pin,low active.
7~8	NC	NO connect.
9	SDA	Serial interface DATA Input/Output.
10	SCK	Serial interface Clock Input.
11	CS	Chip select signal for SPI interface operation.
12	PCLK	Pixel clock signal in RGB I/F.
13	DE	Data enable signal in RGB I/F.
14	VSYNC	Vertical sync. Signal in RGB I/F.
15	HSYNC	Horizontal sync. Signal in RGB I/F.
16~33	DB0~DB17~R7	Data Bus
34	GND	Power ground.
35	TP_INT/NC	TP pin/NC
36	TP_SDA/NC	TP pin/NC
37	TP_SCL/NC	TP pin/NC
38	TP_RESET/NC	TP pin/NC
39	TP_VCI/NC	TP pin/NC
40	GND	Power ground.

*** 所有 I/O 支持 2.8~3.3V.**

***TTL 屏显示或熄屏不显示,请将 VCC ON 或 OFF.不要使用对屏 SLEEP 或 EXIT SLEEP.**

4. BACKLIGHT CHARACTERISTICS 背光电气特性

Item 项目	Symbol 符号	Min 最小值	Typ 中间值	Max 最大值	Unit 单位	Condition 条件
Forward voltage 正向电压	Vf	23.2	25.6	27.2	V（伏）	If=40mA, Ta=25℃
Number of LED LED 灯数	-	16			Piece（颗）	-
Connection mode 连接类型	S/P	Series and Parallel(串联与并联）			-	-

5. ABSOLUTE MAXIMUM RATINGS 极限参数(IC)

Parameter 参数	**Symbol** 符号	**Min** 最小值	**Max** 最大值	**Unit** 单位
Supply voltage for logic 逻辑电压 I/O	IOVCC	-0.3	+4.6	V
Input voltage for analog circuit 输入模拟电压	VCC	-0.3	+6.6	V
Operating temperature 操作温度	TOP	-20	70	。C
Storage temperature 存储温度	TST	-30	80	。C
Humidity 湿度	RH	-	90%(60。C)	RH

6. ELECTRICAL CHARACTERISTICS 模块电气特性

Parameter 参数	Symbol 符号	Min 最小指	Typ 典型值	Max 最大值	Unit 单位
Analog operating voltage 模拟电压	VCC	2.7	2.8	2.9	V
Logic operating voltage 逻辑电压	IOVCC	1.7	1.8	1.9	V
Input voltage “H”level 输入高电平	V_{IH}	0.7 IOVCC	-	IOVCC	V
Input voltage “L”level 输入低电平	V_{IL}	GND	-	0.3 IOVCC	V
Output voltage “H”level 输出高电平	V_{OH}	0.8IOVCC	-	IOVCC	V
Output voltage “L”level 输出低电平	V_{OL}	GND	-	0.2 IOVCC	V

7. OPTICAL CHAYACTERISTICS 光学特性

Item 项目	Symbol 符号	Condition 条件	Min 最小值	Typ 典型值	Max 最大值	Unit 单位	Remark 注释	Note 备注
Response time 响应时间	Tr+Tf	Θ=0° Ø=0° Ta=25°C	-	30	40	ms	FIG1	1
Contrast ratio 对比度	Cr		500	-	-	-	FIG2	2
Color gamut 饱和度	S(%)		-	70	-	%	-	-
Luminance uniformity 均匀度	δWHITE		80	-	-	%	FIG2	3
Viewing angle range 视角范围	Θx+	CR≧10 Ta=25°C	-	85	-	deg	FIG3	4
	Θx-		-	85	-	deg	FIG3	
	Θy+		-	85	-	deg	FIG3	
	Θy-		-	85	-	deg	FIG3	
LCM Luminance LCM 亮度	Lv	Θ=0° Ø=0° Ta=25°C	300	340	-	Cd/m²	FIG2	5
CIE (X,Y) Chromaticity 色度坐标	White(X)		0.26	0.29	0.32	-	FIG2	6
	White(Y)		0.27	0.30	0.33	-		

Note1.Response time is the time required for the display to transition from White to black(Rise Time,Tr)and from black to white(Decay Time,Tf).For additional information see FIG1...

备注 1.响应时间是 Tr（上升时间）与Tf（下降时间）的和，Tr 指显示黑色画面转为显示白色画面需要时间，Tf 指显示白色画面转为显示黑色画面需要时间，详见 FIG1.。

Note2.contrast Ratio(CR) is defined mathematically by the following formula ,For more information see

FIG2.

Contrast Ratio(CR)=Average Surface Luminance with all white pixels/ Average Surface Luminance with all black pixels

备注 2.对比度是由以下公式计算所得。详见 FIG2.

对比度=显示白色画面时平均表面亮度（P1，P2,……)/显示黑色画面时平均表面亮度（P1，P2,……)

Note3.The uniformity in surface luminance(WHITE) is determined by measuring luminance at eath test position,and then dividing the maximum luminance of all white pixels by minimum luminance of all white pixels,For more information seeFIG2.

WHITE=Minimum Surface Luminance with all white pixels(P1,P2,.....)/Maximum Surface Luminance with all white pixels(P1,P2,.....)

备注3.均匀度是在显示白色画面时，测试P1到P9 的亮度，然后再用9个点亮度的最小值除以最大值。详见FIG2.。

均匀度=白色画面下表面亮度最小值（P1，P2,……)/白色画面下表面亮度最大值（P1，P2,……)

Note4.Viewing angle is the angel at which contrast ratio is greater than a specific value.For TET module,the specific value of contrast ratio is 10.For monochrome and color stn module,the specific value of contrast ratio is2.The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface.For more information see FIG3

备注 4.视角指对比度大于等于一个特定值时的可视范围，对 TFT 屏，对比对特定值为 10，对黑白屏 CSTN 屏，对比度特定值为 2，视角由横轴（X 轴），竖轴（Y 轴）同Z 轴（垂直与 LCD 表面）之间的夹角来定义，详见 FIG3.。

Note5. Surface luminance is the LCD surface luminance with all white pixels,For more information see FIG2.

LV=Average Surface Luminance with all white pixels(P1,P2,.....)

备注 5.表面亮度是在显示白色画面时，测试的亮度值，详见 FIG2.

Lv=平均的表面亮度（P1，P2,……)

Note6.CIE(X,Y)chromaticity is the Center point value.For more information see FIG2.

备注 6.选择中心点，分别测试 X，Y 值，详见 FIG2.。

Note7.For Viewing angle and response time testing,the testing date is base on Autronic-Melchers’s ConScope.Series instruments.For contrast ratio,Surface Luminance,Luminance uniformity and CIE,the testing date is base on CS-2000 photo detector.

备注 7.视角和响应时间，测试数据基于Autronil Melchers’s Conoscope 系列，而对比度，表面亮度，均匀度 CIE 坐标，测试数据基于 CS-2000 photo detector。

Note8.For TN type TFT transmissive module,Gray scale reverse occurs in the direction of panel viewing angle

备注 8.TN 型 TFT 全透产品，在视角方向会发生灰度反转。

FIG1. The definition of Response time

响应时间定义

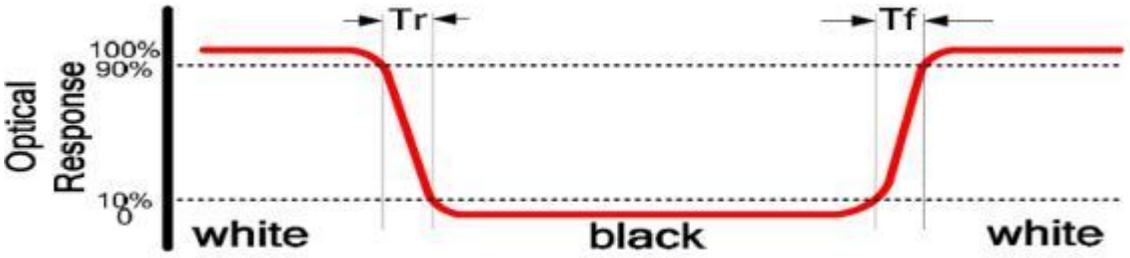


FIG2. Measuring method for Contrast ratio,surface luminance,Luminance uniformity,CIE(X,Y)chromaticity.

对比度，表面亮度，均匀度，CIE 坐标测试方法

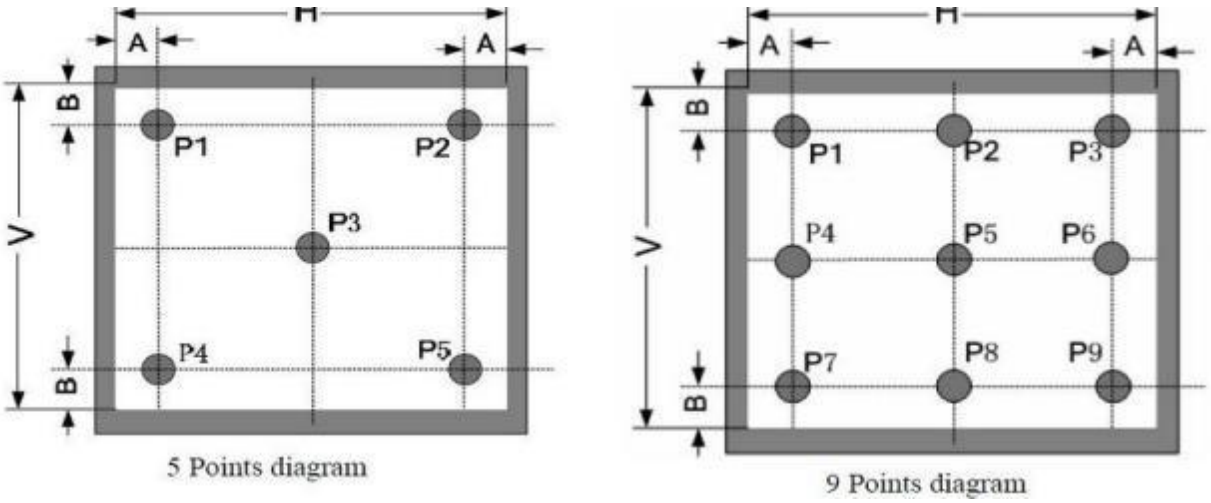
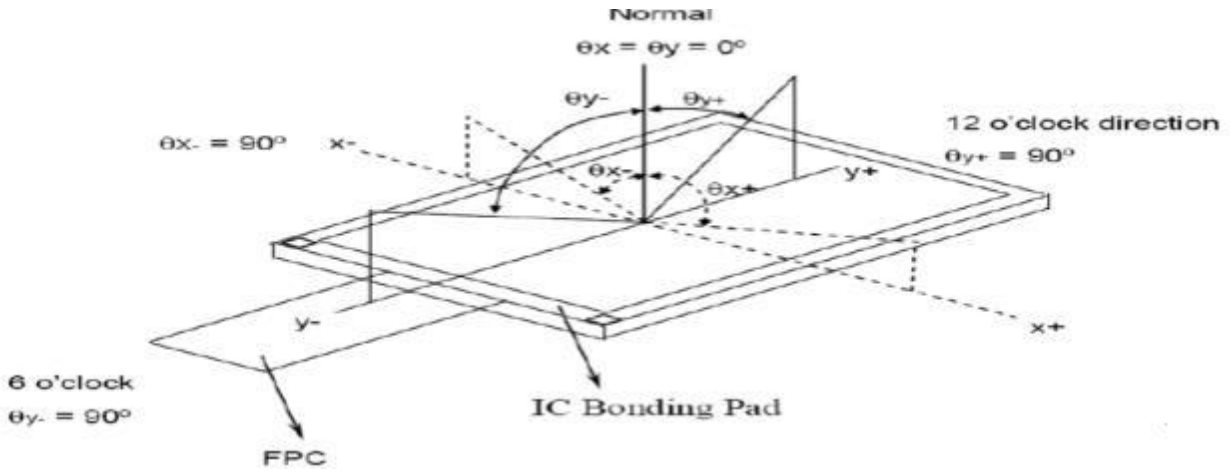


FIG3 The definition of viewing angle
视角定义



8. READ/WRITE TIMING

读/写时序

7.3.2.7 High-speed data-clock timing

This section specifies the required timings on the high-speed signaling interface independent of the electrical characteristics of the signal. The PHY is a source synchronous interface in the Forward direction.

The Master side of the Link shall send a differential clock signal to the Slave side to be used for data sampling. This signal shall be a DDR (half-rate) clock and shall have one transition per data bit time. All timing relationships required for correct data sampling are defined relative to the clock transitions. Therefore, implementations may use frequency spreading modulation on the clock to reduce EMI.

The DDR clock signal shall maintain a quadrature phase relationship to the data signal. Data shall be sampled on both the rising and falling edges of the Clock signal. The term "rising edge" means "rising edge of the differential signal, i.e. CP – CN, and similarly for "falling edge". Therefore, the period of the Clock signal shall be the sum of two successive instantaneous data bit times. This relationship is shown in Figure 7.8.

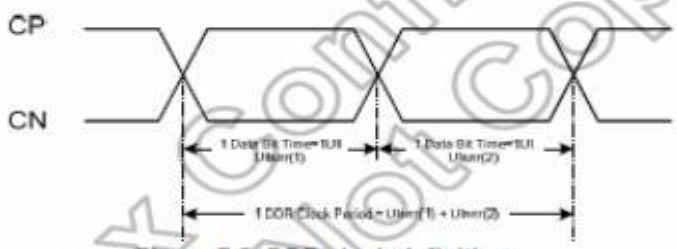


Figure 7.5: DDR clock definition

The same clock source is used to generate the DDR Clock and launch the serial data. Since the Clock and Data signals propagate together over a channel of specified skew, the Clock may be used directly to sample the Data lines in the receiver. Such a system can accommodate large instantaneous variations in UI.

The allowed instantaneous UI variation can cause large, instantaneous data rate variations. Therefore, devices shall either accommodate these instantaneous variations with appropriate FIFO logic outside of the PHY or provide an accurate clock source to the Lane Module to eliminate these instantaneous variations.

The UI_{INST} specifications for the Clock signal are summarized in Table 7.11.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
UI instantaneous	UI_{INST}	-	-	12.5	ns	(1), (2), (3), (4), (5)

Note: (1) This value corresponds to a minimum 80 Mbps data rate.
(2) The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.
(3) Maximum total bit rate is 2Gbps of 4 data lanes 24-bit data format/ 1.5Gbps of 4 data lane 18-bit data format/ 1.33Gbps of 4 data lane 16-bit data format.

Table 7.11: Reverse HS data transmission timing parameters

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 7.9. Data is launched in a quadrature relationship to the clock such that the Clock signal edge may be used directly by the receiver to sample the received data.

The transmitter shall ensure that a rising edge of the DDR clock is sent during the first payload bit of a transmission burst such that the first payload bit can be sampled by the receiver on the rising clock edge, the second bit can be sampled on the falling edge, and all following bits can be sampled on alternating rising and falling edges.

All timing values are measured with respect to the actual observed crossing of the Clock differential signal. The effects due to variations in this level are included in the clock to data timing budget.

Receiver input offset and threshold effects shall be accounted as part of the receiver setup and hold parameters.

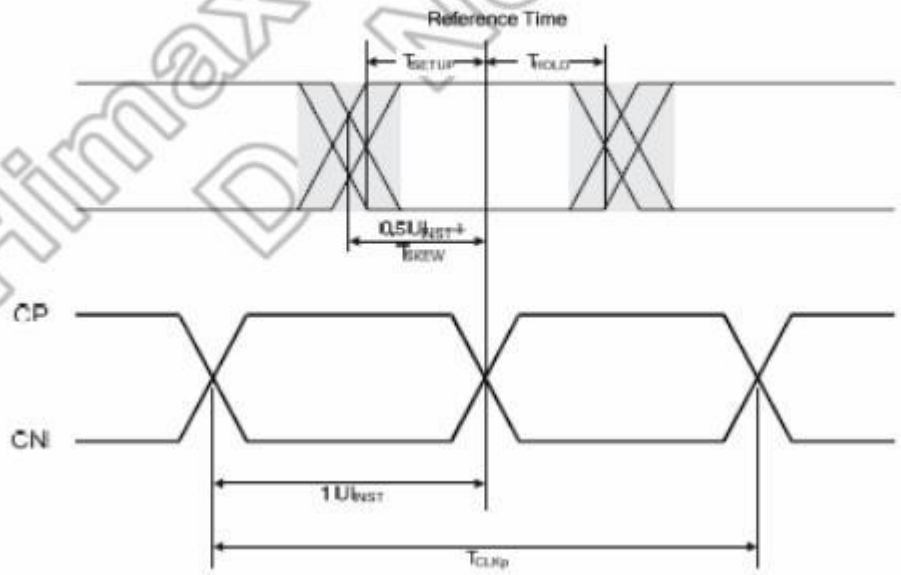


Figure 7.6: Data to clock timing definitions

NOTE: This section is only for reference,Detailsplease refer to the IC specification .
备注：本节仅供参考, 详细信息请参阅 IC 规格书

9. RESET INPUT TIMING 复位时序

5.1.1 Tearing effect line timing

The Tearing Effect signal is described below:

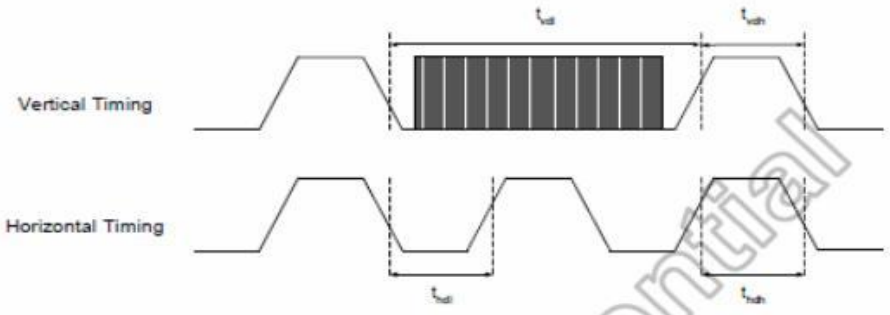


Figure 5.3: Tearing effect output line –tearing effect line timing

Idle Mode Off (Resolution 800x1280 RGB, Frame Rate = 60 Hz)

Symbol	Parameter	Min.	Max.	Unit
tvdl	Vertical Timing Low Duration	15	-	ms
tvdh	Vertical Timing High Duration	VFP+VHP+VBP	-	us
tr	Rise time	-	15	ns
tf	Fall time	-	15	ns

Note: The timings in Table 5.1 apply when MADCTL ML=0 and ML=1

Table 5.1: AC characteristics of tearing effect signal

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

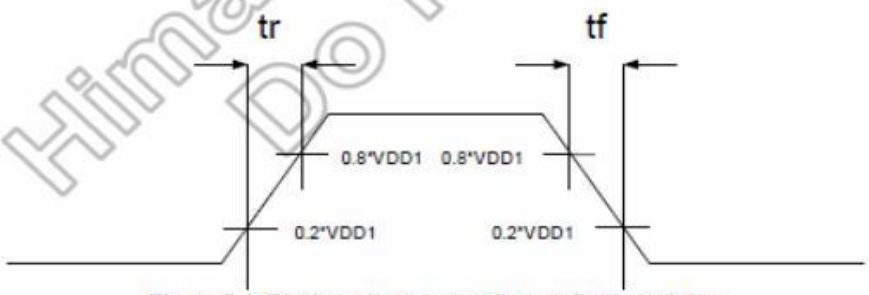


Figure 5.4: Tearing effect output line–definition of tf, tr

NOTE: This section is only for reference,Detailsplease refer to the IC specification. 备注：本节仅供参考,详细信息请参阅 IC 规格书。

10. RELIABILITY TEST CONDITIONS 可靠性试验条件

NO.	Test Item	Test Condition	Inspection after test
1	High Temperature Storage 高温存储测试	80℃±2℃/96 hours	Inspection after 2~4 hours storage at room temperature ,the sample shall be free from defects: 实验结束后，已测试的 LCD 样品必须在室内正常温湿度环境下放置，2~4 小时以上才能进行功能和外观检查，样品不允许有以下缺陷： 1.Air bubble in the LCD; 模块中有气泡 2.Sealleak;封口松脱 3.Non-display;不显示 4.missing segments;漏笔 5.Glass crack;玻璃破碎 6.Current IDD is twice higher than initial value. 电流 IDD 大于初始值的两倍。
2	Low Temperature Storage 低温存储测试	-30℃±2℃/96 hours	
3	High Temperature Operating 高温操作测试	70℃±2℃/96 hours	
4	Low Temperature Operating 低温操作测试	-20℃±2℃/96 hours	
5	Temperature Cycle 冷热循环存储	-20℃±2℃~25℃~70℃±2℃*10cycles (30min.) (5min.) (30min.)	
6	Damp Proof Test 防潮测试	55℃±5℃*90%RH/96 hours	
7	ESD Test 抗静电性测试	测试前对样品进行外观和功能测试，采用空气放电，对 TP 进行单次放电，9 个点每一点放电一次，每次间隔≥5s,9 个点为一个循环。放点电压：±10KV，每一个循环放电后进行检查，如果合格就进行下一循环测试，如果不合格，试验停止，并进行问题判定	试验样品电气功能正常

11. ROHS TEST REPORT
ROHS 测试标准

Tested Item(s) 测试项目	Measured Equipment(s) 测量设备	Report Limit 限定值	Content 内容
Lead(Pb) 铅	XRF	Oganic materials＜100PPM 有机材料＜100PPM Inorganic material＜700PPM 无机材料＜700PPM	N.D.
Mercury(Hg) 汞	XRF	＜700PPM	N.D.
Cadmium(Cd) 镉	XRF	＜70PPM	N.D.
Hexavalent Chromium(Cr(VI)) 六价铬	XRF	＜700PPM	N.D.
Polybrominated Biphenyls(PBBS) 多溴联苯	XRF	＜700PPM	N.D.
Polybrominated Diphenyl Ethers(PBDES) 多溴二苯醚	XRF	＜700PPM	N.D.

Note:-N.D.=Not Detected (<report limit)

-mg/kg=ppm=parts per million

12. SPECIAL REMAKS

注意事项

1. The above specifications are the binding criteria for FGL Technology's outgoing quality inspection.
   以上规格描述为菲格尔的品质出货标准
2. The customer is kindly requested to inform FGL Technology as soon as possible on any questions, remarks, and disagreements regarding these specifications.
   对于规格中的任何问题或存在疑问，客户可随时向菲格尔公司进行咨询。
3. FGL is not responsible for damage to its products due to neglect of the precautions as described in the previous chapter.
   如果不按照规格书要求进行操作而损坏产品的，菲格尔不承担责任。
4. About the limited warranty unless special agreement between FGL and customer FGL will replace or repair any of its products that are found to be functionally defective when inspected in accordance with FGL acceptance standards for a period of one year from data of shipments.
   除菲格尔跟客户签定协议外，对确认为属于产品本身功能性缺陷的 ，在菲格尔可接受范围内可进行退换或维修，菲格尔保质期为从出货日期起一年内有效。