DATA SHEET

Revision: 1.1

Release date:

AGM FPGA

Low Cost and High Performance FPGA

General Description

AGM FPGA devices are targeted to high-volume, cost-sensitive, applications, enabling system designers to meet increasing performance requirements while lowering costs. The SRAM-based FPGA device, its low cost and optimized feature set makes ideal solutions for a wide array of automotive, consumer, communications, video processing, test and measurement, and other end-market solutions. AGM FPGA device family provides the ideal solution for your high-volume, low-power, and cost-sensitive applications.

Features

- High-density architecture with 6K to 10K LEs
- M9K embedded memory blocks, up to 414Kbits of RAM space
- Up to 23 18 x 18-bit embedded multipliers are each configurable as two independent 9 x 9-bit multipliers
- Provides 2 PLLs per device provide clock multiplication and phase shifting
- High-speed differential I/O standard support, including LVDS, RSDS, mini-LVDS, LVPECL
- Single-ended I/O standard support, including 3.3V, 2.5V, 1.8V, and 1.5V LVCMOS and LVTTL
- General package options, LQFP and FBGA.
- Flexible device configuration through JTAG and SPI interface

Table 1-1 Shows AGM FPGA family features

Feature	**AG6K, AG10K**
LUTs	6400, 10K
EBR SRAM (Kbits)	414
Maximum User I/O pins	179
Number of PLLs	2
Package	144-Pin LQFP 256-Pin FBGA

Contents

1. AGM FPGA Architecture

1.1. Functional Description

The AGM FPGA devices contain an industrial state-of-the art two-dimensional row- and column-based architecture to implement custom logic. Column and row interconnects of varies speeds provide signal interconnects between logic blocks (LBs) and IOs.

The logic array consists of LBs, with 16 logic slices (LS) in each LB. A slice is a small unit of logic providing efficient implementation of user logic functions. LBs are grouped into rows and columns across the device. The AGM FPGA devices' density is ranging from 6K to 10K slices.

The device global clock network consists of up to 8 global clock lines that drive through the entire device. The global clock network can provide clocks for all resources within the device, such as input/output elements (IOEs), slices. The global clock lines can also be used for other high fan-out signals.

Each device I/O pin is fed by an IOE located at the ends of LB rows and columns around the periphery of the device. I/O pins support various single-ended standards. Each IOE contains a bidirectional I/O buffer.

1.2. Logic Array Blocks

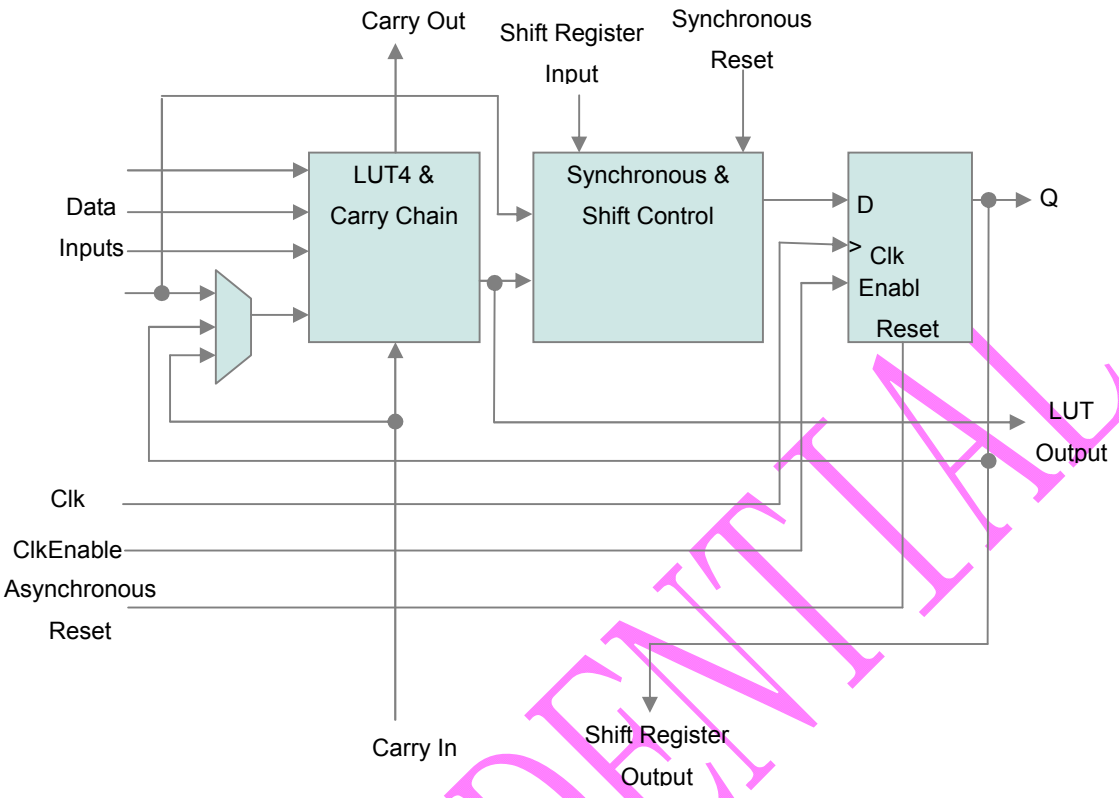
Each Logic Block consists of 16 slices, SLICE carry chains, SLICE control signals, a local interconnect, a look-up table (LUT) chain, and register chain connection lines. There are 32 possible unique inputs into an SLICE. Register chain connections transfer the output of one SLICE's register to the adjacent SLICE's register within a block. The AG software places associated logic within an SLICE or adjacent SLICES, allowing the use of local, LUT chain, and register chain connections for performance and area efficiency.

1.3. Logic Element

The smallest unit of logic in AGM FPGA architecture, the slice, is compact and provides advanced and flexible features with efficient logic utilization. Each slice features:

- Industrial standard four-input look-up table (LUT4), which is a function generator that can implement any combinatorial logic function of four inputs.
- A programmable register
- A carry chain connection
- A register chain connection
- The ability to drive all types of interconnects: local, row, column, register chain, and inter-tile connections
- Support for efficient packing of LUT and register
- Support for register feedback

Figure 1-1. AGM FPGA Logic SLICE



Each slice's register has data, clock, clock enable, and clear inputs. Signals that from global clock network, general-purpose I/O pins, or any internal logic outputs can drive the register's clock and clear control signals. Either general-purpose I/O pins or internal logic can drive the clock enable. For combinational functions, the LUT output bypasses the register and drives directly to the slice outputs resources. The slice is architected so that LUT and register can drive to separate outputs.

1.4. FlexTrack Interconnect

In AGM FPGA device architecture, FlexTrack interconnect consists of continuous, performance-optimized routing lines used for inter- and intra- design block connectivity. The FlexTrack connects to LEs, and IO pins with row and column connection that span fixed distances.

1.5. Clock Networks

The AGM FPGA device support three dedicated clock pins on the left side and four dedicated clock pins on the right side that can drive 10 global clocks (GCLKs).

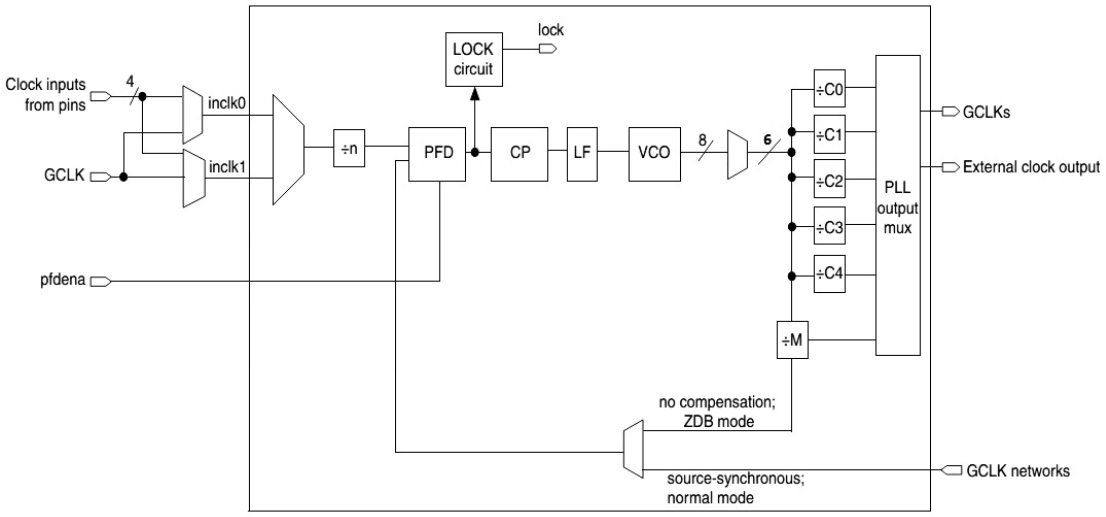
GCLKs drive throughout the entire device, feeding all device quadrants. All resources in the device (I/O elements, logic array blocks (LABs), dedicated multiplier blocks, and M9K memory blocks) can use GCLKs as clock sources. Use these clock network resources for control signals, such as clock enables and clears fed by an external pin. Internal logic can also drive GCLKs for internally generated GCLKs and asynchronous clears, clock enables, or other control signals with high fan-out.

1.6. Phase Locked Loops (PLLs)

AGM FPGA devices contain two general purpose PLLs that provide robust clock management and synthesis for device clock management, external system clock management, and high-speed I/O interfaces.

Figure 1-2 shows a block diagram of the major components of the PLL of AGM FPGA devices.

Figure 1-2. AGM FPGA PLL Block Diagram



Each clock source can come from any of the clock pins located on the same side of the device as the PLL. The general I/O pins cannot drive the PLL clock input pins.

AGM FPGA PLLs support four different clock feedback modes. Each mode allows clock multiplication and division, phase shifting, and programmable duty cycle. For the supported feedback modes and other features, refer to Table 1.1.

Table 1-1. AGM FPGA PLL Features

Hardware Features	Availability
Compensation modes	Source-Synchronous Mode, No Compensation Mode, Normal Mode, Zero Delay Buffer Mode
C (output counters)	5
M, N, C counter sizes	1 to 512
Dedicated clock outputs	1 single-ended or 1 differential pair
Clock input pins	4 single-ended or 2 differential pairs
Spread-spectrum input clock tracking	Support
PLL cascading	Through GCLK
Phase shift resolution	Down to 96-ps increments
Programmable duty cycle	Support

Output counter cascading	Support
Loss of lock detection	Support

1.7. Embedded Block RAM

AGM FPGA contains up to 414 Kbits Embedded Block RAMs (EBRs). The embedded memory structure consists of columns of M9K memory blocks that you can configure to provide various memory functions, such as RAM, shift registers, ROM, and FIFO buffers.

M9K blocks support the following features:

- 8,192 memory bits per block (9,216 bits per block including parity)
- Independent read-enable (rden) and write-enable (wren) signals for each port
- Packed mode in which the M9K memory block is split into two 4.5 K single-port RAMs
- Variable port configurations
- Single-port and simple dual-port modes support for all port widths
- True dual-port (one read and one write, two reads, or two writes) operation
- Byte enables for data input masking during writes
- Two clock-enable control signals for each port (port A and port B)
- Initialization file to pre-load memory content in RAM and ROM modes

Table 1-2. lists the features supported by the M9K memory.

Table 1-2. Summary of M9K Memory Features

Feature	**M9K Blocks**
Configurations (depth × width)	8192 × 1 4096 × 2 2048 × 4 1024 × 8 1024 × 9 512 × 16 512 × 18 256 × 32 256 × 36
Parity bits	Support
Byte enable	Support
Packed mode	Support
Address clock enable	Support
Single-port mode	Support
Simple dual-port mode	Support
True dual-port mode	Support
Embedded shift register mode	Support
ROM mode	Support
FIFO buffer	Support

Simple dual-port mixed width support	Support
True dual-port mixed width support	Support
Memory initialization file	Support
Mixed-clock mode	Support
Power-up condition	Outputs cleared
Register asynchronous clears	Read address registers and output registers only
Latch asynchronous clears	Output latches only
Write or read operation triggering	Write and read: Rising clock edges
Same-port read-during-write	Outputs set to **Old Data** or **New Data**
Mixed-port read-during-write	Outputs set to **Old Data** or **Don't Care**

AGM FPGA devices M9K memory blocks allow you to implement fully-synchronous SRAM memory in multiple modes of operation. M9K memory blocks do not support asynchronous (unregistered) memory inputs. M9K memory blocks support the following modes:

Single-port, Simple dual-port, True dual-port, Shift-register, ROM, FIFO

1.8. Embedded Multipliers

AGM FPGA devices include a combination of on-chip resources that help increase performance, reduce system cost, and lower the power consumption of digital signal processing (DSP) systems. AGM FPGA devices, either alone or as DSP device co-processors, are used to improve price-to-performance ratios of DSP systems. Particular focus is placed on optimizing AGM FPGA devices for applications that benefit from an abundance of parallel processing resources, which include video and image processing, wireless communications, and multi-channel communications and video systems.

The embedded multiplier is configured as either one 18 × 18 multiplier or two 9 × 9 multipliers. For multiplications greater than 18 × 18, the AGM software cascades multiple embedded multiplier blocks together. There are no restrictions on the data width of the multiplier, but the greater the data width, the slower the multiplication process.

You can use an embedded multiplier block in one of two operational modes, depending on the application needs:

- One 18 × 18 multiplier
- Up to two 9 × 9 independent multipliers

You can also use embedded multipliers of AGM FPGA devices to implement multiplier adder and multiplier accumulator functions, in which the multiplier portion of the function is implemented with embedded multipliers, and the adder or accumulator function is implemented in logic elements (LEs).

1.9. Power-On Reset Circuitry

When power is applied to AGM FPGA devices, the POR circuit monitors $_{VCC}$ and begins SRAM download at an approximate voltage of 1.2V AGM FPGA devices.

Entry into user mode is gated by whether V_{CCIO} bank are powered with sufficient operating voltage. If V_{CC} and V_{CCIO} are powered simultaneously, the device enters user mode.

For AGM FPGA when in user mode, the POR circuitry continues to monitor the V_{CC}(but not V_{CCIO}) voltage level to detect a brown-out condition. If there is a V_{CC} voltage sag at during user mode, the POR circuit resets the SRAM and tri-states the I/O pins. Once V_{CC} rises back to approximately 1.2V, the SRAM download restarts and the device begins to operate.

1.10. I/O

AGM FPGA devices support these I/O features:

- Supports 3.3-V, 2.5-V, 1.8-V, and 1.5-V logic levels: LVTTL, LVCMOS
- Programmable drive strength, bus-hold, pull-up resistors, open-drain output, input and output delay, slew rate control.
- Differential I/O standards: LVPECL, True-LVDS, RSDS, Mini-LVDS, BLVDS.

I/O pins on AGM FPGA devices are grouped together into I/O banks. Each bank has a separate power bus. AGM FPGA devices have eight I/O banks. Each device I/O pin is associated with one I/O bank. All single-ended and differential I/O standards are supported in all banks. All differential I/O standards are supported in all banks.

AGM FPGA devices can send and receive data through LVDS signals. For the LVDS transmitter and receiver, the input and output pins of devices support serialization and deserialization through internal logic.

The BLVDS extends the benefits of LVDS to multipoint applications such as bidirectional backplanes. The loading effect and the need to terminate the bus at both ends for multipoint applications require BLVDS to drive out a higher current than LVDS to produce a comparable voltage swing. All the I/O banks support BLVDS for user I/O pins.

The RSDS and mini-LVDS standards are derivatives of the LVDS standard. The RSDS and mini-LVDS I/O standards are similar in electrical characteristics to LVDS, but have a smaller voltage swing and therefore provide increased power benefits and reduced electromagnetic interference (EMI).

The LVDS standard does not require an input reference voltage, but it does require a 100-ohm termination resistor between the two signals at the input buffer. An external resistor network is required on the transmitter side for the top and bottom I/O banks.

2. Device Configuration

2.1. Configuration Mode

AGM FPGA devices use SRAM cells to store configuration data. You must download the configuration data to AGM FPGA devices each time the device powers up because SRAM memory is volatile. AGM FPGA devices are configured using one of the following configuration schemes as Table 2.1:

Table 2-1 Configuration schemes in AGM FPGA devices

Configuration Scheme	Configuration Method
Active serial (AS)	SPI FLASH
Passive serial (PS)	External Host with Flash Memory
	Download Cable
JTAG	External Host with Flash Memory
	Download Cable

2.2. Configuration data compression

AGM FPGA devices support configuration data decompression, which saves configuration memory space and time. This feature allows you to store compressed configuration data in configuration devices or other memory and send the compressed bitstream to AGM FPGA devices. During configuration, AGM FPGA devices decompress the bitstream in real time and program the SRAM cells.

When you enable compression, the AGM software generates configuration files with compressed configuration data. This compressed file reduces the storage requirements in the configuration device or flash memory and decreases the time required to send the bitstream to the AGM FPGA device.

AGM FPGA configuration file is about 2.5 to 3 Mbits. Compression may reduce the configuration bitstream size by 30 to 50%.

3. DC Electrical Characteristics

Table 3-1 Absolute Maximum Ratings for AGM FPGA Devices

Symbol	Parameter	Min	Max	Unit
V_{CCINT}	Core voltage	–0.5	1.8	V
V_{CCA}	Phase-locked loop (PLL) analog power supply	–0.5	3.75	V
V_{CCD_PLL}	PLL digital power supply	–0.5	4.5	V
V_{CCIO}	I/O banks power supply	–0.5	3.75	V

V_{CC_CLKIN}	Differential clock input pins power supply	–0.5	4.5	V
V_I	DC input voltage	–0.5	4.2	V
I_{OUT}	DC output current, per pin	–25	40	mA
T_{STG}	Storage temperature	–65	150	°C
T_J	Operating junction temperature	–40	100	°C

Table 3-2. Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCINT}	Supply voltage for internal logic, 1.2V operation	-	1.15	1.2	1.25	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	-	3.135	3.3	3.465	V
	Supply voltage for output buffers, 2.5-V operation	-	2.375	2.5	2.625	V
	Supply voltage for output buffers, 1.8-V operation	-	1.71	1.8	1.89	V
	Supply voltage for output buffers, 1.5-V operation	-	1.425	1.5	1.575	V
V_{CCA}	Supply (analog) voltage for PLL regulator	-	2.375	2.5	2.625	V
V_{CCD_PLL}	Supply (digital) voltage for PLL, 1.2-V operation	-	1.15	1.2	1.25	V
V_I	Input voltage	-	-0.5	-	3.6	V
V_O	Output voltage	-	0	-	VCCIO	V
T_J	Operating junction temperature	For commercial use	0	-	85	°C
		For industrial use	-40	-	100	°C
t_{RAMP}	Power supply ramp time	Standard power-on reset (POR)	50 µs	-	50 ms	-
		Fast POR	50 µs	-	3 ms	-

Table 3-3. I/O Pin Leakage Current

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_I	Input pin leakage current	V_I = 0 V to $V_{CCIOMAX}$	-10	-	10	µA
I_{OZ}	Tristated I/O pin leakage current	V_O = 0 V to $V_{CCIOMAX}$	-10	-	10	µA

Table 3-4. Single-Ended I/O Standard Specifications

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL}	I_{OH}
	Min	Typ	Max	Min	Max	Min	Max	Max	Min	(mA)	(mA)
3.3-V LVTTL	3.135	3.3	3.465	-	0.8	1.7	3.6	0.45	2.4	4	-4
3.3-V LVCMOS	3.135	3.3	3.465	-	0.8	1.7	3.6	0.2	V_{CCIO} -0.2	2	-2
2.5 V	2.375	2.5	2.625	-0.3	0.7	1.7	V_{CCIO} +0.3	0.4	2.0	1	-1
1.8 V	1.71	1.8	1.89	-0.3	0.35 x V_{CCIO}	0.65 x V_{CCIO}	2.25	0.45	V_{CCIO} -0.45	2	-2
1.5 V	1.425	1.5	1.575	–0.3	0.35 x V_{CCIO}	0.65 x V_{CCIO}	V_{CCIO} +0.3	0.25 x V_{CCIO}	0.75 x V_{CCIO}	2	-2

Table 3-5. Differential I/O Standard Specifications

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)		V_{ICM} (V)		
	Min	Typ	Max	Min	Max	Min	Condition	Max
LVPECL	2.375	2.5	2.625	100	-	0.05	$D_{MAX} \leq$ 500 Mbps	1.80
						0.55	500 Mbps $\leq D_{MAX} \leq$ 700 Mbps	1.80
						1.05	D_{MAX} > 700 Mbps	1.55
LVDS	2.375	2.5	2.625	100	-	0.05	$D_{MAX} \leq$ 500 Mbps	1.80
						0.55	500 Mbps $\leq D_{MAX} \leq$ 700 Mbps	1.80
						1.05	D_{MAX} > 700 Mbps	1.55

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)		V_{OD} (mV)			Vos (V)		
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
LVDS	2.375	2.5	2.625	100	-	247	-	600	1.125	1.25	1.375
BLVDS	2.375	2.5	2.625	100	-	-	-	-	-	-	-
mini-LVDS	2.375	2.5	2.625	-	-	300	-	600	1.0	1.2	1.4
RSDS	2.375	2.5	2.625	-	-	100	200	600	0.5	1.2	1.5

4. Timing Characteristics

Table 4-1. Core Performance Specifications

Device Core	Mode	Performance			Unit
		C6	C7	C8	
Clock Tree	-	500	437	402	MHz
Embedded Multiplier	9 x 9-bit Mode	340	300	260	MHz
	18 x 18-bit Mode	287	250	200	MHz
M9K Block	FIFO 256 × 36	315	274	238	MHz
	Single-port 256 × 36	315	274	238	MHz
	Simple dual-port 256 × 36 CLK	315	274	238	MHz
	True dual port 512 × 18 single CLK	315	274	238	MHz

Table 4-2. PLL Specifications

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input clock frequency	5	-	472.5	MHz
f_{INPFD}	PFD input frequency	5	-	40	MHz
f_{VCO}	PLL internal VCO operating range	500	-	1200	MHz
f_{INDUTY}	Input clock duty cycle	40	-	60	%
$t_{INJITTER\_CCJ}$	Input clock cycle-to-cycle jitter $F_{REF} \geq 100$ MHz	-	-	0.15	UI
	$F_{REF} < 100$ MHz	-	-	±750	ps
f_{OUT_EXT}	PLL output frequency (external clock output)	-	-	472.5	MHz
f_{OUT}	PLL output frequency (to global clock)	-	-	402.5	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	45	50	55	%
t_{LOCK}	Time required to lock from end of device configuration	-	-	1	ms
t_{PLL_PSERR}	Accuracy of PLL phase shift	-	-	±50	ps
t_{ARESET}	Minimum pulse width on areset signal	10	-	-	ns

5. Pin-Outs

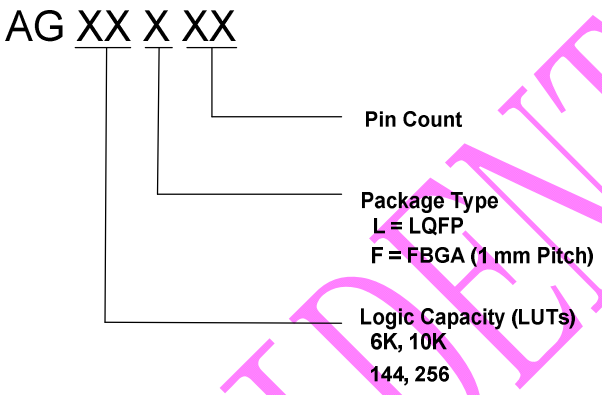
Refer to Pin-Outs printouts for AGM FPGA device family.

6. Software

AGM Software tools support from RTL to bit stream configuration implementation and programming. Supported operating system platforms include Microsoft Windows and Linux.

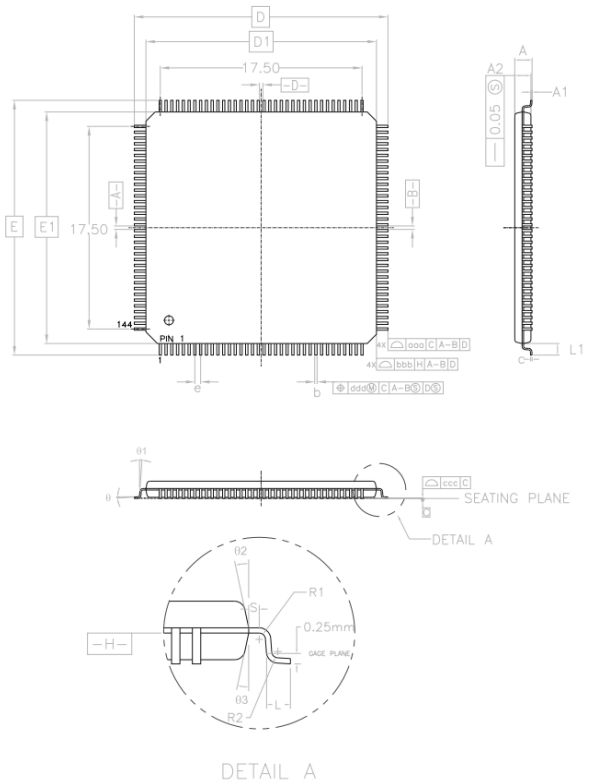
7. Ordering Information

Table 7-1 Device Part Number Description



8. Package

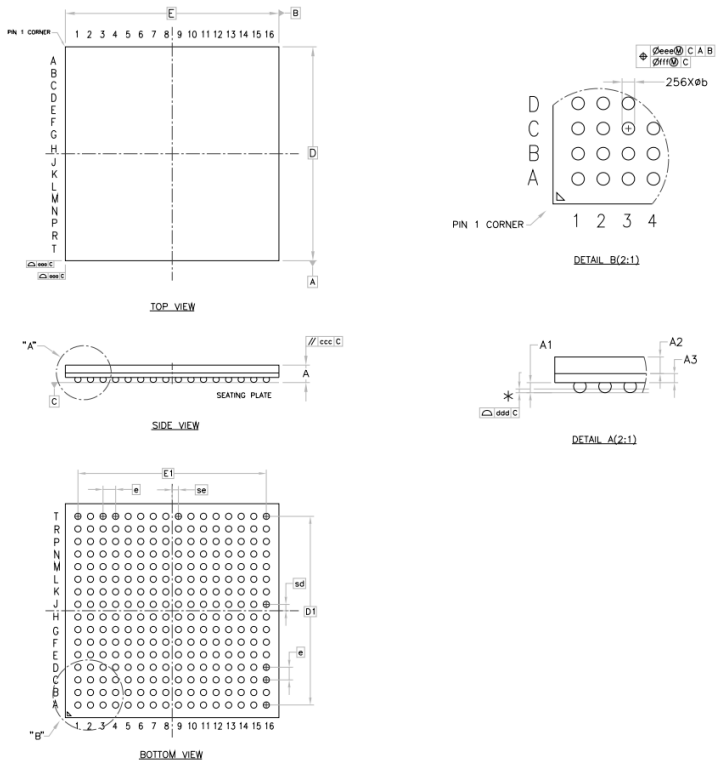
LQFP-144



FOR CUSTOMER ONLY				
PACKAGE TYPE		EP LQFP		
DESCRIPTION	SYMBOL	MILLIMETER		
		MIN	NOM	MAX
TOTAL THICKNESS	A	–	–	1.60
STAND OFF	A1	0.05	–	0.15
TOTAL MOLD THICKNESS	A2	1.35	1.40	1.45
PACKAGE SIZE WITH LEAD	D	–	22 BSC	–
	E	–	22 BSC	–
PACKAGE SIZE	D1	–	20 BSC	–
	E1	–	20 BSC	–
EP SIZE	D3	–	9.74 BSC	–
	E3	–	9.74 BSC	–
LEAD TURN RADIUS	R1	0.08	–	–
LEAD TURN RADIUS	R2	0.08	–	0.20
LEAD TURN ANGLE	θ	0°	3.5°	7°
LEAD TURN ANGLE	θ1	0°	–	–
LEAD TURN ANGLE	θ2	11°	12°	13°
LEAD TURN ANGLE	θ3	11°	12°	13°
LEAD CONTACT LENGTH	L	0.45	0.60	0.75
LEAD LENGTH	L1	–	1.00	–
MATERIAL THICKNESS	c	0.09	–	0.20
LEAD SPAN LENGTH	S	0.20	–	–

PIN COUNT		144		
DESCRIPTION	SYMBOL	MILLIMETER		
		MIN	NOM	MAX
LEAD PITCH	e		0.50 BSC	
LEAD WIDTH	b	0.17	0.20	0.27
LEAD EDGE PROFILE	aaa		0.20	
PACKAGE EDGE PROFILE	bbb		0.20	
LEAD COPLANARITY	ccc		0.08	
LEAD POSITION OFFSET	ddd		0.08	

FBGA-256



FOR CUSTOMER ONLY				
PACKAGE TYPE		LFBGA		
PIN COUNT		256		
DESCRIPTION	SYMBOL	MILLIMETER		
		MIN	NOM	MAX
TOTAL THICKNESS	A	–	1.46	1.55
STAND OFF	A1	0.35	0.40	0.45
MOLD THICKNESS	A2	–	0.70 BSC	–
MATERIAL THICKNESS	A3	0.32	0.36	0.40
PACKAGE SIZE	D	16.90	17.00	17.10
	E	16.90	17.00	17.10
BALL PITCH	e		1.00 BSC	
BALL SIZE	b	0.45	0.50	0.55
EDGE BALL CENTER TO CENTER	D1	–	15.00 BSC	–
	E1	–	15.00 BSC	–
PACKAGE EDGE PROFILE	aaa		0.10	
SUBSTRATE FLATNESS	bbb		–	
MOLD FLATNESS	ccc		0.10	
BALL COPLANARITY	ddd		0.15	
BALL POSITION OFFSET (PACKAGE)	eee		0.15	
BALL POSITION OFFSET (BALL)	fff		0.08	
	sd		0.50	
	se		0.50	

9. Recommended Reflow Profile

Figure. 8-1 Classification Reflow Profile

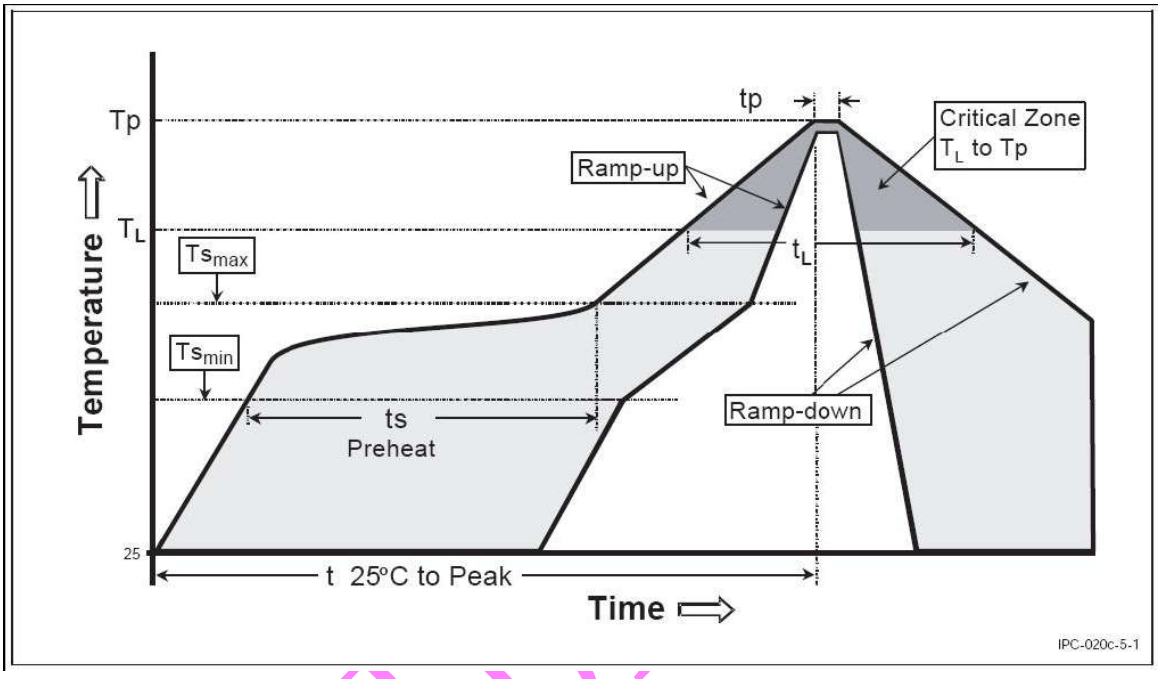


Table 8-1 Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate (TSmax to Tp)	3 ℃/second max.	3 ℃/second max.
Preheat -Temperature Min (Tsmin) -Temperature Max (Tsmax) -Time (tsmin to tsmax)	 100 ℃ 100 ℃ 60-120 seconds	 150 ℃ 200 ℃ 60-180 seconds
Time maintained above: -Temperature (TL) -Time (tL)	 183 ℃ 60-150seconds	 217℃ 60-150 seconds
Peak /Classification Temperature(Tp)	See Table 10	See Table 11
Time within 5 oC of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-Down Rate	6 ℃/second max.	6 ℃/seconds max.
Time 25 oC to Peak Temperature	6 minutes max.	8 minutes max.

Table 8-2 Sn-Pb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm3 <350	Volume mm3 ≥350
＜2.5mm	240 + 0/-5 ℃	225 + 0/-5 ℃
≥2.5mm	225 + 0/-5 ℃	225 + 0/-5 ℃

Table 8-3 Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm3 ＜350	Volume mm3 350-2000	Volume mm3 ＞2000
＜1.6mm	260 + 0 ℃ *	260 + 0 ℃ *	260 + 0 ℃ *
1.6mm – 2.5mm	260 + 0 ℃ *	250 + 0 ℃ *	245 + 0 ℃ *
≥2.5mm	250 + 0 ℃ *	245 + 0 ℃ *	245 + 0 ℃ *
*Tolerance : The device manufacturer/supplier shall assure process compatibility up to and including the stated classification temperature(this mean Peak reflow temperature + 0 ℃. For example 260+ 0 ℃) at the rated MSL Level.			

Note 1: All temperature refer topside of the package. Measured on the package body surface.

Note 2: The profiling tolerance is + 0 ℃, - X ℃ (based on machine variation capability)whatever is required to control the profile process but at no time will it exceed – 5 ℃. The producer assures process compatibility at the peak reflow profile temperatures defined in Table 9-3.

Note 3: Package volume excludes external terminals(balls, bumps, lands, leads) and/or non integral heat sinks.

Note 4: The maximum component temperature reached during reflow depends on package the thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD package may sill exist.

Note 5: Components intended for use in a “lead-free” assembly process shall be evaluated using the “lead free” classification temperatures and profiles defined in Table8-1, 8-2, 8-3 whether or not lead free.

10. Change List

The following table summarizes revisions to this document.

REV	DATE	AUTHER	CHANGE DESCRIPTION
V1.0	04/22/2015		Release Version 1.0
V1.1	09/20/2015		

11. RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) or polybrominated diphenyl ethers (PBDE), and are therefore considered RoHS compliant.

12. ESD Precautions

ESD protection circuitry is contended in this device, but special handling precautions are required.