

AGM CPLD AGRV2K

DATASHEET

General Description

AGM CPLD 2K family provides low-cost instant-on, non-volatile CPLDs, with densities of 2K logic LUTs. The devices offer LQFP 100, 64, 48 pins and QFN 32 pins featuring, and in-system programming. The devices are designed to reduce cost and power while providing programmable solutions for a wide range of applications.

Features

- Low-Cost and low-power CPLD
- Instant-on, non-volatile Compatible FPGA architecture.
- Up to 4 global clock lines in the global clock network that drive throughout the entire device.
- Provides programmable fast propagation delay and clock-to-output times.
- Provides PLL per device provide clock multiplication and phase shifting.
- Supports 3.3-V logic level
- Programmable slew rate, drive strength, bus-hold, programmable pull-up resistors, open-drain output, Schmitt triggers and programmable input delay.
- Built-in Joint Test Action Group (JTAG) boundary-scan test (BST) circuitry complaint with IEEE Std. 1149.1-1990
- ISP circuitry compliant with IEEE Std. 1532
- 3.3-V LVCMOS and LVTTTL standards
- Operating junction temperature from -40 to 85 °C

Table 0-1 AGM CPLD 2K features

Feature	AGRV2KQ32	AGRV2KL48	AGRV2KL64	AGRV2KL100
LUTs	2K	2K	2K	2K
Maximum User I/O pins	24	32	47	76
Operating junction temperature	-40 to 85 °C	-40 to 85 °C	-40 to 85 °C	-40 to 85 °C

The AGM CPLDs are available in LQFP and QFN packages (refer to Chapter 5).

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1. AGM Architecture Overview

1.1.Functional Description

The AGM CPLD devices contain an industrial state-of-the art two-dimensional row- and column-based architecture to implement custom logic. Column and row interconnects of various speeds provide signal interconnects between logic blocks (LBs) and I/Os.

The logic array consists of LBs, with 16 logic slices (LS) in each LB. A slice is a small unit of logic providing efficient implementation of user logic functions. LBs are grouped into rows and columns across the device. The CPLD devices' density range is up to 2K slices.

The device global clock network consists of up to 4 global clock lines that drive through the entire device. The global clock network can provide clocks for all resources within the device, such as input/output elements (IOEs), slices. The global clock lines can also be used for other high fan-out signals.

Each device I/O pin is fed by an IOE located at the ends of LB rows and columns around the periphery of the device. I/O pins support various single-ended standards. Each IOE contains a bidirectional I/O buffer.

Each device is embedded with a flash memory block. The big portion of this flash memory storage is used as dedicated configuration flash memory (CFM) block. The CFM flash memory block provides the non-volatile storage for the all SRAM configuration bits. The CFM automatically downloads and configures the logic blocks and IP during power-on, providing instant-on sequence operation.

1.2.Logic Array Blocks

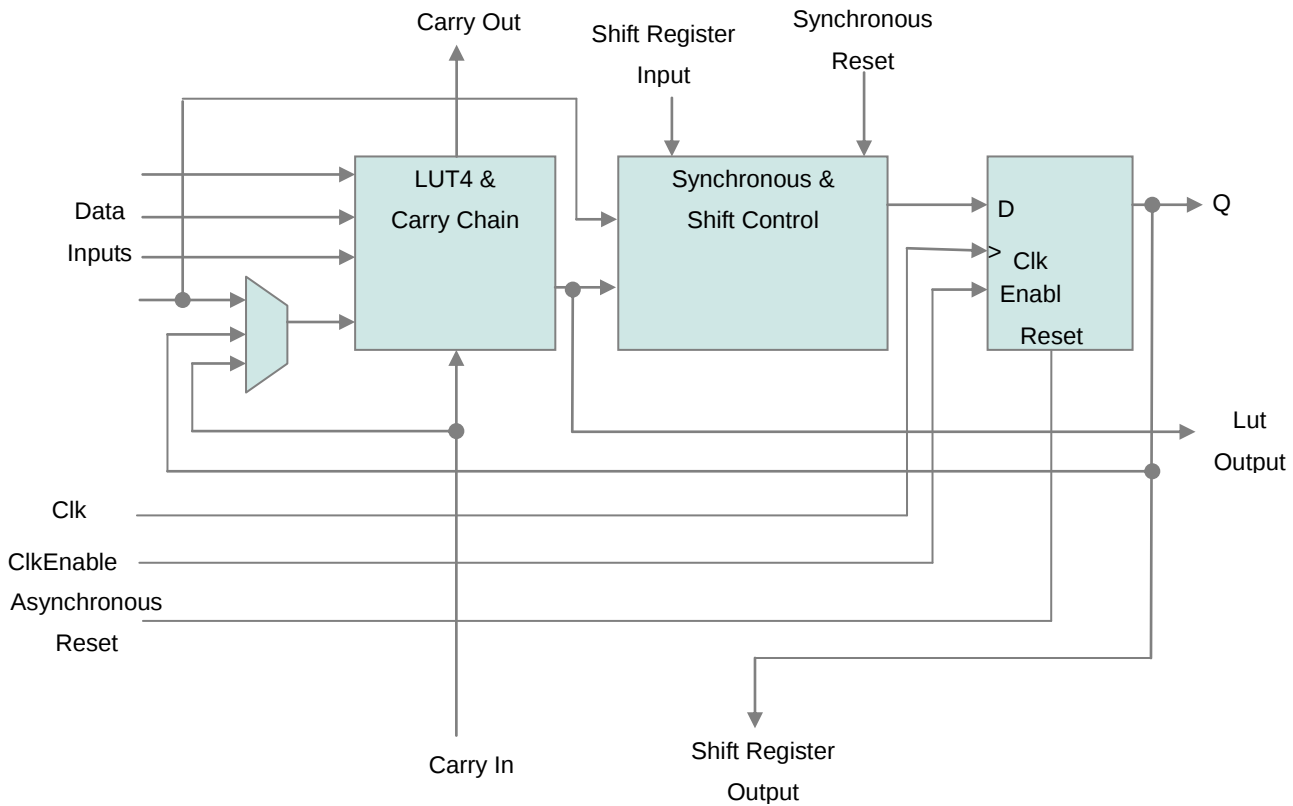
Each Logic Block consists of 16 slices, SLICE carry chains, SLICE control signals, a local interconnect, a look-up table (LUT) chain, and register chain connection lines.

1.3.Logic Element

The smallest unit of logic in AGM architecture, the slice, is compact and provides advanced and flexible features with efficient logic utilization. Each slice features:

- A four-input look-up table (LUT4), which is a function generator that can implement any combinatorial logic function of four inputs.
- A programmable register

Figure 1-1 AGM CPLD Logic SLICE



Each slice's register has data, clock, clock enable, and clear inputs.

1.4.FlexTrack Interconnect

In AGM device architecture, FlexTrack interconnect consists of continuous, performance-optimized routing lines used for inter- and intra- design block connectivity. The FlexTrack connects to LEs, PLL, RAM, and IO pins with row and column connection that span fixed distances.

1.5.Global Signals

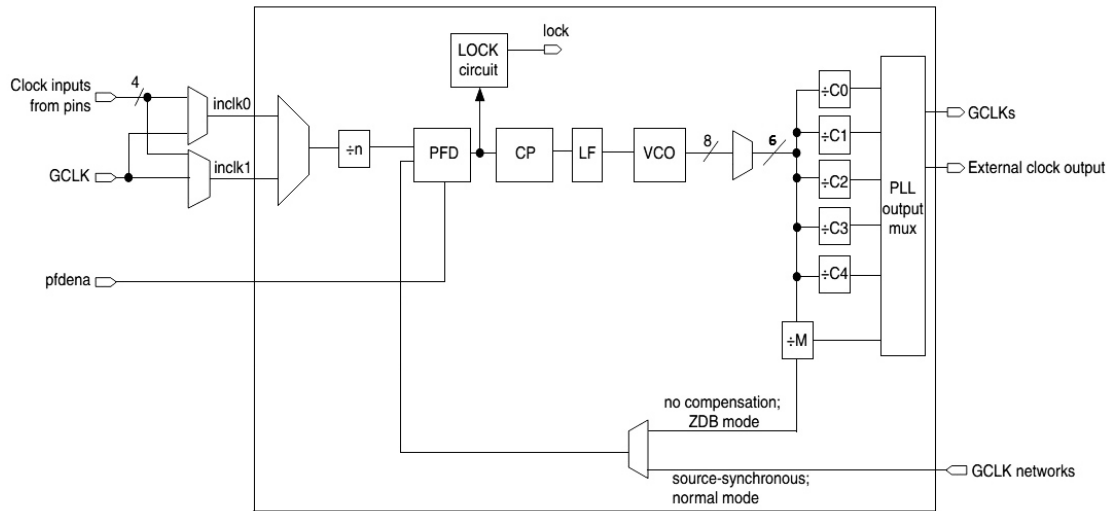
Each device has four dual-purpose dedicated clock pins, two pins on the left side, and two pins on the right. The four global clock lines drive throughout the entire device. The global clock network can provide clocks for all resources within the device including Les, local interconnect. The global lines can be used for global signals distribution.

1.6.Phase Locked Loops (PLLs)

AGRV2K CPLD devices contain 1 general purpose PLL that provide robust clock management and synthesis for device clock management, external system clock management, and high-speed I/O interfaces.

Figure 1-2 shows a block diagram of the major components of the PLL of AGM CPLD 2K devices.

Figure 1-2. AGM PLL Block Diagram



Each clock source can come from any of the clock pins located on the same side of the device as the PLL. The general I/O pins cannot drive the PLL clock input pins.

AGM PLLs support four different clock feedback modes. Each mode allows clock multiplication and division, phase shifting, and programmable duty cycle. For the supported feedback modes and other features, refer to Table 1.1.

Table 1-1. AGM PLL Features

Hardware Features	Availability
Compensation modes	Source-Synchronous Mode, No Compensation Mode, Normal Mode, Zero Delay Buffer Mode
C (output counters)	5
M, N, C counter sizes	1 to 512
Dedicated clock outputs	1 single-ended or 1 differential pair
Clock input pins	4 single-ended or 2 differential pairs
Spread-spectrum input clock tracking	Support
Phase shift resolution	Down to 96-ps increments
Programmable duty cycle	Support
Output counter cascading	Support
Loss of lock detection	Support

1.7. I/O Pin Structure

I/O supported features:

- Supports 3.3-V logic levels
- Programmable slew rate, drive strength, bus-hold, programmable pull-up resistors, open-drain output, Schmitt triggers input and programmable input delay.
- ISP circuitry compliant with IEEE Std. 1532
- 3.3-V LVC MOS and LVTTTL standards

1.8. Embedded Block RAM

AGM CPLD2K contains 4 Embedded Block RAMs (EBRs). The embedded memory structure consists of columns of M9K memory blocks that you can configure to provide various memory functions, such as RAM, shift registers, ROM, and FIFO buffers.

M9K blocks support the following features:

- 8,192 memory bits per block (9,216 bits per block including parity)
- Independent read-enable (rden) and write-enable (wren) signals for each port
- Packed mode in which the M9K memory block is split into two 4.5 K single-port RAMs
- Variable port configurations
- Single-port and simple dual-port modes support for all port widths
- True dual-port (one read and one write, two reads, or two writes) operation
- Byte enables for data input masking during writes
- Two clock-enable control signals for each port (port A and port B)
- Initialization file to pre-load memory content in RAM and ROM modes

AGM FPGA devices M9K memory blocks allow you to implement fully-synchronous SRAM memory in multiple modes of operation. M9K memory blocks do not support asynchronous (unregistered) memory inputs. M9K memory blocks support the following modes:

Single-port, Simple dual-port, True dual-port, Shift-register, ROM, FIFO.

2. JTAG and In-System Programming

2.1.JTAG

AGM devices provide Built-in Joint Test Action Group (JTAG) circuitry compliant with IEEE Std. 1149.1-1990. The JTAG pins support 3.3V I/O standards

2.2.In-System Programming

AGM device supports in-system programming via the industry standard 4-pin IEEE Std. 1149.1 (JTAG) interface. JTAG and ISP provide efficient iteration for design pattern written into the CFM's non-volatile flash storage.

By default, during in-system programming, the I/O pins are tri-stated and weakly pulled-up to VCCIO. AGM CPLD device also support real-time and clamp feature to allow user control of I/O state during in-system programming.

Real-time ISP allows user to program a CPLD while the device is still in operation. The newly programmed design will only take effect when the device is power cycled. This allows in-field updates to AGM CPLD at any time without interrupting the whole system.

ISP clamp feature allow user to hold each I/O to a specific state during real-time ISP. Each I/O can be set to low, high, tri-state, or hold the state when the device enters ISP clamp mode. After the device is successfully programmed the clamped I/O pins will be released the function according to the new design.

3. Power-On Reset Circuitry, On-Chip Oscillator

3.1.Power-On Reset Circuitry

When power is applied to AGM CPLD devices, the POR circuit monitors VDD33 and begins SRAM download AGM devices.

3.2.On-Chip Oscillator

On-Chip oscillator is provided to support frequency to 8 MHz.

4. Timing Characteristics

Table 4-1 Slice Internal Timing Parameters

Symbol	Parameter	Min	Max
T_{LUT}	SLICE Combinatorial LUT Delay	-	1.111ns
T_{CLR}	SLICE Register Clear Delay	0.032ns	-
T_{PRE}	SLICE Register Preset Delay	0.408ns	-
T_{SU}	SLICE Register Setup	0.664ns	-
T_H	SLICE Register Hold	-0.636ns	-
T_{CO}	SLICE Register Clock-To-Output Delay	-	0.455ns
T_{CLKHL}	Minimum Clock High or Low Time	0.300ns	-

Table 4-2 IOE Internal Timing Parameters

Symbol	Parameter	Min	Max
T_{IN}	I/O Input Pad and Buffer Delay	0.767ns	1.308ns
T_{DO}	Output Delay Buffer and Pad Delay	1.421ns	2.140ns
T_{XZ}	Output Buffer Disable Delay	0.867ns	1.322ns
T_{ZX}	Output Buffer Enable Delay	1.242ns	1.532ns

Table 4-3 Routing Internal Timing Parameters

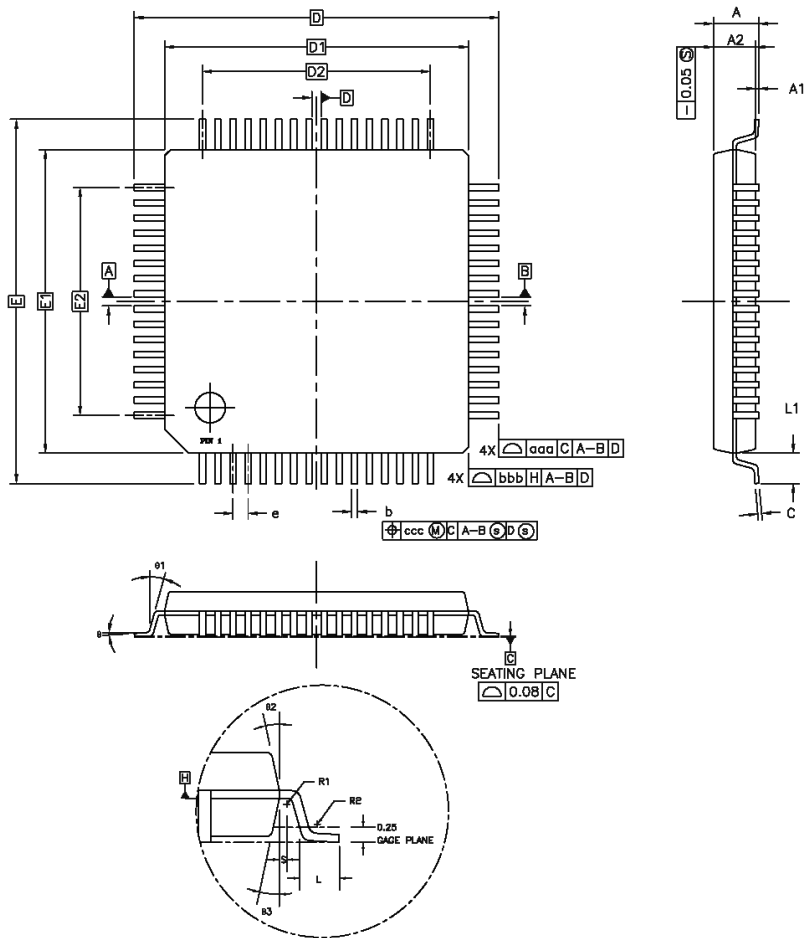
Symbol	Parameter	Min	Max
T_C	Delay for a column interconnect with average loading	-	0.679ns
T_R	Delay for a row interconnect with average loading	-	0.523ns
T_{LOCAL}	Local Routing Delay	-	0.434ns

PIN COUNT	100			
DESCRIPTION	SYMBOL	MILLIMETER		
		MIN	NOM	MAX
LEAD PITCH	e	0.50 BSC.		
LEAD WIDTH	b	0.17	0.20	0.27
LEAD EDGE PROFILE	aaa	0.20		
PACKAGE EDGE PROFILE	bbb	0.20		
LEAD COPLANARITY	ccc	0.08		
LEAD POSITION OFFSET	ddd	0.08		

Table 5-1 AGRV2KL100 pinout

Finger No.	Pin name	Finger No.	Pin name	Finger No.	Pin name	Finger No.	Pin name
1	IO/PIN_1	26	IO/PIN_26	51	IO/PIN_51	76	TCK
2	IO/PIN_2	27	GND	52	IO/PIN_52	77	IO/PIN_77
3	IO/PIN_3	28	VDD33	53	IO/PIN_53	78	IO/PIN_78
4	IO/PIN_4	29	IO/PIN_29	54	IO/PIN_54	79	IO/PIN_79
5	IO/PIN_5	30	IO/PIN_30	55	IO/PIN_55	80	IO/PIN_80
6	VDD33	31	IO/PIN_31	56	IO/PIN_56	81	IO/PIN_81
7	IO_GB/PIN_7	32	IO/PIN_32	57	IO/PIN_57	82	IO/PIN_82
8	NC	33	IO/PIN_33	58	IO/PIN_58	83	IO/PIN_83
9	NC	34	IO/PIN_34	59	IO/PIN_59	84	IO/PIN_84
10	GND	35	IO/PIN_35	60	IO/PIN_60	85	IO/PIN_85
11	VDD33	36	IO/PIN_36	61	IO/PIN_61	86	IO/PIN_86
12	NC	37	IO/PIN_37	62	IO/PIN_62	87	IO/PIN_87
13	NC	38	IO/PIN_38	63	IO/PIN_63	88	IO/PIN_88
14	NRST	39	IO/PIN_39	64	IO/PIN_64	89	IO/PIN_89
15	IO_GB/PIN_15	40	IO/PIN_40	65	IO/PIN_65	90	IO/PIN_90
16	IO/PIN_16	41	IO/PIN_41	66	IO/PIN_66	91	IO/PIN_91
17	IO/PIN_17	42	IO/PIN_42	67	IO/PIN_67	92	IO/PIN_92
18	IO/PIN_18	43	IO/PIN_43	68	IO/PIN_68	93	IO/PIN_93
19	NC	44	IO/PIN_44	69	IO/PIN_69	94	GND
20	GND	45	IO/PIN_45	70	IO/PIN_70	95	IO/PIN_95
21	VDDA33	46	IO/PIN_46	71	IO/PIN_71	96	IO/PIN_96
22	VDDA33	47	IO/PIN_47	72	TMS	97	IO/PIN_97
23	IO/PIN_23	48	IO/PIN_48	73	NC	98	IO/PIN_98
24	IO/PIN_24	49	NC	74	GND	99	GND
25	IO/PIN_25	50	VDD33	75	VDD33	100	VDD33

Figure 5-2 64-pin LQFP package diagram



CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	12.00 BSC.			0.472 BSC.		
D1	10.00 BSC.			0.394 BSC.		
E	12.00 BSC.			0.472 BSC.		
E1	10.00 BSC.			0.394 BSC.		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	7.50 REF			0.295		
E2	7.50 REF			0.295		
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		

Table 5-2 AGRV2KL64 pinout

Finger No.	Pin name	Finger No.	Pin name	Finger No.	Pin name	Finger No.	Pin name
1	VDD33	17	IO/PIN_17	33	IO/PIN_33	49	TCK
2	IO_GB/PIN_2	18	GND	34	IO/PIN_34	50	IO/PIN_50
3	NC	19	VDD33	35	IO/PIN_35	51	IO/PIN_51
4	NC	20	IO/PIN_20	36	IO/PIN_36	52	IO/PIN_52
5	NC	21	IO/PIN_21	37	IO/PIN_37	53	IO/PIN_53
6	NC	22	IO/PIN_22	38	IO/PIN_38	54	IO/PIN_54
7	NRST	23	IO/PIN_23	39	IO/PIN_39	55	IO/PIN_55
8	IO_GB/PIN_8	24	IO/PIN_24	40	IO/PIN_40	56	IO/PIN_56
9	IO/PIN_9	25	IO/PIN_25	41	IO/PIN_41	57	IO/PIN_57
10	IO/PIN_10	26	IO/PIN_26	42	IO/PIN_42	58	IO/PIN_58
11	IO/PIN_11	27	IO/PIN_27	43	IO/PIN_43	59	IO/PIN_59
12	GND	28	IO/PIN_28	44	IO/PIN_44	60	GND
13	VDDA33	29	IO/PIN_29	45	IO/PIN_45	61	IO/PIN_61
14	IO/PIN_14	30	IO/PIN_30	46	TMS	62	IO/PIN_62
15	IO/PIN_15	31	IO/PIN_31	47	IO/PIN_47	63	GND
16	IO/PIN_16	32	VDD33	48	VDD33	64	VDD33

Figure 5-3 48-pin LQFP package diagram

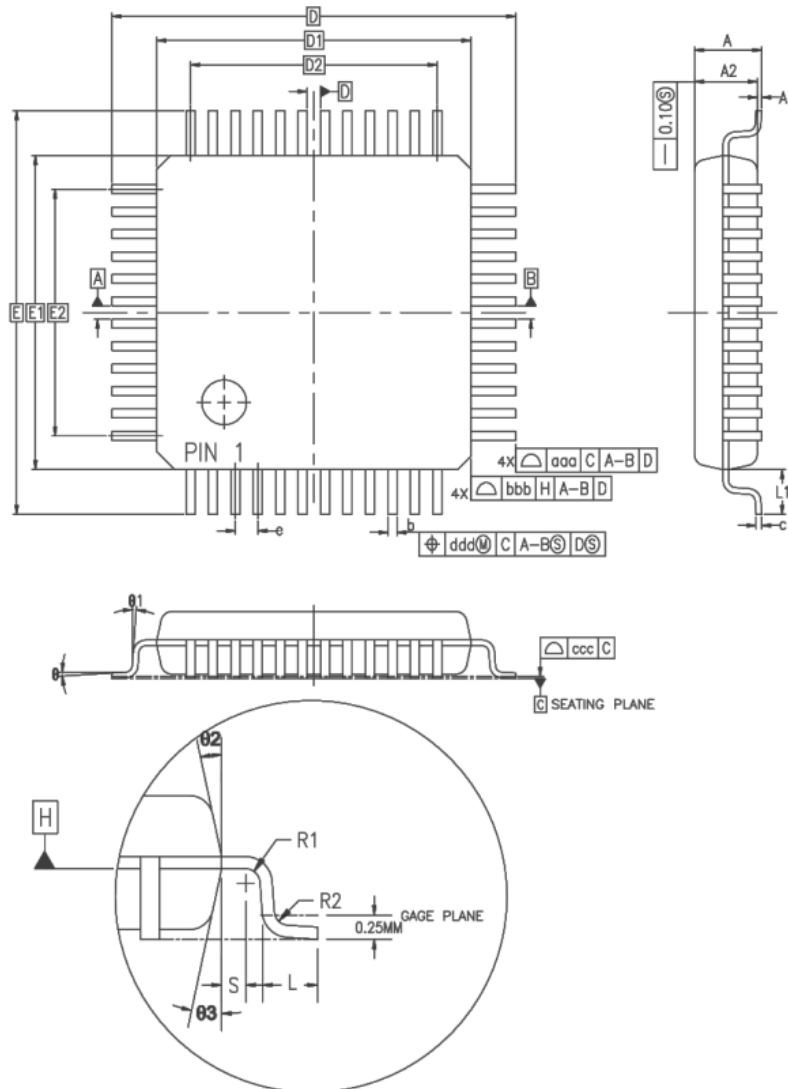


Table 5-3 AGRV2KL48 pinout

Finger No	Pin name	Finger No	Pin name
1	VDD33	25	IO/PIN_25
2	IO_GB/PIN_2	26	IO/PIN_26
3	NC	27	IO/PIN_27
4	NC	28	IO/PIN_28
5	NC	29	IO/PIN_29
6	NC	30	IO/PIN_30
7	NRST	31	IO/PIN_31
8	GND	32	IO/PIN_32
9	VDD33	33	IO/PIN_33
10	IO/PIN_10	34	TMS
11	IO/PIN_11	35	IO/PIN_35
12	IO/PIN_12	36	VDD33
13	IO/PIN_13	37	TCK
14	IO/PIN_14	38	IO/PIN_38
15	IO/PIN_15	39	IO/PIN_39
16	IO/PIN_16	40	IO/PIN_40
17	IO/PIN_17	41	IO/PIN_41
18	IO/PIN_18	42	IO/PIN_42
19	IO/PIN_19	43	IO/PIN_43
20	IO/PIN_20	44	GND
21	IO/PIN_21	45	IO/PIN_45
22	IO/PIN_22	46	IO/PIN_46
23	GND	47	GND
24	VDD33	48	VDD33

Figure 5-4 32-pin QFN package diagram

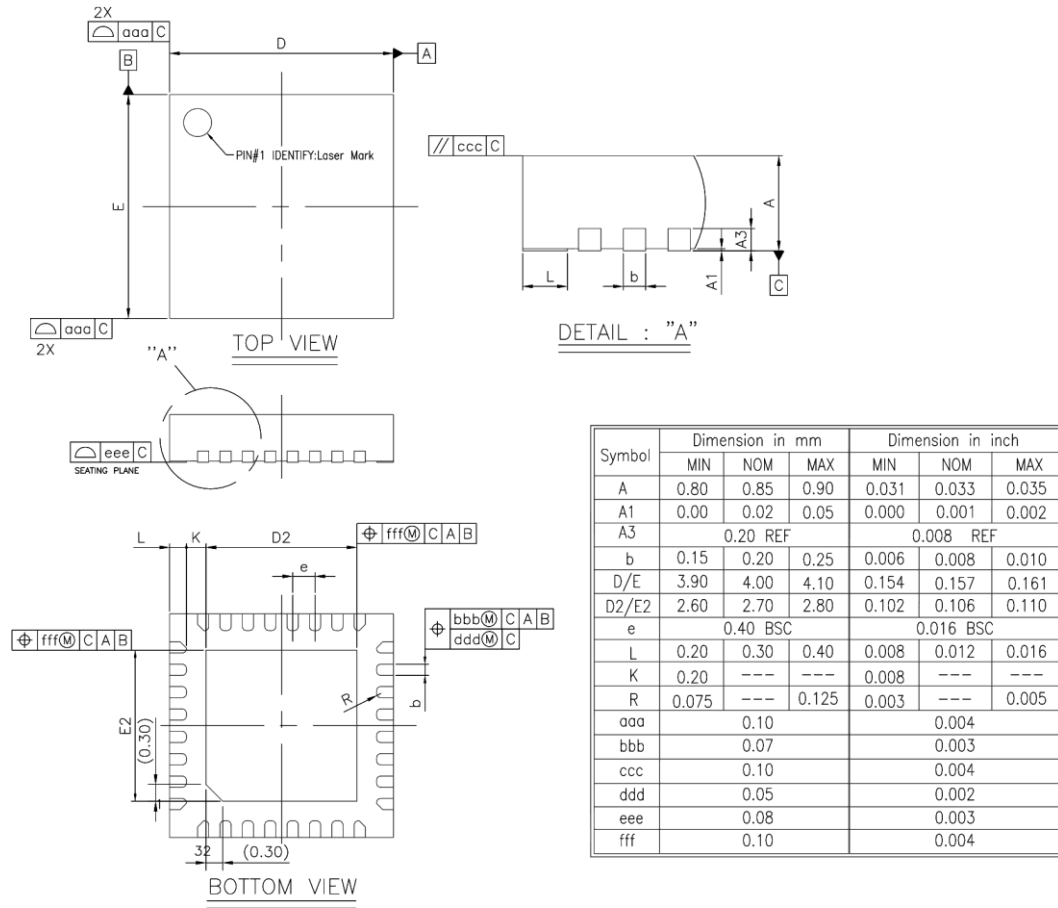


Table 5-4 AGRV2KQ32 pinout

Finger No	Pin name	Finger No	Pin name
1	IO_GB/PIN_1	17	GND
2	IO/PIN_2	18	IO/PIN_18
3	IO/PIN_3	19	IO/PIN_19
4	NRST	20	IO/PIN_20
5	IO/PIN_5	21	IO/PIN_21
6	VDDA33	22	IO/PIN_22
7	IO/PIN_7	23	IO/PIN_23
8	IO/PIN_8	24	JTMS
9	IO/PIN_9	25	JTCK
10	IO/PIN_10	26	IO/PIN_26
11	IO/PIN_11	27	IO/PIN_27
12	IO/PIN_12	28	IO/PIN_28
13	IO/PIN_13	29	IO/PIN_29
14	IO/PIN_14	30	GND
15	IO/PIN_15	31	IO/PIN_31
16	VDD33	32	VDD33

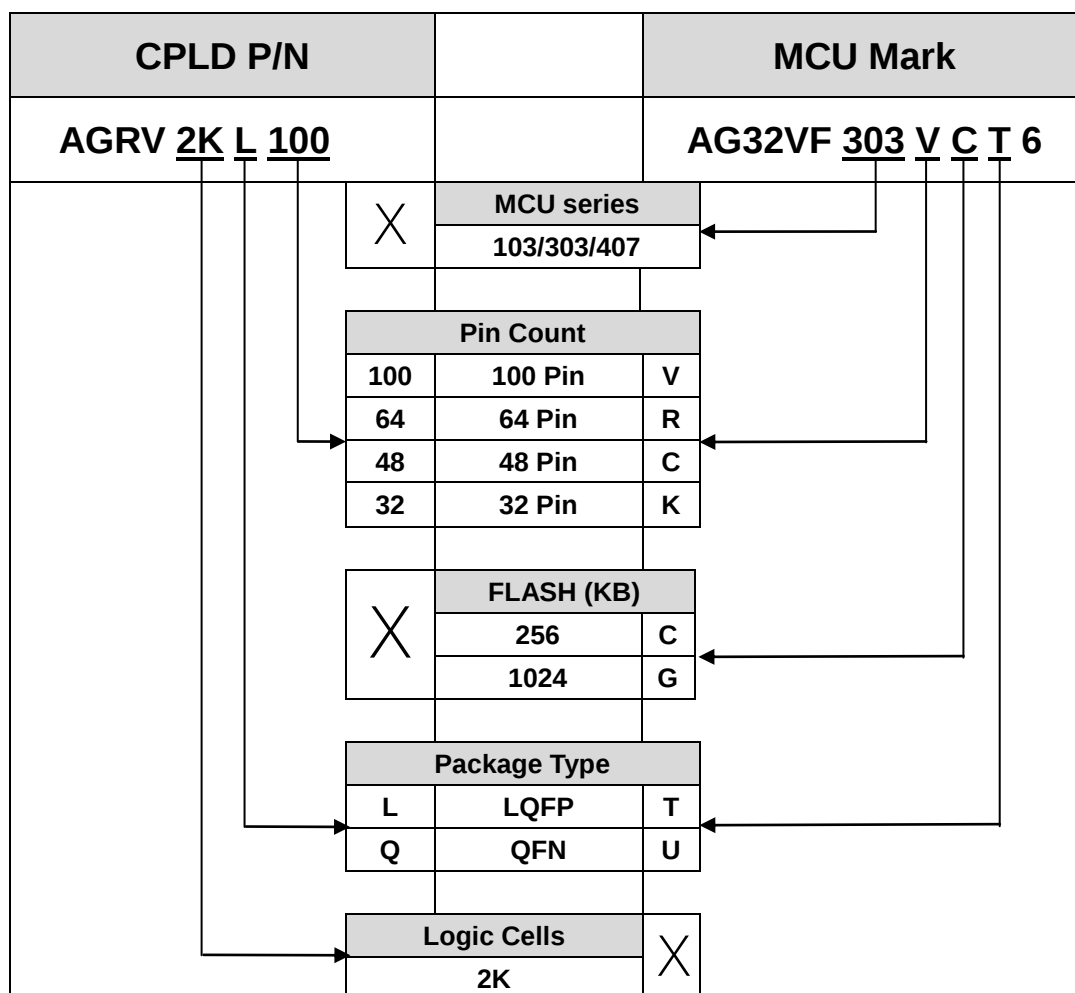
6. Reference and Ordering Information

6.1. Software

AGM Software tools support from RTL to bit stream configuration implementation and programming. Supported operating system platforms include Microsoft Windows and Linux.

6.2. Ordering Information

AGRV2K part number is only used in AGM software. It is a part of AG32 MCU marked with AG32VF series. So use the same package MCU P/N for ordering.



7. REVISION HISTORY

Version No	Description	Date
1.0		
2.0		
3.0		

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