JRS041R65F

Super Junction MOSFET

Description

JRS041R65F, the silicon N-channel Enhanced MOSFETs, is obtained by advanced Super Junction technology which reduce the conduction loss, improve switching performance. The transistor is suitable device for SMPS, high speed switching and general purpose applications

FEATURES

- Fast Switching
- 100% avalanche tested
- Improved dv/dt capability

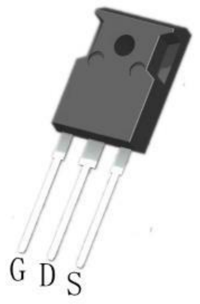
Product Summary

Parameter	Value	Units
$V_{DS@Tj.max}$	700	V
I_D	75	A
$R_{DS(ON).Typ}$@V_{GS}=10V	0.035	Ω

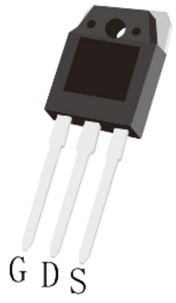
APPLICATIONS

- High frequency switching mode power supply

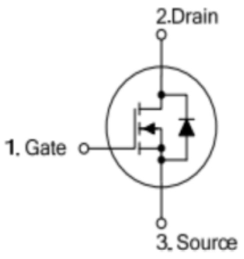
100% DVDS Tested !
100% Avalanche Tested !



TO-247



TO-3PN



Schematic Diagram

Ordering Information

Device	Device Package	Product Code	Packing
JRS041R65F-F	TO-247	S041R65F	Tube
JRS041R65F-W	TO-3PN	S041R65F	Tube

Absolute Maximum Ratings(T_C=25℃unless otherwise noted)

Parameter	Symbol	Rating	Units
Drain-to-Source Voltage	V_{DSS}	650	V
Continuous Drain Current	I_D	75	A
Continuous Drain Current T_C = 100 °C		48	A
Pulsed Drain Current(Note1)	I_{DM}	300	A
Gate-to-Source Voltage	V_{GS}	±30	V
Single Pulse Avalanche Energy(Note2)	E_{AS}	3000	mJ
Peak Diode Recovery dv/dt(Note3)	dv/dt	15	V/ns
Power Dissipation	PD	480	W
Derating Factor above 25°C		4.8	W/℃
Operating Junction and Storage Temperature Range	T_J,T_{stg}	150，–55 to 150	℃
Maximum Temperature for Soldering	T_L	260	℃

Thermal characteristics

Thermal characteristics

Parameter	Symbol	Rating	Units
Junction-to-Case	$R_{\theta JC}$	0.21	℃/W
Junction-to-Ambient	$R_{\theta JA}$	62.0	℃/W

Electrical Characteristics (TC=25℃unless otherwise noted)

Parameter	Symbol	Test Conditions	Values			Units
			Min	Typ	Max	
OFF Characteristics						
Drain to Source Breakdown Voltage	V_{DSS}	V_{GS}=0V, I_D=250μA	650	-	-	V
Bvdss Temperature Coefficient	ΔB_{VDSS} ΔT_J	I_D=250uA, Reference25℃	-	0.6	-	V/℃
Drain to Source Leakage Current	I_{DSS}	V_{DS} =650V, V_{GS}= 0V, T_j = 25℃	-	-	1	μA
		V_{DS} =520V, V_{GS}= 0V, T_j = 125℃	-	-	100	μA
Gate to Source Forward Leakage	$I_{GSS(F)}$	V_{GS} =+30V	- - -	- - -	100	nA
Gate to Source Reverse Leakage	$I_{GSS(R)}$	V_{GS} =-30V	-	-	-100	nA
ON Characteristics						
Drain-to-Source OnResistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=35A(Note4)	-	0.035	0.041	Ω
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D= 250μA(Note4)	3.5	4.0	4.5	V
Dynamic Characteristics						
Gate resistance	Rg	f = 1.0MHz	-	0.7	-	Ω
Output Capacitance	Ciss	V_{GS} = 0V V_{DS} = 25V f = 1.0MHz	-	7360	-	PF
Input Capacitance	Coss		-	790	-	
Reverse Transfer Capacitance	Crss		-	30	-	

Switching Characteristics, at T_J =25 ℃

Parameter	Symbol	Test Conditions	Values			Units
			Min.	Typ.	Max.	
Turn-on Delay Time	$t_{d(on)}$	I_D =50A V_{DD} = 400V V_{GS} = 13V R_G =1.8Ω	-	34	-	ns
Rise Time	tr		-	28	-	
Turn-Off Delay Time	$t_{d(off)}$		-	127	-	
Fall Time	t_f		-	8	-	
Total Gate Charge	Qg	I_D =70A V_{DD}=520V V_{GS} = 10V	-	161	-	nC
Gate to Source Charge	Qgs		-	47	-	
Gate to Drain (“Miller”)Charge	Qgd		-	64	-	

Source-Drain Diode Characteristics

Parameter	Symbol	Test Conditions	Values			Units
			Min.	Typ.	Max.	
Continuous Source Current (Body Diode)	I_S	TC=25 °C	-	-	75	A
Maximum Pulsed Current (Body Diode)	I_{SM}		-	-	300	A
Diode Forward Voltage	V_{SD}	I_S=75A, V_{GS}=0V(Note4)	-	-	1.2	V
Reverse Recovery Time	T_{rr}	I_S=45A, T_j = 25°C dIF/dt=100A/us, V_{GS}=0V	-	250	-	ns
Reverse Recovery Charge	Q_{rr}		-	2000	-	nC

Note1: Pulse width limited by maximum junction temperature

Note2: L=10mH, V_{Ds}=50V, Start T_J=25℃

Note3: I_{SD} =75A,di/dt ≤100A/us,V_{DD}≤BVDS, Start T_J=25℃

Note4: Pulse width tp≤300μs, δ≤2%

Figure 1 Safe Operating Area

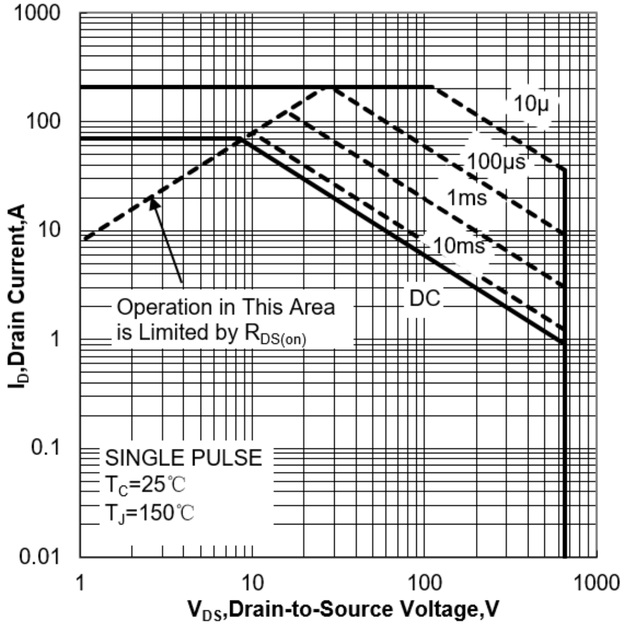


Figure 2 Power Dissipation

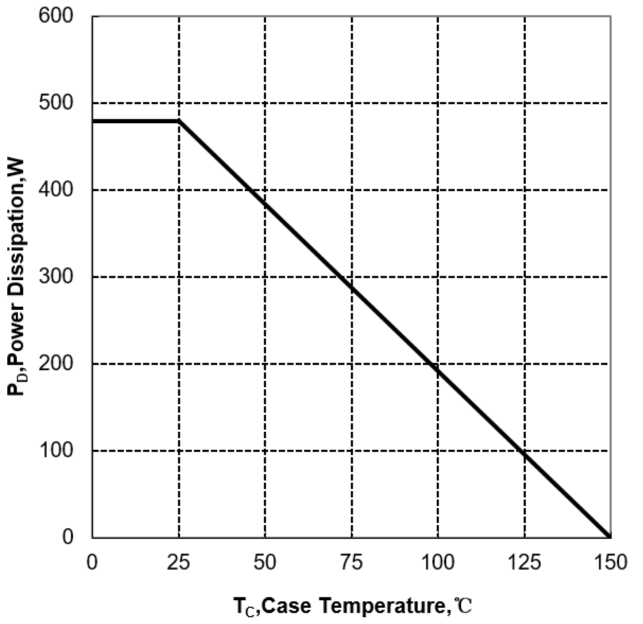
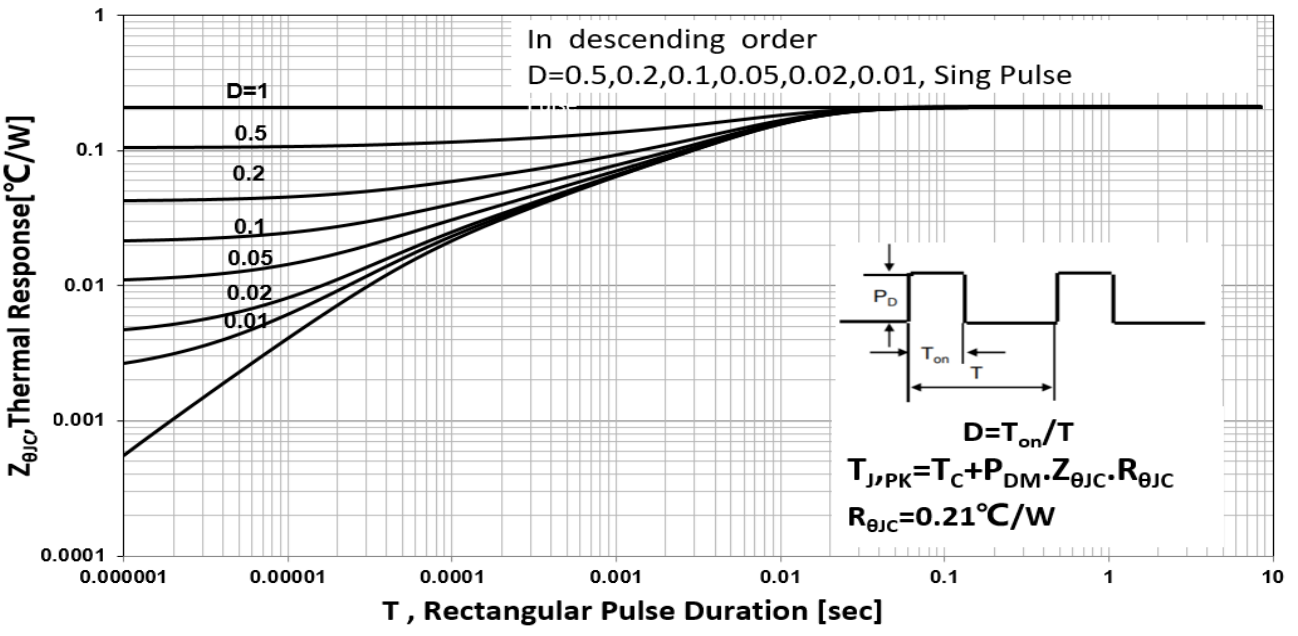


Figure 3 Max Thermal Impendance



Characteristics Curves

Figure 4 Typical Output Characteristics

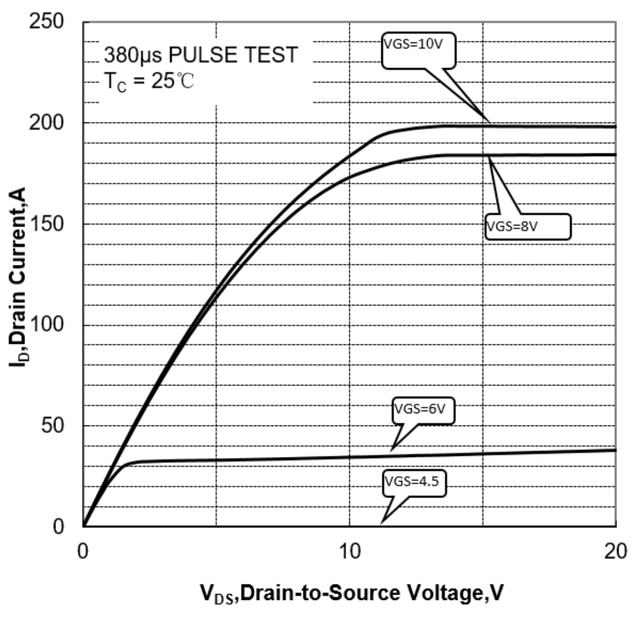


Figure 5 Typical Transfer Characteristics

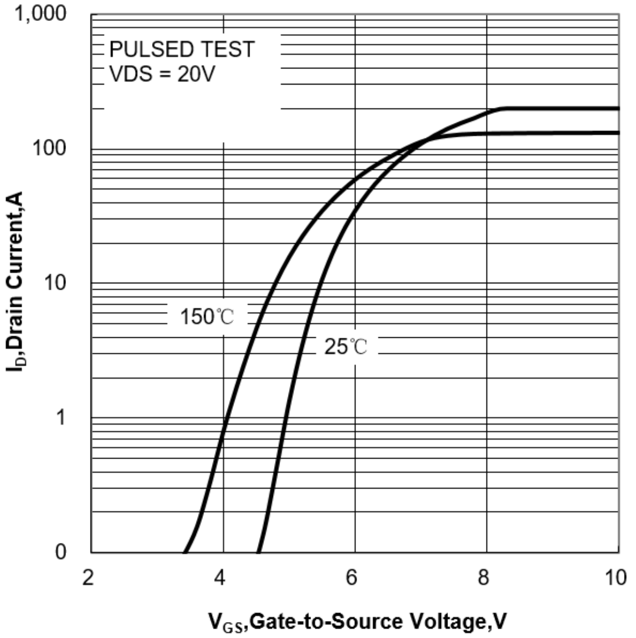


Figure 6 Typical Drain to Source ON Resistance vs Drain Current

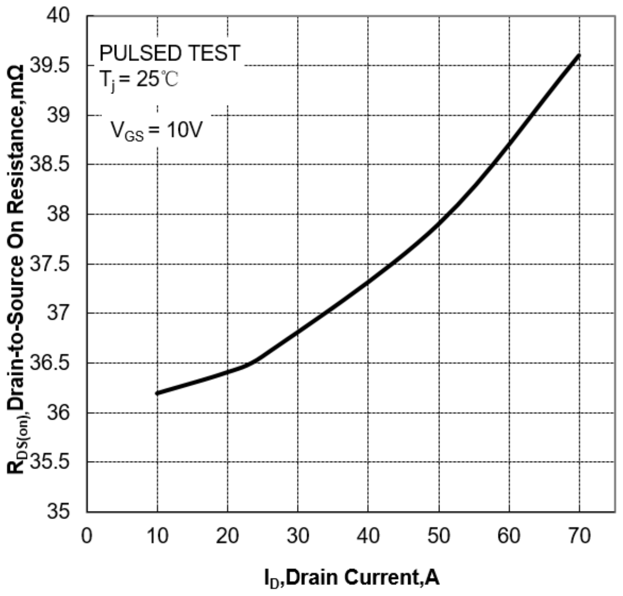


Figure 7 Typical Drian to Source on Resistance vs Junction Temperature

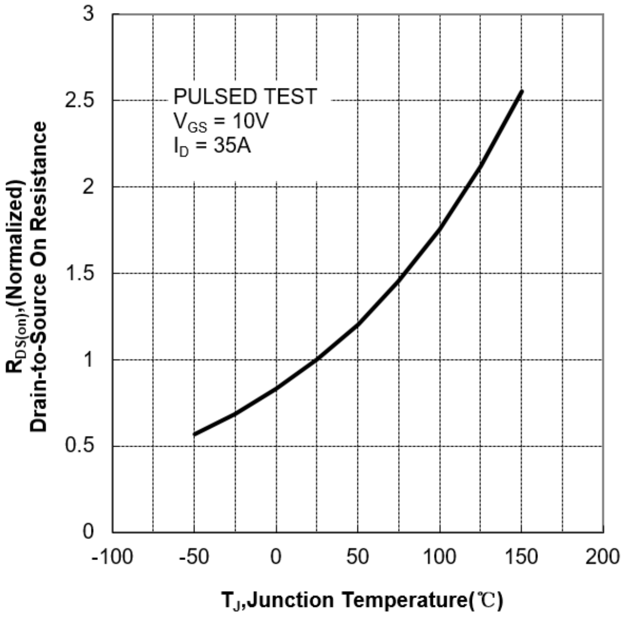


Figure 8 Typical Theshold Voltage vs Junction Temperature

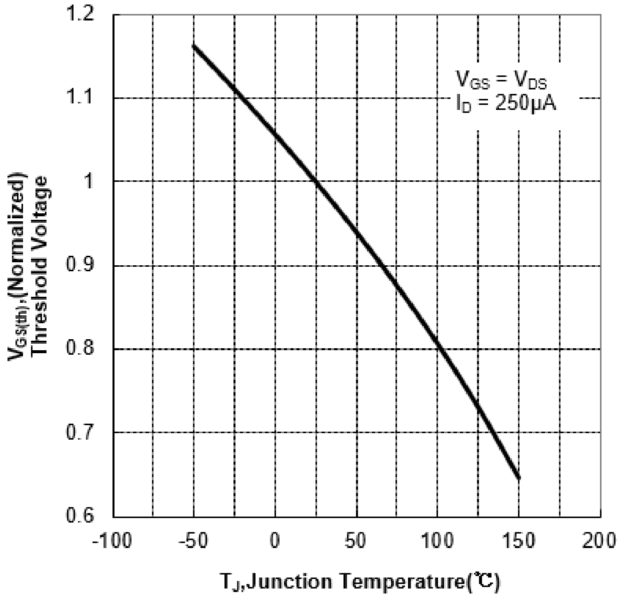


Figure 9 Typical Breakdown Voltage vs Junction Temperature

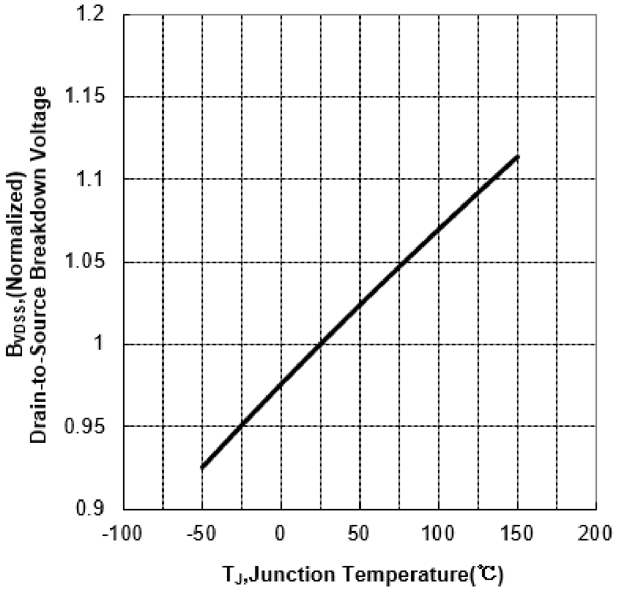


Figure 10 Typical Capacitance vs Drain to Source Voltage

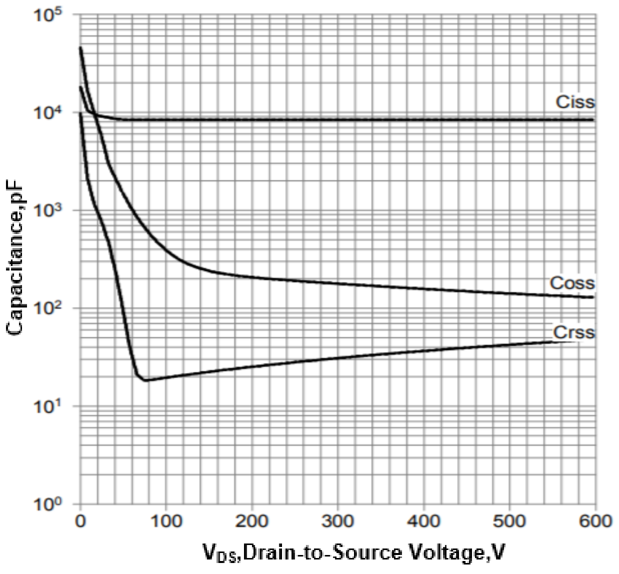
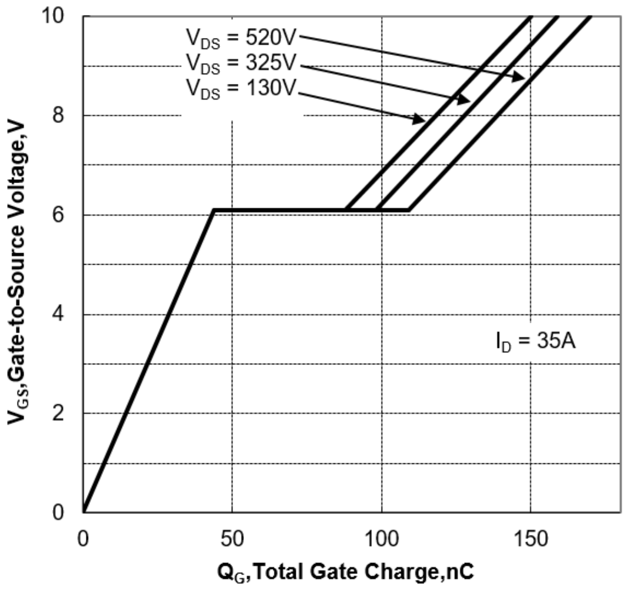


Figure 11 Typical Gate Charge vs Gate to Source Voltage



Test Circuit and Waveform

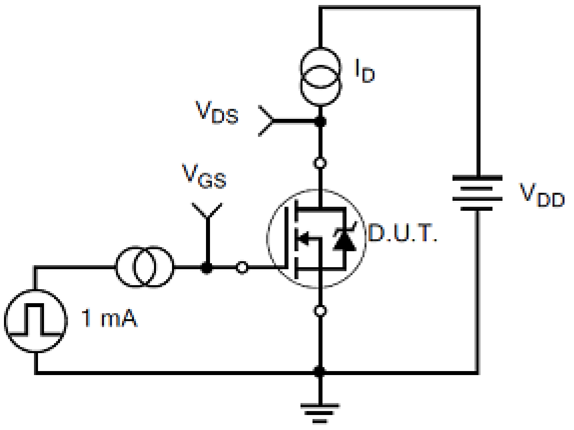
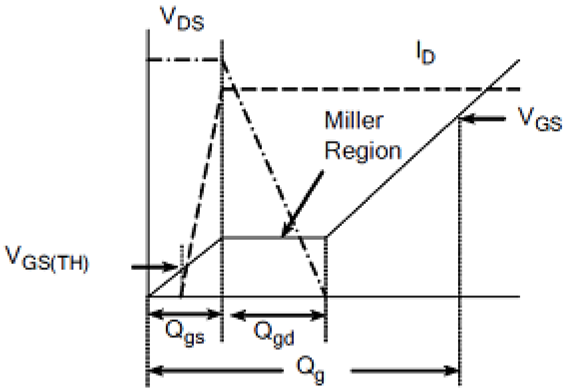
Figure 12 Gate Charge Test Circuit	**Figure 13 Gate Charge Waveforms**
	

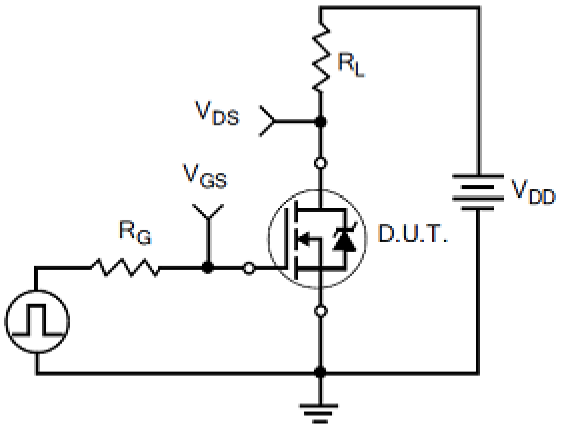
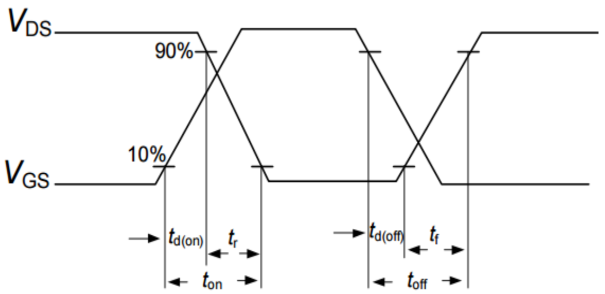
Figure 14 Resistive Switching Test Circuit	**Figure 15 Resistive Switching Waveforms**
	

Figure 16 Diode Reverse Recovery Test Circuit

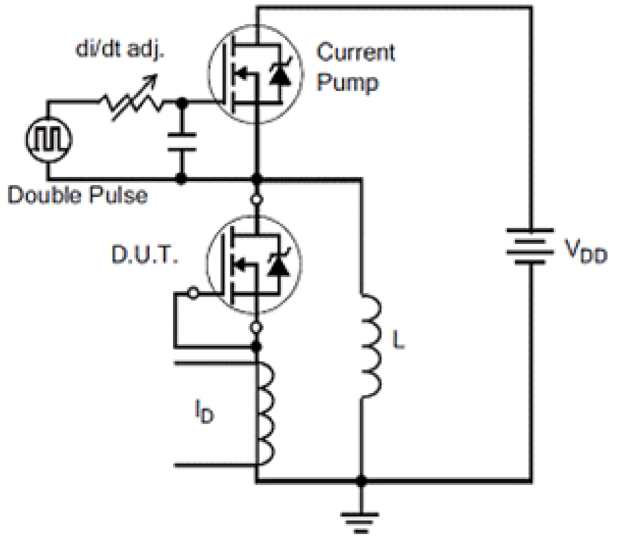


Figure 17 Diode Reverse Recovery Waveform

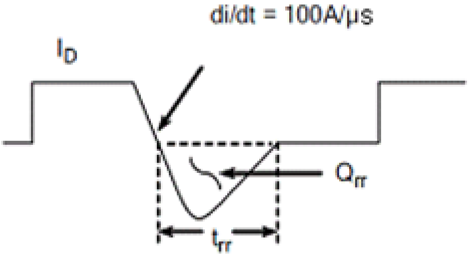


Figure 18 Unclamped Inductive Switching Test Circuit

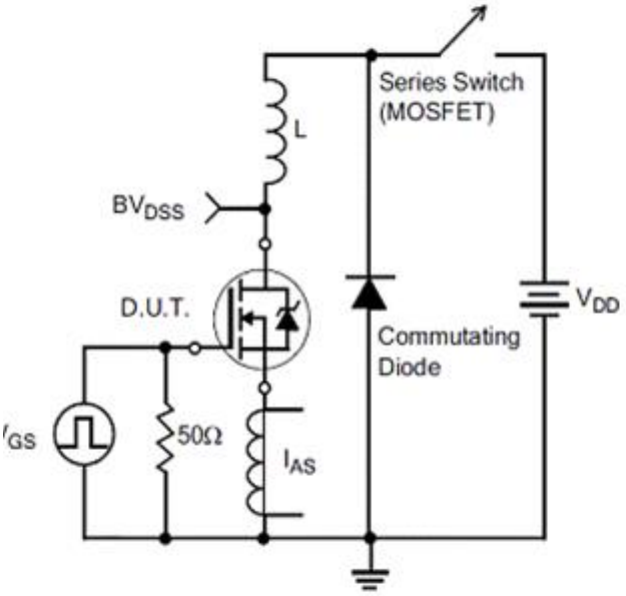
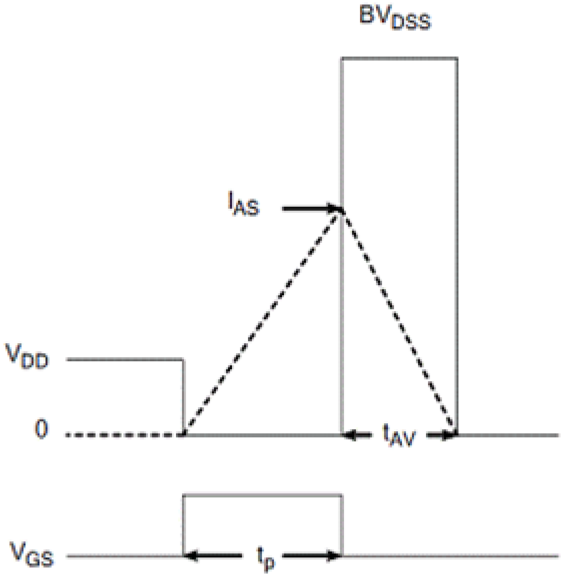
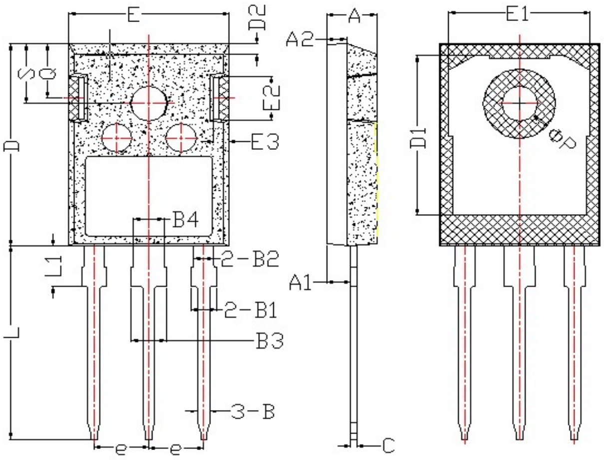


Figure 19 Unclamped Inductive Switching Waveform

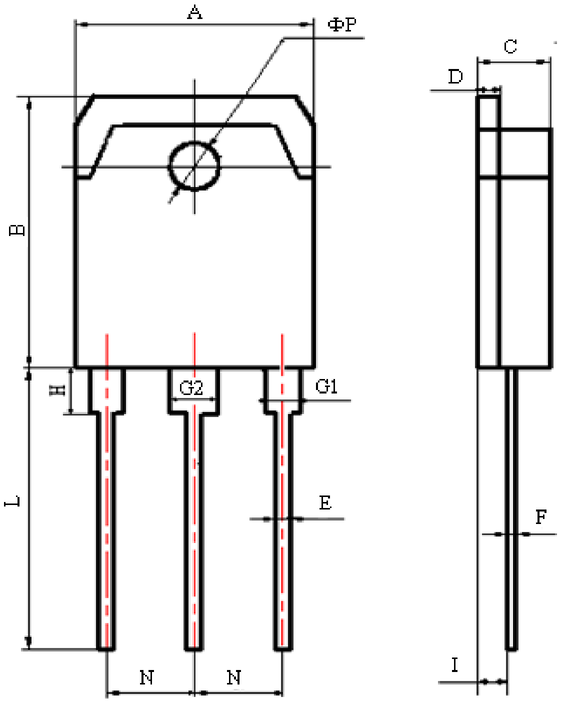


Package Description



Items	Values(mm)	
	MIN	MAX
A	4.6	5.2
A1	2,2	2.6
B	0.9	1.4
B1	1.75	2.35
B2	1.75	2.15
B3	2.8	3.35
B4	2.8	3.15
C	0.5	0.7
D	20.60	21.30
D1	16	18
E	15.5	16.10
E1	13	14.7
E2	3.80	5.3
E3	0.8	2.60
e	5.2	5.7
L	19	20.5
L1	3.9	4.6
ΦP	2.5	3.70
Q	5.2	6.00
S	5.8	6.6

TO-247 Package



Items	Values(mm)	
	MIN	MAX
A	15.00	16.00
B	19.20	20.60
C	4.60	5.00
D	1.40	1.60
E	0.90	1.10
F	0.50	0.70
G1	2.00	2.20
G2	3.00	3.20
H	3.00	3.70
I	1.20	1.70
	2.70	2.90
L	19.00	21.00
N	5.25	5.65
ΦP	3.10	3.30

TO-3PN Package