JERRETT

JRS036R60

Super Junction MOSFET

Description

JRS036R60, the silicon N-channel Enhanced MOSFETs, is obtained by advanced Super Junction technology which reduce the conduction loss, improve switching performance. The transistor is suitable device for SMPS, high speed switching and general purpose applications.

FEATURES

- Fast Switching
- 100% avalanche tested
- Improved dv/dt capability

Product Summary

Parameter	Value	Unit
V_{DSS}	650	V
I_D	75	A
$R_{DS(on).typ}$@V_{GS}=10V	0.032	Ω

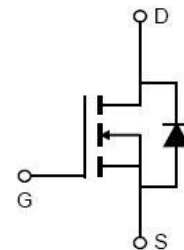
APPLICATIONS

- High frequencyswitching mode power supply

100% DVDS Tested!
100% Avalanche Tested!

TO-247

TO-3PN



Schematic Diagram

Ordering Information

Device	Device Package	Product Code	Packing
JRS036R60-F	TO-263	S036R60	Tube
JRS036R60-W	TO-3PN	S036R60	Tube

Absolute Maximum Ratings(TC=25℃ unless otherwise noted)

Parameter	Symbol	Rating	Units
Drain-Source Voltage	V_{DSS}	600	V
Continuous Drain Current	I_D	75	A
Continuous Drain Current TC =100°C	I_D	48	A
Pulsed Drain Current	I_{DM} Note1	300	A
Gate-Source Voltage	V_{GS}	±30	V
Avalanche Energy	E_{AS} Note2	2200	mJ
Peak Diode Recovery dv/dt	dv/dt Note3	15	V/ns
Power Dissipation	P_D	480	W
Derating Factor above 25°C		4.2	W/℃
Operating Junction and Storage Temperature Range	T_J,T_{STG}	150, – 55 to 150	℃
Maximum Temperature for Soldering	T_L	260	℃

Thermal characteristics

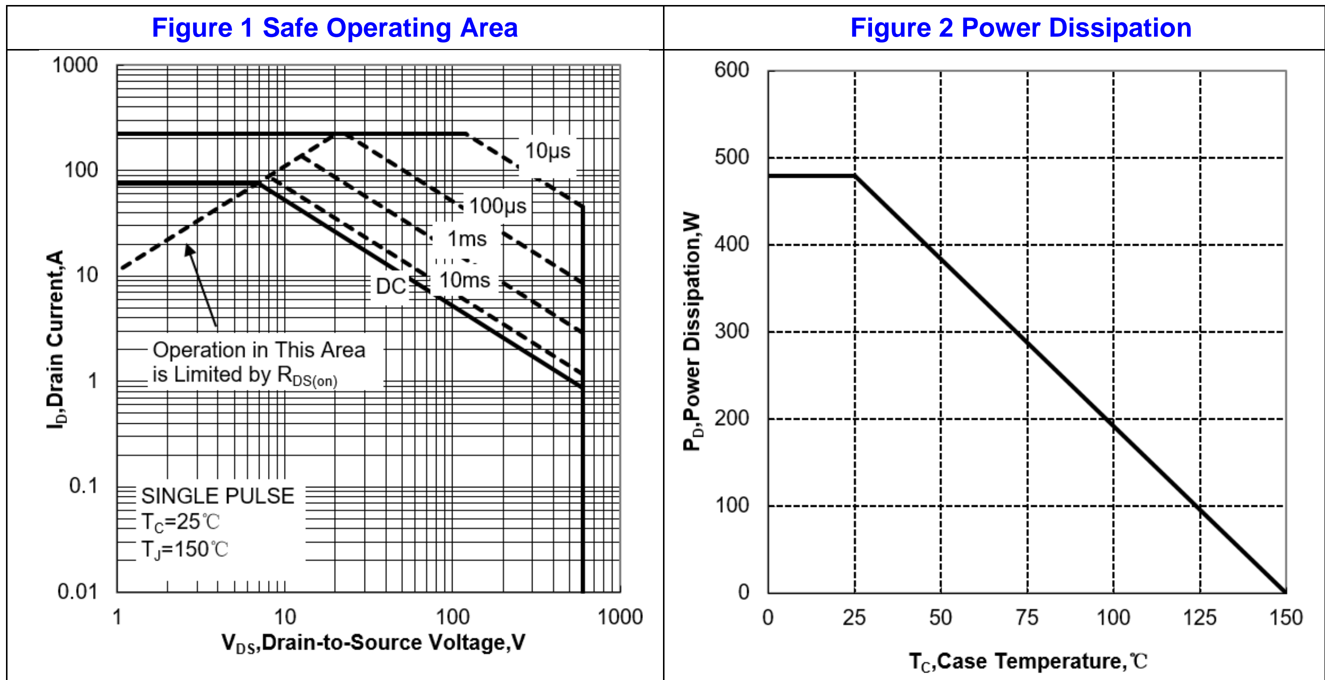
Parameter	Symbol	Max	Units
thermal resistance , Junction- Case	$R_{\theta JC}$	0.24	℃/W
thermal resistance , Junction-Ambient	$R_{\theta JA}$	62.0	℃/W

Note1: Pulse width limited by maximum junction temperature
Note2: L=10mH, VDs=50V, Start TJ=25℃
Note3: ISD =75A,di/dt ≤100A/us,VDD≤BVDS, Start TJ=25℃

Electrical Characteristics (TC=25℃unless otherwise noted)

Parameter	Symbol	Test Conditions	Values			Units
			Min	Typ	Max	
Off Characteristics						
Drain-Source Breakdown Voltage	V_{DSS}	V_{GS}=0V, I_D =250μA	600		-	V
Bvdss Temperature Coefficient	$\Delta BV_{DSS}/\Delta T_J$	ID=250uA, Reference25℃	-	0.58	-	V/℃
Drain-Source Leakage Current	I_{DSS}	V_{DS} =600V, V_{GS} =0V@T_j =125°C	-	-	1	μA
		V_{DS} =480V, V_{GS} =0V @T_j =125°C	-	-	100	μA
Gate-Source Forward Leakage	$I_{GSS(F)}$	V_{GS}=+30V	-	-	100	nA
Gate-Source Reverse Leakage	$I_{GSS(R)}$	V_{GS}=-30V	-	-	- 100	nA
On Characteristics						
Drain- Source On- Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D =50A	-	0.032	0.036	Ω
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} =V_{GS} , I_D =250μA	3.5	4.0	4.5	V
Pulse width tp≤300μs, δ≤2%						
Dynamic Characteristics						
Gate resistance	R_g	f=1 MHz	-	0.98	-	m Ω
Input Capacitance	C_{iss}	V_{DS} =25V, V_{GS} =0, f=1 MHz	-	7900	-	pF
Output Capacitance	C_{oss}		-	9200	-	
Reverse Transfer Capacitance	C_{rss}		-	900	-	
Total Gate Charge	Q_g	V_{DD} =480V, I_D =70A, V_{GS} =10V	-	160	-	nC
Gate- Source charge	Q_{gs}		-	46.5	-	
Gate- Drain charge	Q_{gd}		-	57	-	
Switching Characteristics						
Turn- On Delay Time	$t_{d(on)}$	V_{DD} =400V , I_D=45A, V_{GS} =13V , R_G =1.8Ω ,	-	30	-	ns
Rise Time	t_r		-	28	-	
Turn- Off Delay Time	$t_{d(off)}$		-	90	-	
Fall Time	t_f		-	6	-	
Source-Drain Diode Characteristics						
Continuous Source Current	I_S	TC=25 °C	-	-	75	A
Maximum Pulsed Current	I_{SM}		-	-	225	A
Diode Forward Voltage	V_{SD}	V_{GS} =0V, I_S =75A VGS=0V(Note4)	-	-	1.2	V
Reverse Recovery Time	T_{rr}	I_S =92.5A ,V_{GS} =0, di/dt=100A/us	-	620	-	ns
Reverse Recovery Charge	Q_{rr}		-	11000	-	nC

Characteristics Curves



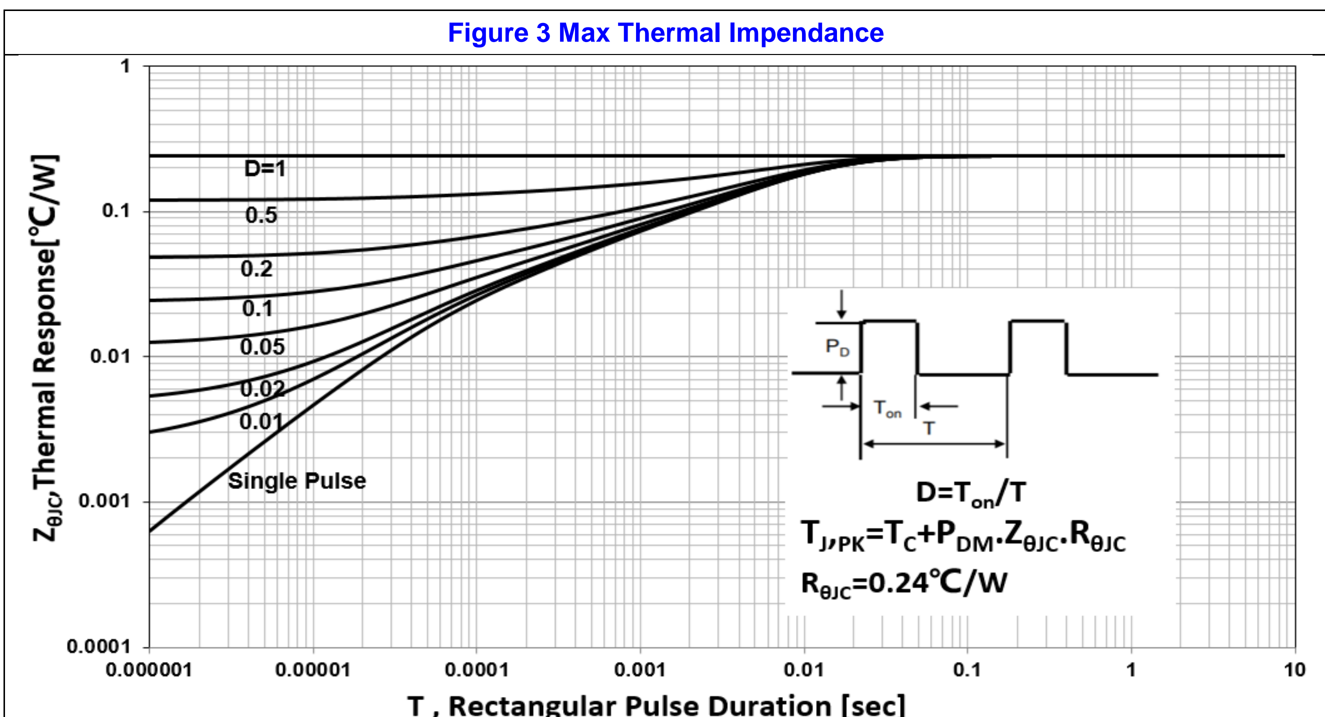


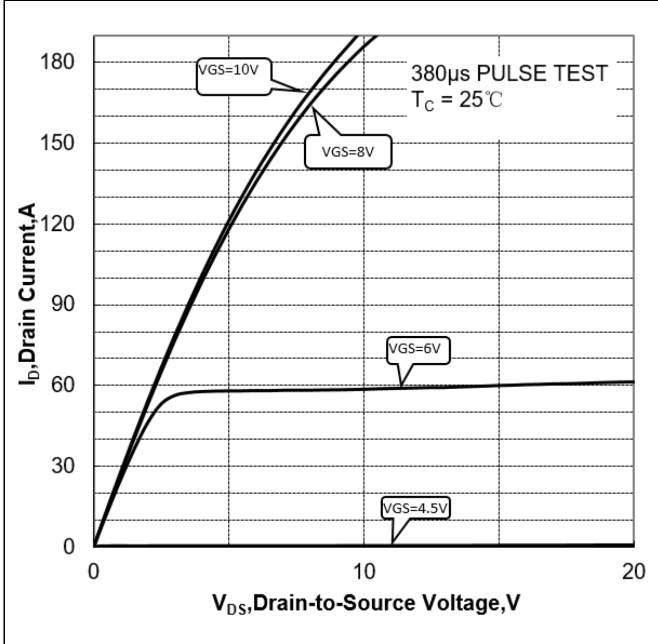
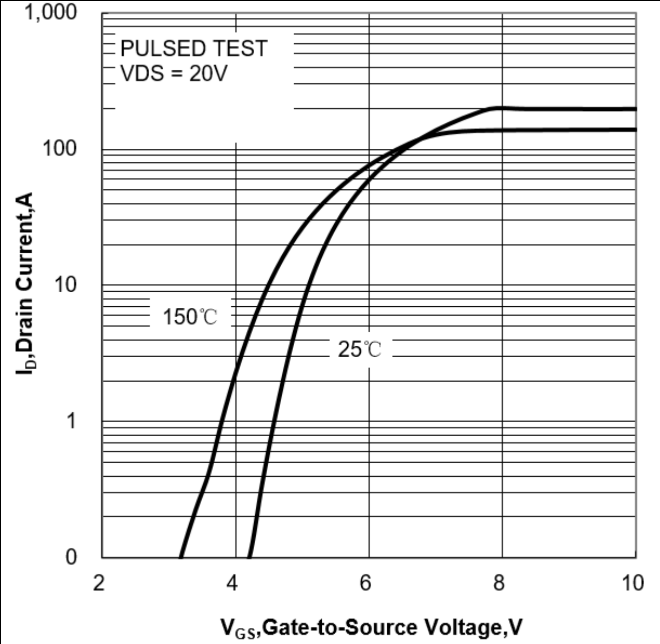
Figure 4 Typical Output Characteristics	Figure 5 Typical Transfer Characteristics
	

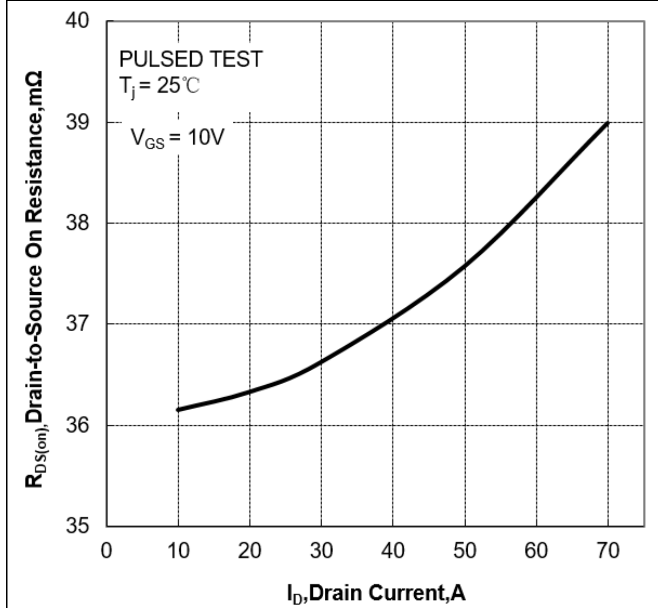
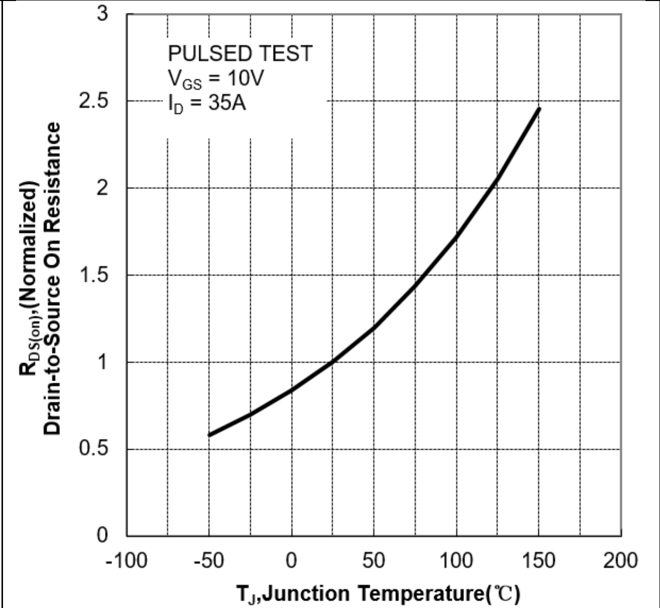
Figure 6 Typical Drain to Source ON Resistance vs Drain Current	Figure 7 Typical Drian to Source on Resistance vs Junction Temperature
	

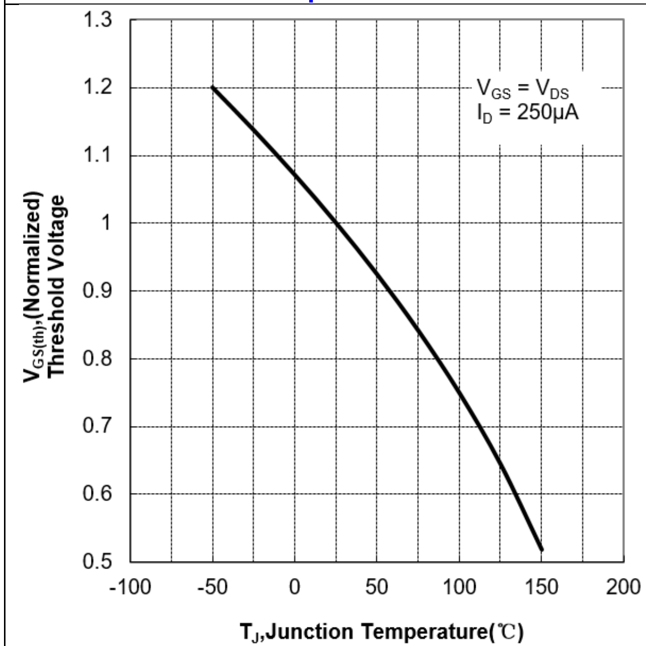
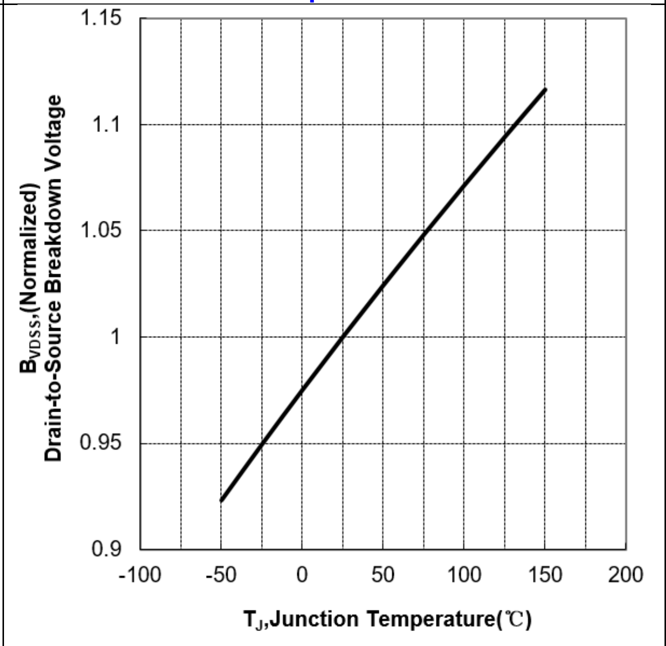
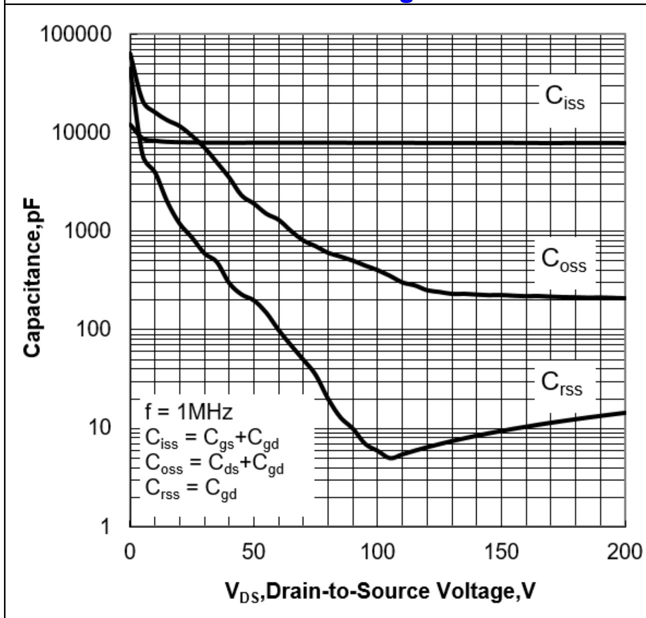
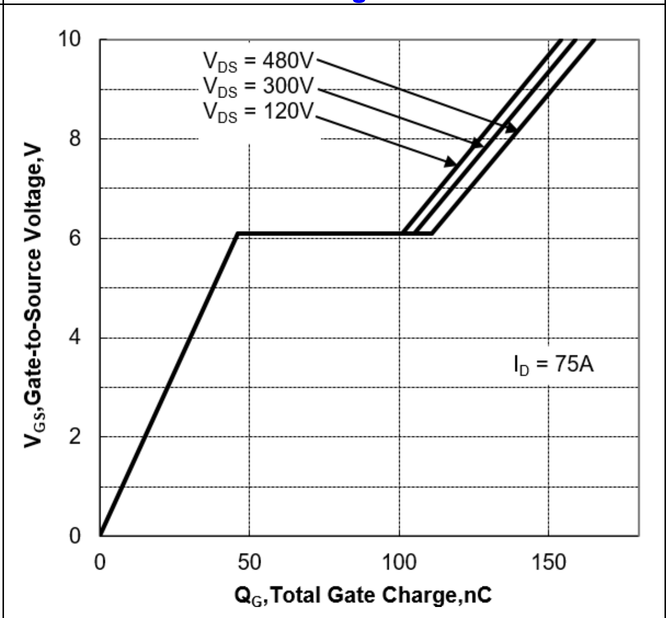
Figure 8 Typical Theshold Voltage vs Junction Temperature	Figure 9 Typical Breakdown Voltage vs Junction Temperature
	

Figure 10 Typical Capacitance vs Drain to Source Voltage	Figure 11 Typical Gate Charge vs Gate to Source Voltage
	

Test Circuit and Waveform

Figure 12 Gate Charge Test Circuit

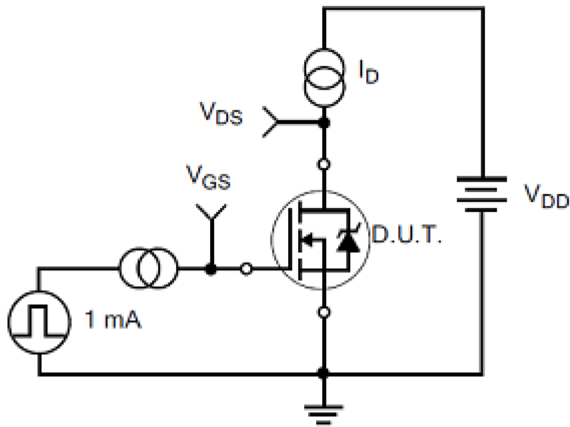


Figure 13 Gate Charge Waveforms

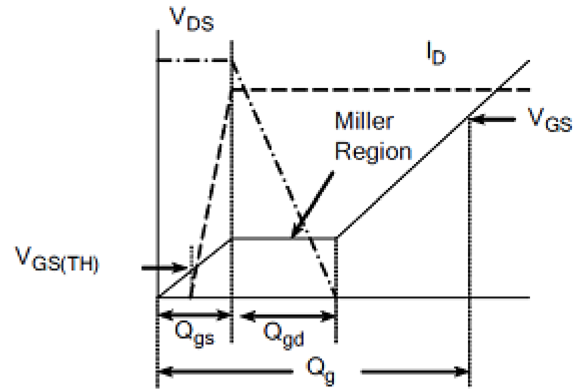


Figure 14 Resistive Switching Test Circuit

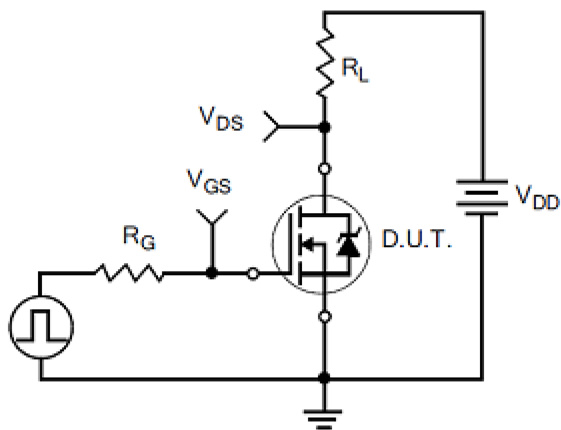


Figure 15 Resistive Switching Waveforms

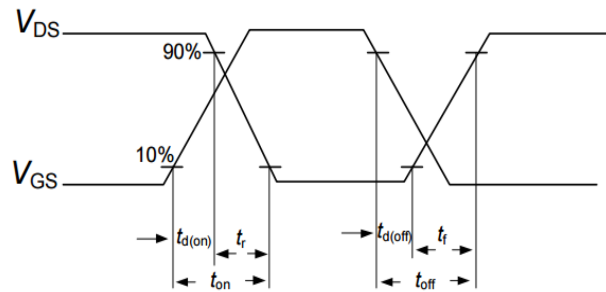


Figure 16 Diode Reverse Recovery Test Circuit

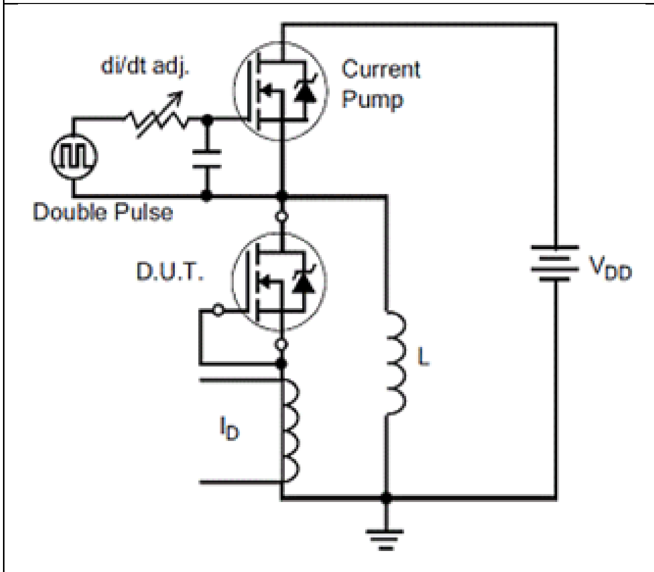


Figure 17 Diode Reverse Recovery Waveform

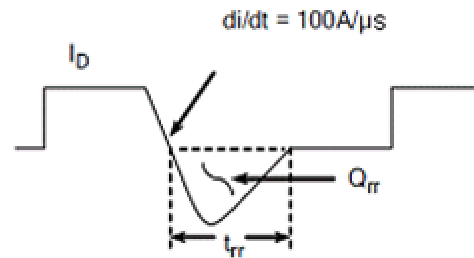


Figure 18 Unclamped Inductive Switching Test Circuit

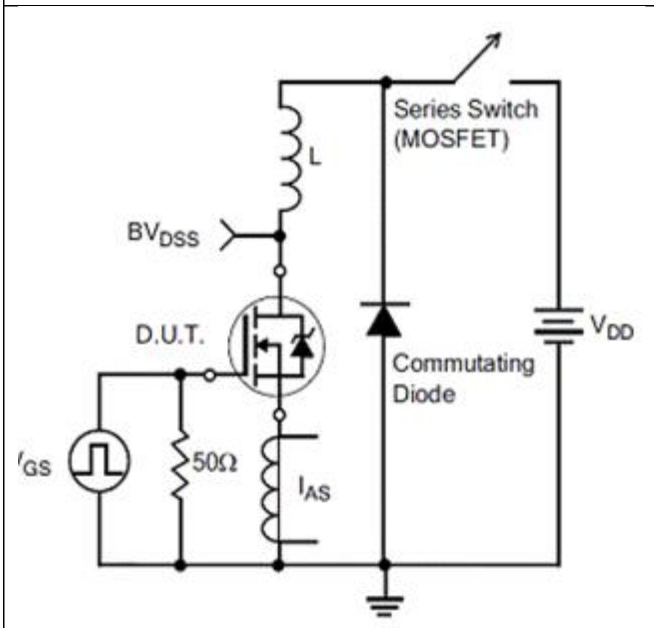
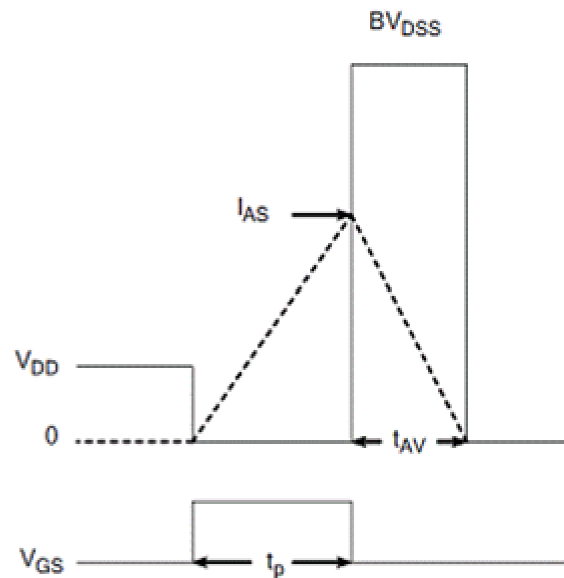
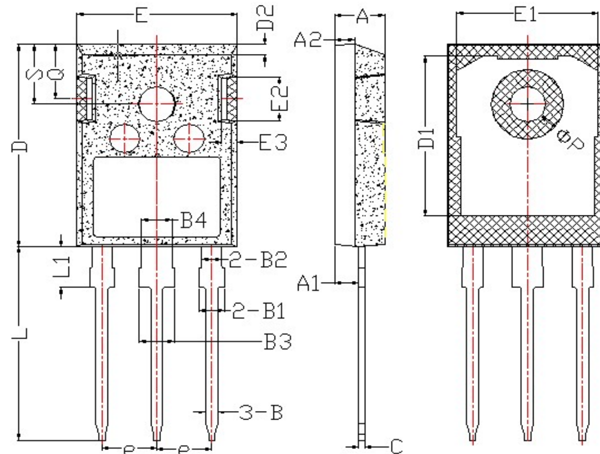


Figure 19 Unclamped Inductive Switching Waveform



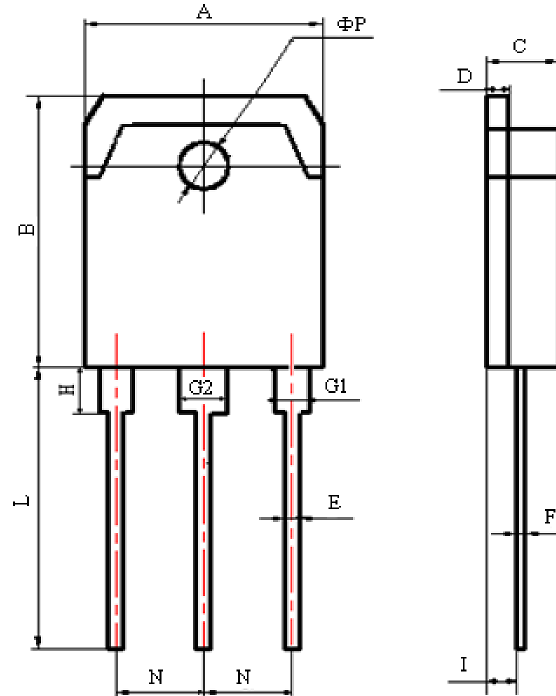
Package Description



Items	Values(mm)	
	MIN	MAX
A	4.6	5.2
A1	2,2	2.6
B	0.9	1.4
B1	1.75	2.35
B2	1.75	2.15
B3	2.8	3.35
B4	2.8	3.15
C	0.5	0.7
D	20.60	21.30
D1	16	18
E	15.5	16.10
E1	13	14.7
E2	3.80	5.3
E3	0.8	2.60
e	5.2	5.7
L	19	20.5
L1	3.9	4.6
Φ_P	2.5	3.70
Q	5.2	6.00
S	5.8	6.6

TO-247 Package

Package Description



Items	Values(mm)	
	MIN	MAX
A	15.00	16.00
B	19.20	20.60
C	4.60	5.00
D	1.40	1.60
E	0.90	1.10
F	0.50	0.70
G1	2.00	2.20
G2	3.00	3.20
H	3.00	3.70
I	1.20	1.70
	2.70	2.90
L	19.00	21.00
N	5.25	5.65
ϕ P	3.10	3.30

TO-3PN Package

NOTE:

1. Exceeding the maximum ratings of the device in performance may cause damage to the device, even the permanent failure, which may affect the dependability of the machine. Please do not exceed the absolute maximum ratings of the device when circuit designing.
2. When installing the heat sink, please pay attention to the torsional moment and the smoothness of the heat sink.
3. MOSFETs is the device which is sensitive to the static electricity, it is necessary to protect the device from being damaged by the static electricity when using it.
4. Shanghai Jerrett reserves the right to make changes in this specification sheet and is subject to change without prior notice.