



上海捷瑞德半导体
Jerrett Semiconductor

JR50N30
Power MOSFET

1. Description

JR50N30, the silicon N-channel Enhanced MOSFETs, is obtained by advanced MOSFET technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor is suitable device for SMPS, high speed switching and general purpose applications.

KEY CHARACTERISTICS

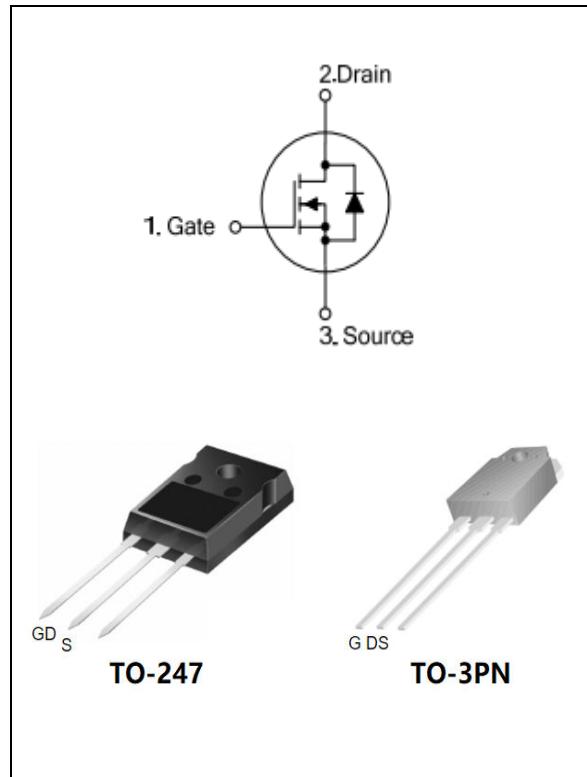
Parameter	Value	Unit
V _{DSS@Tj.max}	300	V
I _D	50	A
R _{DSS(ON).Typ}	53	mΩ

FEATURES

- Fast Switching
- Low Crss
- 100% avalanche tested
- Improved dv/dt capability
- RoHS product

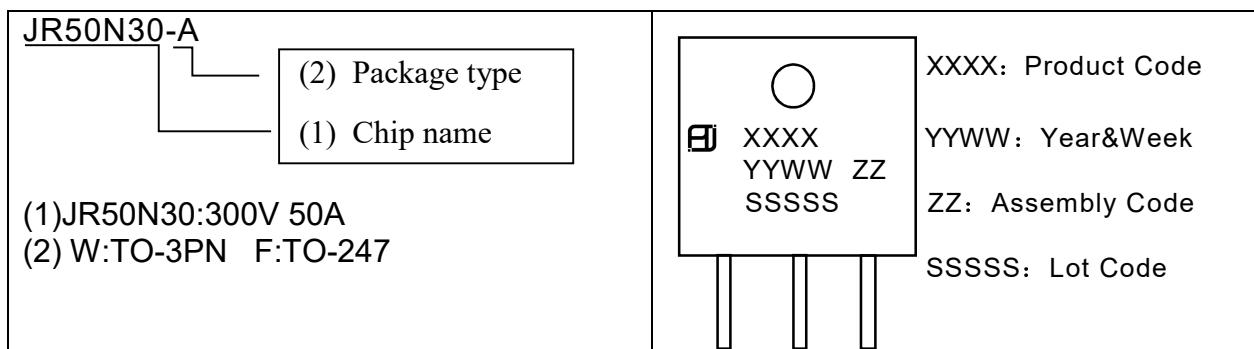
APPLICATIONS

- High frequency switching mode power supply



ORDERING INFORMATION

Ordering Codes	Package	Product Code	Packing
JR50N30-W	TO-3PN	JR50N30	Tube
JR50N30-F	TO-247		Tube





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2. ABSOLUTE RATINGS

at $T_c = 25^\circ\text{C}$, unless otherwise specified

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	300	V
I_D	Continuous Drain Current	50	A
	Continuous Drain Current $T_c = 100^\circ\text{C}$	31	A
I_{DM}	Pulsed Drain Current(Note1)	200	A
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy(Note2)	1800	mJ
dv/dt	Peak Diode Recovery dv/dt (Note3)	5.0	V/ns
P_D	Power Dissipation TO-3PN TO-247	300	W
	Derating Factor above 25°C	2.5	W/ $^\circ\text{C}$
T_J, T_{stg}	Operating Junction and Storage Temperature Range	150, -55 to 150	$^\circ\text{C}$
T_L	Maximum Temperature for Soldering	300	$^\circ\text{C}$

3. Thermal characteristics

Thermal characteristics (No FullPAK) TO-3PN TO-247

Symbol	Parameter	RATINGS	Units
$R_{\theta JC}$	Junction-to-Case	0.41	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient	40	$^\circ\text{C}/\text{W}$



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4. Electrical Characteristics

at $T_C = 25^\circ\text{C}$, unless otherwise specified

OFF Characteristics						
Symbol	Parameter	Test Conditions	Values			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$	300	--	--	V
I_{DSS}	Drain to Source Leakage Current	$V_{DS} = 300\text{V}$, $V_{GS} = 0\text{V}$, $T_j = 25^\circ\text{C}$	--	--	1	μA
		$V_{DS} = 240\text{V}$, $V_{GS} = 0\text{V}$, $T_j = 125^\circ\text{C}$	--	--	100	μA
$I_{GSS(F)}$	Gate to Source Forward Leakage	$V_{GS} = +30\text{V}$	--	--	100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	$V_{GS} = -30\text{V}$	--	--	100	nA

ON Characteristics						
Symbol	Parameter	Test Conditions	Values			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	$V_{GS}=10\text{V}$, $I_D=25\text{A}$ (Note4)	--	53	63	$\text{m}\Omega$
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$ (Note4)	2.0	--	4.0	V
g_{fs}	Forward Transconductance	$V_{DS}=15\text{V}$, $I_D = 25\text{A}$ (Note4)	18	--	--	S

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Values			Units
			Min.	Typ.	Max.	
R_g	Gate resistance	$f = 1.0\text{MHz}$	--	--	2	Ω
C_{iss}	Input Capacitance	$V_{GS} = 0\text{V}$ $V_{DS} = 25\text{V}$ $f = 1.0\text{MHz}$	--	--	8900	PF
C_{oss}	Output Capacitance		--	--	860	
C_{rss}	Reverse Transfer Capacitance		--	--	80	



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Switching Characteristics

Symbol	Parameter	Test Conditions	Values			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	ID =50A VDD = 150V VGS = 10V RG =20Ω	--	--	80	ns
t_r	Rise Time		--	--	100	
$t_{d(OFF)}$	Turn-Off Delay Time		--	--	160	
t_f	Fall Time		--	--	120	
Q_g	Total Gate Charge	ID =50A VDD =240V VGS = 10V	--	--	100	nC
Q_{gs}	Gate to Source Charge		--	--	30	
Q_{gd}	Gate to Drain ("Miller")Charge		--	--	50	

Source-Drain Diode Characteristics

Symbol	Parameter	Test Conditions	Values			Units
			Min.	Typ.	Max.	
I_s	Continuous Source Current (Body Diode)	TC=25 °C	--	--	50	A
I_{sM}	Maximum Pulsed Current (Body Diode)		--	--	200	A
V_{SD}	Diode Forward Voltage	IS=50A, VGS=0V(Note4)	--	--	1.2	V
T_{rr}	Reverse Recovery Time	IS=50A, T _j = 25°C dI/dt=100A/us, VGS=0V	--	460	--	ns
Q_{rr}	Reverse Recovery Charge		--	9562	--	nC

Note1: Pulse width limited by maximum junction temperature

Note2: L=20mH, VDs=50V, Start TJ=25°C

Note3: ISD =50A,di/dt ≤100A/us,VDD≤BVDS, Start TJ=25°C

Note4: Pulse width tp≤300μs, δ≤2%



5. Characteristics Curves

Figure 1a Safe Operating Area

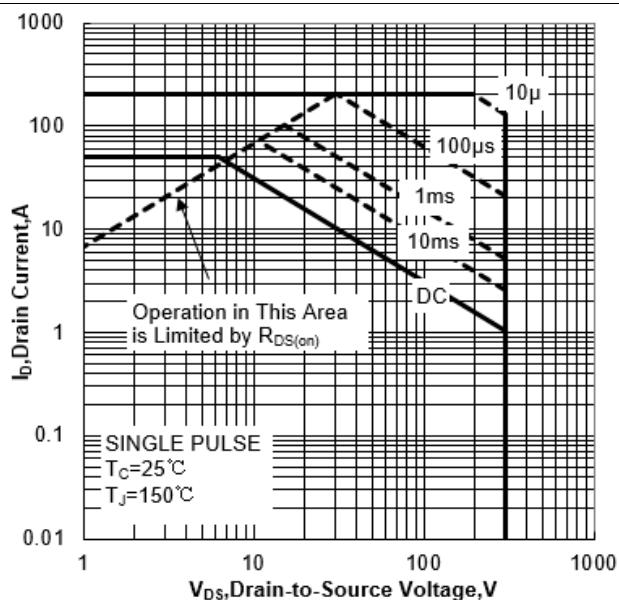


Figure 2 Power Dissipation

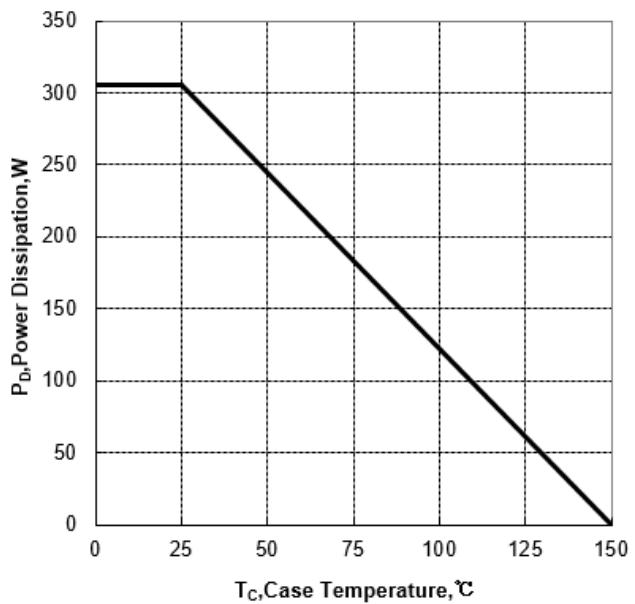


Figure 3 Max Thermal Impedance

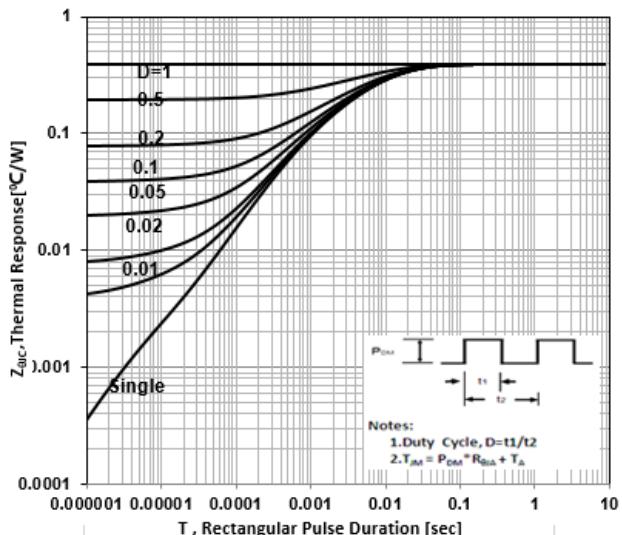
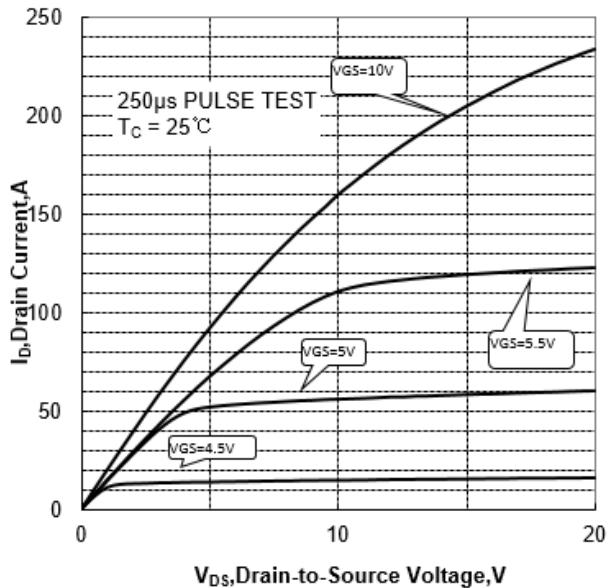


Figure 4 Typical Output Characteristics





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Figure 5 Typical Transfer Characteristics

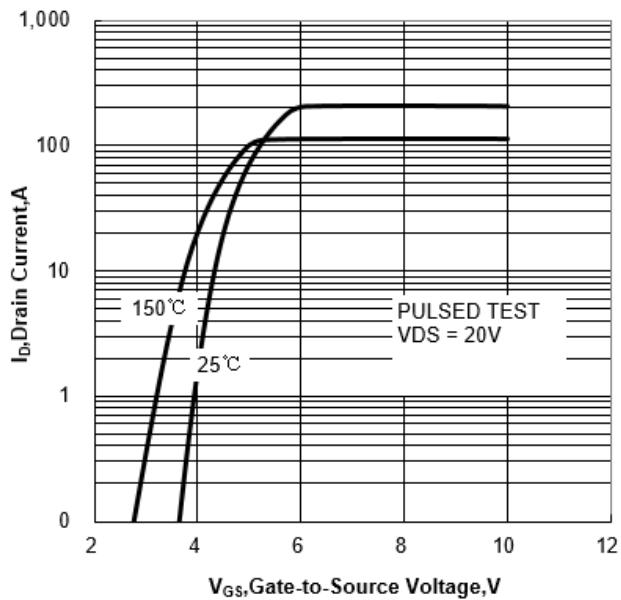


Figure 6 Typical Drain to Source ON Resistance vs Drain Current

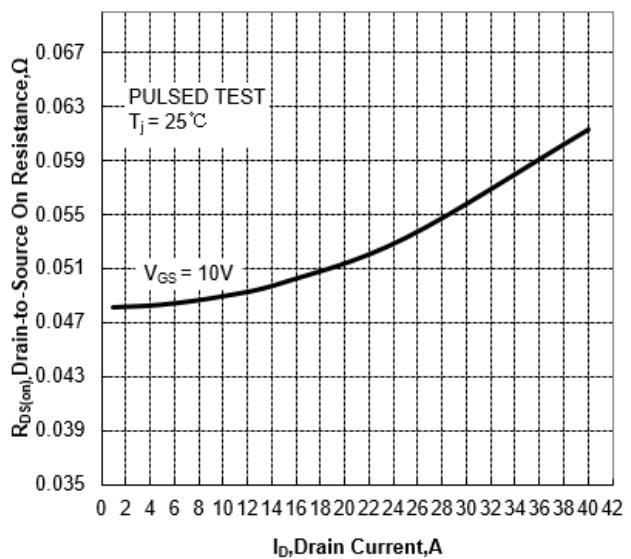


Figure 7 Typical Drian to Source on Resistance vs Junction Temperature

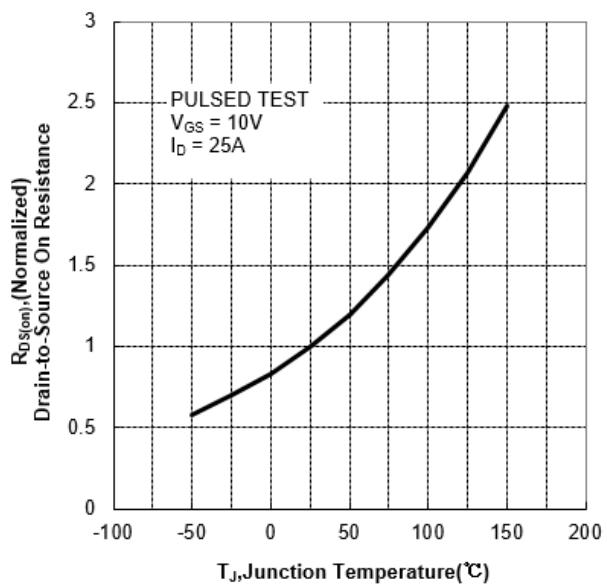
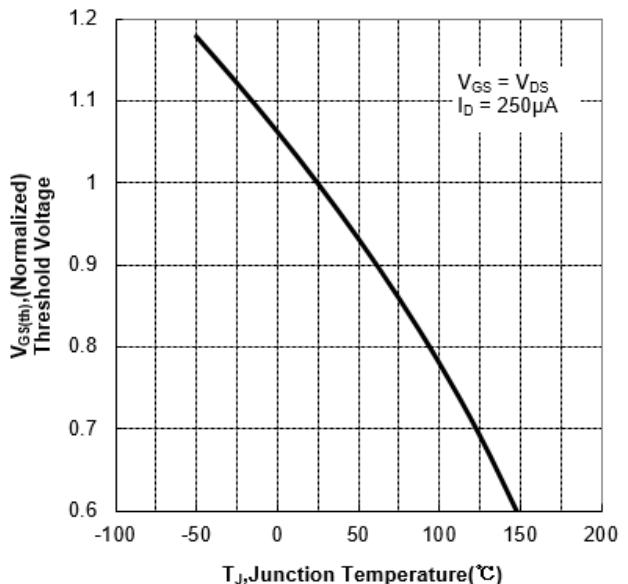


Figure 8 Typical Threshold Voltage vs Junction Temperature





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Figure 9 Typical Breakdown Voltage vs Junction Temperature

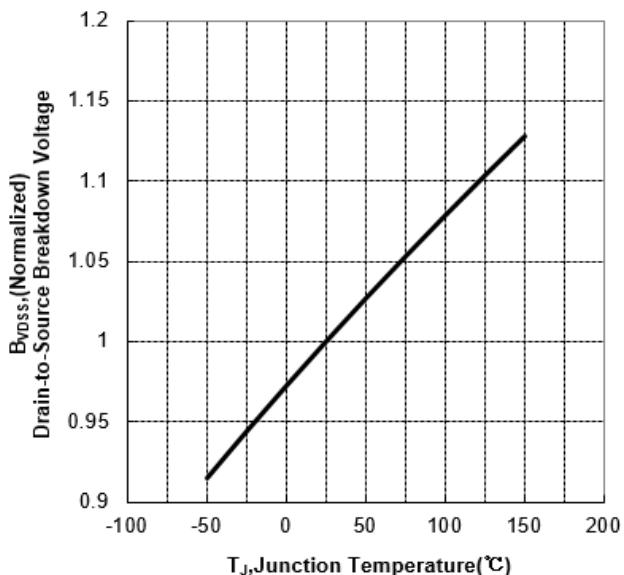


Figure 10 Typical Capacitance vs Drain to Source Voltage

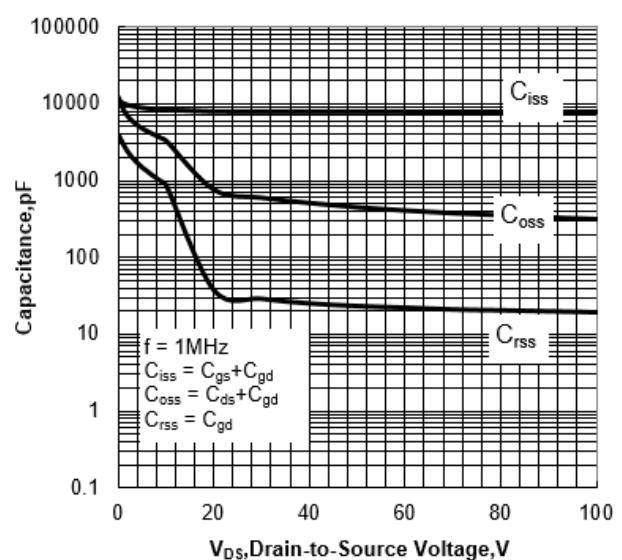
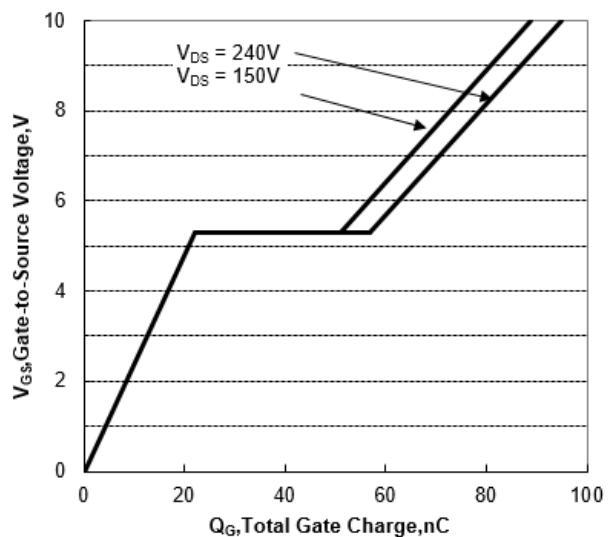


Figure 11 Typical Gate Charge vs Gate to Source Voltage





6. Test Circuit and Waveform

Figure 12 Gate Charge Test Circuit

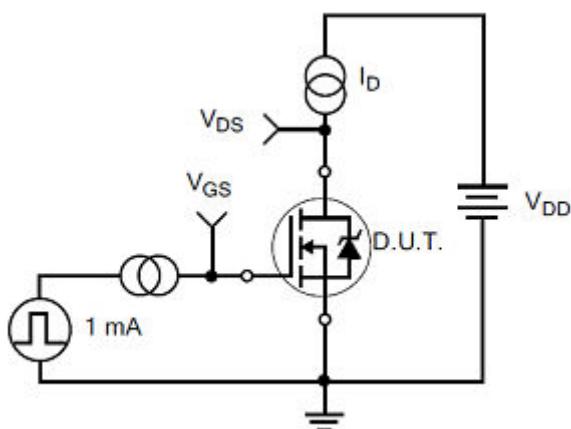


Figure 13 Gate Charge Waveforms

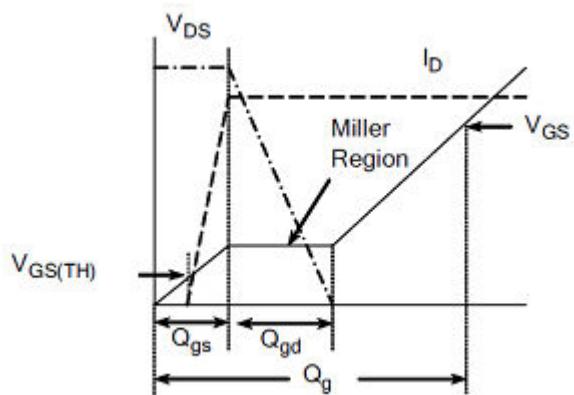


Figure 14 Resistive Switching Test Circuit

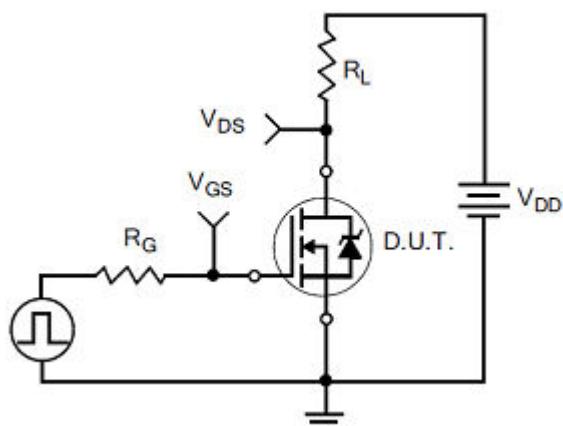
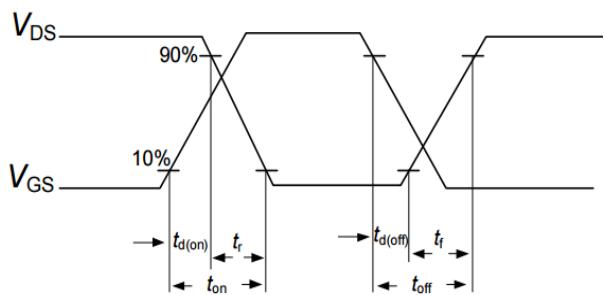


Figure 15 Resistive Switching Waveforms





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Figure 16 Diode Reverse Recovery Test Circuit

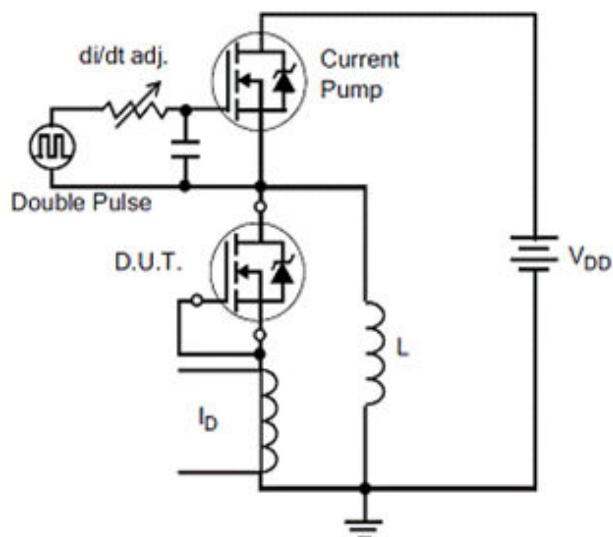


Figure 17 Diode Reverse Recovery Waveform

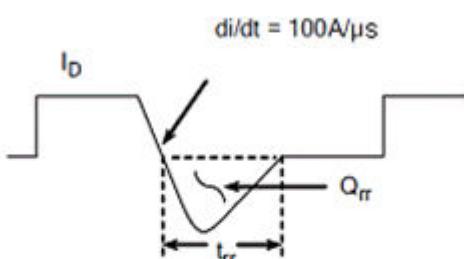


Figure 18 Unclamped Inductive Switching Test Circuit

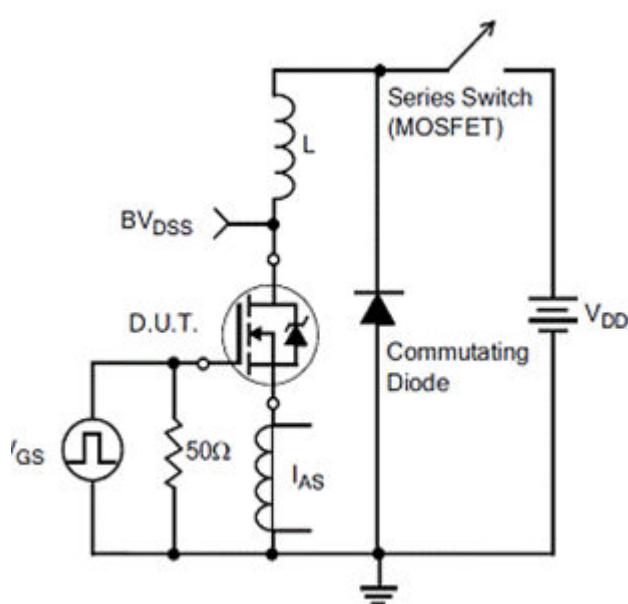
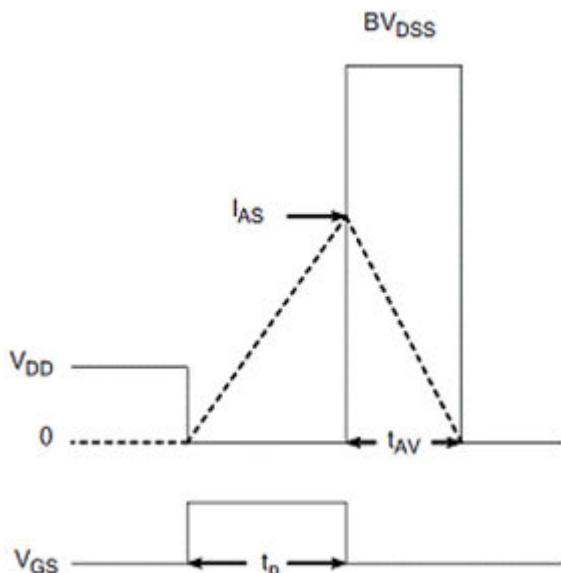
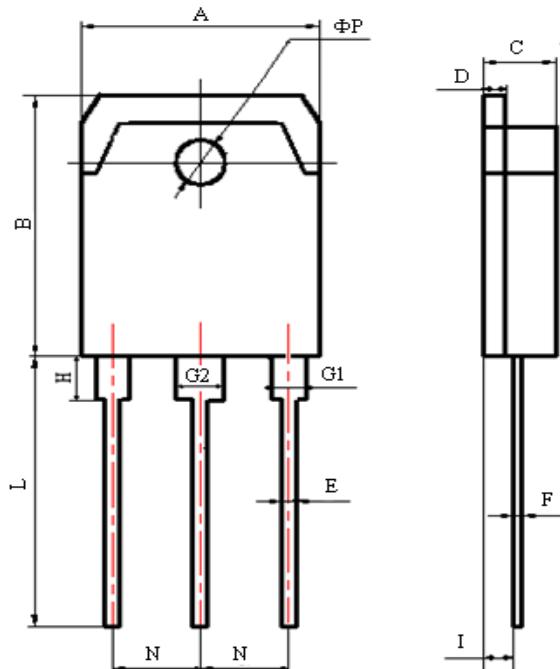


Figure 19 Unclamped Inductive Switching Waveform



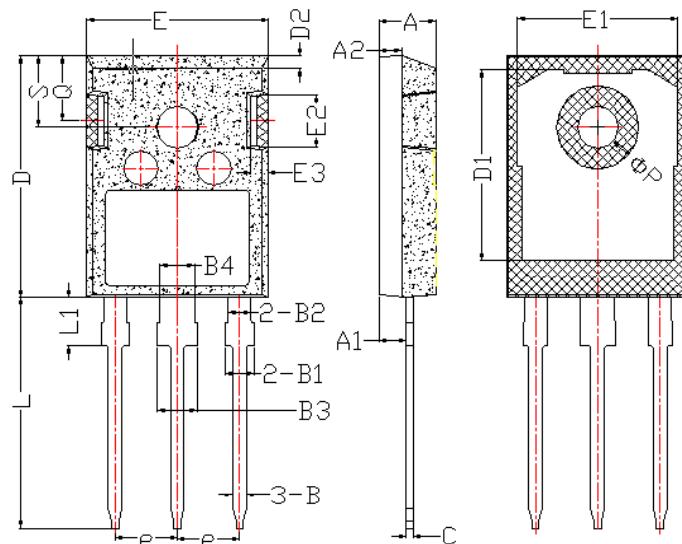


7. Package Description



Items	Values(mm)	
	MIN	MAX
A	15.00	16.00
B	19.20	20.60
C	4.60	5.00
D	1.40	1.60
E	0.90	1.10
F	0.50	0.70
G1	2.00	2.20
G2	3.00	3.20
H	3.00	3.70
I	1.20	1.70
	2.70	2.90
L	19.00	21.00
N	5.25	5.65
Φ P	3.10	3.30

TO-3PN Package



Items	Values(mm)	
	MIN	MAX
A	4.6	5.2
A1	2.2	2.6
B	0.9	1.4
B1	1.75	2.35
B2	1.75	2.15
B3	2.8	3.35
B4	2.8	3.15
C	0.5	0.7
D	20.60	21.30
D1	16	18
E	15.5	16.10
E1	13	14.7
E2	3.80	5.3
E3	0.8	2.60
e	5.2	5.7
L	19	20.5
L1	3.9	4.6
ΦP	3.3	3.70
Q	5.2	6.00
S	5.8	6.6

TO-247 Package



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NOTE:

1. Exceeding the maximum ratings of the device in performance may cause damage to the device, even the permanent failure, which may affect the dependability of the machine. Please do not exceed the absolute maximum ratings of the device when circuit designing.
2. When installing the heat sink, please pay attention to the torsional moment and the smoothness of the heat sink.
3. MOSFETs is the device which is sensitive to the static electricity, it is necessary to protect the device from being damaged by the static electricity when using it.
4. Shanghai Jerrett reserves the right to make changes in this specification sheet and is subject to change without prior notice.