



上海捷瑞德半导体
Jerrett Semiconductor

JR4N65A
Power MOSFET

1. Description

JR4N65A, the silicon N-channel Enhanced MOSFETs, is obtained by advanced MOSFET technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor is suitable device for SMPS, high speed switching and general purpose applications.

KEY CHARACTERISTICS

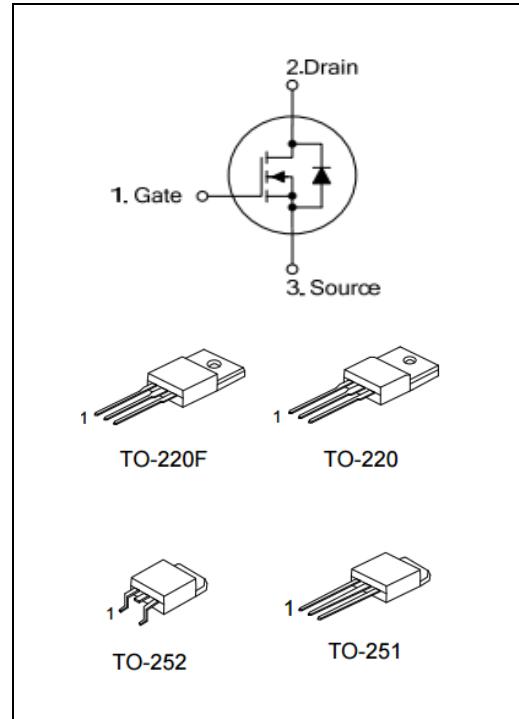
Parameter	Value	Unit
V_{DS}	650	V
I_D	4	A
$R_{DS(ON).Typ}$	2.4	Ω

FEATURES

- Fast Switching
- Low Crss
- 100% avalanche tested
- Improved dv/dt capability
- RoHS product

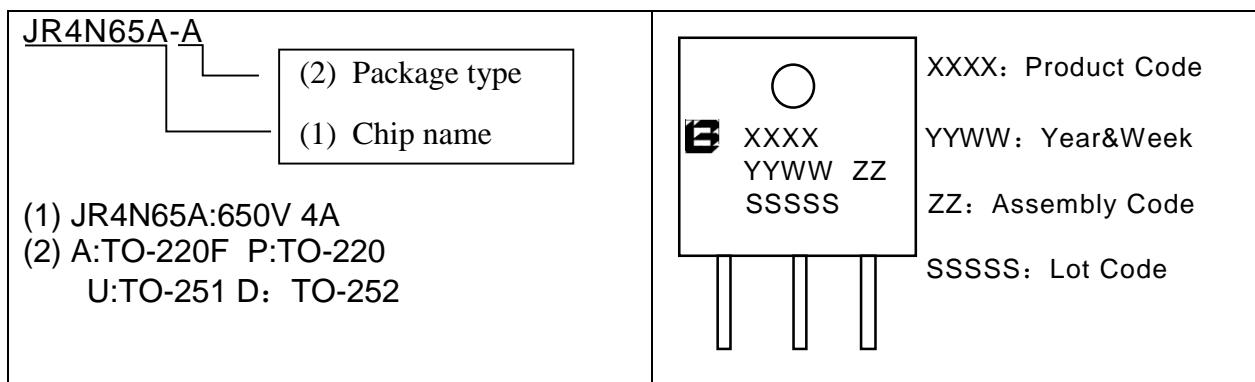
APPLICATIONS

- High frequency switching mode power supply



ORDERING INFORMATION

Ordering Codes	Package	Product Code	Packing
JR4N65A-P	TO-220	4N65A	Tube
JR4N65A-A	TO-220F		Tube
JR4N65A-U	TO-251		Tube
JR4N65A-D	TO-252		Tape Reel





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2. ABSOLUTE RATINGS

at $T_c = 25^\circ\text{C}$, unless otherwise specified

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	650	V
I_D	Continuous Drain Current	4	A
	Continuous Drain Current $T_c = 100^\circ\text{C}$	2.5	A
I_{DM}	Pulsed Drain Current(Note1)	16	A
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy(Note2)	205	mJ
dv/dt	Peak Diode Recovery dv/dt (Note3)	5.0	V/ns
P_D	Power Dissipation No FullPAK	75	W
	Derating Factor above 25°C	0.77	W/ $^\circ\text{C}$
P_D	Power Dissipation FullPAK	30	W
	Derating Factor above 25°C	0.29	W/ $^\circ\text{C}$
T_J, T_{stg}	Operating Junction and Storage Temperature Range	150, -55 to 150	$^\circ\text{C}$
T_L	Maximum Temperature for Soldering	300	$^\circ\text{C}$

3. Thermal characteristics

Thermal characteristics No FullPAK

Symbol	Parameter	RATINGS	Units
$R_{\theta JC}$	Junction-to-Case	1.3	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient	62.5	$^\circ\text{C}/\text{W}$

Thermal characteristics FullPAK

Symbol	Parameter	RATINGS	Units
$R_{\theta JC}$	Junction-to-Case	3.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient	62.5	$^\circ\text{C}/\text{W}$



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4. Electrical Characteristics

at $T_c = 25^\circ\text{C}$, unless otherwise specified

OFF Characteristics						
Symbol	Parameter	Test Conditions	Values			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$	650	--	--	V
$\Delta V_{DSS}/\Delta T_J$	Bvdss Temperature Coefficient	$ID=250\mu\text{A}$, Reference 25°C	--	0.45	--	$\text{V}/^\circ\text{C}$
I_{DSS}	Drain to Source Leakage Current	$V_{DS}=650\text{V}$, $V_{GS}=0\text{V}$, $T_j = 25^\circ\text{C}$	--	--	1	μA
		$V_{DS}=520\text{V}$, $V_{GS}=0\text{V}$, $T_j = 125^\circ\text{C}$	--	--	10	μA
$I_{GSS(F)}$	Gate to Source Forward Leakage	$V_{GS} = +30\text{V}$	--	--	100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	$V_{GS} = -30\text{V}$	--	--	-100	nA

ON Characteristics						
Symbol	Parameter	Test Conditions	Values			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	$V_{GS}=10\text{V}$, $ID=2\text{A}$ (Note4)	--	2.4	2.9	Ω
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $ID = 250\mu\text{A}$ (Note4)	2.0	3.0	4.0	V
g_{fs}	Forward Transconductance	$V_{DS}=15\text{V}$, $ID = 4\text{A}$ (Note4)	--	2.4	--	S

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Values			Units
			Min.	Typ.	Max.	
R_g	Gate resistance	$f = 1.0\text{MHz}$	--	3.3	--	Ω
C_{iss}	Input Capacitance	$V_{GS} = 0\text{V}$ $V_{DS} = 25\text{V}$ $f = 1.0\text{MHz}$	--	607	--	PF
C_{oss}	Output Capacitance		--	50	--	
C_{rss}	Reverse Transfer Capacitance		--	1.5	--	



Switching Characteristics

Symbol	Parameter	Test Conditions	Values			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	ID = 4A VDD = 325V VGS = 10V	--	18	--	ns
t_r	Rise Time		--	16	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	35	--	
t_f	Fall Time		--	38	--	
Q_g	Total Gate Charge	ID = 4A VDD = 520V VGS = 10V	--	15.8	--	nC
Q_{gs}	Gate to Source Charge		--	5.4	--	
Q_{gd}	Gate to Drain ("Miller")Charge		--	3.7	--	

Source-Drain Diode Characteristics

Symbol	Parameter	Test Conditions	Values			Units
			Min.	Typ.	Max.	
I_s	Continuous Source Current (Body Diode)	TC=25 °C	--	--	4	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	16	A
V_{SD}	Diode Forward Voltage	IS=4A, VGS=0V(Note4)	--	--	1.2	V
T_{rr}	Reverse Recovery Time	IS=4A, T _j = 25°C dI/dt=100A/us, VGS=0V	--	220	--	ns
Q_{rr}	Reverse Recovery Charge		--	1020	--	nC

Note1: Pulse width limited by maximum junction temperature

Note2: L=20mH, VDs=50V, Start TJ=25°C

Note3: ISD =4A,di/dt ≤100A/us,VDD≤BVDS, Start TJ=25°C

Note4: Pulse width tp≤300μs, δ≤2%



5. Characteristics Curves

Figure 1a Safe Operating Area (No FullPAK)

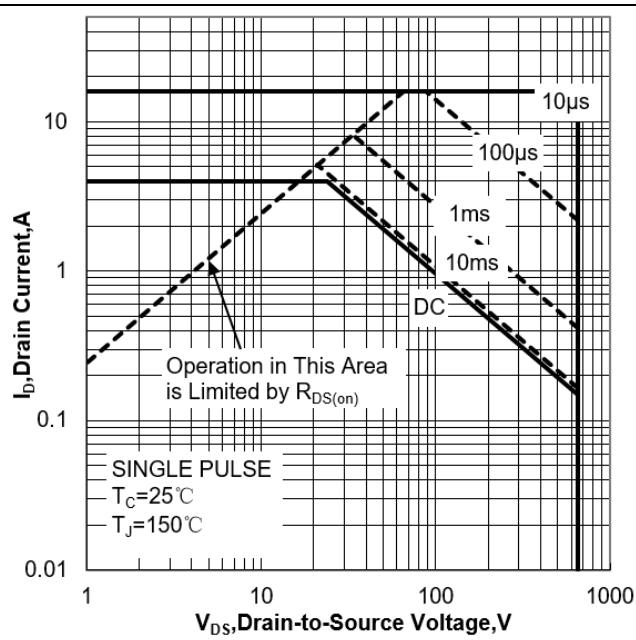


Figure 1b Safe Operating Area (FullPAK)

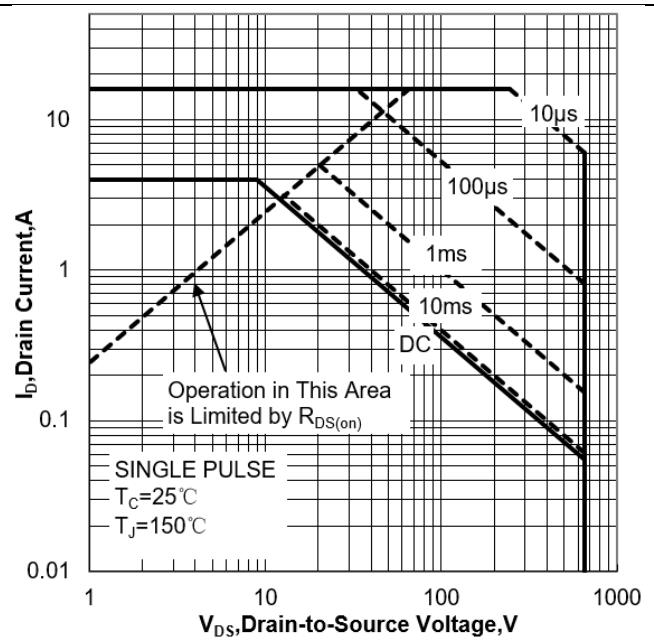


Figure 2a Power Dissipation (No FullPAK)

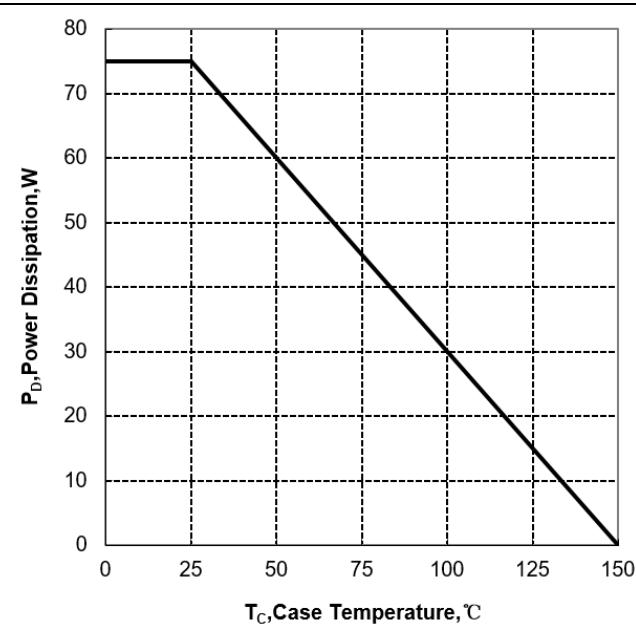


Figure 2b Power Dissipation (FullPAK)

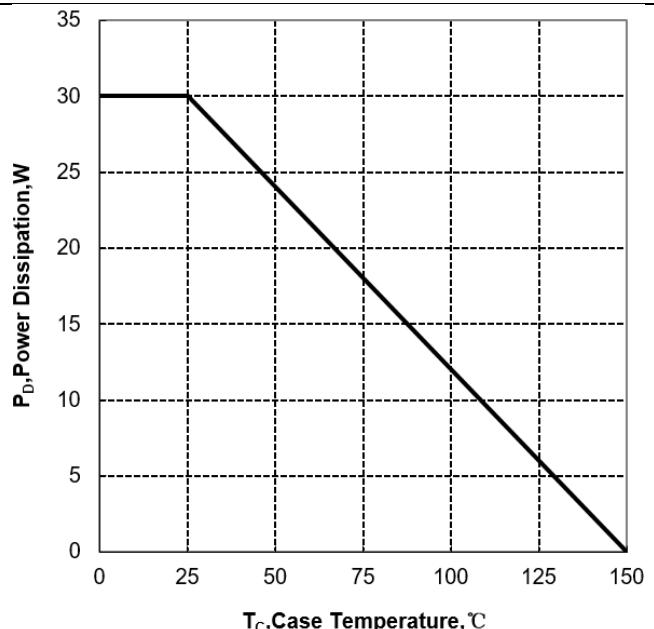




Figure 3a Max Thermal Impedance (No FullPAK)

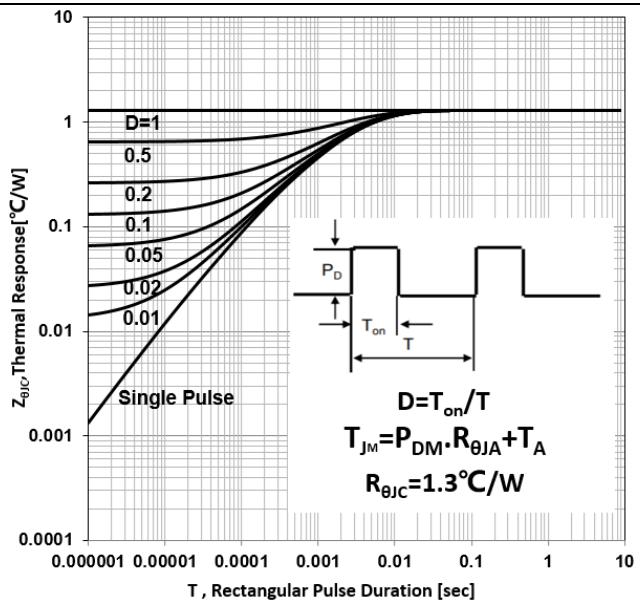


Figure 3b Max Thermal Impedance (FullPAK)

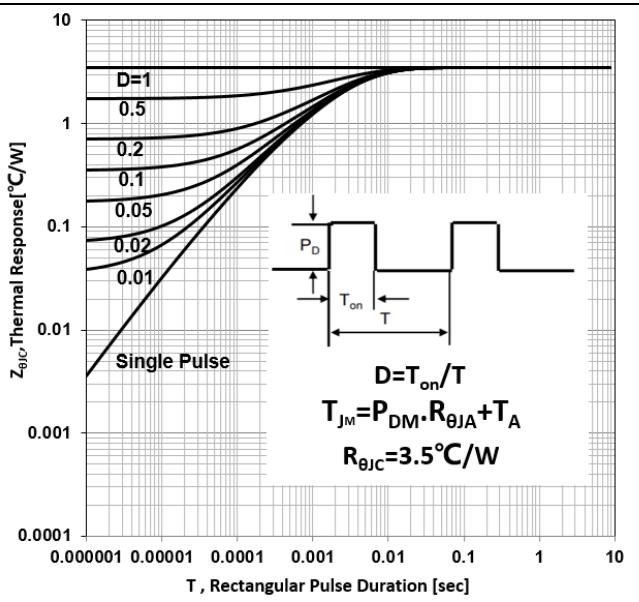


Figure 4 Typical Output Characteristics

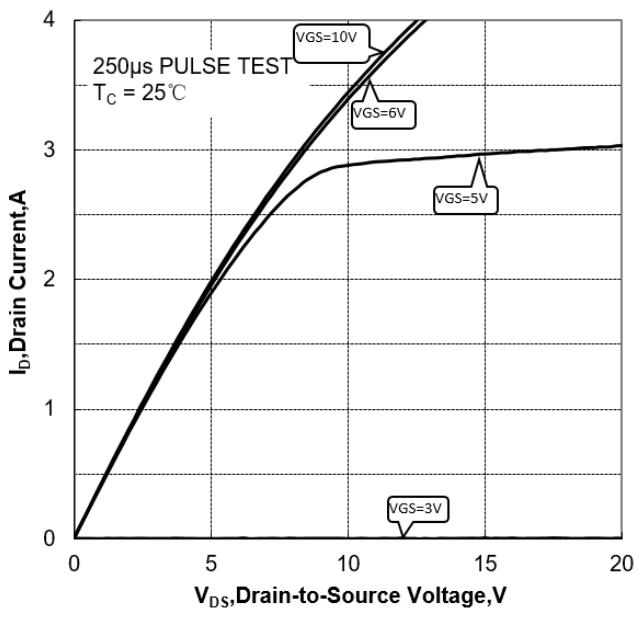
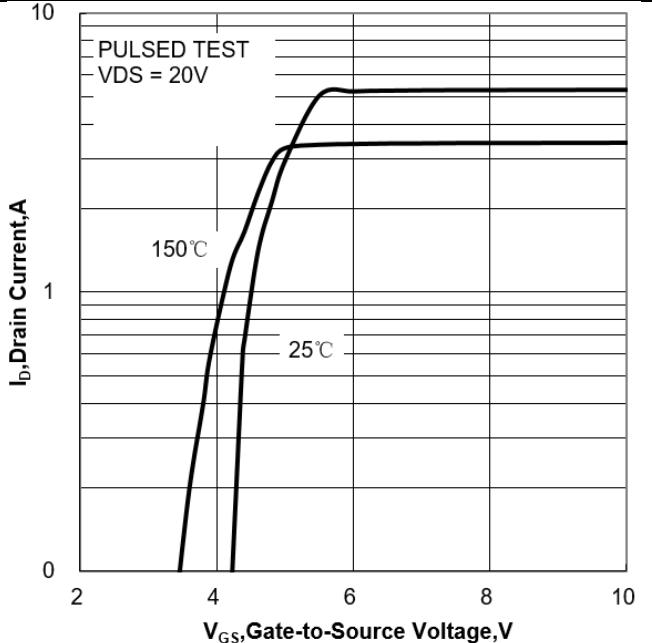


Figure 5 Typical Transfer Characteristics





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Figure 6 Typical Drain to Source ON Resistance vs Drain Current

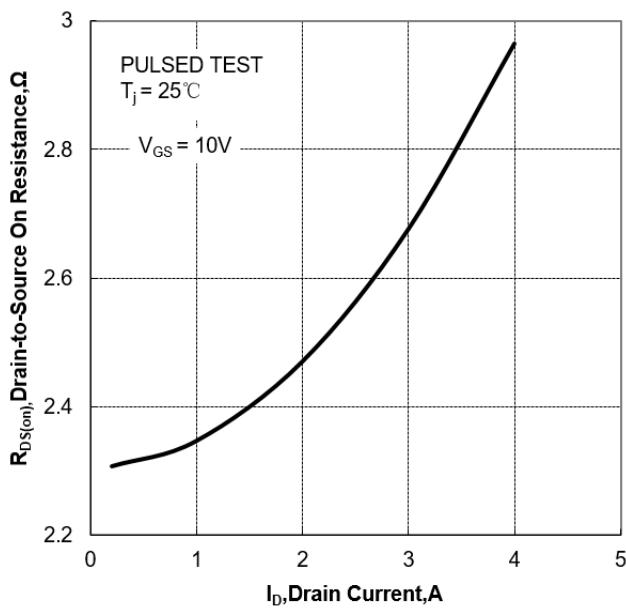


Figure 7 Typical Drian to Source on Resistance vs Junction Temperature

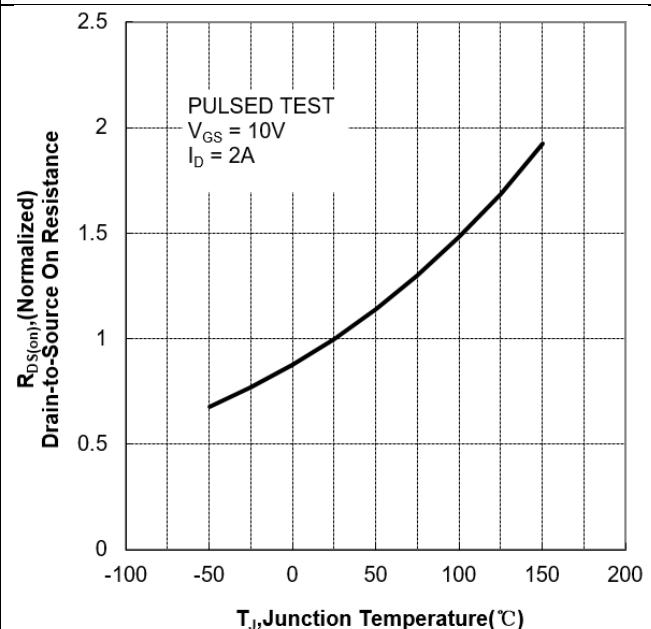


Figure 8 Typical Threshold Voltage vs Junction Temperature

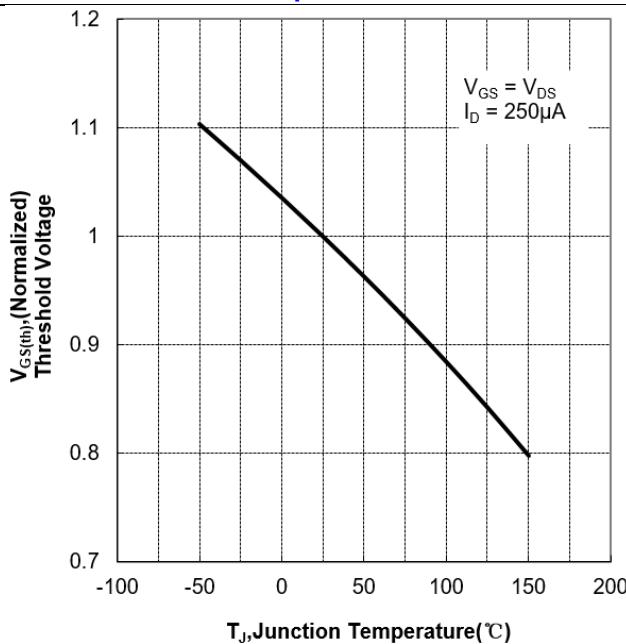


Figure 9 Typical Breakdown Voltage vs Junction Temperature

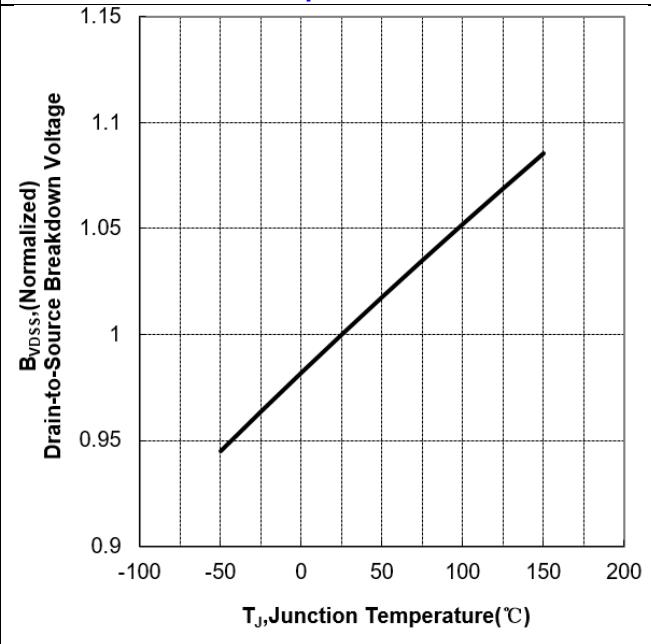




Figure 10 Typical Capacitance vs Drain to Source Voltage

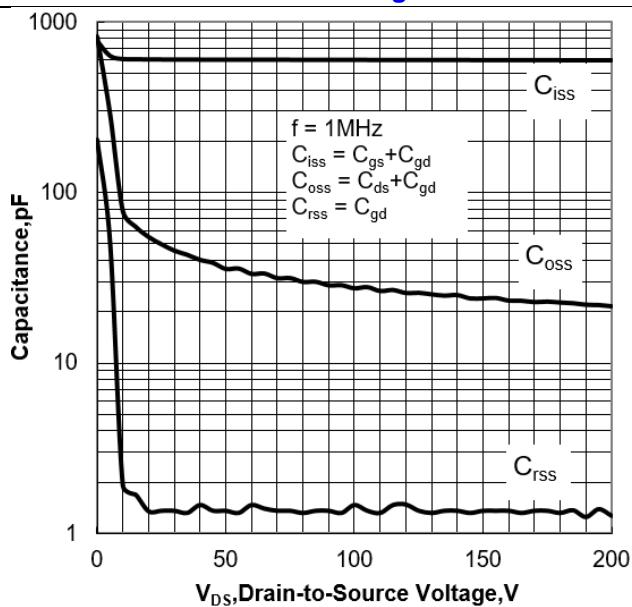
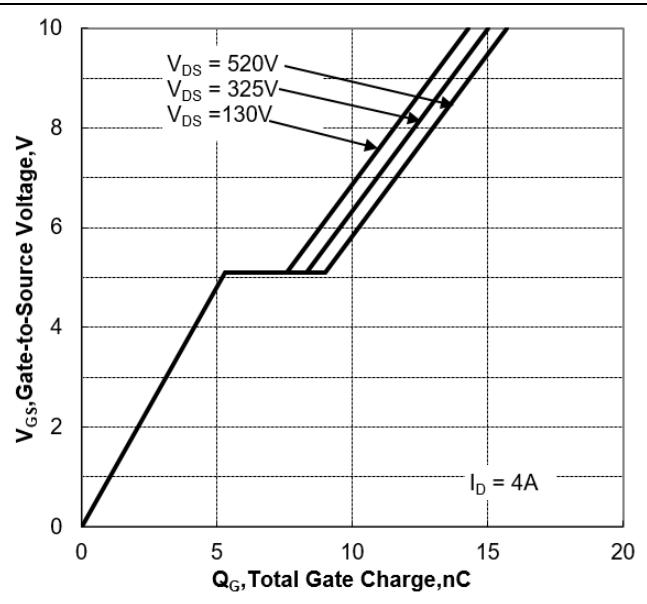


Figure 11 Typical Gate Charge vs Gate to Source Voltage





6. Test Circuit and Waveform

Figure 12 Gate Charge Test Circuit

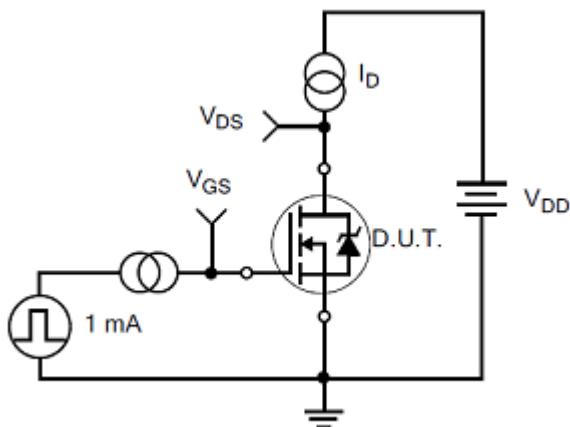


Figure 13 Gate Charge Waveforms

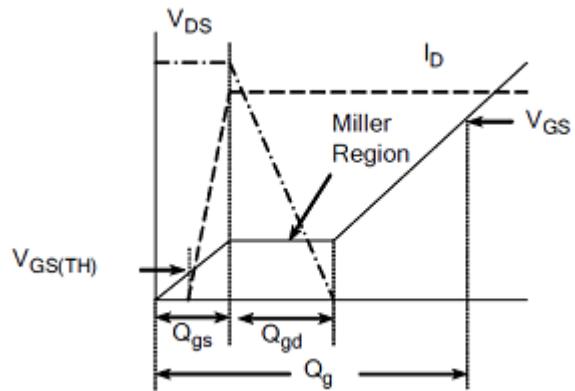


Figure 14 Resistive Switching Test Circuit

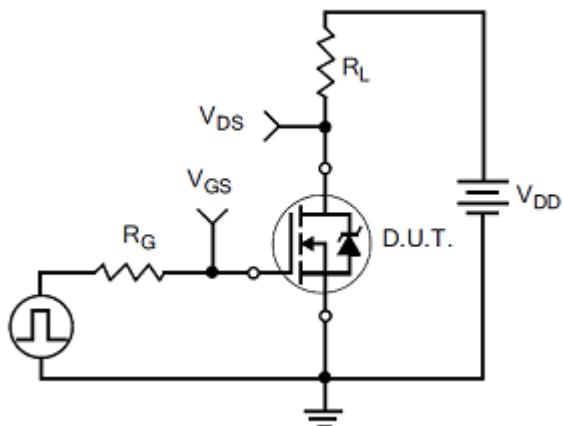


Figure 15 Resistive Switching Waveforms

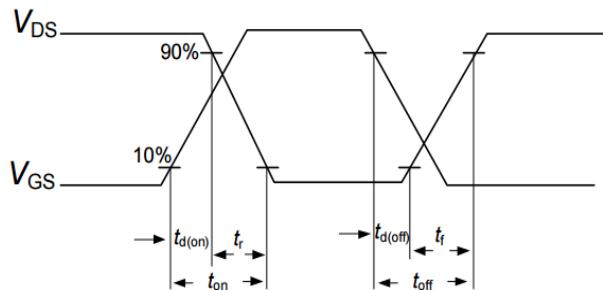




Figure 16 Diode Reverse Recovery Test Circuit

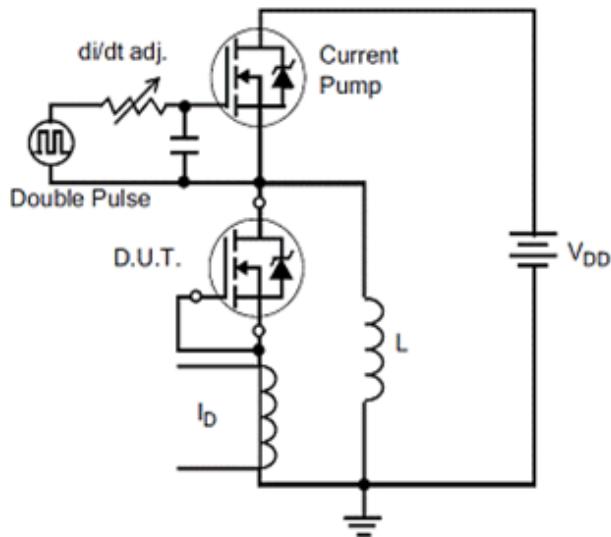


Figure 17 Diode Reverse Recovery Waveform

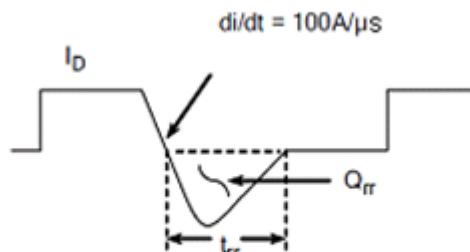


Figure 18 Unclamped Inductive Switching Test Circuit

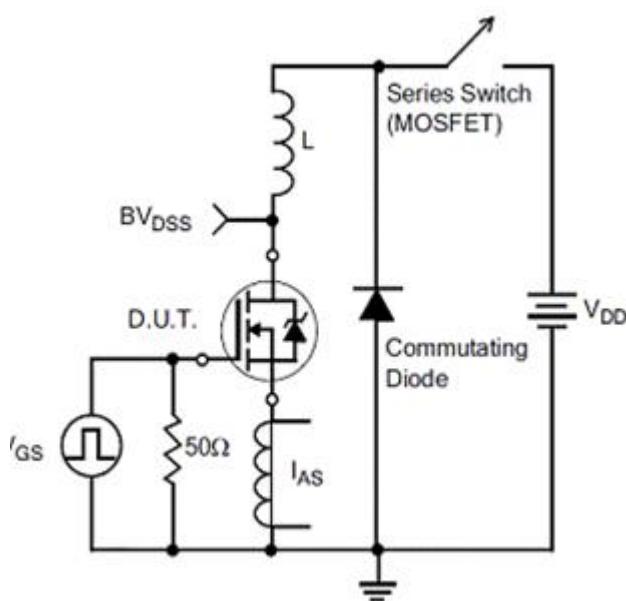
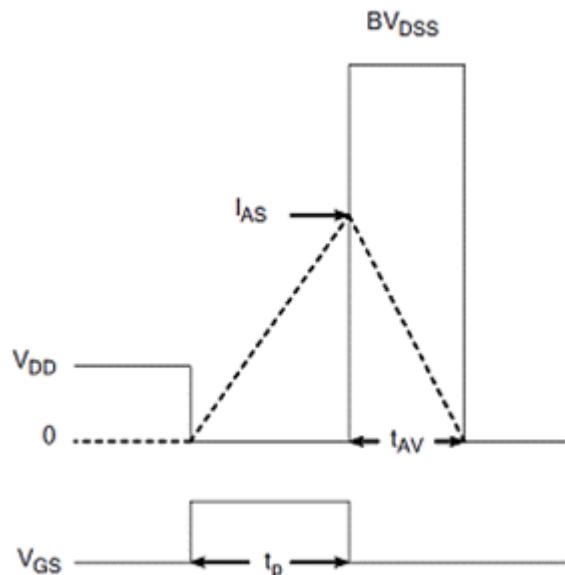
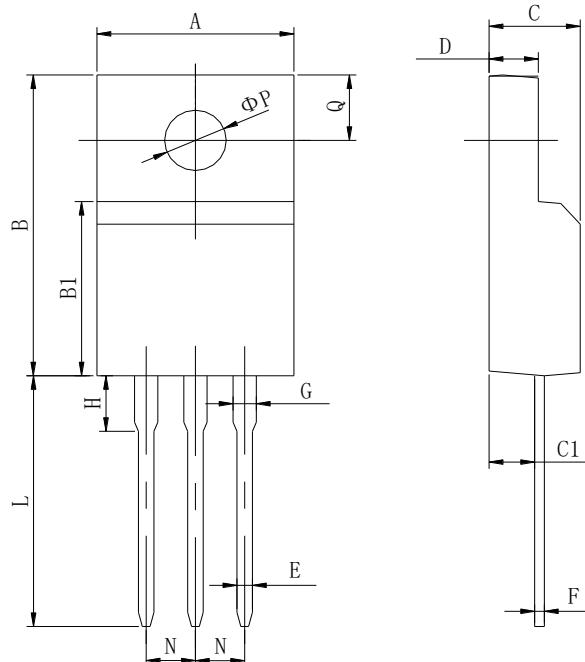


Figure 19 Unclamped Inductive Switching Waveform





7. Package Description



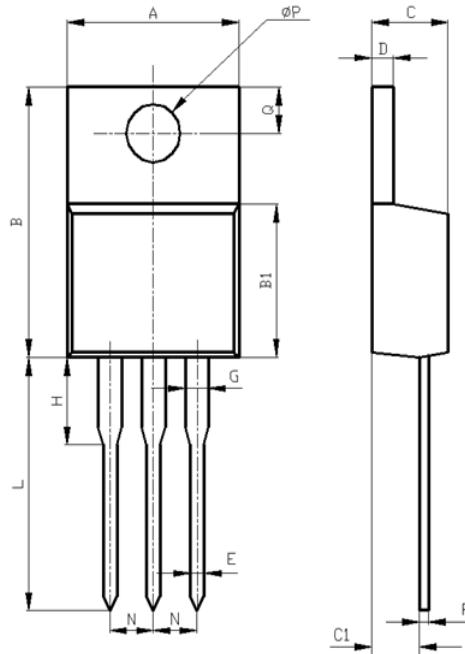
Items	Values(mm)	
	MIN	MAX
A	9.60	10.4
B	15.4	16.2
B1	8.90	9.50
C	4.30	4.90
C1	2.10	3.00
D	2.40	3.00
E	0.60	1.00
F	0.30	0.60
G	1.12	1.42
H	3.40	3.80
	1.60	2.90
L	12.0	14.0
N	2.34	2.74
Q	3.15	3.55
Φ P	2.90	3.30

TO-220F Package



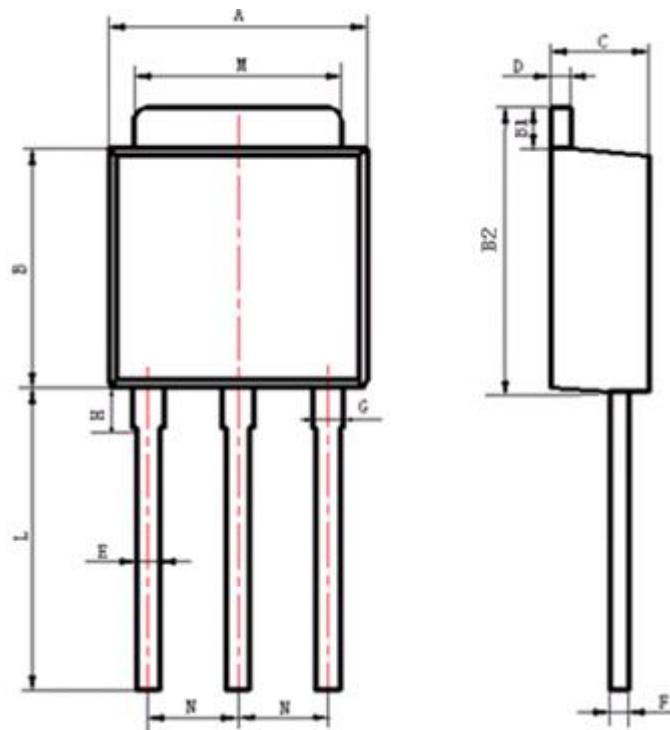
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Items	Values(mm)	
	MIN	MAX
A	9.60	10.6
B	15.0	16.0
B1	8.90	9.50
C	4.30	4.80
C1	2.30	3.10
D	1.20	1.40
E	0.70	0.90
F	0.30	0.60
G	1.17	1.37
H	2.70	3.80
L	12.6	14.8
N	2.34	2.74
Q	2.40	3.00
Ø P	3.50	3.90

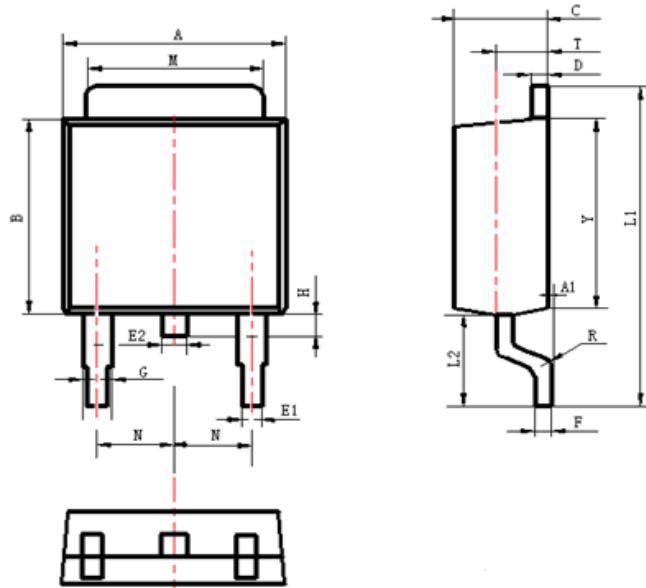
TO-220 Package



Items	Values(mm)	
	MIN	MAX
A	6.30	6.90
B	5.70	6.30
B1	1.00	1.20
B2	6.80	7.40
C	2.10	2.50
D	0.30	0.60
E	0.50	0.70
F	0.30	0.60
G	0.70	1.00
H	1.60	2.40
L*	3.9	4.3
M	5.10	5.50
N	2.09	2.49

*: adjustable

TO-251 Package



Items	Values(mm)	
	MIN	MAX
A	6.30	6.90
A1	0	0.13
B	5.70	6.30
C	2.10	2.50
D	0.30	0.60
E1	0.60	0.90
E2	0.70	1.00
F	0.30	0.60
G	0.70	1.20
L1	9.60	10.50
L2	2.70	3.10
H	0.60	1.00
M	5.10	5.50
N	2.09	2.49
R	0.3	
T	1.40	1.60
Y	5.10	6.30

TO-252 Package



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Power MOSFET

NOTE:

1. Exceeding the maximum ratings of the device in performance may cause damage to the device, even the permanent failure, which may affect the dependability of the machine. Please do not exceed the absolute maximum ratings of the device when circuit designing.
2. When installing the heat sink, please pay attention to the torsional moment and the smoothness of the heat sink.
3. MOSFETs is the device which is sensitive to the static electricity, it is necessary to protect the device from being damaged by the static electricity when using it.
4. Shanghai Jerrett reserves the right to make changes in this specification sheet and is subject to change without prior notice.