eMCP Datesheet

8GB eMMC + 8Gb (x32) LPDDR4 SDRAM

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Using This Document

This document is intended for hardware and software engineer’s general information on the XCBL4NVAM-QSNTF. Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

Revision History

Revision	Date	Description
Rev 1.0	2022/02/18	Create new document
Rev 1.1	2023/05/20	Update logo

Document Index

1. INTRODUCTION

XCBL4NVAM-QSNTF is a embedded Multi Chip Package Memory (eMCP) that integrated eMMC controller which combines 8GB NAND Flash and 8Gb LPDDR4 SDRAM by advanced SiP (System-in-a-Package) technology. XCBL4NVAM-QSNTF offers space saving advantage that could miniaturize your portable device, and it is conformed with Green regulations.

1.1 Application

- Compact DSC / CAR Black Box / Action Cam / 360 Cam
- Drone
- Wearable

1.2 Features

PRODUCT LIST

- XCBL4NVAM-QSNTF
  - eMMC: 8GB
  - LPDDR4 SDRAM: 8Gb (32M x 8-Bank x 32-bit (2 channels x 16 I/O))

POWER SUPPLY

- eMMC
  - VCC: 3.3V (2.7-3.6V)
  - VCCQ: 3.3V (2.7-3.6V)
- LPDDR4 SDRAM
  - LDR4_V_{DD1}: 1.8V (1.7–1.95V)
  - LDR4_V_{DD2}: 1.1V (1.06–1.17V)
  - LDR4_V_{DDQ}: 1.1V (1.06–1.17V)

PACKAGE

- FBGA 11.5 x 13 x 1.0mm, 254 Balls
- Ball Pitch: 0.5mm
- Weight: TBD

Temperature

- Operating: -10 to +85°C
- Storage: -55 to +125°C

eMMC-Specific Features

- Supports features of eMMC5.1 which are defined in JEDEC Standard
  - Supported Features : Boot, RPMB, Write Protection, DDR, HS200, Multi-partitioning, Secure Erase/Trim, Trim, HPI, Background operation, Enhance Reliable Write, Discard, Sanitize, Security features, Partition types, Packed commands, Real time clock, Dynamic device capacity, Power off notification, Thermal spec,Cache, HS400, Field Firmware Update, Security Removal type, Device Health Report, Enhanced Strobe, Command Queuing, Secure Write protection
  - Non-supported Features : Large Sector Size (4KB)
- Full backward compatibility with previous eMMC 4.41/4.5/5.0 specification
- Programmable bus width : 1bit (Default), 4bit and 8bit Data bus.
- eMMC I/F Clock Frequency : 0 ~ 200MHz

  eMMC I/F Boot Frequency : 0 ~ 52MHz

LPDDR4 SDRAM

- Ultra-low-voltage core and I/O power supplies
  - V_{DD1} = 1.70–1.95V; 1.80V nominal
  - V_{DD2}/V_{DDQ} = 1.06–1.17V; 1.10V nominal
- Frequency range
  - 1600–10 MHz (data rate range: 3200–20 Mb/s/pin)
- 16n prefetch DDR architecture
- 8 internal banks per channel for concurrent operation
- Single-data-rate CMD/ADR entry
- Bidirectional/differential data strobe per byte lane
- Programmable READ and WRITE latencies (RL/WL)
- Programmable and on-the-fly burst lengths (BL =16, 32)
- Directed per-bank refresh for concurrent bank operationand ease of command scheduling
- Up to 8.5 GB/s per die
- On-chip temperature sensor to control self refresh rate
- Partial-array self refresh (PASR)
- Selectable output drive strength (DS)
- Clock-stop capability
- RoHS-compliant, “green” packaging
- Programmable V_{SS} (ODT) termination

Device Addressing

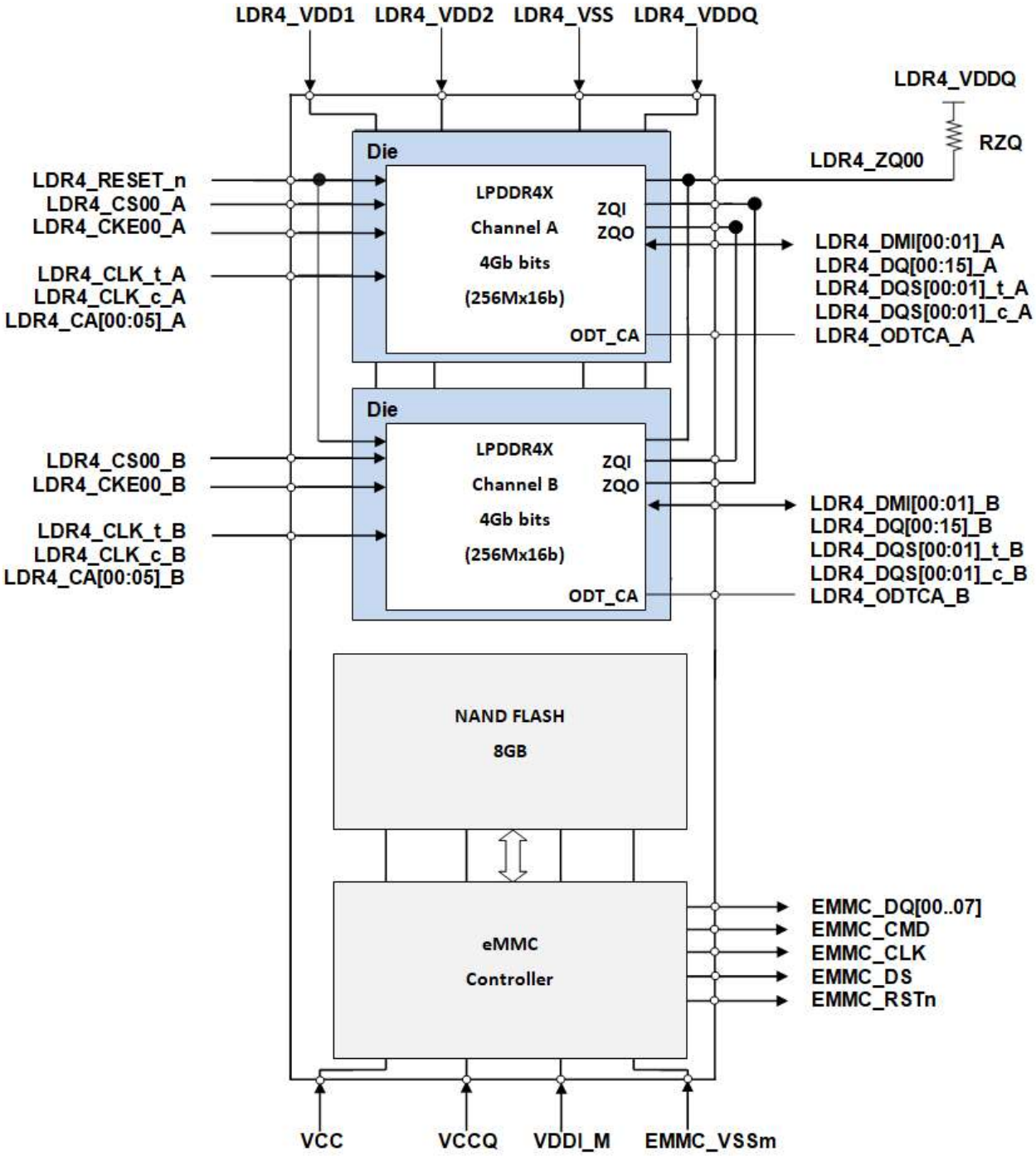
Configuration		**256M32 (8Gb)**
Die per package		**2**
Device density (per die)		**4Gb**
Device density (per channel)		**4Gb**
Configuration		32Mb x 16 DQ x 8 banks x 2channels x 1 rank
Number of channels (per die)		1
Number of ranks per channel		1
Number of banks (per channel)		8
Array prefetch (bits) (per channel)		256
Number of rows (per bank)		32,768
Number of columns (fetch boundaries)		64
Page size (bytes)		2048
Channel density (bits per channel)		4,294,967,296
Total density (bits per die)		4,294,967,296
Bank address		BA[2:0]
x16	Row addresses	R[14:0]
	Column addresses	C[9:0]
Burst starting address boundary		64-bit

Notes:

1. The lower two column addresses (C0–C1) are assumed to be zero and are not transmitted on the CA bus.
2. Row and column address values on the CA bus that are not used for a particular density are "Don't Care."
3. For non-binary memory densities, only half of the row address space is valid. When the MSB address bit isHIGH, theMSB-1 address bit must be LOW.

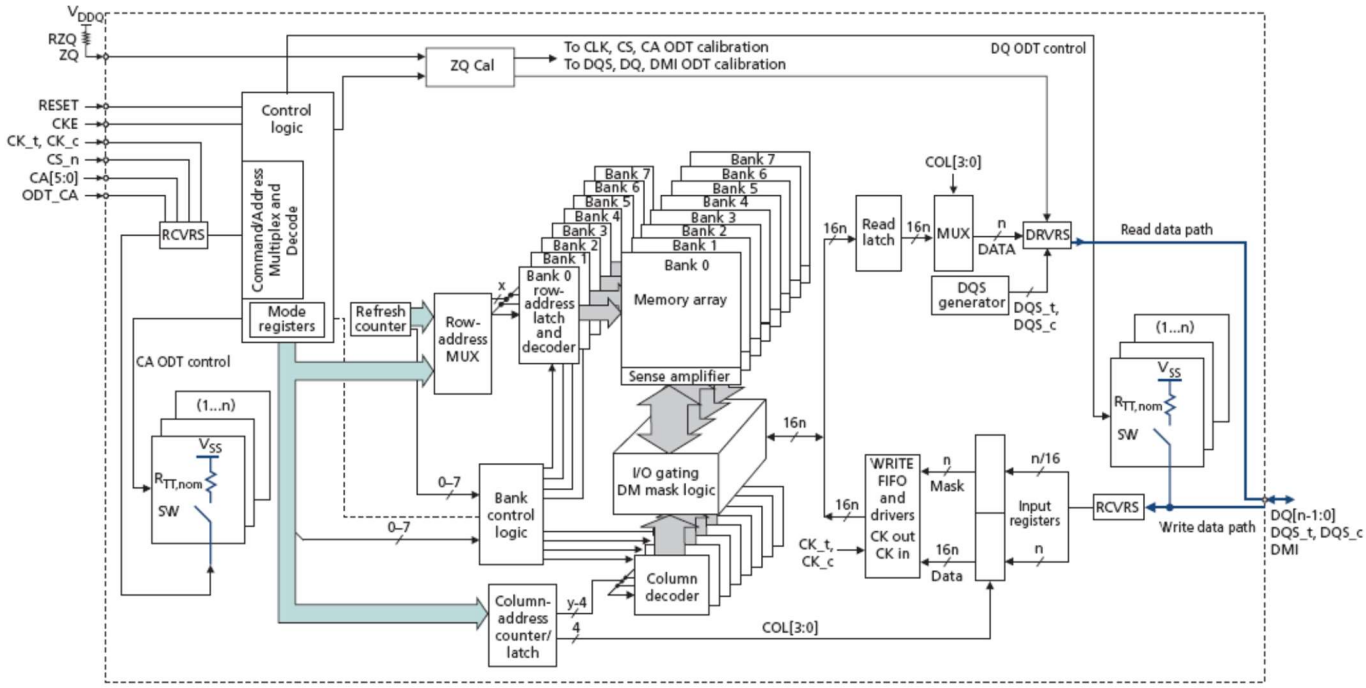
2. FUNCTION DIAGRAM

2.1 eMCP

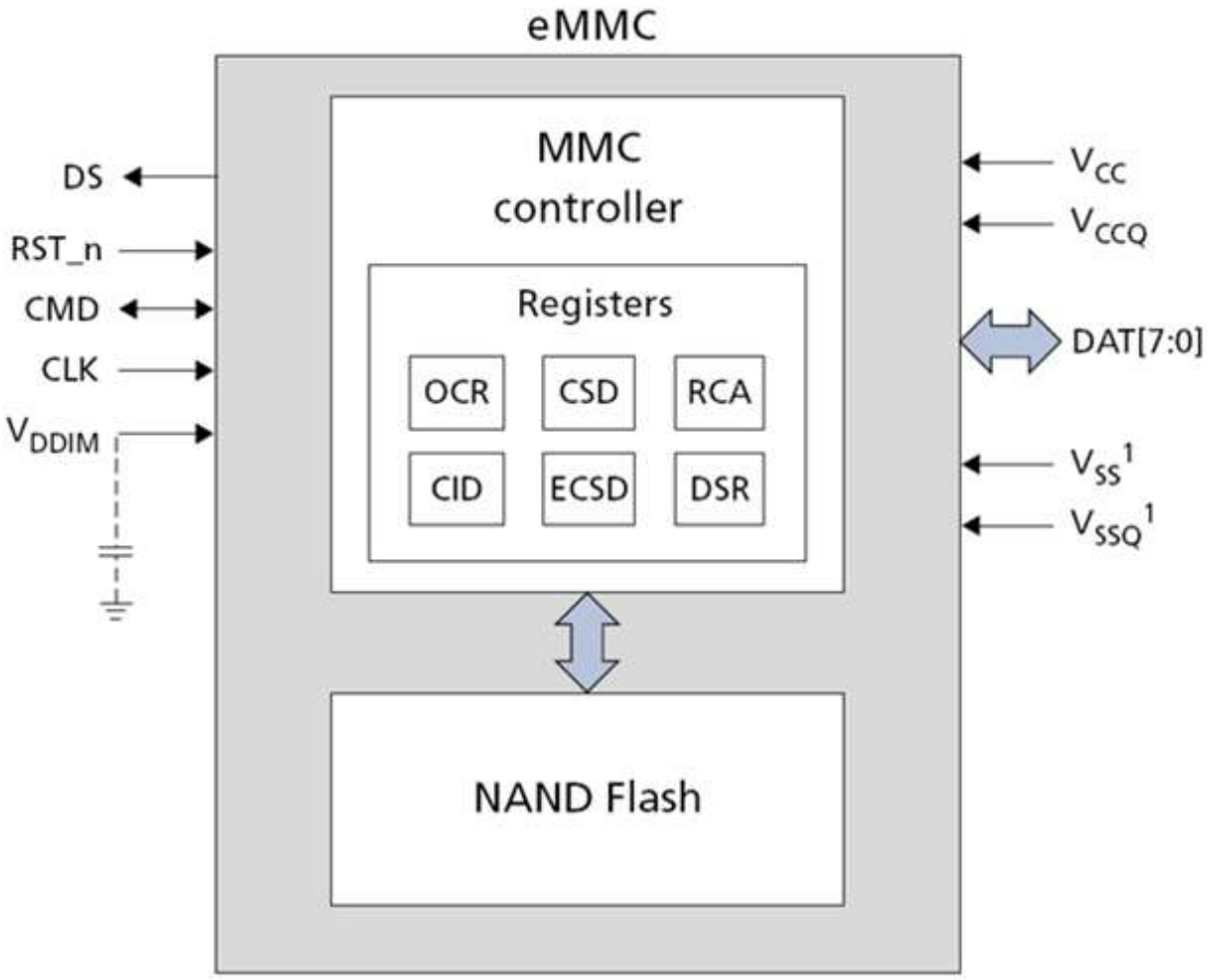


2.2 LPDDR4 SDRAM Logic Block Diagram

Functional Block Diagram (per die)



2.3 eMMC



Note:

1. V_{SS} and V_{SSQ} are internally connected.

3. PIN CONFIGURATION

3.1 Pin Assignment

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	DNU	DNU	LDR4_DQ00_A	LDR4_VDD1	LDR4_VDD2	LDR4_VDDQ	LDR4_VDDQ	LDR4_VDD2	LDR4_VDD1				LDR4_VDDQ	LDR4_VDDQ	LDR4_VDD1	LDR4_VDD1	DNU	DNU
B	DNU		LDR4_DQ01_A	LDR4_VSS	LDR4_VDDQ	LDR4_VSS	LDR4_DQ04_A	LDR4_VSS	LDR4_VDD2				LDR4_VDD2	LDR4_VDD2	LDR4_VDD1	LDR4_ZQ00		DNU
C			LDR4_DQ02_A	LDR4_VSS	LDR4_VSS	LDR4_DQ05_A	LDR4_VSS	LDR4_DQ07_A	LDR4_DQS00_t_A				LDR4_CA02_A	LDR4_VSS	LDR4_CA05_A	NC/ LDR4_ZQ01		
D			LDR4_DQ03_A	LDR4_VSS	LDR4_DMI00_A	LDR4_VSS	LDR4_DQ06_A	LDR4_VSS	LDR4_DQS00_c_A				LDR4_CA03_A	LDR4_VSS	LDR4_VSS	NC/ LDR4_ZQ02		
E													LDR4_CA04_A	LDR4_VSS	LDR4_CS00_A	LDR4_CKE00_A		
F													LDR4_CA01_A	LDR4_VSS	NC/ LDR4_CS01_A	NC/ LDR4_CKE01_A		
G			LDR4_DQ13_A	LDR4_VSS	LDR4_VSS	LDR4_VSS	LDR4_VDD2	LDR4_VDD2	LDR4_VDD2				LDR4_VSS	LDR4_CA00_A	LDR4_VSS	LDR4_CLK_c_A		
H			LDR4_DMI01_A	LDR4_VSS	LDR4_VDDQ	LDR4_DQ14_A	LDR4_VSS	LDR4_DQ15_A	LDR4_VDDQ				LDR4_VSS	NC/ LDR4_CS02_A	LDR4_VSS	LDR4_CLK_t_A		
J			LDR4_DQ11_A	LDR4_VDDQ	LDR4_VDDQ	LDR4_VSS	LDR4_DQ12_A	LDR4_VDDQ	LDR4_DQS01_c_A				LDR4_ODTCA_A	NC/ LDR4_CKE02_A	VCCQ	VCCQ	VCCQ	
K		LDR4_VDD2	LDR4_DQ10_A	LDR4_VSS	LDR4_DQ08_A	LDR4_DQ09_A	LDR4_VSS	LDR4_VSS	LDR4_DQS01_t_A				EMMC_VSSm	EMMC_VSSm	VCCQ	EMMC_VSSm	NC	
L							LDR4_VDD2	LDR4_VDD2	LDR4_VDD2			EMMC_VSSm	EMMC_DAT7	EMMC_DAT6	EMMC_VSSm	EMMC_VSSm	VDDI_M	
M			VSF1	VSF3	VSF5	VSF7	VSF9	EMMC_VSSm	EMMC_CMD			EMMC_DS	EMMC_VSSm	EMMC_VSSm	EMMC_DAT1	EMMC_DAT4	VCC	
N			VSF2	VSF4	VSF6	VSF8	NC	EMMC_VSSm	EMMC_RSTn			EMMC_VSSm	EMMC_DAT2	EMMC_DAT5	EMMC_VSSm	EMMC_VSSm	VCC	
P							LDR4_VDD2	LDR4_VDD2	LDR4_VDD2			EMMC_CLK	EMMC_VSSm	EMMC_VSSm	EMMC_DAT3	EMMC_DAT0	VCC	
R		LDR4_VDD2	LDR4_DQ10_B	LDR4_VSS	LDR4_DQ08_B	LDR4_DQ09_B	LDR4_VSS	LDR4_VSS	LDR4_DQS01_t_B				VCCQ	VCCQ	EMMC_VSSm	EMMC_VSSm	EMMC_VSSm	
T			LDR4_DQ11_B	LDR4_VDDQ	LDR4_VDDQ	LDR4_VSS	LDR4_DQ12_B	LDR4_VDDQ	LDR4_DQS01_c_B				LDR4_ODTCA_B	NC/ LDR4_CKE02_B	VCCQ	VCCQ	NC	
U			LDR4_DMI01_B	LDR4_VSS	LDR4_VDDQ	LDR4_DQ14_B	LDR4_VSS	LDR4_DQ15_B	LDR4_VDDQ				LDR4_VSS	NC/ LDR4_CS02_B	LDR4_VSS	LDR4_CLK_t_B		
V			LDR4_DQ13_B	LDR4_VSS	LDR4_VSS	LDR4_VSS	LDR4_VDD2	LDR4_VDD2	LDR4_VDD2				LDR4_VSS	LDR4_CA00_B	LDR4_VSS	LDR4_CLK_c_B		
W													LDR4_CA01_B	LDR4_VSS	NC/ LDR4_CS01_B	NC/ LDR4_CKE01_B		
Y													LDR4_CA04_B	LDR4_VSS	LDR4_CS00_B	LDR4_CKE00_B		
AA			LDR4_DQ03_B	LDR4_VSS	LDR4_DMI00_B	LDR4_VSS	LDR4_DQ06_B	LDR4_VSS	LDR4_DQS00_c_B				LDR4_CA03_B	LDR4_VSS	LDR4_VSS	LDR4_RESET_n		
AB			LDR4_DQ02_B	LDR4_VSS	LDR4_VSS	LDR4_DQ05_B	LDR4_VSS	LDR4_DQ07_B	LDR4_DQS00_t_B				LDR4_CA02_B	LDR4_VSS	LDR4_CA05_B	NC		
AC	DNU		LDR4_DQ01_B	LDR4_VSS	LDR4_VDDQ	LDR4_VSS	LDR4_DQ04_B	LDR4_VSS	LDR4_VDD2				LDR4_VDD2	LDR4_VDD2	LDR4_VDD1	NC		DNU
AD	DNU	DNU	LDR4_DQ00_B	LDR4_VDD1	LDR4_VDD2	LDR4_VDDQ	LDR4_VDDQ	LDR4_VDD2	LDR4_VDD1				LDR4_VDDQ	LDR4_VDDQ	LDR4_VDD1	LDR4_VDD1	DNU	DNU

TOP VIEW

3.2 Pin Descriptions

Type Symbol	Description	Type Symbol	Description
I	Input	P	Power
O	Output	G	Ground
I/O	Bi-direction	X	No connect (No function, don't care)

Symbol	Type	Count	Description
LDR4_CLK_t_A LDR4_CLK_c_A LDR4_CLK_t_B LDR4_CLK_c_B (CK, CK_t, CK_c)	I	4	**Clock:** CK_t and CK_c are differential clock inputs. All address, command and control input signals are sampled on positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters are referenced to clock. Each channel (A, B) has its own clock pair.
LDR4_CKE00_A LDR4_CKE00_B (CKE)	I	2	**Clock enable:** CKE HIGH activates and CKE LOW deactivates the internal clock signals,input buffers, and output drivers. Power-saving modes are entered and exited via CKEtransitions. CKE is sampled at the rising edge of CK.
LDR4_CS00_A LDR4_CS00_B (CS,CS_n)	I	2	**Chip select:** Each channel (A, B) has its own CS signals.
LDR4_CA[00:05]_A LDR4_CA[00:05]_B (CA)	I	12	**Command/Address inputs:** Provide the command and address inputs according to the command truth table. Each channel (A, B) has its own CA signals.
LDR4_ODTCA_A LDR4_ODTCA_B (ODT_CA)	I	2	**CA ODT control:** The ODT_CA pin is used in conjunction with the mode register to turn on/off the on-die termination for CA pins. It is bonded to V_{DD2} within the package, or at the package ball, for the terminating rank, and the non-terminating ranks are bonded to V_{SS} (or left floating with a weak pull-down on the DRAM die). The terminating rank is the DRAM that terminates the CA bus for all die on the same channel.
LDR4_DQ[00..15]_A LDR4_DQ[00..15]_B (DQ, DQs)	I/O	32	**Data input/output:** Bidirectional data bus.
LDR4_DQS[00..01]_t_A LDR4_DQS[00..01]_c_A LDR4_DQS[00..01]_t_B LDR4_DQS[00..01]_c_B (DQS, DQS_t, DQS_c)	I/O	8	**Data strobe:** DQS_t and DQS_c are bi-directional differential output clock signals used to strobe data during a READ or WRITE. The data strobe is generated by the DRAM for a READ and is edge-aligned with data. The data strobe is generated by the SoC memory controller for a WRITE and is trained to precede data. Each byte of data has a data strobe signal pair. Each channel (A, B) has its own DQS_t and DQS_c strobes.
LDR4_DMI[00..01]_A LDR4_DMI[00..01]_B (DMI)	I/O	4	**Data mask/Data bus inversion:** DMI is a dual use bi-directional signal used to indicate data to be masked, and data which is inverted on the bus. For data bus inversion(DBI), the DMI signal is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. DBI can be disabled via a mode register setting. For data mask, the DMI signal is used in combination with the data lines to indicate data to be masked in a MASK WRITE command (see the Data Mask (DM) and Data Bus Inversion (DBI) sections for details). The data mask function can be disabled via a mode register setting. Each byte of data has a DMI signal. Each channel has its own DMI signals.

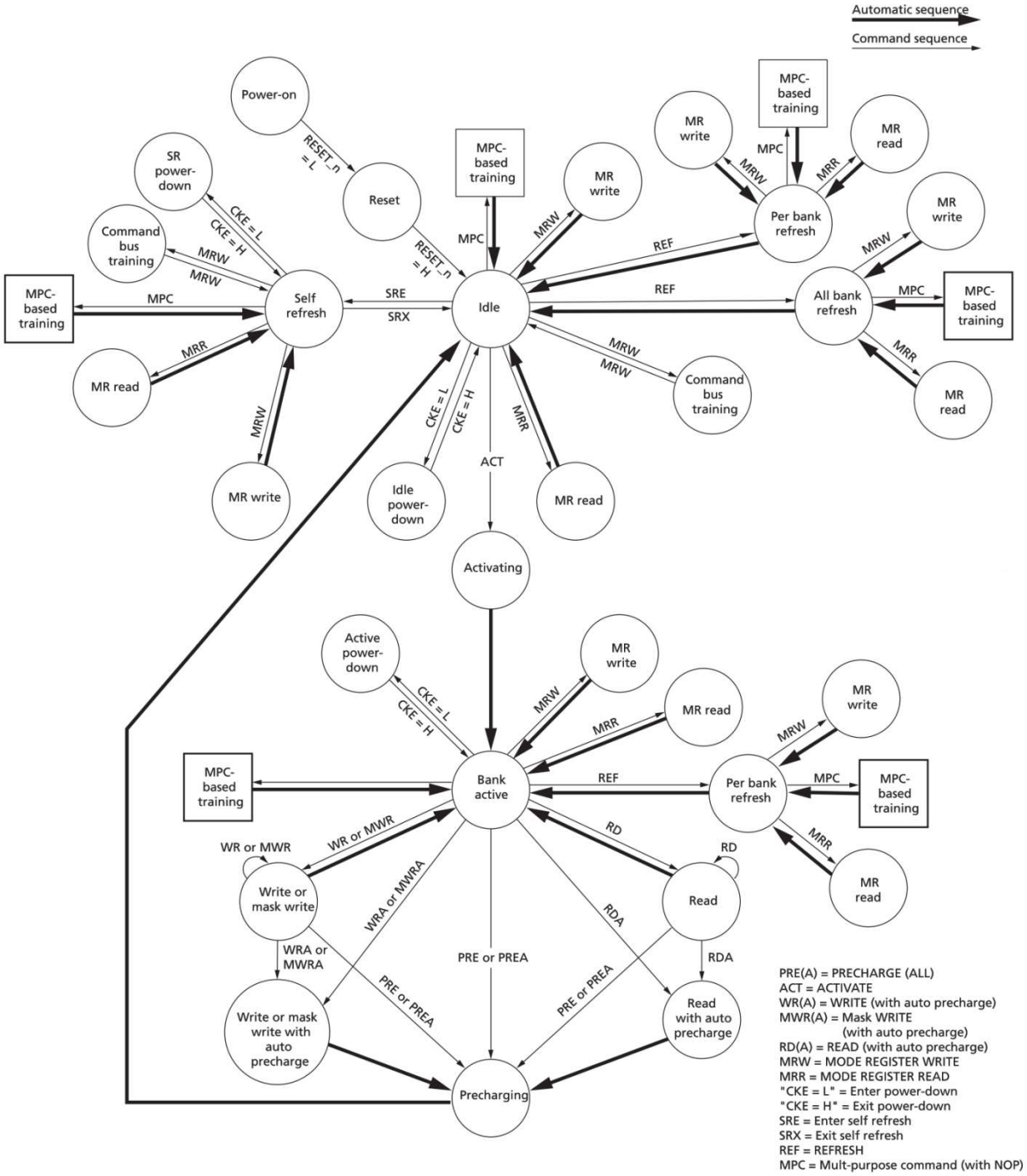
LDR4_ZQ00 (ZQ)	P	1	**ZQ calibration reference:** Used to calibrate the output drive strength and the termination resistance. The ZQ pin shall be connected to V_{DDQ} through a 240Ω ±1% resistor.
LDR_V_{DDQ}, LDR4_V_{DD1}, LDR4_V_{DD2} (V_{DDQ}, V_{DD1}, V_{DD2})	P	54	**Power supplies:** Isolated on the die for improved noise immunity.
LDR4_V_{SS} (V_{SS})	G	54	**Ground reference:** Power supply ground reference.
LDR4_RESET_n (RESET, RESET_n)	I	1	**RESET:** When asserted LOW, the RESET pin resets all channels of the die.
DNU	X	12	**Do not use:** Must be grounded or left floating.
NC	X	24	**No connect:** Not internally connected.
EMMC_DAT[00..07] DAT[7:0]	I/O	8	eMMC interface data bus
EMMC_CMD (CMD)	I	1	eMMC interface command line
EMMC_CLK (CLK)	I	1	eMMC interface clock line
EMMC_DS (DS)	I	1	eMMC interface data strobe
EMMC_RSTn (RSTn)	I	1	eMMC interface hardware reset
VCC	P	3	eMMC Power Supply
VCCQ (VCCIO)	P	8	eMMC Power Supply
VDDI_M (VDDIM)	P	1	eMMC Power Supply
EMMC_VSSm (GNDIO, VSS, VSSQ)	G	18	Ground

4. LPDDR4 SDRAM SPECIFICATION

4.1 Simplified Bus Interface State Diagram

The state diagram provides a simplified illustration of the bus interface, supported state transitions, and the commands that control them. For a complete description of device behavior, use the information provided in the state diagram with the truth tables and timing specifications. The truth tables describe device behavior and applicable restrictions when considering the actual state of all banks. For command descriptions, see theCommands and Timing section.

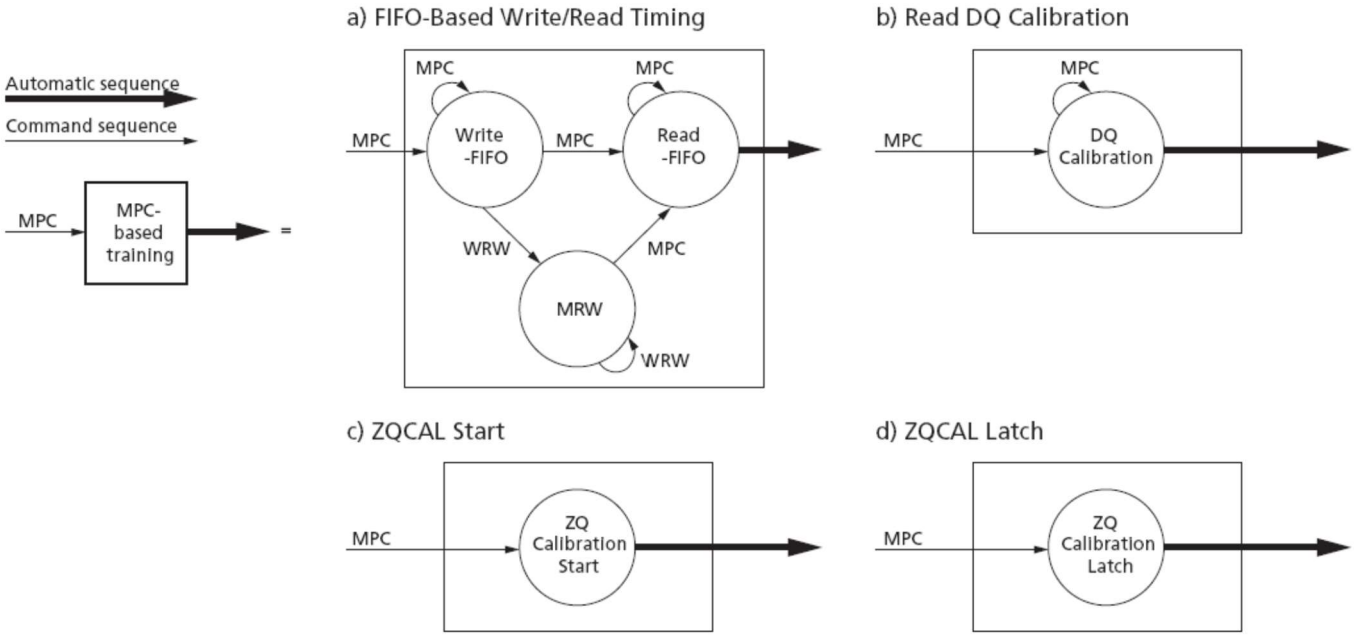
Simplified State Diagram



Notes:

1. From the self refresh state, the device can enter power-down, MRR, MRW, or any of thetraining modes initiated with the MPC command. See the Self Refresh section.
2. All banks are precharged in the idle state.
3. In the case of using an MRW command to enter a training mode, the state machine willnot automatically return to the idle state at the conclusion of training. See the applicabletraining section for more information.
4. In the case of an MPC command to enter a training mode, the state machine may notautomatically return to the idle state at the conclusion of training. See the applicabletraining section for more information.
5. This diagram is intended to provide an overview of the possible state transitions andcommands to control them; however, it does not contain the details necessary to operatethe device. In particular, situations involving more than one bank are not capturedin complete detail.
6. States that have an "automatic return" and can be accessed from more than one priorstate (that is, MRW from either idle or active states) will return to the state where theywere initiated (that is, MRW from idle will return to idle).
7. The RESET pin can be asserted from any state and will cause the device to enter the resetstate. The diagram shows RESET applied from the power-on and idle states as an example,but this should not be construed as a restriction on RESET.
8. MRW commands from the active state cannot change operating parameters of the devicethat affect timing. Mode register fields which may be changed via MRW from theactive state include: MR1-OP[3:0], MR1-OP[7], MR3-OP[7:6], MR10-OP[7:0], MR11-OP[7:0], MR13-OP[5], MR15-OP[7:0], MR16-OP[7:0], MR17-OP[7:0], MR20-OP[7:0], andMR22-OP[4:0].

Simplified State Diagram



4.2 General Description

The 8Gb Mobile Low-Power DDR4 SDRAM is a high-speedCMOS, dynamic random-access memory. The device is internally configured with x16I/O, 8-banks (each channel).

Each channel of the x16's 1,073,741,824-bit banks is organized as 65,536 rows by 1024 columnsby 16 bits.

General Notes
Throughout the data sheet, figures and text refer to DQs as "DQ." DQ should be interpretedas any or all DQ collectively, unless specifically stated otherwise.

"DQS" and "CK" should be interpreted as DQS_t, DQS_c and CK_t, CK_c respectively,unless specifically stated otherwise. "CA" includes all CA pins used for a given density.

In timing diagrams, "CMD" is used as an indicator only. Actual signals occur on CA[5:0].VREF indicates VREF(CA) and VREF(DQ).

Complete functionality may be described throughout the entire document. Any page ordiagram may have been simplified to convey a topic and may not be inclusive of all requirements.

Any specific requirement takes precedence over a general statement.

Any functionality not specifically stated herein is considered undefined, illegal, is notsupported, and will result in unknown operation.

4.3 MR0, MR[6:5], MR8, MR13, MR24 Definition

Table 4-1: Mode Register Contents

Mode Register	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR0							Latency Mode	REF
	OP[0] =0b: Both legacy and modified refresh mode supported OP[1] =0b: Device supports normal latency							
MR5	Manufacturer ID							
	1111 1111b							
MR6	Revision ID1							
	0000 0000b							
MR8	I/O Width		Density					
	OP[7:6] = 00b: x16/channel		OP[7:6] = 00b: x16/channel					
MR13						VRO		
	OP[2] = 0b: Normal operation (default) 1b: Output the $V_{REF(CA)}$ value on DQ7 and $V_{REF(DQ)}$ value on DQ6							
MR24	TRR Mode				Unlimited MAC	MAC Value		
	OP[3:0] = 1000b: Unlimited MAC OP[7] = 0b: Disable (default) 1b: Reserved							

Notes:

1. The contents of MR0, MR[6:5], MR8, MR13, and MR24 will reflect information specific to each die in these packages.
2. Other bits not defined above and other mode registers are referred to Mode Register Assignments and Definitions section.

4.4 I_{DD} Specifications

Refer to I_{DD} Specification Parameters and Test Conditions section for detailed conditions.

Table 4-2: I_{DD} Specifications

V_{DD2}, V_{DDQ} = 1.06–1.17V; V_{DD1} = 1.70–1.95V; T_C = –10°C to +85°C

Parameter	Supply	Speed Grade	Unit	Note
		3200 Mbps		
I_{DD01}	V_{DD1}	5.40	mA	
I_{DD02}	V_{DD2}	63		
I_{DD0Q}	V_{DDQ}	1.35		
I_{DD2P1}	V_{DD1}	1.62	mA	
I_{DD2P2}	V_{DD2}	2.34		
I_{DD2PQ}	V_{DDQ}	1.35		
I_{DD2PS1}	V_{DD1}	1.62	mA	
I_{DD2PS2}	V_{DD2}	2.34		
I_{DD2PSQ}	V_{DDQ}	1.35		
I_{DD2N1}	V_{DD1}	1.62	mA	
I_{DD2N2}	V_{DD2}	37.8		
I_{DD2NQ}	V_{DDQ}	1.35		
I_{DD2NS1}	V_{DD1}	1.62	mA	
I_{DD2NS2}	V_{DD2}	27		
I_{DD2NSQ}	V_{DDQ}	1.35		
I_{DD3P1}	V_{DD1}	1.62	mA	
I_{DD3P2}	V_{DD2}	14.4		
I_{DD3PQ}	V_{DDQ}	1.35		
I_{DD3PS1}	V_{DD1}	1.62	mA	
I_{DD3PS2}	V_{DD2}	14.4		
I_{DD3PSQ}	V_{DDQ}	1.35		
I_{DD3N1}	V_{DD1}	2.16	mA	
I_{DD3N2}	V_{DD2}	41.4		
I_{DD3NQ}	V_{DDQ}	1.35		
I_{DD3NS1}	V_{DD1}	2.16	mA	
I_{DD3NS2}	V_{DD2}	30.6		
I_{DD3NSQ}	V_{DDQ}	1.35		

Table 4-2:I_{DD} Specifications (Continued)

V_{DD2}, V_{DDQ} = 1.06–1.17V; V_{DD1} = 1.70–1.95V; T_C = –10°C to +85°C

Parameter	Supply	Speed Grade	Unit	Note
		3200 Mbps		
I_{DD4R1}	V_{DD1}	3.78	mA	3
I_{DD4R2}	V_{DD2}	579.6		
I_{DD4RQ}	V_{DDQ}	246.6		
I_{DD4W1}	V_{DD1}	3.42	mA	
I_{DD4W2}	V_{DD2}	477		
I_{DD4WQ}	V_{DDQ}	1.35		
I_{DD51}	V_{DD1}	16.2	mA	
I_{DD52}	V_{DD2}	122.4		
I_{DD5Q}	V_{DDQ}	1.35		
I_{DD5AB1}	V_{DD1}	2.16	mA	
I_{DD5AB2}	V_{DD2}	45		
I_{DD5ABQ}	V_{DDQ}	1.35		
I_{DD5PB1}	V_{DD1}	2.16	mA	
I_{DD5PB2}	V_{DD2}	45		
I_{DD5PBQ}	V_{DDQ}	1.35		

Notes:
1. Published I_{DD} values except I_{DD4RQ} are the maximum of the distribution of the arithmeticmean. Refer to the following note for I_{DD4RQ}; refer to I_{DD6} Full-Array Self Refresh Currenttable for I_{DD6}.
2. I_{DD4RQ} value is reference only. Typical value. DBI disabled, V_{OH} = V_{DDQ}/3, T_C = 25°C.

Table 4-3: IDD6 Full-Array Self Refresh Current

V_{DD2}, V_{DDQ} = 1.06–1.17V; V_{DD1} = 1.70–1.95V

Temperature	Supply	Full-Array Self Refresh Current	Unit
25°C	V_{DD1}	0.342	mA
	V_{DD2}	0.846	
	V_{DDQ}	0.018	
85°C	V_{DD1}	1.8	
	V_{DD2}	6.84	
	V_{DDQ}	1.35	

Notes:
1. I_{DD6} 25°C is the typical, and I_{DD6} 85°C is the maximum of the distribution of the arithmeticmean.

4.5 Functional Description

The Mobile Low-Power DDR4 SDRAM (LPDDR4) is a high-speed CMOS, dynamic random-access memory internally configured with either 1 or 2 channels. Each channel iscomprised of 16 DQs and 8 banks.

LPDDR4 uses a 2-tick, single-data-rate (SDR) protocol on the CA bus to reduce thenumber of input signals in the system. The term "2-tick" means that the command/address is decoded across two transactions, such that half of the command/address iscaptured with each of two consecutive rising edges of CK. The 6-bit CA bus containscommand, address, and bank information. Some commands such as READ, WRITE, MASKED WRITE, and ACTIVATE require two consecutive 2-tick SDR commands tocomplete the instruction.

LPDDR4 uses a double-data-rate (DDR) protocol on the DQ bus to achieve high-speedoperation. The DDR interface transfers two data bits to each DQ lane in one clock cycleand is matched to a 16n-prefetch DRAMarchitecture. A write/read access consists of asingle 16n-bit-wide data transfer to/from the DRAM core and 16 corresponding n-bitwidedata transfers at the I/O pins.

Read and write accesses to the device are burst-oriented. Accesses start at a selectedcolumn address and continue for a programmed number of columns in a programmedsequence.

Accesses begin with the registration of an ACTIVATE command to open a row in thememory core, followed by a WRITE or READ command to access column data withinthe open row. The address and bank address (BA) bits registered by the ACTIVATE commandare used to select the bank and row to be opened. The address and BA bits registeredwith the WRITE or READ command are used to select the bank and the startingcolumn address for the burst access.

Prior to normal operation, the LPDDR4 SDRAM must be initialized. Following sectionsprovide detailed information about device initialization, register definition, commanddescriptions and device operations.

Monolithic Device Addressing

The table below includes all monolithic device addressing options defined by JEDEC.
Under the SDRAM Addressing heading near the beginning of this data sheet are addressingdetails for this productdata sheet.

Table 4-4: Monolithic Device Addressing – 2 Channels Die

Memory density (per die)		4Gb	6Gb	8Gb	12Gb	16Gb
Memory density (per channel)		2Gb	3Gb	4Gb	6Gb	8Gb
Configuration		16Mb x 16DQ x 8 banks x 2 channels	24Mb x 16DQ x 8 banks x 2 channels	32Mb x 16DQ x 8 banks x 2 channels	48Mb x 16DQ x 8 banks x 2 channels	64Mb x 16DQ x 8 banks x 2 channels
Number of channels (per die)		2	2	2	2	2
Number of banks (per channel)		8	8	8	8	8
Array prefetch (bits, per channel)		256	256	256	256	256
Number of rows (per channel)		16,384	24,576	32,768	49,152	65,536
Number of columns (fetch boundaries)		64	64	64	64	64
Page size (bytes)		2048	2048	2048	2048	2048
Channel density (bits per channel)		2,147,483,648	3,221,225,472	4,294,967,296	6,442,450,944	8,589,934,592
Total density (bits per die)		4,294,967,296	6,442,450,944	8,589,934,592	12,884,901,888	17,179,869,184
Bank address		BA[2:0]	BA[2:0]	BA[2:0]	BA[2:0]	BA[2:0]
x16	Row add	R[13:0]	R[14:0] (R13 = 0 when R14 = 1)	R[14:0]	R[15:0] (R14 = 0 when R15 = 1)	R[15:0]
	Col. Add	C[9:0]	C[9:0]	C[9:0]	C[9:0]	C[9:0]
Burst starting address boundary		64 bit	64 bit	64 bit	64 bit	64 bit

Table 4-5: Monolithic Device Addressing – 1 Channel Die

Memory density (per die)		4Gb	6Gb	8Gb	12Gb	16Gb
Memory density (per channel)		4Gb	6Gb	8Gb	12Gb	16Gb
Configuration		32Mb x 16 DQ x 8 banks	48Mb x 16 DQ x 8 banks	64Mb x 16 DQ x 8 banks	48Mb x 16DQ x 8 banks x 2 channels	64Mb x 16DQ x 8 banks x 2 channels
Number of channels (per die)		1	1	1	2	2
Number of banks (per channel)		8	8	8	8	8
Array prefetch (bits, per channel)		256	256	256	256	256
Number of rows (per channel)		32,768	49,152	65,536	98,304	131,072
Number of columns (fetch boundaries)		64	64	64	64	64
Page size (bytes)		2048	2048	2048	2048	2048
Channel density (bits per channel)		4,294,967,296	6,442,450,944	8,589,934,592	12,884,901,888	17,179,869,184
Total density (bits per die)		4,294,967,296	6,442,450,944	8,589,934,592	12,884,901,888	17,179,869,184
Bank address		BA[2:0]	BA[2:0]	BA[2:0]	BA[2:0]	BA[2:0]
x16	Row add	R[14:0]	R[15:0] (R14 = 0 when R15 = 1)	R[15:0]	R[16:0] (R15 = 0 when R16 = 1)	R[16:0]
	Column add	C[9:0]	C[9:0]	C[9:0]	C[9:0]	C[9:0]
Burst starting address boundary		64 bit	64 bit	64 bit	64 bit	64 bit

Notes:

1. The lower two column addresses (C[1:0]) are assumed to be zero and are not transmittedon the CA bus.
2. Row and column address values on the CA bus that are not used for a particular densityshould be at valid logic levels.
3. For non-binary memory densities, only a quarter of the row address space is invalid.When the MSB address bit is HIGH, then the MSB - 1 address bit must be LOW.

4.6 Power-Up and Initialization

To ensure proper functionality for power-up and reset initialization, default values forthe MR settings are provided in the table below.

Table 4-6: Mode Register Default Settings

Item	Mode Register Setting	Default Setting	Description
FSP-OP/WR	MR13 OP[7:6]	00b	FSP-OP/WR[0] are enabled
WLS	MR2 OP[6]	0b	WRITE latency set A is selected
WL	MR2 OP[5:3]	000b	WL = 4
RL	MR2 OP[2:0]	000b	RL = 6, nRTP = 8
nWR	MR1 OP[6:4]	000b	nWR = 6
DBI-WR/RD	MR3 OP[7:6]	00b	Write and read DBI are disabled
CA ODT	MR11 OP[6:4]	000b	CA ODT is disabled
DQ ODT	MR11 OP[2:0]	000b	DQ ODT is disabled
$V_{REF(CA)}$ setting	MR12 OP[6]	1b	$V_{REF(CA)}$ range[1] is enabled
$V_{REF(CA)}$ value	MR12 OP[5:0]	011101b	Range1: 50.3% of V_{DDQ}
$V_{REF(DQ)}$ setting	MR14 OP[6]	1b	$V_{REF(DQ)}$ range[1] enabled
$V_{REF(DQ)}$ value	MR14 OP[5:0]	011101b	Range1: 50.3% of V_{DDQ}

The following sequence must be used to power up the device. Unless specified otherwise,this procedure is mandatory. The power-up sequence of all channels must proceedsimultaneously.

Voltage Ramp

1. While applying power (after Ta), RESET_n should be held LOW (≤0.2 × V_{DD2}), and allother inputs must bebetween $V_{IL,min}$ and $V_{IH,max}$. The device outputs remain at High-Zwhile RESET_n is held LOW. Power supplyvoltage requirements are provided inthe table below. V_{DD1} must ramp at the same time or earlier than V_{DD2}.V_{DD2} must rampat the same time or earlier than V_{DDQ}.

Table 4-7: Voltage Ramp Conditions

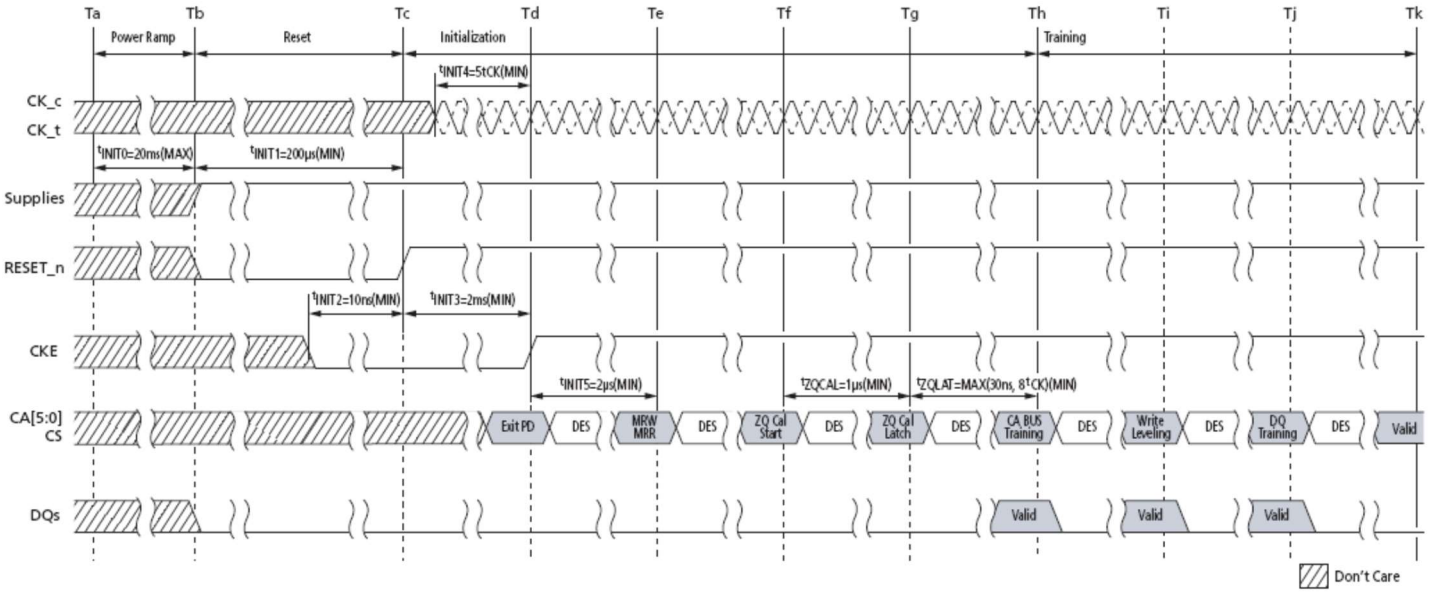
After…	licable Conditions
Ta is reached	V_{DD1} must be greater than V_{DD2}
	V_{DD2} must be greater than V_{DDQ} - 200mV

Notes:

1. Ta is the point when any power supply first reaches 300mV.
2. Voltage ramp conditions in above table apply between Ta and power-off (controlled oruncontrolled).
3. Tb is the point at which all supply and reference voltages are within their defined operatingranges.
4. Power ramp duration ^{t}INIT0 (Tb–Ta) must not exceed 20ms.
5. The voltage difference between any V_{SS} and V_{SSQ} must not exceed 100mV.

2. Following completion of the of the voltage ramp (Tb), RESET_n must be held LOW fortINIT1. DQ, DMI, DQS_t, and DQS_c voltage levels must be between VSSQ and VDDQduring voltage ramp to avoid latch-up. CK_t and CK_c, CS, and CA input levels must bebetween VSS and VDD2 during voltage ramp to avoid latch-up. Voltage ramppower supplyrequirements are provided in the table below.
3. Beginning at Tb, RESET_n must remain LOW for at least tINIT1(Tc), after which RESET_n can be de-asserted toHIGH(Tc). At least 10ns before CKE de-assertion, CKE isrequired to be set LOW. All other input signals are"Don't Care."

Figure 4-1: Voltage Ramp and Initialization Sequence



Note:

1. Training is optional and may be done at the system designer's discretion. The order oftraining may be different than what is shown here.

4. After RESET_n is de-asserted(Tc), wait at least tINIT3 before activating CKE. CK_t,CK_c must be started andstabilized for tINIT4 before CKE goes active(Td). CS must remainLOW when the controller activates CKE.
5. After CKE is set to HIGH, wait a minimum of tINIT5 to issue any MRR or MRW commands(Te). For MRR andMRW commands,the clock frequency must be within therange defined for tCKb. Some AC parameters (forexample, tDQSCK) could have relaxedtimings (such as tDQSCKb) before the system is appropriately configured.
6. After completing all MRW commands to set the pull-up, pull-down, and Rx terminationvalues, the controller canissue the ZQCAL START command to the memory(Tf).This command is used to calibrate the VOH level and theoutput impedance over process,voltage, and temperature. In systems where more than one device share oneexternalZQ resistor, the controller must not overlap the ZQ calibration sequence of each device.The ZQcalibration sequence is completed after tZQCAL (Tg). The ZQCAL LATCHcommand must be issued to updatethe DQ drivers and DQ + CA ODT to the calibratedvalues.
7. After tZQLAT is satisfied (Th), the command bus (internal $V_{REF(CA)}$, CS, and CA)should be trained for high-speedoperation by issuing an MRW command (commandbus training mode). This command is used to calibrate thedevice's internal V_{REF} andalign CS/CA with CK for high-speed operation. The device will power-up with receiversconfigured for low-speed operations and with $V_{REF(CA)}$ set to a default factory setting.Normal device operation atclock speeds higher than tCKb may not be possible untilcommand bus training is complete. The command bustraining MRW command usesthe CA bus as inputs for the calibration data stream, and it outputs the resultsasynchro-nously on the DQ bus. See command bus training in the MRW section for informationon how toenter/exit the training mode.
8. After command bus training, the controller must perform write leveling. Write levelingmode is enabled when MR2OP[7] is HIGH(Ti). See the Write Leveling section for adetailed description of the write leveling entry and exitsequence. In write levelingmode, the controller adjusts write DQS timing to the point where the device recognizesthe start of write DQ data burst with desired WRITE latency.

9. After write leveling, the DQ bus (internal $V_{REF(DQ)}$, DQS, and DQ) should be trainedfor high-speed operation usingthe MPC TRAINING commands and by issuing MRWcommands to adjust $V_{REF(DQ)}$. The device will power-up withreceivers configured forlow-speed operations and with $V_{REF(DQ)}$ set to a default factory setting. Normal deviceoperation at clock speeds higher than tCKb should not be attempted until DQ bus trainingis complete. TheMPC[READ DQ CALIBRATION] command is used together withMPC[READ-FIFO] or MPC[WRITE-FIFO]commands to train the DQ bus without disturbingthe memory array contents. See the DQ Bus Training section formore informationon the DQ bus training sequence.
10. At Tk, the device is ready for normal operation and is ready to accept any valid command.Any mode registersthat have not previously been configured for normal operationshould be written at this time.

Table 4-8: Initialization Timing Parameters

Parameter	Min	Max	Unit	Comment
^{t}INIT0	–	20	ms	Maximum voltage ramp time
^{t}INIT1	200	–	µs	Minimum RESET_n LOW time after completion of voltage ramp
^{t}INIT2	10	–	ns	Minimum CKE LOW time before RESET_n goes HIGH
^{t}INIT3	2	–	ms	Minimum CKE LOW time after RESET_n goes HIGH
^{t}INIT4	5	–	^{t}CK	Minimum stable clock before first CKE HIGH
^{t}INIT5	2	–	µs	Minimum idle time before first MRW/MRR command
^{t}CKb	Note 1, 2	Note 1, 2	ns	Clock cycle time during boot

Notes:
1. Minimum ^{t}CKb guaranteed by DRAM test is 18ns.
2. The system may boot at a higher frequency than dictated by minimum ^{t}CKb. The higherboot frequency is system dependent.

Reset Initialization with Stable Power

The following sequence is required for RESET at no power interruption initialization.

1. Assert RESET_n below 0.2 × VDD2 anytime when reset is needed. RESET_n needsto be maintained forminimum tPW_RESET. CKE must be pulled LOW at least10ns before de-asserting RESET_n.
2. Repeat steps 4–10 in Voltage Ramp section.

Table 4-9: Reset Timing Parameter

Parameter	Value		Unit	Comment
	Min	Max		
^{t}PW_RESET	100	–	ns	Minimum RESET_n LOW time for reset initialization with stable power

4.7 Power-Off Sequence

Controlled Power-Off

While powering off, CKE must be held LOW (≤0.2 × V_{DD2}); all other inputs must be between$V_{IL,min}$ and $V_{IH,max}$. The device outputs remain at High-Z while CKE is held LOW.

DQ, DMI, DQS_t, and DQS_c voltage levels must be between V_{SSQ} and V_{DDQ}during thepower-off sequence to avoid latch-up. CK_t, CK_c, CS, and CA input levels must be betweenV_{SS} and V_{DD2} during the power-off sequence to avoid latch-up.

Tx is the point where any power supply drops below the minimum value specified inthe minimum DC Operating Condition.

Tz is the point where all power supplies are below 300mV. After Tz, the device is poweredoff.

Table 4-10: Power Supply Conditions

The voltage difference between V_{SS} and V_{SSQ} must not exceed 100mV

Between…	Applicable Conditions
Tx and Tz	V_{DD1} must be greater than V_{DD2}
	V_{DD2} must be greater than V_{DDQ} - 200mV

Uncontrolled Power-Off

When an uncontrolled power-off occurs, the following conditions must be met.

- At Tx, when the power supply drops below the minimum values specified in the RecommendedDC OperatingConditions table,all power supplies must be turned off andall power supply current capacity must be at zero,except for any static charge remainingin the system.
- After Tz (the point at which all power supplies first reach 300mV), the device mustpower off. During this period,the relative voltage between power supplies is uncontrolled.VDD1 and VDD2 must decrease with a slope lower than0.5 V/µs between Txand Tz.

An uncontrolled power-off sequence can occur a maximum of 400 times over the life ofthe device.

Table 4-11: Power-Off Timing

Parameter	Symbol	Min	Max	Unit
Power-off ramp time	^{t}POFF	–	2	sec

4.8 Mode Registers

Mode Register Assignments and Definitions

Mode register definitions are provided in the Mode Register Assignments table. In theaccess column of the table, R indicates read-only; W indicates write-only; R/W indicatesread- or write-capable or enabled. The MRR command is used to read from a register.The MRW command is used to write to a register.

Table 4-12: Mode Register Assignments

Notes 1–5 apply to entire table

MR#	MA[7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	00h	Device info	R	CATR	RFU	RFU	RZQI		RFU		REF
1	01h	Device feature 1	W	RD-PST	nWR (for AP)			RD-PRE	WR-PRE	BL	
2	02h	Device feature 2	W	WR Lev	WLS	WL			RL		
3	03h	I/O config-1	W	DBI-WR	DBI-RD	PDDS			PPRP	WR-PST	PU-CAL
4	04h	Refresh and training	R /W	TUF	Thermal offset		PPRE	SR abort	Refresh rate		
5	05h	Basic config-1	R	Manufacturer ID							
6	06h	Basic config-2	R	Revision ID1							
7	07h	Basic config-3	R	Revision ID2							
8	08h	Basic config-4	R	I/O width		Density				Type	
9	09h	Test mode	W	Vendor-specific test mode							
10	0Ah	I/O calibration	W	RFU							ZQ RST
11	0Bh	ODT	W	RFU	CA ODT			RFU	DQ ODT		
12	0Ch	$V_{REF(CA)}$	R /W	RFU	VR_{CA}	$V_{REF(CA)}$					
13	0Dh	Register control	W	FSP-OP	FSP-WR	DMD	RRO	VRCG	VRO	RPT	CBT
14	0Eh	$V_{REF(DQ)}$	R /W	RFU	VR_{DQ}	$V_{REF(DQ)}$					
15	0Fh	DQI-LB	W	Lower-byte invert register for DQ calibration							
16	10h	PASR_Bank	W	PASR bank mask							
17	11h	PASR_Seg	W	PASR segment mask							
18	12h	IT-LSB	R	DQS oscillator count – LSB							
19	13h	IT-MSB	R	DQS oscillator count – MSB							
20	14h	DQI-UB	W	per-byte invert register for DQ calibration							
21	15h	Vendor use	W	RFU							

Table 4-12: Mode Register Assignments (Continued)

Notes 1–5 apply to entire table

MR#	MA[7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
22	16h	ODT feature 2	W	RFU		ODTD-CA	ODTE-CS	ODTE-CK	SoC ODT		
23	17h	DQS oscillator stop	W	DQS oscillator run-time setting							
24	18h	TRR control	R /W	TRR mode	TRR mode Ban			Unltd MAC	MAC value		
25	19h	PPR resources	R	B7	B6	B5	B4	B3	B2	B1	B0
26-29	1Ah~1Dh	–	–	Reserved for future use							
30	1Eh	–	W	SDRAM will ignore							
31	1Fh	Do not use	–	Reserved for future use							
32	20h	DQ calibration pattern B	W	See DQ calibration section							
33-38	21h≈26h	Do not use	–	Do not use							
39	27h	Reserved for test	W	SDRAM will ignore							
40	28h	DQ calibration pattern B	W	See DQ calibration section							
41-47	29h≈2Fh	Do not use	–	Do not use							
48-63	30h≈3Fh	Reserved	–	Reserved for future use							

Notes:

1. RFU bits must be set to 0 during MRW commands.
2. RFU bits are read as 0 during MRR commands.
3. All mode registers that are specified as RFU or write-only shall return undefined datawhen read via an MRR command.
4. RFU mode registers must not be written.
5. Writes to read-only registers will not affect the functionality of the device.

Table 4-13: MR0 Device Feature 0 (MA[7:0] = 00h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU			RZQI		RFU	Latency mode	REF

Table 4-14: MR0 Op-Code Bit Definitions

Register Information	Type	OP	Definition	Notes
Refresh mode	Readonly	OP[0]	0b: Both legacy and modified refresh mode supported 1b: Only modified refresh mode supported	
Latency mode	Readonly	OP[1]	0b: Device supports normal latency 1b: Device supports byte mode latency	5, 6
Built-in self-test for RZQ information	Readonly	OP[4:3]	00b: RZQ self-test not supported 01b: ZQ may connect to V_{SSQ} or float 10b: ZQ may short to V_{DDQ} 11b: ZQ pin self-test completed, no error condition detected (ZQ may not connect to V_{SSQ}, float, or short to V_{DDQ})	1-4

Notes:

1. RZQI MR value, if supported, will be valid after the following sequence:
   - Completion of MPC[ZQCAL START] command to either channel
   - Completion of MPC[ZQCAL LATCH] command to either channel then ^{t}ZQLAT is satisfied

   RZQI value will be lost after reset.
2. If ZQ is connected to V_{SSQ} to set default calibration, OP[4:3] must be set to 01b. If ZQ isnot connected to V_{SSQ}, either OP[4:3] = 01b or OP[4:3] = 10b might indicate a ZQ pin assemblyerror. It is recommended that the assembly error be corrected.
3. In the case of possible assembly error, the device will default to factory trim settings forRON, and will ignore ZQ CALIBRATION commands. In either case, the device may notfunction as intended.

4. If the ZQ pin self-test returns OP[4:3] = 11b, the device has detected a resistor connectedto the ZQ pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor meets the specified limits (that is, 24Ω±1%).
5. See byte mode addendum spec for byte mode latency details.
6. Byte mode latency for 2Ch. x16 device is only allowed when it is stacked in a same packagewith byte mode device.

Table 4-15: MR1 Device Feature 1 (MA[5:0] = 01h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RD-PST	nWR (for AP)			RD-PRE	WR-PRE	BL	

Table 4-16: MR1 Op-Code Bit Definitions

Feature	Type	OP	OP	Notes
BL Burst length	Write only	OP[1:0]	00b: BL = 16 sequential (default) 01b: BL= 32 sequential 10b: BL = 16 or 32 sequential (on-the-fly) 11b: Reserved	1
WR-PRE Write preamble length	Write only	OP[2]	0b: Reserved 1b: WR preamble = 2 × ^{t}CK	5, 6
RD-PRE Read preamble type	Write only	OP[3]	0b: RD preamble = Static (default) 1b: RD preamble = Toggle	3, 5, 6
nWR Write-recovery for AUTO PRECHARGE command	Write only	OP[6:4]	000b: nWR = 6 (default) 001b: nWR = 10 010b: nWR = 16 011b: nWR = 20 100b: nWR = 24 101b: nWR = 30 110b: nWR = 34 111b: nWR = 40	2, 5, 6
RD-PST Read postamble length	Write only	OP[7]	0b: RD postamble = 0.5 × ^{t}CK (default) 1b: RD postamble = 1.5 × ^{t}CK	4, 5, 6

Notes:

1. Burst length on-the-fly can be set to either BL = 16 or BL = 32 by setting the BL bit in thecommand operands. See the Command Truth Table.
2. The programmed value of nWR is the number of clock cycles the device uses to determinethe starting point of an internal precharge after a write burst with auto precharge(AP) enabled. See Frequency Ranges for RL, WL, and nWR Settings table.
3. For READ operations, this bit must be set to select between a toggling preamble and anon-toggling preamble. (See the Preamble section.)
4. OP[7] provides an optional READ postamble with an additional rising and falling edgeof DQS_t. The optional postamble cycle is provided for the benefit of certain memorycontrollers.
5. There are two physical registers assigned to each bit of this MR parameter, designatedset point 0 and set point 1. Only the registers for the set point determined by the stateof the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MRaddress.
6. There are two physical registers assigned to each bit of this MR parameter, designatedset point 0 and set point 1. The device will operate only according to the values storedin the registers for the active set point, that is, the set point determined by the state ofthe FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will beignored by the device and may be changed without affecting device operation.

Table 4-17: Burst Sequence for Read

C4	C3	C2	C1	C0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
16-Bit READ Operation																																				
V	**0**	**0**	**0**	**0**	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F																
V	**0**	**1**	**0**	**0**	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3																
V	**1**	**0**	**0**	**0**	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7																
V	**1**	**1**	**0**	**0**	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B																
32-Bit READ Operation																																				
0	**0**	**0**	**0**	**0**	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
0	**0**	**1**	**0**	**0**	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13
0	**1**	**0**	**0**	**0**	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	14	15	16	17
0	**1**	**1**	**0**	**0**	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	1C	1D	1E	1F	10	11	12	13	14	15	16	17	18	19	1A	1B
1	**0**	**0**	**0**	**0**	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	**0**	**1**	**0**	**0**	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3
1	**1**	**0**	**0**	**0**	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	14	15	16	17	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
1	**1**	**1**	**0**	**0**	1C	1D	1E	1F	10	11	12	13	14	15	16	17	18	19	1A	1B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B

Notes:
1. C[1:0] are not present on the CA bus; they are implied to be zero.
2. The starting burst address is on 64-bit (4n) boundaries.

Table 4-18: Burst Sequence for Write

C4	C3	C2	C1	C0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
16-Bit WRITE Operation																																				
V	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F																
32-Bit WRITE Operation																																				
0	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F

Notes:
1. C[1:0] are not present on the CA bus; they are implied to be zero.
2. The starting burst address is on 256-bit (16n) boundaries for burst length 16.
3. The starting burst address is on 512-bit (32n) boundaries for burst length 32.
4. C[3:2] must be set to 0 for all WRITE operations.

Table 4-19: MR2 Device Feature 2 (MA[5:0] = 02h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
WR Lev	WLS	WL			RL		

Table 4-20: MR2 Op-Code Bit Definitions

Feature	Type	OP	Definition	Notes
RL READ latency	Write -only	OP[2:0]	RL and nRTP for DBI-RD disabled (MR3 OP[6] = 0b) 000b: RL = 6, nRTP = 8 (default) 001b: RL = 10, nRTP = 8 010b: RL = 14, nRTP = 8 011b: RL = 20, nRTP = 8 100b: RL = 24, nRTP = 10 101b: RL = 28, nRTP = 12 110b: RL = 32, nRTP = 14 111b: RL = 36, nRTP = 16	1, 3, 4
			RL and nRTP for DBI-RD enabled (MR3 OP[6] = 1b) 000b: RL = 6, nRTP = 8 001b: RL = 12,nRTP = 8 010b: RL = 16, nRTP = 8 011b: RL = 22, nRTP = 8 100b: RL = 28, nRTP = 10 101b: RL = 32, nRTP = 12 110b: RL = 36, nRTP = 14 111b: RL = 40, nRTP = 16	
WL WRITE latency	Write -only	OP[5:3]	WL set A (MR2 OP[6] = 0b) 000b: WL = 4 (default) 001b: WL = 6 010b: WL = 8 011b: WL = 10 100b: WL = 12 101b: WL = 14 110b: WL = 16 111b: WL = 18	1, 3, 4
			WL set B (MR2 OP[6] = 1b) 000b: WL = 4 001b: WL = 8 010b: WL = 12 011b: WL = 18 100b: WL = 22 101b: WL = 26 110b: WL = 30 111b: WL = 34	
WLS WRITE latencyset	Write -only	OP[6]	0b: Use WL set A (default) 1b: Use WL set B	1, 3, 4
WR Lev Write leveling	Write -only	OP[7]	0b: Disable write leveling (default) 1b: Enable write leveling	2

Notes:

1. See Latency Code Frequency Table for allowable frequency ranges for RL/WL/nWR.
2. After an MRW command to set the write leveling enable bit (OP[7] = 1b), the device remainsin the MRW state until another MRW command clears the bit (OP[7] = 0b). Noother commands are allowed until the write leveling enable bit is cleared.
3. There are two physical registers assigned to each bit of this MR parameter, designatedset point 0 and set point 1. Only the registers for the set point determined by the stateof the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command this MR address,or read from with an MRR command to this address.
4. There are two physical registers assigned to each bit of this MR parameter, designatedset point 0 and set point 1. The device will operate only according to the values storedin the registers for the active set point, that is, the set point determined by the state ofthe FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will beignored by the device and may be changed without affecting device operation.
5. nRTP is valid for BL16 only. For BL32, the SDRAM will add 8 clocks to the nRTP value beforestarting a precharge.

Table 4-21: Frequency Ranges for RL, WL, nWR, and nRTP Settings

READ Latency		WRITE Latency		nWR	nRTP	Lower Frequency Limit (>)	Upper Frequency Limit(≤)	Units	Notes
No DBI	w/DBI	Set A	Set B						
6	6	4	4	6	8	10	266	MHz	1–6
10	12	6	8	10	8	266	533		
14	16	8	12	16	8	533	800		
20	22	10	18	20	8	800	1066		
24	28	12	22	24	10	1066	1333		
28	32	14	26	30	12	1333	1600		
32	36	16	30	34	14	1600	1866		
36	40	18	34	40	16	1866	2133		

Notes:

1. The device should not be operated at a frequency above the upper frequency limit orbelow the lower frequency limit shown for each RL, WL, or nWR value.
2. DBI for READ operations is enabled in MR3 OP[6]. When MR3 OP[6] = 0, then the "NoDBI" column should be used for READ latency. When MR3 OP[6] = 1, then the "w/DBI"column should be used for READ latency.
3. WRITE latency set A and set B are determined by MR2 OP[6]. When MR2 OP[6] = 0, thenWRITE latency set A should be used. When MR2 OP[6] = 1, then WRITE latency set Bshould be used.
4. The programmed value for nRTP is the number of clock cycles the device uses to determinethe starting point of an internal PRECHARGE operation after a READ burst with AP(auto precharge) enabled . It is determined by RU(^{t}RTP/^{t}CK).
5. The programmed value of nWR is the number of clock cycles the device uses to determinethe starting point of an internal PRECHARGE operation after a WRITE burst withAP (auto precharge) enabled. It is determined by RU(^{t}WR/^{t}CK).
6. nRTP shown in this table is valid for BL16 only. For BL32, the device will add 8 clocks tothe nRTP value before starting a precharge.

Table 4-22: MR3 I/O Configuration 1 (MA[5:0] = 03h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DBI-WR	DBI-RD	PDDS			PPRP	WR-PST	PU-CAL

Table 4-23: MR3 Op-Code Bit Definitions

Feature	Type	OP	Definition	Notes
PU-CAL (Pull-up calibration point)	Write-only	OP[0]	0b: V_{DDQ}/0.6 1b: V_{DDQ}/0.5 (default)	1–4
WR-PST (WR postamble length)		OP[1]	0b: WR postamble = 0.5 × ^{t}CK (default) 1b: WR postamble = 1.5 × ^{t}CK	2, 3, 5
PPRP (Post-package repair protec-tion)		OP[2]	0b: PPR protection disabled (default) 1b: PPR protection enabled	6
PDDS (Pull-down drive strength)		OP[5:3]	000b: RFU 001b: R_{ZQ}/1 010b: R_{ZQ}/2 011b: R_{ZQ}/3 100b: R_{ZQ}/4 101b: R_{ZQ}/5 110b: R_{ZQ}/6 (default) 111b: Reserved	1, 2, 3
DBI-RD (DBI-read enable)		OP[6]	0b: Disabled (default) 1b: Enabled	2, 3
DBI-WR (DBI-write enable)		OP[7]	0b: Disabled (default) 1b: Enabled	2, 3

Notes:

1. All values are typical. The actual value after calibration will be within the specified tolerancefor a given voltage and temperature. Recalibration may be required as voltage andtemperature vary.
2. There are two physical registers assigned to each bit of this MR parameter: designatedset point 0 and set point 1. Only the registers for the set point determined by the stateof the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MRaddress, or read from with an MRR command to this address.
3. There are two physical registers assigned to each bit of this MR parameter: designatedset point 0 and set point 1.The device will operate only according to the values stored inthe registers for the active set point, for example, the set point determined by the stateof the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point willbe determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registersfor the inactive set point will be ignored by the device, and may be changed withoutaffecting device operation.
4. For dual-channel device, PU-CAL (MR3-OP[0]) must be set the same for both channels ona die. The SDRAM will read the value of only one register (Ch.A or Ch.B); the choice isvendor-specific, so both channels must be set the same.
5. 1.5 × tCK apply > 1.6 GHz clock.
6. If MR3 OP[2] is set to 1b, PPR protection mode is enabled. The PPR protection bit is asticky bit and can only be set to 0b by a power on reset. MR4 OP[4] controls entry to PPRmode. If PPR protection is enabled then the DRAM will not allow writing of 1b to MR4OP[4].

Table 4-24: MR4 Device Temperature (MA[5:0] = 04h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF	Thermal offset		PPRE	SR abort	Refresh rate		

Table 4-25: MR4 Op-Code Bit Definitions

Feature	Type	OP	Definition	Notes
Refresh rate	Read-only	OP[2:0]	000b: SDRAM low temperature operating limit exceeded 001b: 4x refresh 010b: 2x refresh 011b: 1x refresh (default) 100b: 0.5x refresh 101b: 0.25x refresh, no derating 110b: 0.25x refresh, with derating 111b: SDRAM high temperature operating limit exceeded	1–4, 7–9
SR abort (Self RefreshAbort)	Write	OP[3]	0b: Disable (default) 1b: Device dependent	9
PPRE (Post-package repair entry/exit)	Write	OP[4]	0b: Exit PPR mode (default) 1b: Enter PPR mode (Reference MR25 OP[7:0] for available PPR resources)	5, 9
Thermal Offset-Controller offset to TCSR	Write	OP[6:5]	00b: No offset, 0~5°C gradient (default) 01b: 5°C offset, 5~10°C gradient 10b: 10°C offset, 10~15°C gradient 11b: Reserved	9
TUF (Temperature updateflag)	Read-only	OP7	0b: OP[2:0] No change in OP[2:0] since last MR4 read (default) 1b: Change in OP[2:0] since last MR4 read	6–8

Notes:

1. The refresh rate for each MR4 OP[2:0] setting applies to ^{t}REFI, ^{t}REFIpb, and ^{t}REFW. MR4OP[2:0] = 011b corresponds to a device temperature of 85°C. Other values require eithera longer (2x, 4x) refresh interval at lower temperatures or a shorter (0.5x, 0.25x) refreshinterval at higher temperatures. If MR4 OP[2] = 1b, the device temperature is greaterthan 85°C.
2. At higher temperatures (>85°C), AC timing derating may be required. If derating is requirethe device will set MR4 OP[2:0] = 110b. See derating timing requirements in theAC Timing section.
3. DRAM vendors may or may not report all of the possible settings over the operatingtemperature range of the device. Each vendor guarantees that their device will work atany temperature within the range using the refresh interval requested by their device.
4. The device may not operate properly when MR4 OP[2:0] = 000b or 111b.
5. Post-package repair can be entered or exited by writing to MR4 OP[4].
6. When MR4 OP[7] = 1b, the refresh rate reported in MR4 OP[2:0] has changed since thelast MR4 read. A mode register read from MR4 will reset MR4 OP[7] to 0b.
7. MR4 OP[7] = 0b at power-up. MR4 OP[2:0] bits are valid after initialization sequence(Te).
8. See the Temperature Sensor section for information on the recommendedfrequency ofreading MR4.
9. MR4 OP[6:3] can be written in this register. All other bits will be ignored by the deviceduring an MRW command to this register.

Table 4-26: MR5 Basic Configuration 1 (MA[5:0] = 05h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Manufacturer ID							

Table 4-27: MR5 Op-Code Bit Definitions

Feature	Type	OP	Definition
Manufacturer ID	Read-only	OP[7:0]	1111 1111b All others: Reserved

Table 4-28: MR6 Basic Configuration 2 (MA[5:0] = 06h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID1							

Note:
1. MR6 is vendor-specific.

Table 4-29: MR6 Op-Code Bit Definitions

Feature	Type	OP	Definition
Revision ID1	Read-only	OP[7:0]	xxxx xxxxb: Revision ID1

Note:
1.MR6 is vendor-specific.

Table 4-30: MR7 Basic Configuration 3 (MA[5:0] = 07h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID2							

Table 4-31: MR7 Op-Code Bit Definitions

Feature	Type	OP	Definition
Revision ID2	Read-only	OP[7:0]	xxxx xxxxb: Revision ID2

Note:
1. MR7 is vendor-specific.

Table 4-32: MR8 Basic Configuration 4 (MA[5:0] = 08h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
I/O width		Density				Type	

Table 4-33: MR8 Op-Code Bit Definitions

Feature	Type	OP	Definition
Type	Read-only	OP[1:0]	00b: S16 SDRAM (16n prefetch) All others: Reserved
Density	Read-only	OP[5:2]	0000b: 4Gb dual-channel die/2Gb single-channel die 0001b: 6Gb dual-channel die/3Gb single-channel die 0010b: 8Gb dual-channel die/4Gb single-channel die 0011b: 12Gb dual-channel die/6Gb single-channel die 0100b: 16Gb dual-channel die/8Gb single-channel die 0101b: 24Gb dual-channel die/12Gb single-channel die 0110b: 32Gb dual-channel die/16Gb single-channel die 1100b: 2Gb dual-channel die/1Gb single-channel die All others: Reserved
I/O width	Read-only	OP[7:6]	00b: x16/channel All others: Reserved

Table 4-34: MR9 Test Mode (MA[5:0] = 09h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Vendor-specific test mode							

Table 4-35: MR9 Op-Code Definitions

Feature	Type	OP	Definition
Test mode	Write-only	OP[7:0]	0000000b; Vendor-specific test mode disabled (default)

Table 4-36: MR10 Calibration (MA[5:0] = 0Ah)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU							ZQ RESET

Table 4-37: MR10 Op-Code Bit Definitions

Feature	Type	OP	Definition
ZQ reset	Write-only	OP[0]	0b: Normal operation (default) 1b: ZQ reset

Notes:

1. See AC Timing table for calibration latency and timing.
2. If ZQ is connected to V_{DDQ} through R_{ZQ}, either the ZQ CALIBRATION function or defaultcalibration (via ZQ reset) is supported. If ZQ is connected to V_{SS}, the device operateswith default calibration and ZQ CALIBRATION commands are ignored. In both cases, theZQ connection must not change after power is supplied to the device.

Table 4-38: MR11 ODT Control (MA[5:0] = 0Bh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU	CA ODT			RFU	DQ ODT		

Table 4-39: MR11 Op-Code Bit Definitions

Feature	Type	OP	Definition	Notes
DQ ODT DQ bus receiver on-die termination	Write-only	OP[2:0]	000b: Disable (default) 001b: RZQ/1 010b: RZQ/2 011b: RZQ/3 100b: RZQ/4 101b: RZQ/5 110b: RZQ/6 111b: RFU	1, 2, 3
CA ODT CA bus receiver on-die termination	Write-only	OP[6:4]	000b: Disable (default) 001b: RZQ/1 010b: RZQ/2 011b: RZQ/3 100b: RZQ/4 101b: RZQ/5 110b: RZQ/6 111b: RFU	1, 2, 3

Notes:

1. All values are typical. The actual value after calibration will be within the specified tolerancefor a given voltage and temperature. Re-calibration may be required as voltageand temperature vary.
2. There are two physical registers assigned to each bit of this MR parameter, designatedset point 0 and set point 1. Only the registers for the set point determined by the stateof the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MRaddress, or read from with an MRR command to this address.
3. There are two physical registers assigned to each bit of this MR parameter, designatedset point 0 and set point 1. The device will operate only according to the values storedin the registers for the active set point, i.e., the set point determined by the state of theFSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignoredby the device and may be changed without affecting device operation.

Table 4-40: MR12 Register Information (MA[5:0] = 0Ch)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU	V_{RCA}	$V_{REF(CA)}$					

Table 4-41: MR12 Op-Code Bit Definitions

Feature	Type	OP	Definition	Notes
$V_{REF(CA)}$ $V_{REF(CA)}$ settings	Read/ Write	OP[5:0]	000000b–110010b: See V_{REF} Settings Table All others: Reserved	1–3, 5, 6
V_{RCA} $V_{REF(CA)}$ range	Read/ Write	OP[6]	0b: $V_{REF(CA)}$ range[0] enabled 1b: $V_{REF(CA)}$ range[1] enabled (default)	1, 2, 4, 5,6

Notes:

1. This register controls the $V_{REF(CA)}$ levels for frequency set point[1:0]. Values from eitherVR(ca)[0] or VR(ca)[1] may be selected by setting MR12 OP[6] appropriately.
2. A read to MR12 places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQwill be set to 0. See the MRR Operation section.
3. A write to MR12 OP[5:0] sets the internal $V_{REF(CA)}$ level for FSP[0] when MR13 OP[6] = 0bor sets the internal $V_{REF(CA)}$ level for FSP[1] when MR13 OP[6] = 1b. The time required for$V_{REF(CA)}$ to reach the set level depends on the step size from the current level to the newlevel. See the $V_{REF(CA)}$ training section.
4. A write to MR12 OP[6] switches the device between two internal $V_{REF(CA)}$ ranges. Therange (range[0] or range[1]) must be selected when setting the $V_{REF(CA)}$ register. The value,once set, will be retained until overwritten or until the next power-on or resetevent.
5. There are two physical registers assigned to each bit of this MR parameter, designatedset point 0 and set point 1. Only the registers for the set point determined by the stateof the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MRaddress, or read from with an MRR command to this address.
6. There are two physical registers assigned to each bit of this MR parameter, designatedset point 0 and set point 1. The device will operate only according to the values storedin the registers for the active set point, i.e., the set point determined by the state of theFSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignoredby the device, and may be changed without affecting device operation.

Table 4-42: MR13 Register Control (MA[5:0] = 0Dh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
FSP-OP	FSP-WR	DMD	RRO	VRCG	VRO	RPT	CBT

Table 4-43: MR13 Op-Code Bit Definition

Feature	Type	OP	Definition	Notes
CBT Command bus training	Write-only	OP[0]	0b: Normal operation (default) 1b: Command bus training mode enabled	1
RPT Read preamble training		OP[1]	0b: Disabled (default) 1b: Read preamble training mode enabled	
VRO V_{REF} output		OP[2]	0b: Normal operation (default) 1b: Output the $V_{REF(CA)}$ and $V_{REF(DQ)}$ values on DQ bits	2
VRCG VREF current generator		OP[3]	0b: Normal operation (default) 1b: Fast response (high current) mode	3
RRO Refresh rate option		OP[4]	0b: Disable codes 001 and 010 in MR4 OP[2:0] 1b: Enable all codes in MR4 OP[2:0]	4, 5
DMD Data mask disable		OP[5]	0b: DATA MASK operation enabled (default) 1b: DATA MASK operation disabled	6
FSP-WR Frequency set point write /read		OP[6]	0b: Frequency set point[0] (default) 1b: Frequency set point[1]	7
FSP-OP Frequency set point operationmode		OP[7]	0b: Frequency set point[0] (default) 1b: Frequency set point[1]	8

Notes:

1. A write to set OP[0] = 1 causes the LPDDR4 SDRAM to enter the command bus trainingmode. When OP[0] = 1 and CKE goes LOW, commands are ignored and the contents ofCA[5:0] are mapped to the DQ bus. CKE must be brought HIGH before doing a MRW toclear this bit (OP[0] = 0) and return to normal operation. See the Command Bus Trainingsection for more information.
2. When set, the device will output the $VR_{EF(CA)}$ and $V_{REF(DQ)}$ voltage on DQ pins. Only the"active" frequency set point, as defined by MR13 OP[7], will be output on the DQ pins.This function allows an external test system to measure the internal V_{REF} levels. The DQpins used for V_{REF} output are vendor-specific.
3. When OP[3] = 1, the V_{REF} circuit uses a high current mode to improve V_{REF} settling time.
4. MR13 OP[4] RRO bit is valid only when MR0 OP[0] = 1. For LPDDR4 SDRAM with MR0OP[0] = 0, MR4 OP[2:0] bits are not dependent on MR13 OP[4].
5. When OP[4] = 0, only 001b and 010b in MR4 OP[2:0] are disabled. LPDDR4 SDRAM mustreport 011b instead of 001b or 010b in this case. Controller should follow the refreshmode reported by MR4 OP[2:0], regardless of RRO setting. TCSR function does not dependon RRO setting.
6. When enabled (OP[5] = 0b) data masking is enabled for the device. When disabled(OP[5] = 1b), the device will ignore any mask patterns issued during a MASKED WRITEcommand. See the Data Mask section for more information.
7. FSP-WR determines which frequency set point registers are accessed with MRW andMRR commands for the following functions such as $V_{REF(CA)}$ setting, $V_{REF(CA)}$ range,$V_{REF(DQ)}$ setting, $V_{REF(DQ)}$ range. For more information, refer to Frequency Set Point section.
8. FSP-OP determines which frequency set point register values are currently used to specifydevice operation for the following functions such as $V_{REF(CA)}$ setting, $V_{REF(CA)}$ range,$V_{REF(DQ)}$ setting, $V_{REF(DQ)}$ range. For more information, refer to Frequency Set Point section.

Table 4-44: Mode Register14 (MA[5:0] = 0Eh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU	VR_{DQ}	$V_{REF(DQ)}$					

Table 4-45: MR14 Op-Code Bit Definition

Feature	Type	OP	Definition	Notes
$V_{REF(DQ)}$ $V_{REF(DQ)}$ settings	Read/ Write	OP[5:0]	000000b–110010b: See V_{REF} Settings Table All others: Reserved	1–3, 5, 6
VR_{DQ} $V_{REF(DQ)}$ range		OP[6]	0b: $V_{REF(DQ)}$ range[0] enabled 1b: $V_{REF(DQ)}$ range[1] enabled (default)	1, 2, 4–6

Notes:

1. This register controls the $V_{REF(DQ)}$ levels for frequency set point[1:0]. Values from eitherVR_{DQ}[0] (vendor defined) or VR_{DQ}[1] (vendor defined) may be selected by setting OP[6]appropriately.
2. A read (MRR) to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits andunused DQ shall be set to 0. See the MRR Operation section.
3. A write to OP[5:0] sets the internal $V_{REF(DQ)}$ level for FSP[0] when MR13 OP[6] = 0b, orsets FSP[1] when MR13 OP[6] = 1b. The time required for $V_{REF(DQ)}$ to reach the set leveldepends on the step size from the current level to the new level. See the $V_{REF(DQ)}$ trainingsection.
4. A write to OP[6] switches the device between two internal $V_{REF(DQ)}$ ranges. The range(range[0] or range[1]) must be selected when setting the $V_{REF(DQ)}$ register. The value,once set, will be retained until overwritten, or until the next power-on or reset event.
5. There are two physical registers assigned to each bit of this MR parameter, designatedset point 0 and set point 1. Only the registers for the set point determined by the stateof the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MRaddress, or read from with an MRR command to this address.
6. There are two physical registers assigned to each bit of this MR parameter, designatedset point 0 and set point 1. The device will operate only according to the values storedin the registers for the active set point, i.e., the set point determined by the state of theFSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignoredby the device, and may be changed without affecting device operation.

Table 4-46: V_{REF} Setting for Range[0] and Range[1]

Notes 1-3 apply to entire table

Function	OP	Range[0] Values		Range[1] Values	
		$V_{REF(CA)}$ (% of V_{DDQ}) $V_{REF(DQ)}$ (% of V_{DDQ})		$V_{REF(CA)}$ (% of V_{DDQ}) $V_{REF(DQ)}$ (% of V_{DDQ})	
V_{REF} Setting for MR12 and MR14	OP[5:0]	000000b: 15.0%	011010b: 30.5%	000000b: 32.9%	011010b: 48.5%
		000001b: 15.6%	011011b: 31.1%	000001b: 33.5%	011011b: 49.1%
		000010b: 16.2%	011100b: 31.7%	000010b: 34.1%	011100b: 49.7%
		000011b: 16.8%	011101b: 32.3%	000011b: 34.7%	011101b: 50.3%(default)
		000100b: 17.4%	011110b: 32.9%	000100b: 35.3%	011110b: 50.9%
		000101b: 18.0%	011111b: 33.5%	000101b: 35.9%	011111b: 51.5%
		000110b: 18.6%	100000b: 34.1%	000110b: 36.5%	100000b: 52.1%
		000111b: 19.2%	100001b: 34.7%	000111b: 37.1%	100001b: 52.7%
		001000b: 19.8%	100010b: 35.3%	001000b: 37.7%	100010b: 53.3%
		001001b: 20.4%	100011b: 35.9%	001001b: 38.3%	100011b: 53.9%
		001010b: 21.0%	100100b: 36.5%	001010b: 38.9%	100100b: 54.5%
		001011b: 21.6%	100101b: 37.1%	001011b: 39.5%	100101b: 55.1%
		001100b: 22.2%	100110b: 37.7%	001100b: 40.1%	100110b: 55.7%
		001101b: 22.8%	100111b: 38.3%	001101b: 40.7%	100111b: 56.3%
		001110b: 23.4%	101000b: 38.9%	001110b: 41.3%	101000b: 56.9%
		001111b: 24.0%	101001b: 39.5%	001111b: 41.9%	101001b: 57.5%
		010000b: 24.6%	101010b: 40.1%	010000b: 42.5%	101010b: 58.1%
		010001b: 25.1%	101011b: 40.7%	010001b: 43.1%	101011b: 58.7%
		010010b: 25.7%	101100b: 41.3%	010010b: 43.7%	101100b: 59.3%
		010011b: 26.3%	101101b: 41.9%	010011b: 44.3%	101101b: 59.9%
		010100b: 26.9%	101110b: 42.5%	010100b: 44.9%	101110b: 60.5%
		010101b: 27.5%	101111b: 43.1%	010101b: 45.5%	101111b: 61.1%
		010110b: 28.1%	110000b: 43.7%	010110b: 46.1%	110000b: 61.7%
		010111b: 28.7%	110001b: 44.3%	010111b: 46.7%	110001b: 62.3%
		011000b: 29.3%	110010b: 44.9%	011000b: 47.3%	110010b: 62.9%
		011001b: 29.9%	All Others: Reserved	011001b: 47.9%	All Others: Reserved

Notes:

1. These values may be used for MR14 OP[5:0] and MR12 OP[5:0] to set the $V_{REF(CA)}$ or$V_{REF(DQ)}$ levels in the device.
2. The range may be selected in each of the MR14 or MR12 registers by setting OP[6] appropriately.
3. Each of the MR14 or MR12 registers represents either FSP[0] or FSP[1]. Two frequency setpoints each for CA and DQ are provided to allow for faster switching between terminatedand unterminated operation or between different high-frequency settings, whichmay use different terminations values.

Table 4-47: MR15 Register Information (MA[5:0] = 0Fh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Lower-byte invert register for DQ calibration							

Table 4-48: MR15 Op-code Bit Definition

Feature	Type	OP	Definition	Notes
Lower-byte invert for DQ calibration	Write-only	OP[7:0]	The following values may be written for any operand OP[7:0] and will be applied to the corresponding DQ locations DQ[7:0] within a byte lane 0b: Do not invert 1b: Invert the DQ calibration patterns in MR32 andMR40 Default value for OP[7:0] = 55h	1–3

Notes:
1. This register will invert the DQ Calibration pattern found in MR32 and MR40 for any singleDQ or any combination of DQ. Example: If MR15 OP[7:0] = 00010101b, then the DQcalibration patterns transmitted on DQ[7, 6, 5, 3, 1] will not be inverted, but the DQ calibrationpatterns transmitted on DQ[4, 2, 0] will be inverted.
2. DM[0] is not inverted and always transmits the "true" data contained in MR32 andMR40.
3. No data bus inversion (DBI) function is enacted during DQ read calibration, even if DBI isenabled in MR3-OP[6].

Table 4-49: MR15 Invert Register Pin Mapping

PIN	DQ0	DQ1	DQ2	DQ3	DMIO	DQ4	DQ5	DQ6	DQ7
MR15	OP0	OP1	OP2	OP3	No invert	OP4	OP5	OP6	OP7

Table 4-50: MR16 PASR Bank Mask (MA[5:0] = 010h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
PASR bank mask							

Table 4-51: MR16 Op-Code Bit Definitions

Feature	Type	OP	Definition
Bank[7:0] mask	Write-only	OP[7:0]	0b: Bank refresh enabled (default) 1b: Bank refresh disabled

OP[n]	Bank Mask	8-Bank SDRAM
0	xxxxxxx1	Bank 0
1	xxxxxx1x	Bank 1
2	xxxxx1xx	Bank 2
3	xxxx1xxx	Bank 3
4	xxx1xxxx	Bank 4
5	xx1xxxxx	Bank 5
6	x1xxxxxx	Bank 6
7	1xxxxxxx	Bank 7

Notes:
1. When a mask bit is asserted (OP[n] = 1), refresh to that bank is disabled.
2. PASR bank masking is on a per-channel basis; the two channels on the die may have differentbank masking.

Table 4-52: MR17 PASR Segment Mask (MA[5.:0] = 11h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
PASR segment mask							

Table 4-53: MR17 PASR Segment Mask Definitions

Feature	Type	OP	Definition
Segment[7:0] mask	Write-only	OP[7:0]	0b: Segment refresh enabled (default) 1b: Segment refresh disabled

Table 4-54: MR17 PASR Segment Mask

Segment	OP	Segment Mask	Density (per channel)							
			1Gb	2Gb	3Gb	4Gb	6Gb	8Gb	12Gb	16Gb
			R[12:10]	R[13:11]	R[14:12]	R[14:12]	R[15:13]	R[15:13]	R[16:14]	R[16:14]
0	0	XXXXXXX1	000b							
1	1	XXXXXX1X	001b							
2	2	XXXXX1XX	010b							
3	3	XXXX1XXX	011b							
4	4	XXX1XXXX	100b							
5	5	XX1XXXXX	101b							
6	6	X1XXXXXX	110b	110b	Not allowed	110b	Not allowed	110b	Not allowed	110b
7	7	1XXXXXXX	111b	111b		111b		111b		111b

Notes:
1. This table indicates the range of row addresses in each masked segment. "X" is “Don’tCare” for a particular segment.
2. PASR segment-masking is on a per-channel basis. The two channels on the die may havedifferent segment masking indual-channel devices.
3. For 3Gb, 6Gb, and 12Gb density per channel, OP[7:6] must always be LOW (= 00b).

Table 4-55: MR18 Register Information (MA[5:0]=12h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQS oscillator count - LSB							

Table 4-56: MR18 LSB DQS Oscillator Count

Notes 1–3 apply to entire table

Function	Type	OP	Definition
DQS oscillatorcount (WR trainingDQS oscillator)	Read-only	OP[7:0]	0h–FFh LSB DRAM DQS oscillator count

Notes:
1. MR18 reports the LSB bits of the DRAM DQS oscillator count. The DRAM DQS oscillatorcount value is used to train DQS to the DQ data valid window. The value reported bythe DRAM in this mode register can be used by the memory controller to periodicallyadjust the phase of DQS relative to DQ.
2. Both MR18 and MR19 must be read (MRR) and combined to get the value of the DQSoscillator count.
3. The value in this register is reset each time an MPC command is issued to start in theDQS oscillator counter.

Table 4-57: MR19 Register Information (MA[5:0] = 13h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQS oscillator count – MSB							

Table 4-58: MR19 DQS Oscillator Count

Notes 1–3 apply to the entire table

Function	Type	OP	Definition
DQS oscillatorcount – MSB (WRtraining DQS oscillator)	Read-only	OP[7:0]	0h–FFh MSB DRAM DQS oscillator count

Notes:
1. MR19 reports the MSB bits of the DRAM DQS oscillator count. The DRAM DQS oscillatorcount value is used to train DQS to the DQ data valid window. The value reported bythe DRAM in this mode register can be used by the memory controller to periodicallyadjust the phase of DQS relative to DQ.
2. Both MR18 and MR19 must be read (MRR) and combined to get the value of the DQSoscillator count.
3. A new MPC[START DQS OSCILLATOR] should be issued to reset the contents of MR18/MR19.

Table 4-59: MR20 Register Information (MA[5:0] = 14h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Upper-byte invert register for DQ calibration							

Table 4-60: MR20 Register Information

Notes 1–3 apply to entire table

Function	Type	OP	Definition
Upper-byte invert for DQ calibration	Write-only	OP[7:0]	The following values may be written for any operand OP[7:0] and willbe applied to the corresponding DQ locations DQ[15:8] within a bytelane 0b: Do not invert 1b: Invert the DQ calibration patterns in MR32 and MR40 Default value for OP[7:0] = 55h

Notes:

1. This register will invert the DQ calibration pattern found in MR32 and MR40 for any singleDQ or any combination of DQ. For example, if MR20 OP[7:0] = 00010101b, the DQcalibration patterns transmitted on DQ[15, 14, 13, 11, 9] will not be inverted, but the DQcalibration patterns transmitted on DQ[12, 10, 8] will be inverted.
2. DM[1] is not inverted and always transmits the true data contained in MR32 and MR40.
3. No data bus inversion (DBI) function is enacted during DQ read calibration, even if DBI isenabled in MR3 OP[6].

Table 4-61: MR20 Invert Register Pin Mapping

Pin	DQ8	DQ9	DQ10	DQ11	DMI1	DQ12	DQ13	DQ14	DQ15
MR20	OP0	OP1	OP2	OP3	No invert	OP4	OP5	OP6	OP7

Table 4-62: MR21 Register Information (MA[5:0] = 15h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU							

Table 4-63: MR22 Register Information (MA[5:0] = 16h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
ODTD for x8_2ch		ODTD-CA	ODTE-CS	ODTE-CK	SOC ODT		

Table 4-64: MR22 Register Information

Function	Type	OP	Data	Notes
SOC ODT (controller ODT value for V_{OH} calibration)	Write-only	OP[2:0]	000b: Disable (default) 001b: R_{ZQ}/1(Illegal if MR3 OP[0] = 0b) 010b: R_{ZQ}/2 011b: R_{ZQ}/3(Illegal if MR3 OP[0] = 0b) 100b: R_{ZQ}/4 101b: R_{ZQ}/5(Illegal if MR3 OP[0] = 0b) 110b: R_{ZQ}/6(Illegal if MR3 OP[0] = 0b) 111b: RFU	1, 2, 3
ODTE-CK (CK ODT enabled for non-terminating rank)	Write-only	OP[3]	ODT bond PAD is ignored 0b: ODT-CK override disabled (default) 1b: ODT-CK override enabled	2, 3
ODTE-CS (CS ODT enabled for non-terminating rank)	Write-only	OP[4]	ODT bond PAD is ignored 0b: ODT-CS override disabled (default) 1b: ODT-CS override enabled	2, 3
ODTD-CA (CA ODT termination disable)	Write-only	OP[5]	ODT bond PAD is ignored 0b: CA ODT obeys ODT_CA bond pad (default) 1b: CA ODT disabled	2, 3
ODTD for x8_2ch (Byte)mode	Write-only	OP[7:6]	See Byte Mode section	

Notes:

1. All values are typical.
2. There are two physical registers assigned to each bit of this MR parameter: designatedset point 0 and set point 1. Only the registers for the set point determined by the stateof the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MRaddress, or read from with an MRR command to this address.
3. There are two physical registers assigned to each bit of this MR parameter: designatedset point 0 and set point 1. The device will operate only according to the values storedin the registers for the active set point, for example, the set point determined by thestate of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive setpoint will be ignored by the device, and may be changed without affecting device operation.

Table 4-65: MR23 Register Information (MA[5:0] = 17h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQS interval timer run-time setting							

Table 4-66: MR23 Register Information

Notes 1–2 apply to entire table

Function	Type	OP	Data
DQS interval timer runtime	Write-only	OP[7:0]	00000000b: Disabled (default) 00000001b: DQS timer stops automatically at the 16th clock aftertimer start 00000010b: DQS timer stops automatically at the 32nd clock aftertimer start 00000011b: DQS timer stops automatically at the 48th clock aftertimer start 00000100b: DQS timer stops automatically at the 64th clock aftertimer start --------- Through --------- 00111111b: DQS timer stops automatically at the (63 × 16)th clockafter timer start 01XXXXXXb: DQS timer stops automatically at the 2048th clock aftertimer start 10XXXXXXb: DQS timer stops automatically at the 4096th clock aftertimer start 11XXXXXXb: DQS timer stops automatically at the 8192nd clock aftertimer start

Notes:

1. MPC command with OP[6:0] = 1001101b (stop DQS Interval Oscillator) stops the DQS intervaltimer in the case of MR23 OP[7:0] = 00000000b.
2. MPC command with OP[6:0] = 1001101b (stop DQS Interval Oscillator) is illegal with validnonzero values in MR23 OP[7:0].

Table 4-67: MR24 Register Information (MA[5:0] = 18h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TRR mode	TRR mode Ban			Unlimited MAC	MAC value		

Table 4-68: MR24 Register Information

Function	Type	OP	Data	Notes
MAC value	Read	OP[2:0]	000b: Unknown (OP[3] = 0) or Unlimited (OP[3] =1) 001b: 700K 010b: 600K 011b: 500K 100b: 400K 101b: 300K 110b: 200K 111b: Reserved	1 , 2
Unlimited MAC	Read	OP[3]	0b: OP[2:0] defines the MAC value 1b: Unlimited MAC value	2, 3
TRR mode Ban	Write	OP[6:4]	000b: Bank 0 001b: Bank 1 010b: Bank 2 011b: Bank 3 100b: Bank 4 101b: Bank 5 110b: Bank 6 111b: Bank 7	
TRR mode	Write	OP[7]	0b: Disabled (default) 1b: Enabled	

Notes:

1. Unknown means that the device is not tested for tMAC and pass/fail values are unknown.Unlimited means that there is no restriction on the number of activates betweenrefresh windows.
2. There is no restriction to the number of activates.
3. MR24 OP[2:0] set to 000b.

Table 4-69: MR25 Register Information (MA[5:0] = 19h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Bank 7	Bank 6	Bank 5	Bank 4	Bank 3	Bank 2	Bank 1	Bank 0

Table 4-70: MR25 Register Information

Function	Type	OP	Data
PPR resources	Read-only	OP[7:0]	0b: PPR resource is not available 1b: PPR resource is available

Note:

1. When OP[n] = 0, there is no PPR resource available for that bank. When OP[n] = 1, thereis a PPR resource available for that bank, and PPR can be initiated by the controller.

Table 4-71: MR26:29 Register Information (MA[5:0] = 1Ah–1Fh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Reserved for future use							

Table 4-72: MR30 Register Information (MA[5:0] = 1Eh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Valid 0 or 1							

Table 4-73: MR30 Register Information

Function	Type	OP	Data
SDRAM will ignore	Write-only	OP[7:0]	Don't care

Note:

1. This register is reserved for testing purposes. The logical data values written to OP[7:0]will have no effect on SDRAM operation; however, timings need to be observed as forany other MR access command.

Table 4-74: MR31 Register Information (MA[5:0] = 1Fh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Reserved for future use							

Table 4-75: MR32 Register Information(MA[5:0] = 20h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQ calibration pattern A (default = 5Ah)							

Table 4-76: MR32 Register Information

Function	Type	OP	Data	Notes
Return DQ calibration pattern MR32 + MR40	Write-only	OP[7:0]	Xb: An MPC command issued with OP[6:0] = 1000011b causes the device to return the DQ calibration pattern contained in this register and (followed by) the contents of MR40. A default pattern 5Ah is loaded at power-up or reset, or the pattern may be overwritten with a MRW to this register. The contents of MR15 and MR20 will invert the MR32/MR40 data pattern for a given DQ (see MR15/ MR20 for more information).	1, 2, 3

Notes:

1. The patterns contained in MR32 and MR40 are transmitted on DQ[15:0] and DMI[1:0]when read DQ calibration is initiated via an MPC command. The pattern is transmittedserially on each data lane and organized little endian such that the low-order bit in abyte is transmitted first. If the data pattern is 27H, the first bit transmitted is a 1 followedby 1, 1, 0, 0, 1, 0, and 0. The bit stream will be 00100111.
2. MR15 and MR20 may be used to invert the MR32/MR40 data pattern on the DQ pins.
See MR15 and MR20 for more information. Data is never inverted on the DMI[1:0] pins.
3. The data pattern is not transmitted on the DMI[1:0] pins if DBI-RD is disabled via MR3OP[6].
4. No DATA BUS INVERSION (DBI) function is enacted during read DQ calibration, even ifDBI is enabled in MR3 OP[6].

Table 4-77: MR33:38 Register Information (MA[5:0] = 21h–26h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Do not use							

Table 4-78: MR39 Register Information (MA[5:0] = 27h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Valid 0 or 1							

Table 4-79: MR30 Register Information

Function	Type	OP	Data
SDRAM will ignore	Write-only	OP[7:0]	Don't care

Note:

1. This register is reserved for testing purposes. The logical data values written to OP[7:0]will have no effect on SDRAM operation; however, timings need to be observed as forany other MR access command.

Table 4-80: MR40 Register Information (MA[5:0] = 28h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQ calibration pattern B (default = 3Ch)							

Table 4-81: MR40 Register Information

Function	Type	OP	Data	Notes
Return DQ calibration pattern MR32 + MR40	Write-only	OP[7:0]	Xb: A default pattern 3Ch is loaded at power-up or reset, or the pattern may be overwritten with a MRW to this register. See MR32 for more information.	1, 2, 3

Notes:

1. The pattern contained in MR40 is concatenated to the end of MR32 and transmitted onDQ[15:0] and DMI[1:0] when DQ read calibration is initiated via an MPC command. Thepattern is transmitted serially on each data lane and organized little endian such thatthe low-order bit in a byte is transmitted first. If the data pattern in MR40 is 27H, thefirst bit transmitted will be a 1, followed by 1, 1, 0, 0, 1, 0, and 0. The bit stream will be00100111.
2. MR15 and MR20 may be used to invert the MR32/MR40 data patterns on the DQ pins.See MR15 and MR20 for more information. Data is never inverted on the DMI[1:0] pins.
3. The data pattern is not transmitted on the DMI[1:0] pins if DBI-RD is disabled via MR3OP[6].
4. No data bus inversion (DBI) function is enacted during DQ read calibration, even if DBI isenabled in MR3 OP[6].

Table 4-82: MR41:47 Register Information (MA[5:0] = 29h–2Fh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Do not use							

Table 4-83: MR48:63 Register Information (MA[5:0] = 30h–3Fh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Reserved for future use							

4.9 Commands and Timing

Commands transmitted on the CA bus are encoded into two parts and are latched ontwo consecutive rising edges of the clock. This is called 2-tick CA capture because eachcommand requires two clock edges to latch and decode the entire command.

Truth Tables

Truth tables provide complementary information to the state diagram. They also clarifydevice behavior and applicable restrictions when considering the actual state of thebanks.

Unspecified operations and timings are illegal. To ensure proper operation after an illegalevent, the device must be either reset by asserting the RESET_n command or powereddown and then restarted using the specified initialization sequence before normaloperation can continue.

CKE signal has to be held HIGH when the commands listed in the command truth tableinput.

Table 4-84: Command Truth Table

Commands are transmitted to the device across a six-lane interface and use CK, CKE, and CS to control the capture oftransmitted data

Command	CS	SDR CA Pins						CK Edge	Notes
		CA0	CA1	CA2	CA3	CA4	CA5		
MRW-1	H	L	H	H	L	L	OP7	↑	1, 11
	L	MA0	MA1	MA2	MA3	MA4	MA5	↓	
MRW-2	H	L	H	H	L	H	OP6	↑	1, 11
	L	OP0	OP1	OP2	OP3	OP4	OP5	↓	
MRR-1	H	L	H	H	H	L	V	↑	1, 2, 12
	L	MA0	MA1	MA2	MA3	MA4	MA5	↓	
REFRESH (all/per bank)	H	L	L	L	H	L	AB	↑	1, 2, 3, 4
	L	BA0	BA1	BA2	V	V	V	↓	
ENTER SELF REFRESH	H	L	L	L	H	H	V	↑	1, 2
	L	V						↓	
ACTIVATE-1	H	H	L	R12	R13	R14	R15	↑	1, 2, 3, 11
	L	BA0	BA1	BA2	R16	R10	R11	↓	
ACTIVATE-2	H	H	H	R6	R7	R8	R9	↑	1, 11
	L	R0	R1	R2	R3	R4	R5	↓	
WRITE-1	H	L	L	H	L	L	BL	↑	1, 2, 3, 6, 7, 9
	L	BA0	BA1	BA2	V	C9	AP	↓	
EXIT SELF REFRESH	H	L	L	H	L	H	V	↑	1, 2
	L	V						↓	
MASK WRITE-1	H	L	L	H	H	L	BL	↑	1, 2, 3, 5, 6, 7, 9
	L	BA0	BA1	BA2	V	C9	AP	↓	
RFU	H	L	L	H	H	H	V	↑	1, 2
	L	V						↓	
RFU	H	L	H	L	H	L	V	↓	1, 2
	L	V						↓	
RFU	H	L	H	L	H	H	V	↓	1, 2
	L	V						↓	
READ-1	H	L	H	L	L	L	BL	↑	1, 2, 3, 6, 7, 9
	L	BA0	BA1	BA2	V	C9	AP	↓	
CAS-2 (WRITE-2, MASKED WRITE-2, READ-2, MRR-2, MPC (except NOP)	H	L	H	L	L	H	C8	↑	1, 8, 9
	L	C2	C3	C4	C5	C6	C7	↓	
PRECHARGE (all/per bank)	H	L	L	L	L	H	AB	↑	1, 2, 3, 4
	L	BA0	BA1	BA2	V	V	V	↓	
MPC (TRAIN, NOP)	H	L	L	L	L	L	OP6	↑	1, 2, 13
	L	OP0	OP1	OP2	OP3	OP4	OP5	↓	
DESELECT	L	X						↑	1, 2

Notes:

1. All commands except for DESELECT are two clock cycles and are defined by the currentstate of CS and CA[5:0] at the rising edge of the clock. DESELECT command is one clockcycle and is not latched by the device.
2. V = H or L (a defined logic level); X = "Don't Care," in which case CS, CK_t, CK_c, andCA[5:0] can be floated.
3. Bank addresses BA[2:0] determine which bank is to be operated upon.
4. AB HIGH during PRECHARGE or REFRESH commands indicate the command must be appliedto all banks, and the bank addresses are "Don't Care."
5. MASK WRITE-1 command only supports BL16. For MASK WRITE-1 commands, CA5 mustbe driven LOW on the first rising clock cycle (R1).
6. AP HIGH during a WRITE-1, MASK WRITE-1, or READ-1 command indicates that an autoprecharge will occur to the bank the command is operating on. AP LOW indicates thatno auto precharge will occur and the bank will remain open upon completion of thecommand.
7. When enabled in the mode register, BL HIGH during a WRITE-1, MASK-WRITE-1, orREAD-1 command indicates the burst length should be set on-the-fly to BL = 32; BL LOWduring one of these commands indicates the burst length should be set on-the-fly to BL= 16. If on-the-fly burst length is not enabled in the mode register, this bit should bedriven to a valid level and is ignored by the device.
8. For CAS-2 commands (WRITE-2, MASK WRITE-2, READ-2, MRR-2, or MPC (only WRITEFIFO,READ-FIFO, and READ DQ CALIBRATION)), C[1:0] are not transmitted on the CA[5:0] bus and are assumed to be zero. Note that for CAS-2 WRITE-2 or CAS-2 MASKWRITE-2 command, C[3:2] must be driven LOW.
9. WRITE-1, MASK-WRITE-1, READ-1, MODE REGISTER READ-1, or MPC (only WRITE-FIFO,READ-FIFO, and READ DQ CALIBRATION) command must be immediately followed byCAS-2 command consecutively without any other command in between. WRITE-1, MASKWRITE-1, READ-1, MRR-1, or MPC (only WRITE-FIFO, READ-FIFO, and READ DQ CALIBRATION)command must be issued first before issuing CAS-2 command. MPC (only STARTand STOP DQS OSCILLATOR, ZQCAL START and LATCH) commands do not require CAS-2command; they require two additional DES or NOP commands consecutively before issuingany other commands.
10. The ACTIVATE-1 command must be followed by the ACTIVATE-2 command consecutivelywithout any other command between them. The ACTIVATE-1 command must be issuedprior to the ACTIVATE-2 command. When the ACTIVATE-1 command is issued, the ACTIVATE-2 command must be issued before issuing another ACTIVATE-1 command.
11. The MRW-1 command must be followed by the MRW-2 command consecutively withoutany other command between them. The MRW-1 command must be issued prior to theMRW-2 command.
12. The MRR-1 command must be followed by the CAS-2 command consecutively withoutany other commands between them. The MRR-1 command must be issued prior to theCAS-2 command.
13. The MPC command for READ or WRITE TRAINING operations must be followed by theCAS-2 command consecutively without any other commands between them. The MPCcommand must be issued prior to the CAS-2 command.

4.10 ACTIVATE Command

The ACTIVATE command must be executed before a READ or WRITE command can beissued. The ACTIVATE command is issued in two parts: The bank and upper-row addressesare entered with activate-1 and the lower-row addresses are entered with ACTIVATE-2. ACTIVATE-1 and ACTIVATE-2 are executed by strobing CS HIGH while settingCA[5:0] at valid levels (see Command table) at the rising edge of CK.

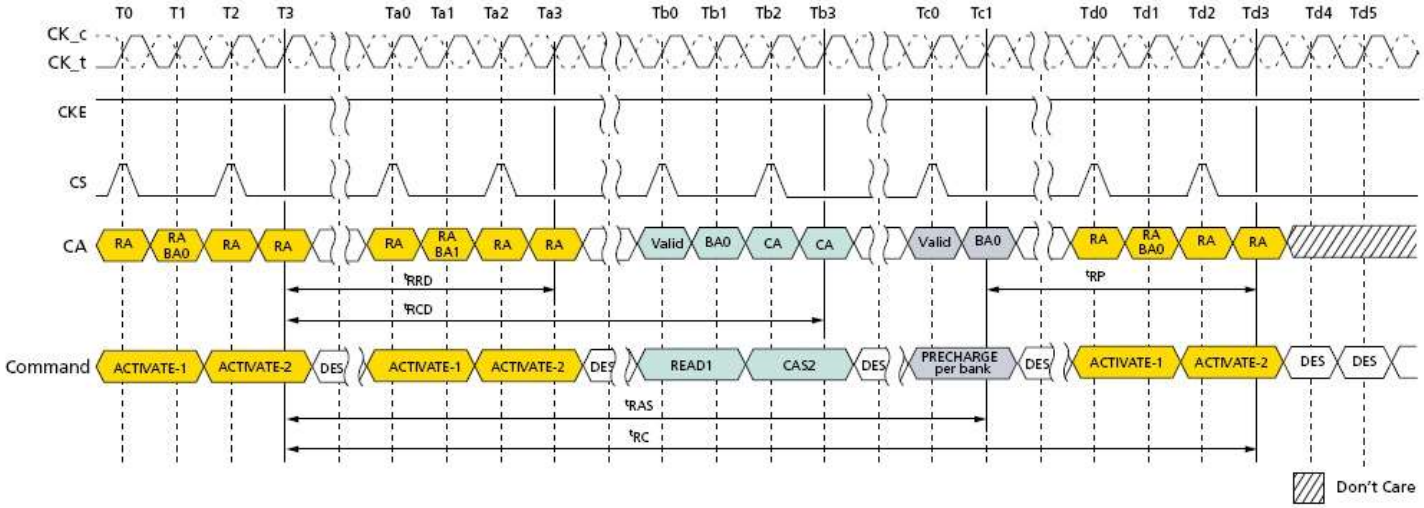
The bank addresses (BA[2:0]) are used to select the desired bank. The row addresses(R[15:0]) are used to determine which row to activate in the selected bank. The ACTIVATE-2 command must be applied before any READ or WRITE operation can be executed.The device can accept a READ or WRITE command at time ^{t}RCD after the ACTIVATE-2 command is sent. After a bank has been activated, it must be precharged toclose the active row before another ACTIVATE-2 command can be applied to the samebank. The bank active and precharge times are defined as ^{t}RAS and ^{t}RP, respectively.

The minimum time interval between successive ACTIVATE-2 commands to the samebank is determined by the row cycle time of the device (^{t}RC). The minimum time intervalbetween ACTIVATE-2 commands to different banks is ^{t}RRD.

Certain restrictions must be observed for bank ACTIVATE and REFpb operations.

- Four-activate window (^{t}FAW): No more than 4 banks may be activated (or refreshed,in the case of REFpb) per channel in a rolling ^{t}FAW window. Convert to clocks by dividing^{t}FAW[ns] by ^{t}CK[ns] and rounding up to the next integer value. As an exampleof the rolling window, if RU[(^{t}FAW/^{t}CK)] is 64 clocks, and an ACTIVATE command is issued on clock N, no more than three additional ACTIVATE commands may be issuedbetween clock N + 1 and N + 63. REFpb also counts as bank activation for thepurposes of ^{t}FAW.
- 8-bank per channel, precharge all banks (AB) allowance: ^{t}RP for a PRECHARGE ALLBANKS command for an 8-bank device must equal ^{t}RPab, which is greater than^{t}RPpb.

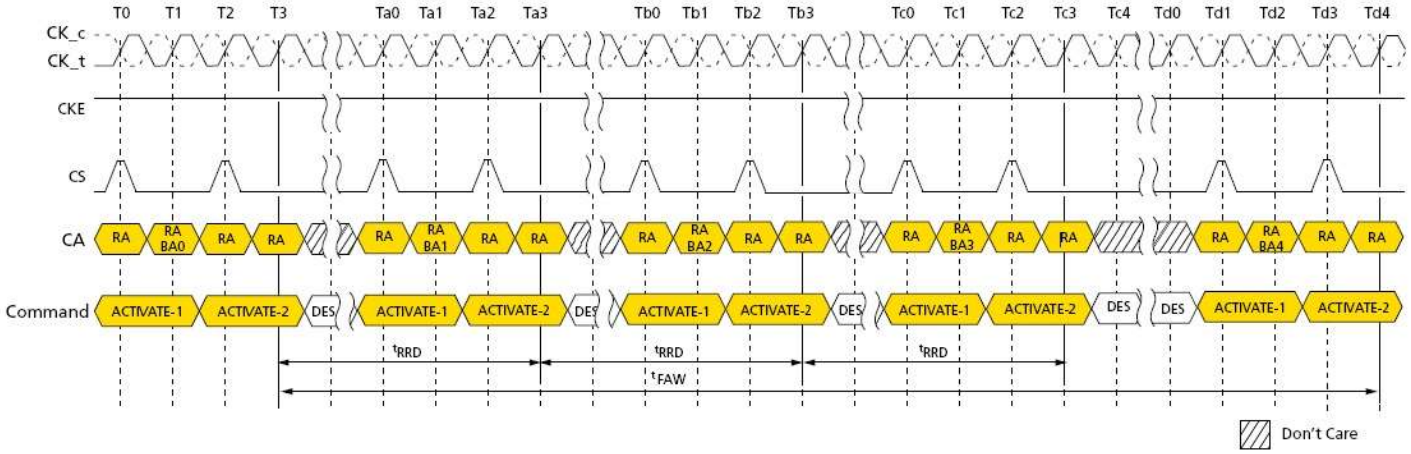
Figure 4-2: ACTIVATE Command



Note:

1. A PRECHARGE command uses ^{t}RPab timing for all-bank precharge and ^{t}RPpb timing forsingle-bank precharge. In this figure, ^{t}RP is used to denote either all-bank precharge ora single-bank precharge. ^{t}CCD = MIN, 1.5nCK postamble, 533 MHz < clock frequency ≤800 MHz, ODT worst timing case.

Figure 4-3: ᵗFAW Timing



Note:

1. REFpb may be substituted for one of the ACTIVATE commands for the purposes of ᵗFAW.

4.11 Read and Write Access Modes

After a bank has been activated, a READ or WRITE command can be executed. This isaccomplished by asserting CKE asynchronously, with CS and CA[5:0] set to the properstate (see Command Truth Table) on the rising edge of CK.

The device provides a fast column access operation. A single READ or WRITE commandwill initiate a burst READ or WRITE operation, where data is transferred to/from the deviceon successive clock cycles. Burst interrupts are not allowed; however, the optimalburst length may be set on-the-fly (see Command Truth Table).

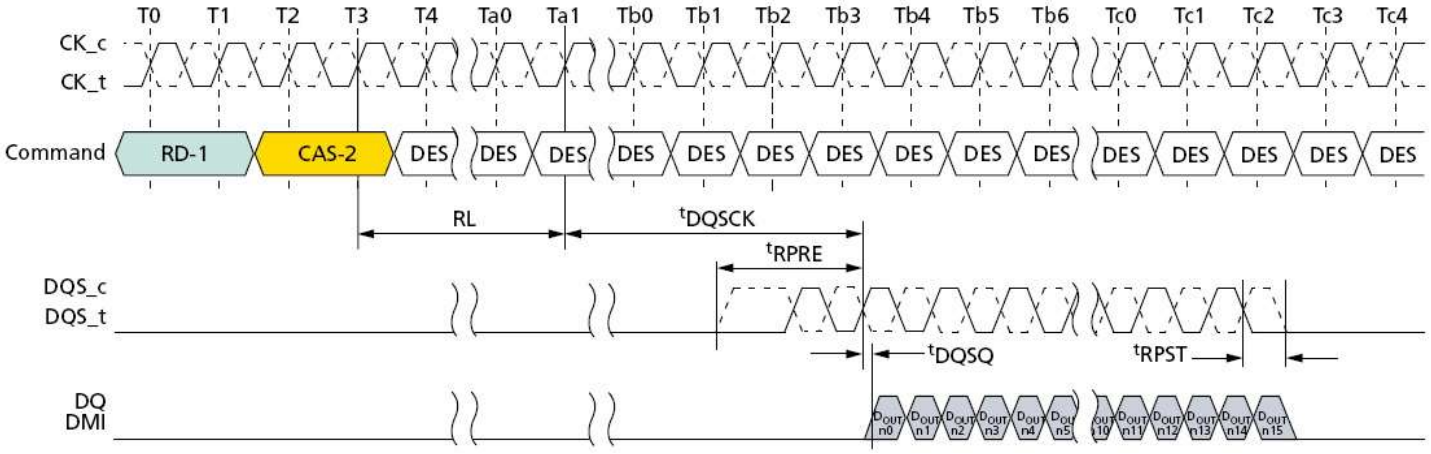
4.12 Preamble and Postamble

The DQS strobe for the device requires a preamble prior to the first latching edge (therising edge of DQS_t with data valid), and it requires a postamble after the last latchingedge. The preamble and postamble options are set via MODE REGISTER WRITE commands.

The read preamble is two ^{t}CK in length and is either static or has one clock toggle beforethe first latching edge. The read preamble option is enabled via MRW to MR1 OP[3] (0 =Static; 1 = Toggle).

The read postamble has a programmable option to extend the postamble by 1nCK(^{t}RPSTE). The extended postamble option is enabled via MRW to MR1 OP[7] (0 =0.5nCK; 1 = 1.5nCK).

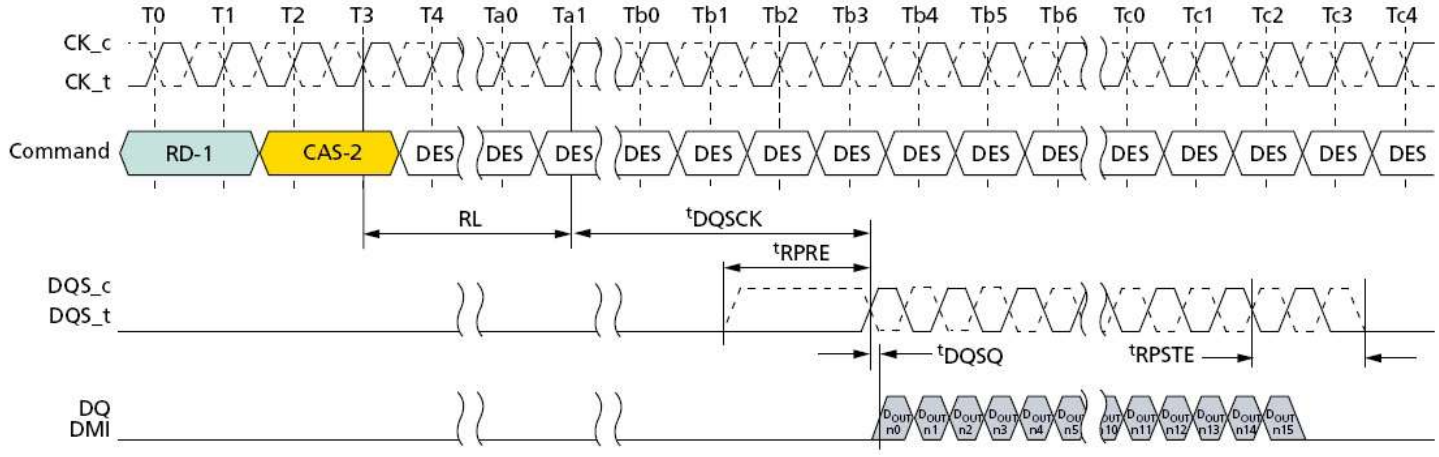
Figure 4-4: DQS Read Preamble and Postamble – Toggling Preamble and 0.5nCK Postamble



Notes:

1. BL = 16, Preamble = Toggling, Postamble = 0.5nCK.
2. DQS and DQ terminated V_{SSQ}.
3. DQS_t/DQS_c is "Don't Care" prior to the start of ^{t}RPRE. No transition of DQS is implied,as DQS_t/DQS_c can be HIGH,LOW, or High-Z prior to ^{t}RPRE.

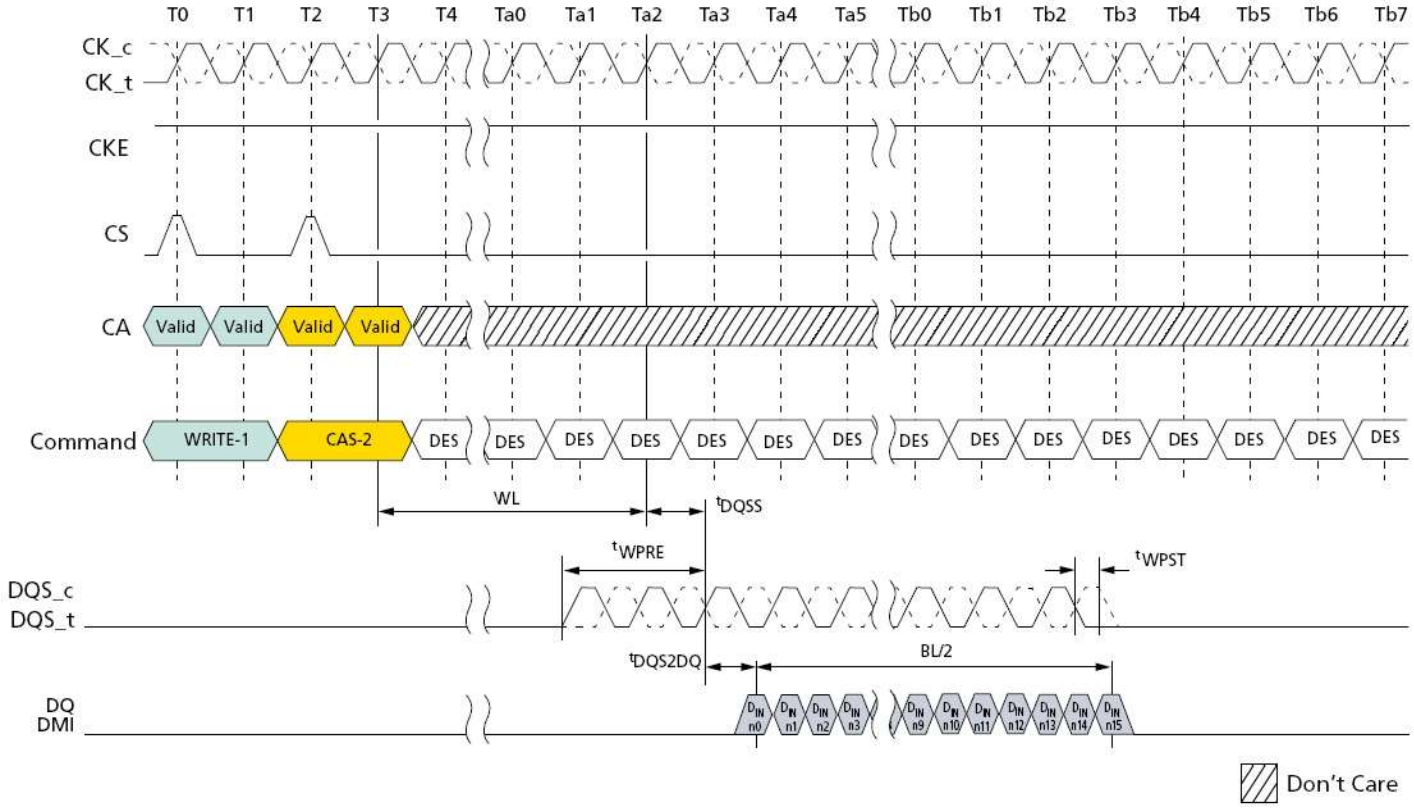
Figure 4-5: DQS Read Preamble and Postamble – Static Preamble and 1.5nCK Postamble



Notes:

1. BL = 16, Preamble = Static, Postamble = 1.5nCK (extended).
2. DQS and DQ terminated V_{SSQ}.
3. DQS_t/DQS_c is "Don' t Care" prior to the start of ^{t}RPRE. No transition of DQS is implied,as DQS_^{t}/DQS_c can be HIGH, LOW, or High-Z prior to ^{t}RPRE.

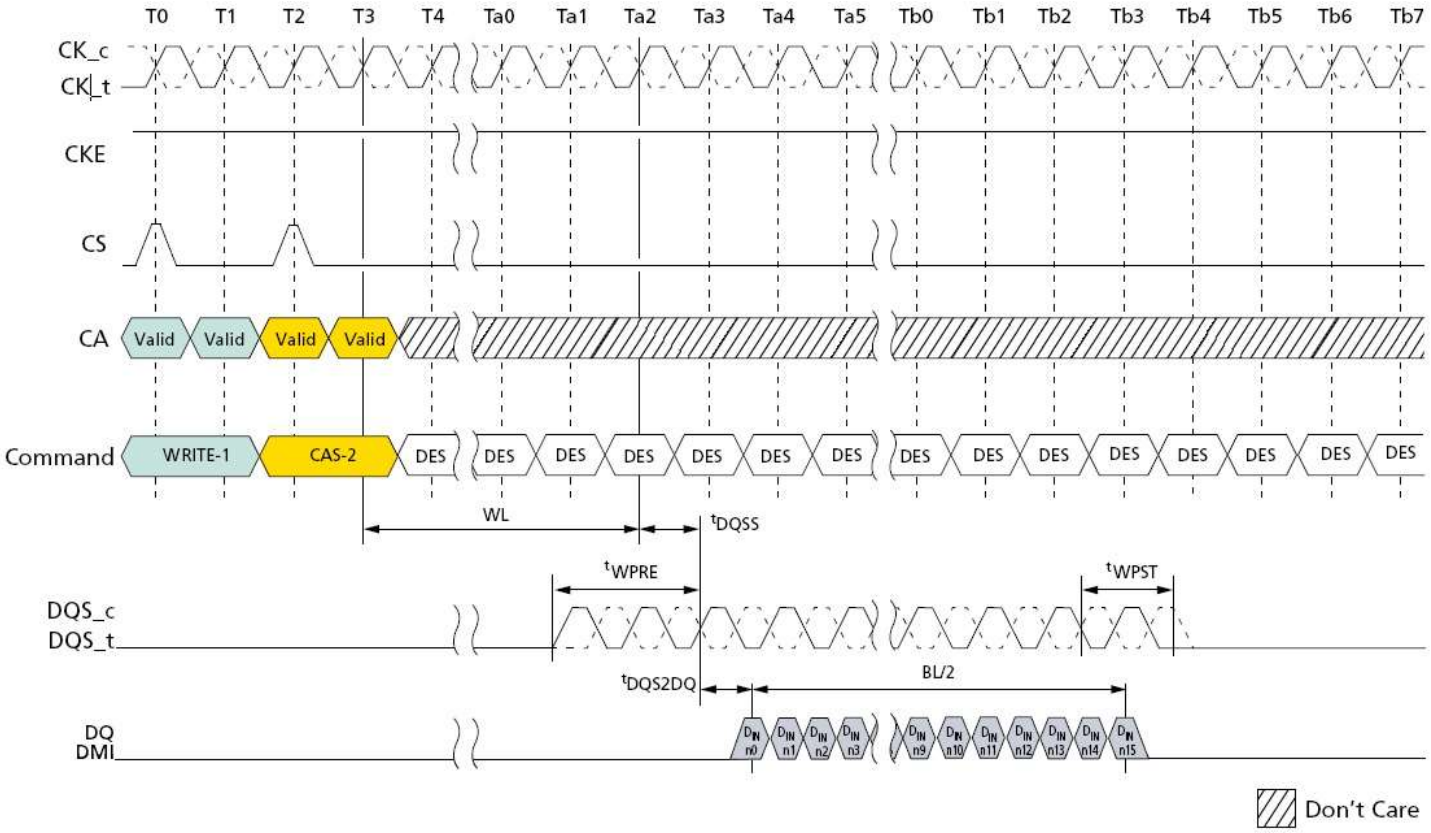
Figure 4-6: DQS Write Preamble and Postamble – 0.5nCK Postamble



Notes:

1. BL = 16, Postamble = 0.5nCK.
2. DQS and DQ terminated V_{SSQ}.
3. DQS_t/DQS_c is "Don't Care" prior to the start of ^{t}WPRE. No transition of DQS is implied,as DQS_ t/DQS_c can be HIGH,LOW, or High-Z prior to ^{t}WPRE.

Figure 4-7: DQS Write Preamble and Postamble – 1.5nCK Postamble



Notes:

1. BL = 16, Postamble = 1.5nCK.
2. DQS and DQ terminated V_{SSQ}.
3. DQS_t/DQS_c is "Don′ t Care" prior to the start of ^{t}WPRE. No transition of DQS is implied,as DQS_t/DQS_c can be HIGH,LOW, or High-Z prior to ^{t}WPRE.

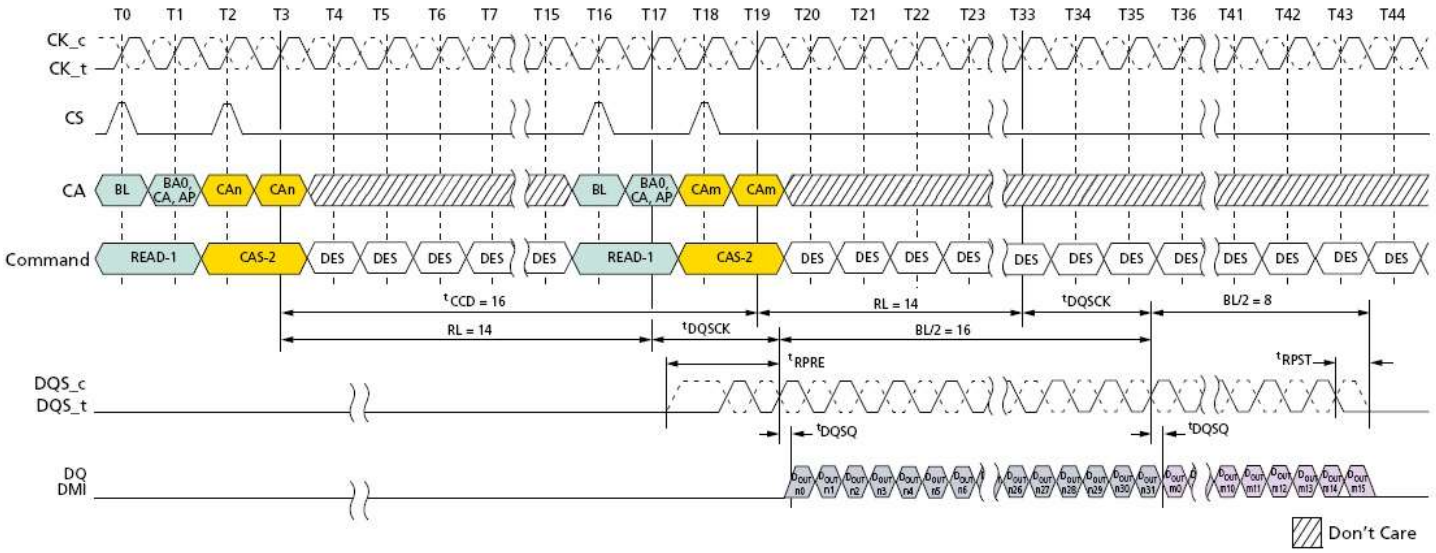
4.13 Burst READ Operation

A burst READ command is initiated with CKE, CS, and CA[5:0] asserted to the properstate on the rising edge of CK, as defined by the Command Truth Table. The commandaddress bus inputs determine the starting column address for the burst. The two loworderaddress bits are not transmitted on the CA bus and are implied to be 0; therefore, the starting burst address is always a multiple of four (that is, 0x0, 0x4, 0x8, 0xC).

The READ latency (RL) is defined from the last rising edge of the clock that completes aREAD command (for example, the second rising edge of the CAS-2 command) to therising edge of the clock from which the ^{t}DQSCK delay is measured. The first valid data isavailable RL ×^{t}CK + ^{t}DQSCK + ^{t}DQSQ after the rising edge of clock that completes aREAD command.

The data strobe output is driven ^{t}RPRE before the first valid rising strobe edge. The firstdata bit of the burst is synchronized with the first valid (post-preamble) rising edge ofthe data strobe. Each subsequent data-out appears on each DQ pin, edge-aligned withthe data strobe. At the end of a burst, the DQS signals are driven for another half cyclepostamble, or for a 1.5-cycle postamble if the programmable postamble bit is set in themode register. The RL is programmed in the mode registers. Pin timings for the datastrobe are measured relative to the cross-point of DQS_t and DQS_c.

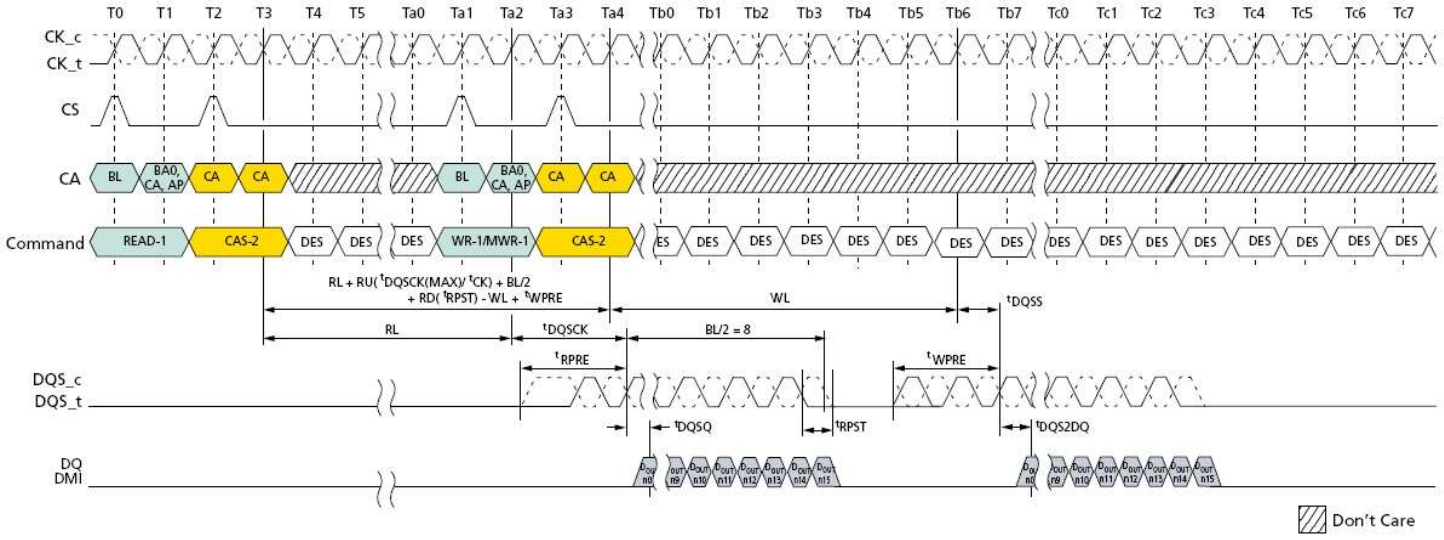
Figure 4-8: Burst Read Timing



Notes:

1. BL = 32 for column n, BL = 16 for column m, RL = 14, Preamble = Toggle, Postamble =0.5nCK, DQ/DQS: V_{SSQ} termination.
2. D_{OUT} n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid atthese times.

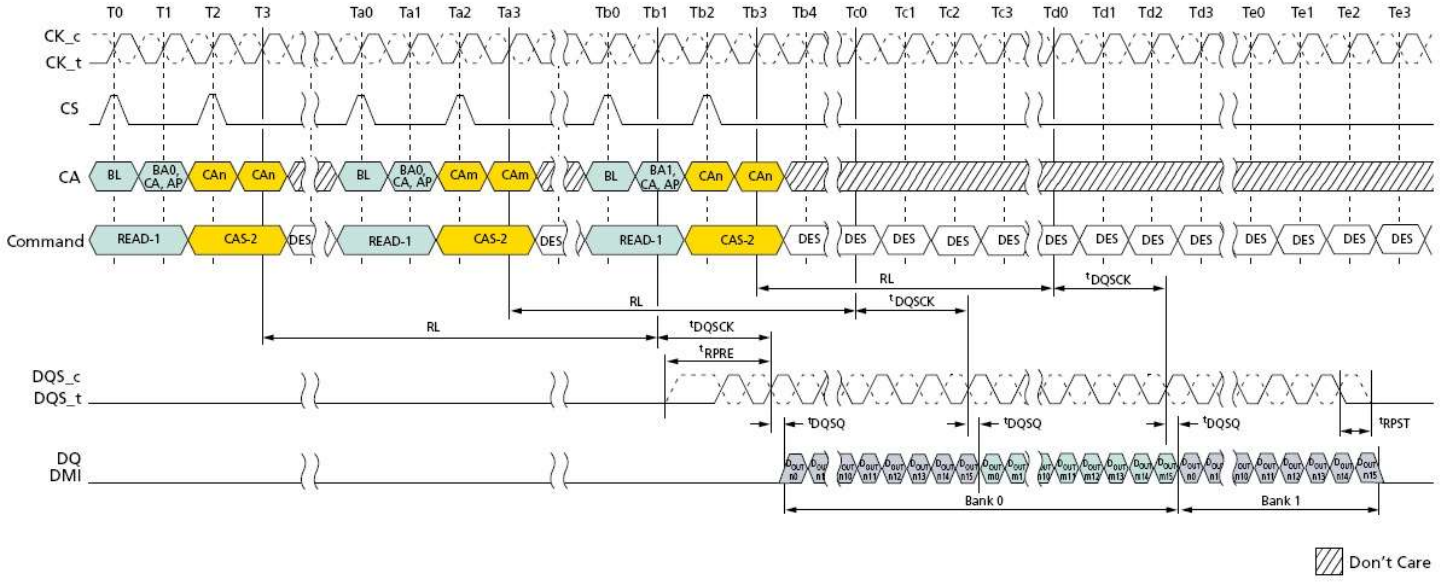
Figure 4-9: Burst Read Followed by Burst Write or Burst Mask Write



Notes:

1. BL=16, Read preamble = Toggle, Read postamble = 0.5nCK, Write preamble = 2nCK,Write postamble = 0.5nCKDQ/DQS: V_{SSQ} termination.
2. D_{OUT} n = data-out from column n and D_{IN} n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid atthese times.

Figure 4-10: Seamless Burst Read

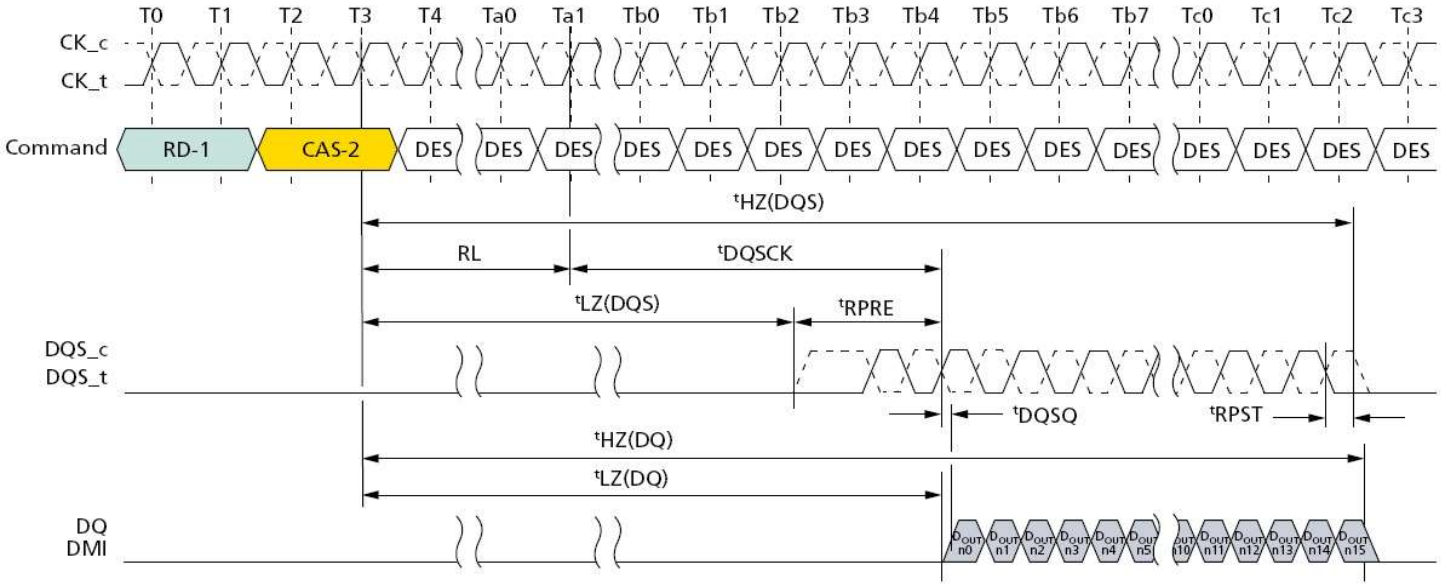


Notes:

1. BL = 16, ^{t}CCD = 8, Preamble = Toggle, Postamble = 0.5nCK, DQ/DQS: V_{SSQ} termination.
2. D_{OUT} n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid atthese times.

Read Timing

Figure 4-11: Read Timing



Notes:

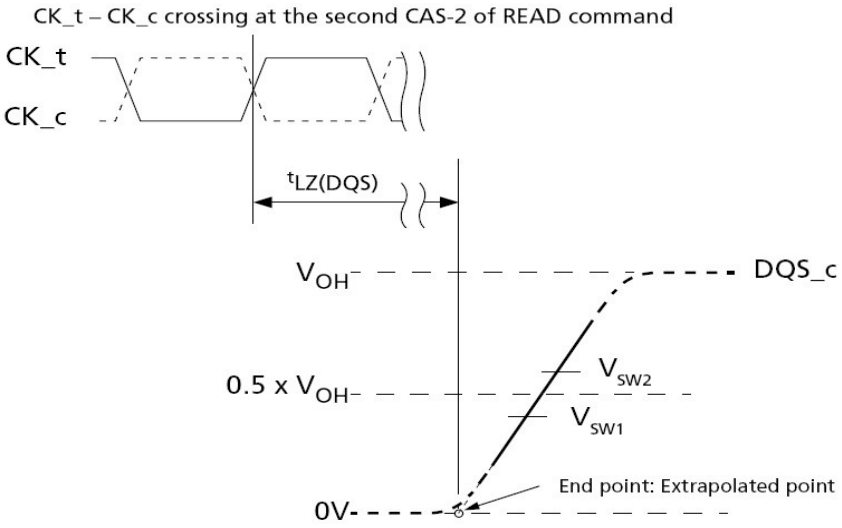
1. BL = 16, Preamble = Toggling, Postamble = 0.5nCK.
2. DQS, DQ, and DMI terminated V_{SSQ}.
3. Output driver does not turn on before an endpoint of ^{t}LZ(DQS) and ^{t}LZ(DQ).
4. Output driver does not turn off before an endpoint of ^{t}HZ(DQS) and ^{t}HZ(DQ).

^{t}LZ(DQS), ^{t}LZ(DQ), ^{t}HZ(DQS), ^{t}HZ(DQ) Calculation

^{t}HZ and ^{t}LZ transitions occur in the same time window as valid data transitions. Theseparameters are referenced to a specific voltage level that specifies when the device outputis no longer driving ^{t}HZ(DQS) and ^{t}HZ(DQ), or begins driving ^{t}LZ(DQS) and^{t}LZ(DQ). This section shows a method to calculate the point when the device is no longerdriving ^{t}HZ(DQS) and ^{t}HZ(DQ), or begins driving ^{t}LZ(DQS) and ^{t}LZ(DQ), by measuringthe signal at two different voltages. The actual voltage measurement points arenot critical as long as the calculation is consistent. The parameters ^{t}LZ(DQS), ^{t}LZ(DQ),^{t}HZ(DQS), and ^{t}HZ(DQ) are defined as single ended.

tLZ(DQS) and tHZ(DQS) Calculation for ATE (Automatic Test Equipment)

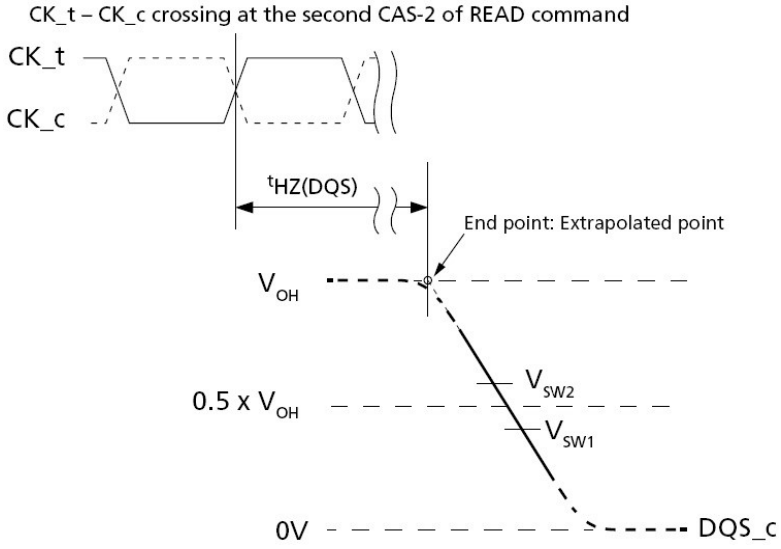
Figure 4-12: tLZ(DQS) Method for Calculating Transitions and Endpoint



Notes:

1. Conditions for calibration: Pull down driver R_{ON} = 40 ohm, V_{OH} = V_{DDQ} x 0.5.
2. Termination condition for DQS_t and DQS_C = 50 ohm to V_{SSQ}.
3. The V_{OH} level depends on MR22 OP[2:0] and MR3 OP[0] settings as well as device tolerances.Use the actual V_{OH} value for tHZ and tLZ measurements.

Figure 4-13: tHZ(DQS) Method for Calculating Transitions and Endpoint



Notes:

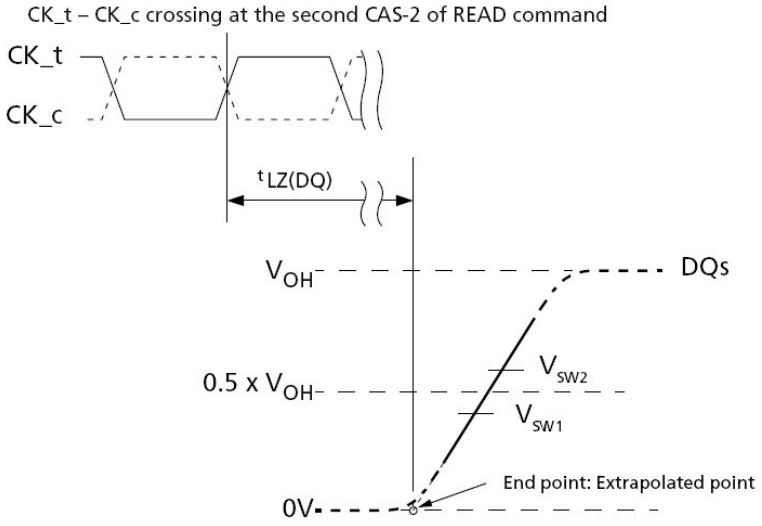
1. Conditions for calibration: Pull down driver R_{ON} = 40 ohm, V_{OH} = V_{DDQ} x 0.5.
2. Termination condition for DQS_t and DQS_C = 50 ohm to V_{SSQ}.
3. The VOH level depends on MR22 OP[2:0] and MR3 OP[0] settings as well as device tolerances.Use the actual VOH value for tHZ and tLZ measurements.

Table 4-85: Reference Voltage for ^{t}LZ(DQS), ^{t}HZ(DQS) Timing Measurements

Measured Parameter	Measured Parameter Symbol	Vsw1	Vsw2	Unit
DQS_c Low-Z time from CK_t, CK_c	^{t}LZ(DQS)	0.4 × V_{OH}	0.6 × V_{OH}	V
DQS_c High-Z time from CK_t, CK_c	^{t}HZ(DQS)	0.4 × V_{OH}	0.6 × V_{OH}	

^{t}LZ(DQ) and ^{t}HZ(DQ) Calculation for ATE (Automatic Test Equipment)

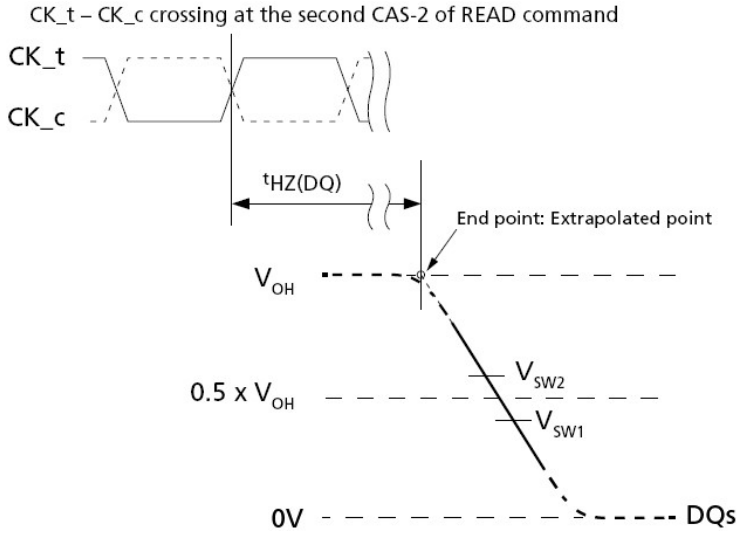
Figure 4-14: ^{t}LZ(DQ) Method for Calculating Transitions and Endpoint



Notes:

1. Conditions for calibration: Pull down driver R_{ON} = 40 ohm, V_{OH} = V_{DDQ} x 0.5.
2. Termination condition for DQ and DMI = 50 ohm to V_{SSQ}.
3. The V_{OH} level depends on MR22 OP[2:0] and MR3 OP[0] settings as well as device tolerances.Use the actual V_{OH} value for ^{t}HZ and ^{t}LZ measurements.

Figure 4-15: ^{t}HZ(DQ) Method for Calculating Transitions and Endpoint



Notes:

1. Conditions for calibration: Pull down driver R_{ON} = 40 ohm, V_{OH} = V_{DDQ} x 0.5.
2. Termination condition for DQ and DMI = 50 ohm to V_{SSQ}.
3. The V_{OH} level depends on MR22 OP[2:0] and MR3 OP[0] settings as well as device tolerances.Use the actual V_{OH} value for ^{t}HZ and ^{t}LZ measurements.

Table 4-86: Reference Voltage for ^{t}LZ(DQ), ^{t}HZ(DQ) Timing Measurements

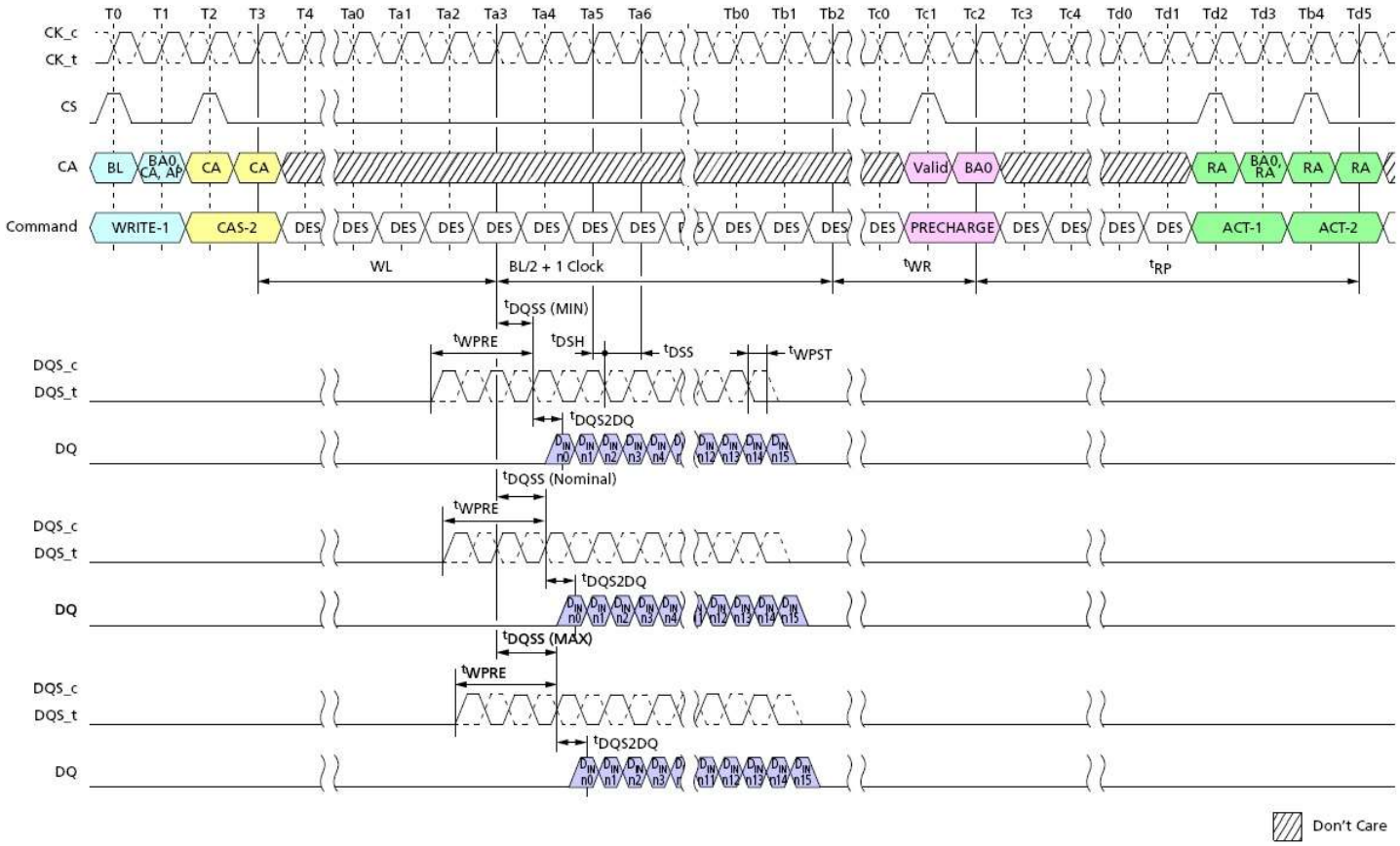
Measured Parameter	Measured Parameter Symbol	Vsw1	Vsw2	Unit
DQ Low-Z time from CK_t, CK_c	^{t}LZ(DQ)	0.4 × V_{OH}	0.6 × V_{OH}	V
DQ High-Z time from CK_t, CK_c	^{t}HZ(DQ)	0.4 × V_{OH}	0.6 × V_{OH}	

4.14 Burst WRITE Operation

A burst WRITE command is initiated with CKE, CS, and CA[5:0] asserted to the properstate at the rising edge of CK, as defined by the Command Truth Table. Column addressesC[3:2] should be driven LOW for burst WRITE commands, and column addressesC[1:0] are not transmitted on the CA bus and are assumed to be zero so that the startingcolumn burst address is always aligned with a 32-byte boundary. The WRITE latency(WL) is defined from the last rising edge of the clock that completes a WRITE command(for example, the second rising edge of the CAS-2 command) to the rising edge of theclock from which ^{t}DQSS is measured. The first valid latching edge of DQS must be drivenWL ×^{t} CK + ^{t}DQSS after the rising edge of clock that completes a WRITE command.

The device uses an unmatched DQS DQ path for lower power, so the DQS strobe mustarrive at the SDRAM ball prior to the DQ signal by ^{t}DQS2DQ. The DQS strobe outputmust be driven ^{t}WPRE before the first valid rising strobe edge. The ^{t}WPRE preamble isrequired to be 2 ×^{t}CK at any speed ranges. The DQS strobe must be trained to arrive atthe DQ pad latch center-aligned with the DQ data. The DQ data must be held forTdiVW, and the DQS must be periodically trained to stay roughly centered in the TdiVW.Burst data is captured by the SDRAM on successive edges of DQS until the 16- or 32-bitdata burst is complete. The DQS strobe must remain active (toggling) for ^{t}WPST (writepostamble) after the completion of the burst WRITE. After a burst WRITE operation,^{t}WR must be satisfied before a PRECHARGE command to the same bank can be issued.Signal input timings are measured relative to the cross point of DQS_t and DQS_c.

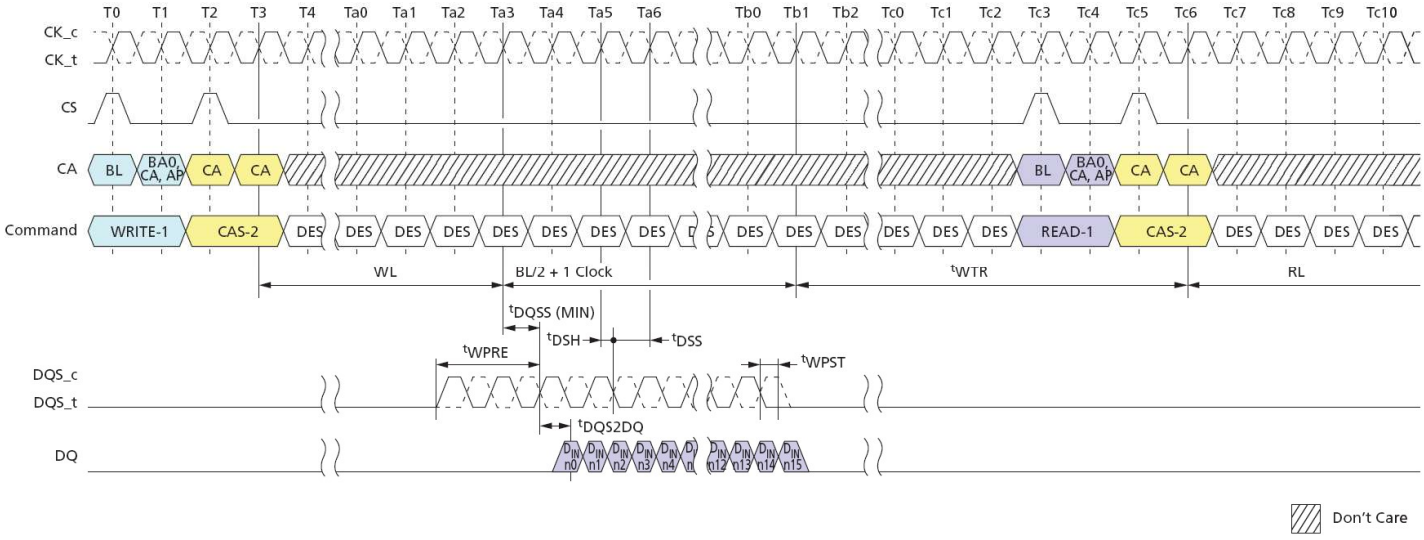
Figure 4-16: Burst WRITE Operation



Notes:

1. BL = 16, Write postamble = 0.5nCK, DQ/DQS: V_{SSQ} termination.
2. D_{IN} n = data-in to column n.
3. ^{t}WR starts at the rising edge of CK after the last latching edge of DQS.
4. DES commands are shown for ease of illustration; other commands may be valid atthese times.

Figure 4-17: Burst Write Followed by Burst Read

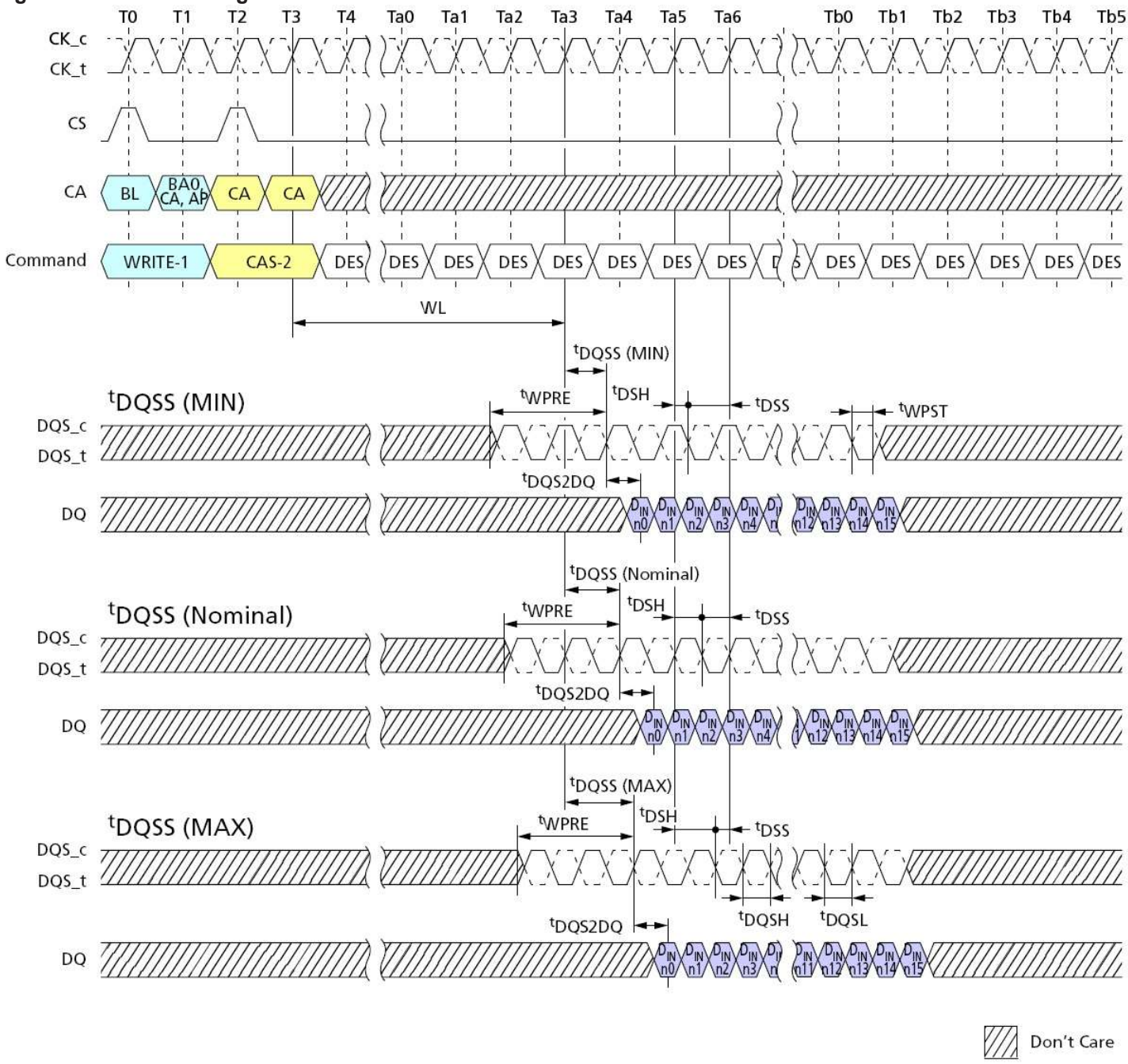


Notes:

1. BL = 16, Write postamble = 0.5nCK, DQ/DQS: V_{SSQ} termination.
2. D_{IN} n = data-in to column n.
3. The minimum number of clock cycles from the burst WRITE command to the burst READcommand for any bank is [WL + 1 + BL/2 + RU(t_{WTR}/t_{CK})].
4. t_{WTR} starts at the rising edge of CK after the last latching edge of DQS.
5. DES commands are shown for ease of illustration; other commands may be valid atthese times.

Write Timing

Figure 4-18: Write Timing

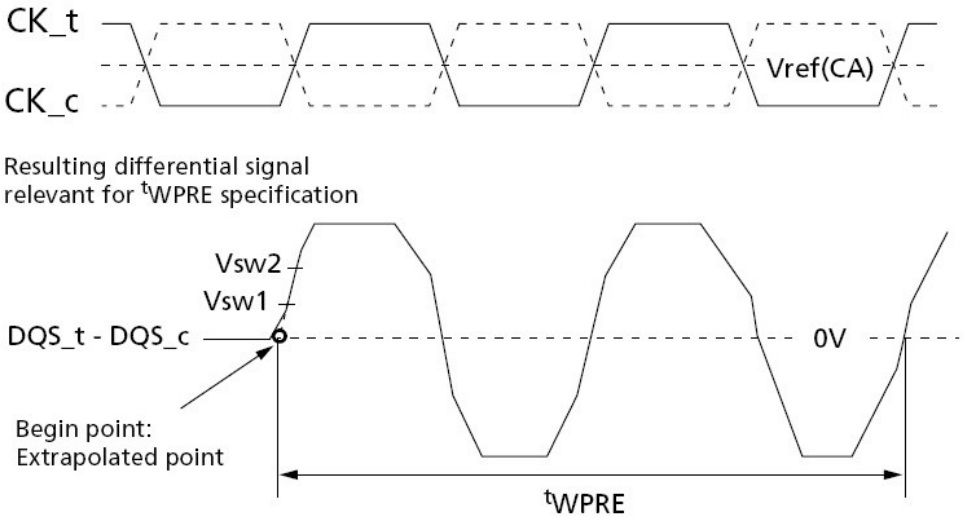


Notes:

1. BL = 16, Write postamble = 0.5nCK.
2. D_{IN} n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid atthese times.

tWPRE Calculation for ATE (Automatic Test Equipment)

Figure 4-19: Method for Calculating tWPRE Transitions and Endpoints



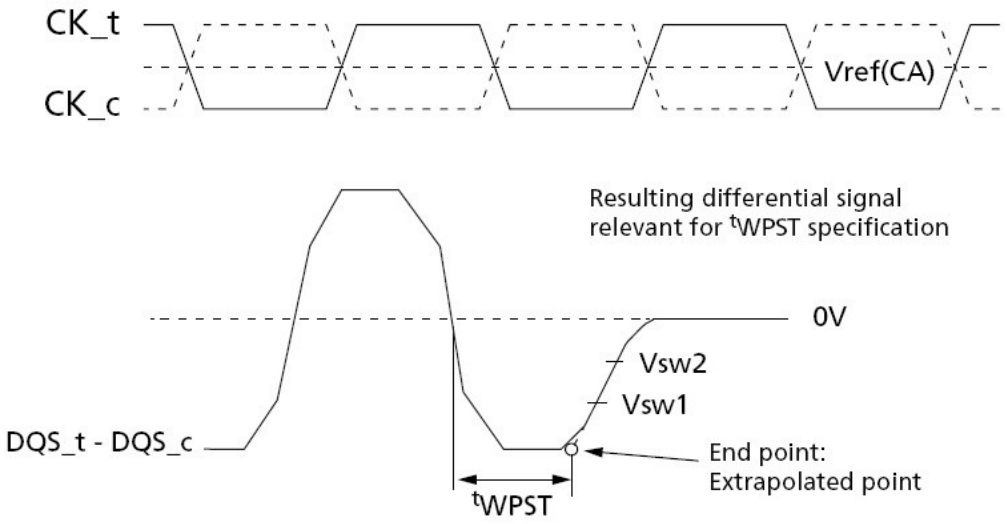
Note:
1. Termination condition for DQS_t, DQS_c, DQ, and DMI = 50 ohm to V_{SSQ}.

Table 4-87: Method for Calculating tWPRE Transitions and Endpoints

Measured Parameter	Measured Parameter Symbol	Vsw1	Vsw2	Unit
DQS_t, DQS_c differential write preamble	tWPRE	V_{IHL_AC} × 0.3	V_{IHL_AC} × 0.7	V

tWPST Calculation for ATE (Automatic Test Equipment)

Figure 4-20: Method for Calculating tWPST Transitions and Endpoints



Notes:

1. Termination condition for DQS_t, DQS_c, DQ, and DMI = 50 ohm to V_{SSQ}.
2. Write postamble: 0.5tCK
3. The method for calculating differential pulse widths for 1.5tCK postamble is same as0.5tCK postamble.

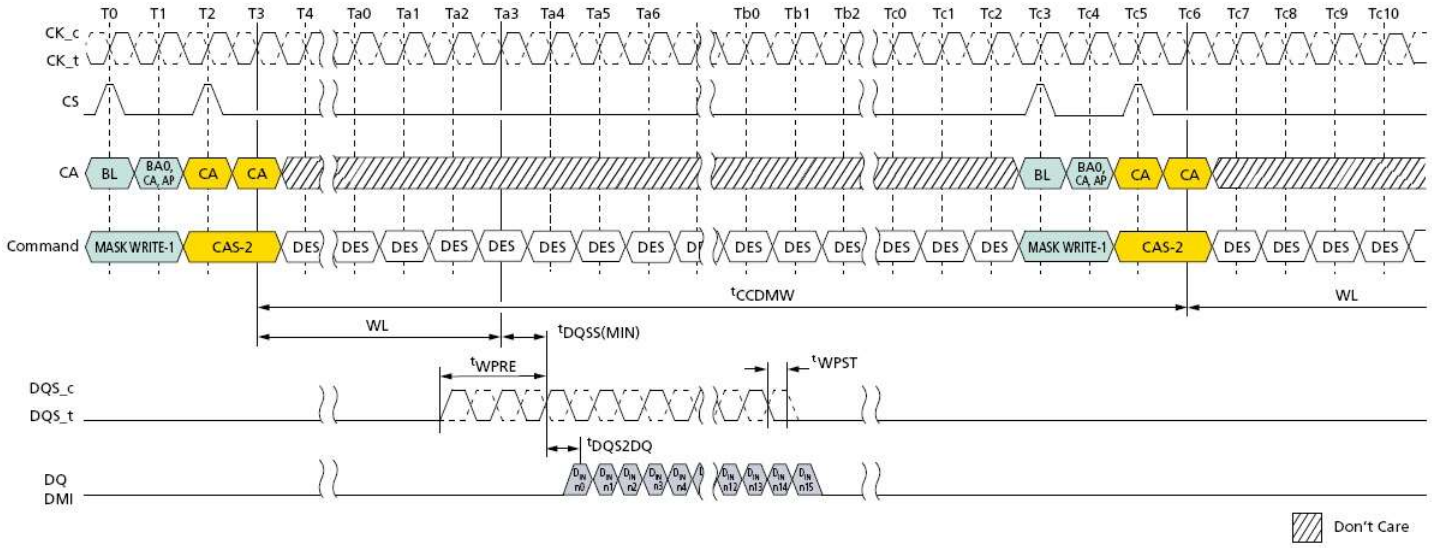
Table 4-88: Reference Voltage for tWPST Timing Measurements

Measured Parameter	Measured Parameter Symbol	Vsw1	Vsw2	Unit
DQS_t, DQS_c differential write postamble	tWPST	$-(V_{IHL\_AC} \times 0.7)$	$-(V_{IHL\_AC} \times 0.3)$	V

4.15 MASK WRITE Operation

The device requires that WRITE operations that include a byte mask anywhere in theburst sequence must use the MASK WRITE command. This allows the device to implementefficient data protection schemes based on larger data blocks. The MASKWRITE-1 command is used to begin the operation, followed by a CAS-2 command. AMASKED WRITE command to the same bank cannot be issued until ^{t}CCDMW later, toallow the device to finish the internal READ-MODIFY-WRITE operation. One datamask-invert (DMI) pin is provided per byte lane, and the data-mask-invert timingsmatch data bit (DQ) timing. See Data Mask Invert for more information on the use ofthe DMI signal.

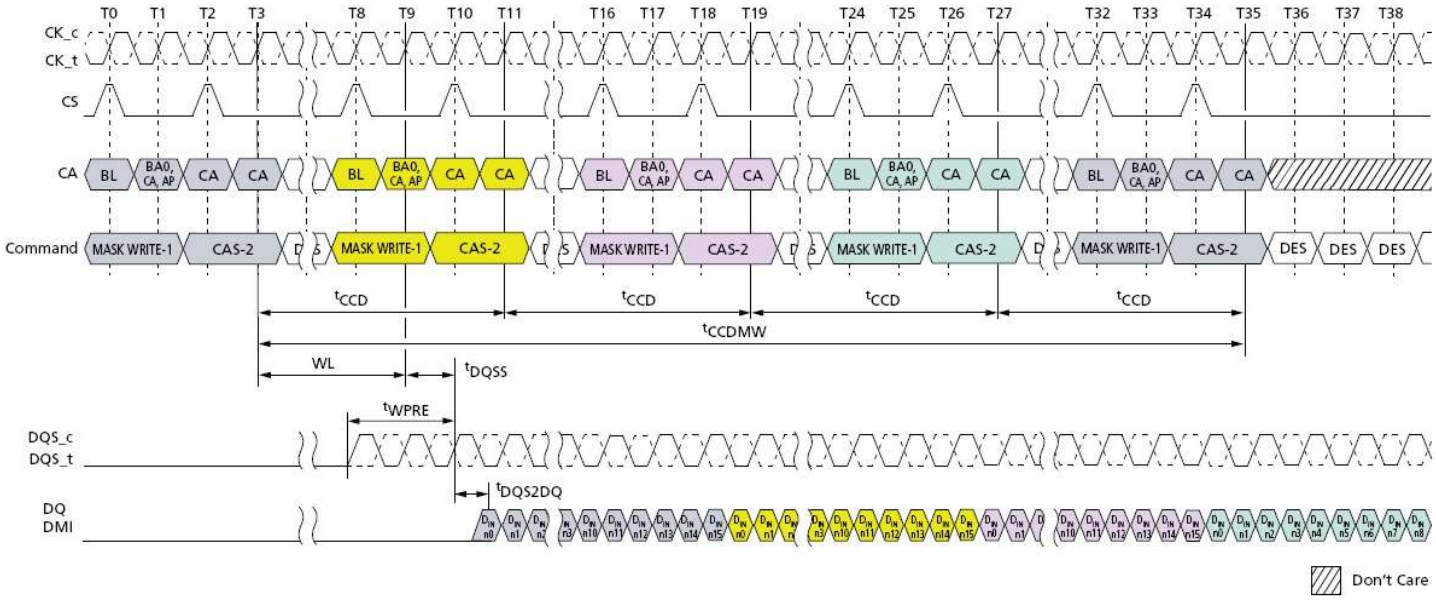
Figure 4-21: MASK WRITE Command – Same Bank



Notes:

1. BL = 16, Write postamble = 0.5nCK, DQ/DQS: V_{SSQ} termination.
2. D_{IN} n = data-in to column n.
3. Mask-write supports only BL16 operations. For BL32 configuration, the system needs toinsert only 16-bit wide data for MASKED WRITE operation.
4. DES commands are shown for ease of illustration; other commands may be valid atthese time.

Figure 4-22: MASK WRITE Command – Different Bank



Notes:
1. BL = 16, DQ/DQS/DMI: V_{SSQ} termination.
2. D_{IN} n = data-in to column n.
3. Mask-write supports only BL16 operations. For BL32 configuration, the system needs toinsert only 16-bit wide data for MASKED WRITE operation.
4. DES commands are shown for ease of illustration; other commands may be valid atthese time.

Mask Write Timing Constraints for BL16

Table 4-89: Same Bank (ODT Disabled)

Next CMD / Current CMD	ACTIVE	READ (BL = 16 or 32)	WRITE (BL = 16 or 32)	MASK WRITE	PRECHARGE
ACTIVE	Illegal	RU(tRCD/tCK)	RU(tRCD/tCK)	RU(tRCD/tCK)	RU(tRAS/tCK)
READ (with BL = 16)	Illegal	8[1]	RL + RU(tDQSCK(MAX)/tCK) + BL/2 - WL + tWPRE + RD(tRPST)	RL + RU(tDQSCK(MAX)/tCK) + BL/2 - WL + tWPRE + RD(tRPST)	BL/2 + MAX{(8,RU(tRTP/tCK)} - 8
READ (with BL = 32)	Illegal	16[2]	RL + RU(tDQSCK(MAX)/tCK) + BL/2 - WL + tWPRE + RD(tRPST)	RL + RU(tDQSCK(MAX)/tCK) + BL/2 - WL + tWPRE + RD(tRPST)	BL/2 + MAX{(8,RU(tRTP/tCK)} - 8
WRITE (with BL = 16)	Illegal	WL + 1+ BL/2 + RU(tWTR/tCK)	8[1]	tCCDMW[3]	WL + 1 + BL/2 + RU(tWR/tCK)
WRITE (with BL = 32)	Illegal	WL + 1+ BL/2 + RU(tWTR/tCK)	16[2]	tCCDMW + 8[4]	WL + 1 + BL/2 + RU(tWR/tCK)
MASK WRITE	Illegal	WL + 1+ BL/2 + RU(tWTR/tCK)	tCCD	tCCDMW[3]	WL + 1 + BL/2 + RU(tWR/tCK)
PRECHARGE	RU(tRP/tCK), RU(tRPab/tCK)	Illegal	Illegal	Illegal	4

Notes:
1. In the case of BL = 16, tCCD is 8 ×tCK.
2. In the case of BL = 32, tCCD is 16 ×tCK.
3. tCCDMW = 32 ×tCK (4 ×tCCD at BL = 16).
4. WRITE with BL = 32 operation is 8 ×tCK longer than BL = 16.

Table 4-90: Different Bank (ODT Disabled)

Next CMD / Current CMD	ACTIVE	READ (BL = 16 or 32)	WRITE (BL = 16 or 32)	MASK WRITE	PRECHARGE
ACTIVE	RU(tRRD/tCK)	4	4	4	2[2]
READ (with BL = 16)	4	8[1]	RL + RU(tDQSCK(MAX)/ tCK) + BL/2 - WL + tWPRE + RD(tRPST)	RL + RU(tDQSCK(MAX)/ tCK) + BL/2 - WL + tWPRE + RD(tRPST)	2[2]
READ (with BL = 32)	4	16[2]	RL + RU(tDQSCK(MAX)/ tCK) + BL/2 - WL + tWPRE + RD(tRPST)	RL + RU(tDQSCK(MAX)/ tCK) + BL/2 - WL + tWPRE + RD(tRPST)	2[2]
WRITE (with BL = 16)	4	WL + 1+ BL/2 + RU(tWTR/tCK)	8[1]	8[1]	2[2]
WRITE (with BL = 32)	4	WL + 1+ BL/2 + RU(tWTR/tCK)	16[2]	16[2]	2[2]
MASK WRITE	4	WL + 1+ BL/2 + RU(tWTR/tCK)	8[1]	8[1]	2[2]
PRECHARGE	4	4	4	4	4

Notes:
1. In the case of BL = 16, tCCD is 8 ×tCK
2. In the case of BL = 32, tCCD is 16 ×tCK

Table 4-91: Same Bank (ODT Enabled)

Next CMD / Current CMD	ACTIVE	READ (BL = 16 or 32)	WRITE (BL = 16 or 32)	MASK WRITE	PRECHARGE
ACTIVE	Illegal	RU(tRCD/tCK)	RU(tRCD/tCK)	RU(tRCD/tCK)	RU(tRAS/tCK)
READ (with BL = 16)	Illegal	8[1]	RL + RU(tDQSCK(MAX)/ tCK) + BL/2 + RD(tRPST) - ODTLon - RD(tODTon(MIN)/ tCK)	RL + RU(tDQSCK(MAX)/ tCK) + BL/2 + RD(tRPST) - ODTLon - RD(tODTon(MIN)/ tCK)	BL/2 + MAX{(8,RU(tRTP/ tCK)} - 8
READ (with BL = 32)	Illegal	16[2]	RL + RU(tDQSCK(MAX)/ tCK) + BL/2 + RD(tRPST) - ODTLon - RD(tODTon(MIN)/ tCK)	RL + RU(tDQSCK(MAX)/ tCK) + BL/2 + RD(tRPST) - ODTLon - RD(tODTon(MIN)/ tCK)	BL/2 + MAX{(8,RU(tRTP/ tCK)} - 8
WRITE (with BL = 16)	Illegal	WL + 1+ BL/2 + RU(tWTR/tCK)	8[1]	tCCDMW[3]	WL + 1+ BL/2 + RU(tWR/tCK)
WRITE (with BL = 32)	Illegal	WL + 1+ BL/2 + RU(tWTR/tCK)	16[2]	tCCDM+8[4]	WL + 1+ BL/2 + RU(tWR/tCK)
MASK WRITE	Illegal	WL + 1+ BL/2 + RU(tWTR/tCK)	tCCD	tCCDMW[3]	WL + 1+ BL/2 + RU(tWR/tCK)
PRECHARGE	RU(tRP/tCK), RU(tRPab/tCK)	Illegal	Illegal	Illegal	4

Notes:
1. In the case of BL = 16, tCCD is 8 ×tCK.
2. In the case of BL = 32, tCCD is 16 ×tCK.
3. tCCDMW = 32 ×tCK (4 ×tCCD at BL = 16).
4. WRITE with BL = 32 operation is 8 ×tCK longer than BL = 16.

Table 4-92: Different Bank (ODT Enabled)

Next CMD Current CMD	ACTIVE	READ (BL = 16 or 32)	WRITE (BL = 16 or 32)	MASK WRITE	PRECHARGE
ACTIVE	RU(^{t}RRD/^{t}CK)	4	4	4	2[2]
READ (with BL = 16)	4	8[1]	RL + RU(^{t}DQSCK(MAX)/ ^{t}CK) + BL/2 + RD(^{t}RPST) - ODTLon - RD(^{t}ODTon(MIN)/ ^{t}CK)	RL + RU(^{t}DQSCK(MAX)/ ^{t}CK) + BL/2 + RD(^{t}RPST) - ODTLon - RD(^{t}ODTon(MIN)/ ^{t}CK)	2[2]
READ (with BL = 32)	4	16[2]	RL + RU(^{t}DQSCK(MAX)/ ^{t}CK) + BL/2 + RD(^{t}RPST) - ODTLon - RD(^{t}ODTon(MIN)/ ^{t}CK)	RL + RU(^{t}DQSCK(MAX)/ ^{t}CK) + BL/2 + RD(^{t}RPST) - ODTLon - RD(^{t}ODTon(MIN)/ ^{t}CK)	2[2]
WRITE (with BL = 16)	4	WL + 1+ BL/2 + RU(^{t}WTR/^{t}CK)	8[1]	8[1]	2[2]
WRITE (with BL = 32)	4	WL + 1+ BL/2 + RU(^{t}WTR/^{t}CK)	16[2]	16[2]	2[2]
MASK WRITE	4	WL + 1+ BL/2 + RU(^{t}WTR/^{t}CK)	8[1]	8[1]	2[2]
PRECHARGE	4	4	4	4	4

Notes:

1. In the case of BL = 16, ^{t}CCD is 8 ×^{t}CK.
2. In the case of BL = 32, ^{t}CCD is 16 ×^{t}CK

4.16 Data Mask and Data Bus Inversion (DBI [DC]) Function

Data mask (DM) is supported for WRITE operations and the data bus inversion DBI(DC) is supported for READ, WRITE, MASK WRITE, MRR, and MRW operations. DMand DBI (DC) functions are supported with byte granularity. DBI (DC) for READ operations(READ, MRR) can be enabled or disabled via MR3 OP[6]. DBI (DC) for WRITE operations(WRITE, MASK WRITE, MRW) can be enabled or disabled via MR3 OP[7]. DMfor MASK WRITE operations can be enabled or disabled via MR13 OP[5]. The device hasone data mask inversion (DMI) pin per byte and a total of two DMI pins per channel.The DMI signal is a bidirectional DDR signal, is sampled with the DQ signals, and iselectrically identical to a DQ signal.

There are eight possible states for the device with the DM and DBI (DC) functions.

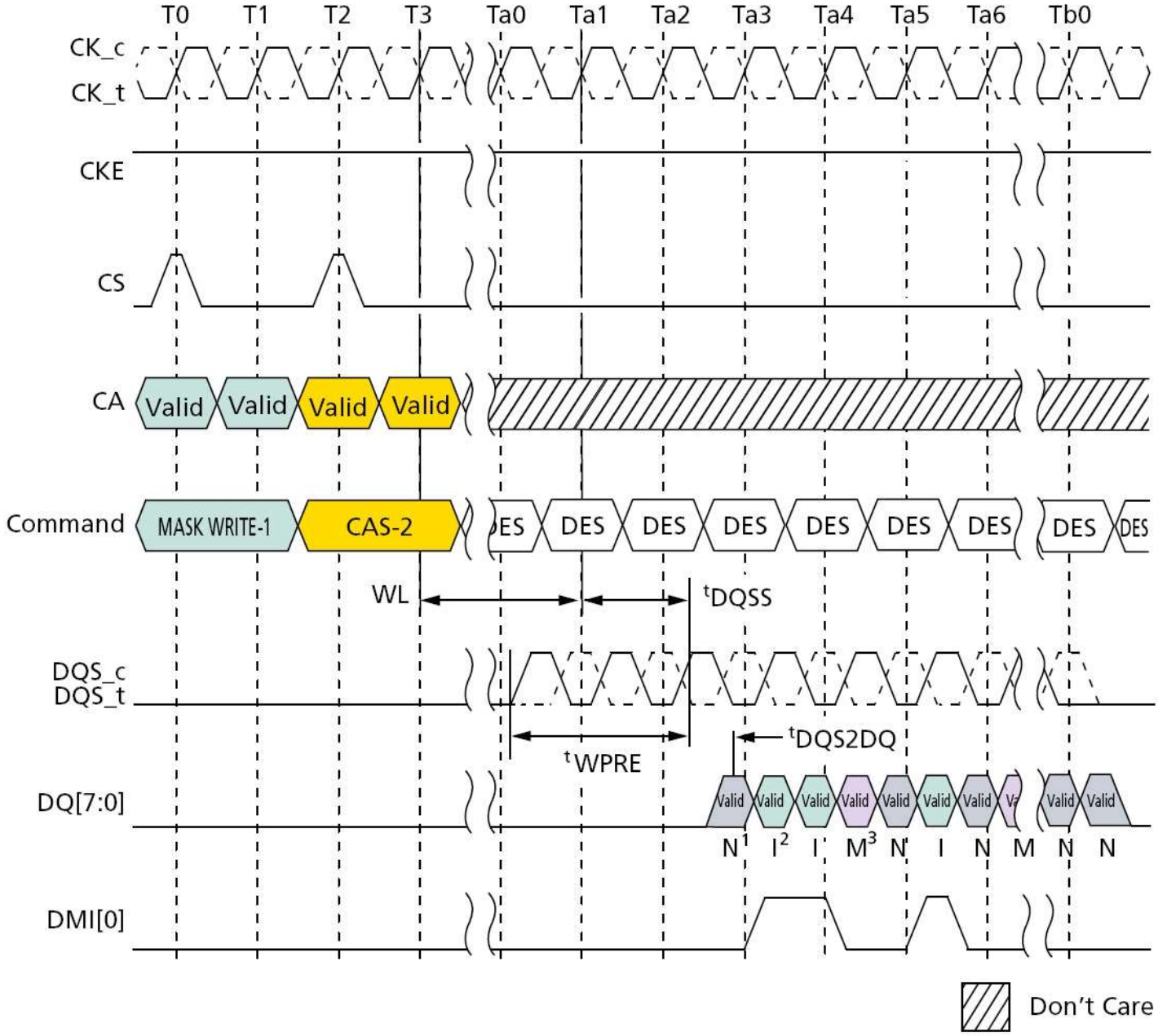
Table 4-93: Function Behavior of DMI Signal During WRITE, MASKED WRITE, and READ Operations

DM Function	Write DBI (DC)	Read DBI (DC)	DMI Signal					
			During WRITE	During MASKED WRITE	During READ	During MPC[WRITE-FIFO]	During MPC[READFIFO]	During MPC[READ DQ CAL]
Disabled	Disabled	Disabled	Don't Care[1]	Illegal[1, 3]	High-Z[2]	Don't Care[1]	High-Z[2]	High-Z[2]
Disabled	Enabled	Disabled	DBI (DC)[4]	Illegal[3]	High-Z[2]	Train[9]	Train[10]	Train[11]
Disabled	Disabled	Enabled	Don't Care[1]	Illegal[3]	DBI (DC)[5]	Train[9]	Train[10]	Train[11]
Disabled	Enabled	Enabled	DBI (DC)[4]	Illegal[3]	DBI (DC)[5]	Train[9]	Train[10]	Train[11]
Enabled	Disabled	Disabled	Don't Care[6]	DM[7]	High-Z[2]	Train[9]	Train[10]	Train[11]
Enabled	Enabled	Disabled	DBI (DC)[4]	DBI (DC)[8]	High-Z[2]	Train[9]	Train[10]	Train[11]
Enabled	Disabled	Enabled	Don't Care[6]	DM[7]	DBI (DC)[5]	Train[9]	Train[10]	Train[11]
Enabled	Enabled	Enabled	DBI (DC)[4]	DBI (DC)[8]	DBI (DC)[5]	Train[9]	Train[10]	Train[11]

Notes:

1. The DMI input signal is "Don’ t Care". DMI input receivers are turned off.
2. DMI output drivers are turned off.
3. The MASK WRITE command is not allowed and is considered an illegal command whenthe DM function is disabled.
4. The DMI signal is treated as DBI and indicates whether the device needs to invert thewrite data received on DQ within a byte. The device inverts write data received on theDQ inputs if DMI is sampled HIGH and leaves the write data non-inverted if DMI is sampledLOW.
5. The device inverts read data on its DQ outputs associated within a byte and drives theDMI signal HIGH when more than four data bits = 1 within a given byte lane; otherwise,the device does not invert the read data and drives DMI signal LOW.
6. The device does not perform a MASK operation when it receives a WRITE (or MRW)command. During the WRITE burst, the DMI signal must be driven LOW.
7. The device requires an explicit MASKED WRITE command for all MASKED WRITE operations.The DMI signal is treated as a data mask (DM) and indicates which bytes within aburst will be masked. When the DMI signal is sampled HIGH, the device masks that beatof the burst for the given byte lane. All DQ input signals within a byte are "Don't Care"(either HIGH or LOW) when DMI is HIGH. When the DMI signal is sampled LOW, the devicedoes not perform a MASK operation and data received on the DQ inputs is writtento the array.
8. The device requires an explicit MASKED WRITE command for all MASKED WRITE operations.The device masks the write data received on the DQ inputs if five or more databits = 1 on DQ[2:7] or DQ[10:15] (for lower byte or upper byte respectively) and the DMIsignal is LOW. Otherwise, the device does not perform the MASK operation and treats itas a legal DBI pattern. The DMI signal is treated as a DBI signal, and data received onthe DQ input is written to the array.
9. The DMI signal is treated as a training pattern. The device does not perform any MASKoperation and does not invert write data received on the DQ inputs.
10. The DMI signal is treated as a training pattern. The device returns the data pattern writtento the WRITE-FIFO.
11. The DMI signal is treated as a training pattern. For more information, see the Read DQCalibration Training section.

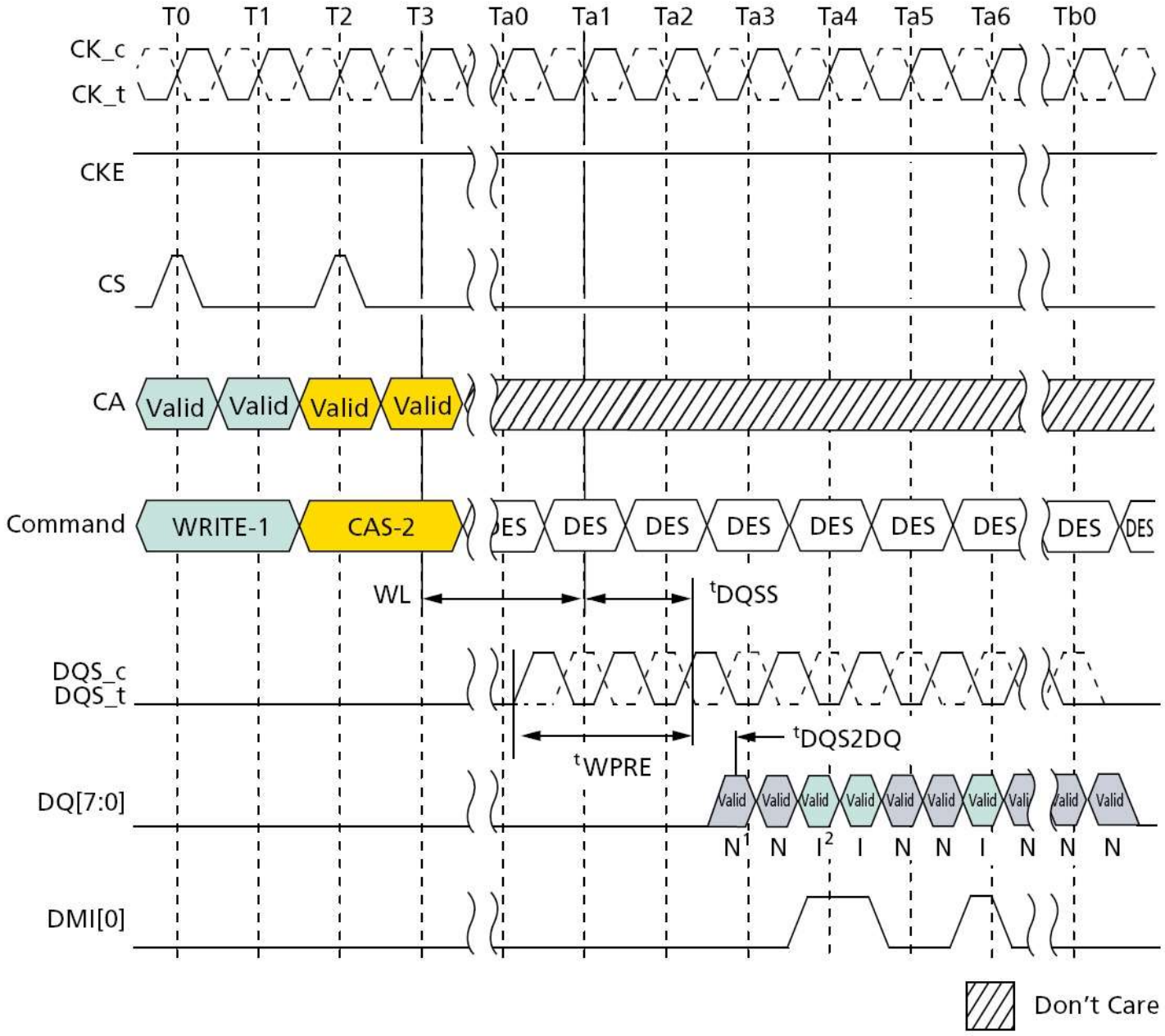
Figure 4-23: MASKED WRITE Command with Write DBI Enabled; DM Enabled



Notes:

1. N: Input data is written to DRAM cell.
2. I: Input data is inverted, then written to DRAM cell.
3. M: Input data is masked. The total count of 1 data bits on DQ[7:2] is equal to or greaterthan five.
4. Data mask (DM) is enable: MR13 OP [5] = 0, Data bus inversion (DBI) write is enable:MR3 OP[7] = 1.

Figure 4-24: WRITE Command with Write DBI Enabled; DM Disabled



Notes:

1. N: Input data is written to DRAM cell.
2. I: Input data is inverted, then written to DRAM cell.
3. Data mask (DM) is disable: MR13 OP [5] = 1, Data bus inversion (DBI) write is enable:MR3 OP[7] = 1.

4.17 Preamble and Postamble Behavior

Preamble, Postamble Behavior in READ-to-READ Operations

The following illustrations show the behavior of the device's read DQS_t and DQS_cpins during cases where the preamble, postamble, and/or data clocking overlap.

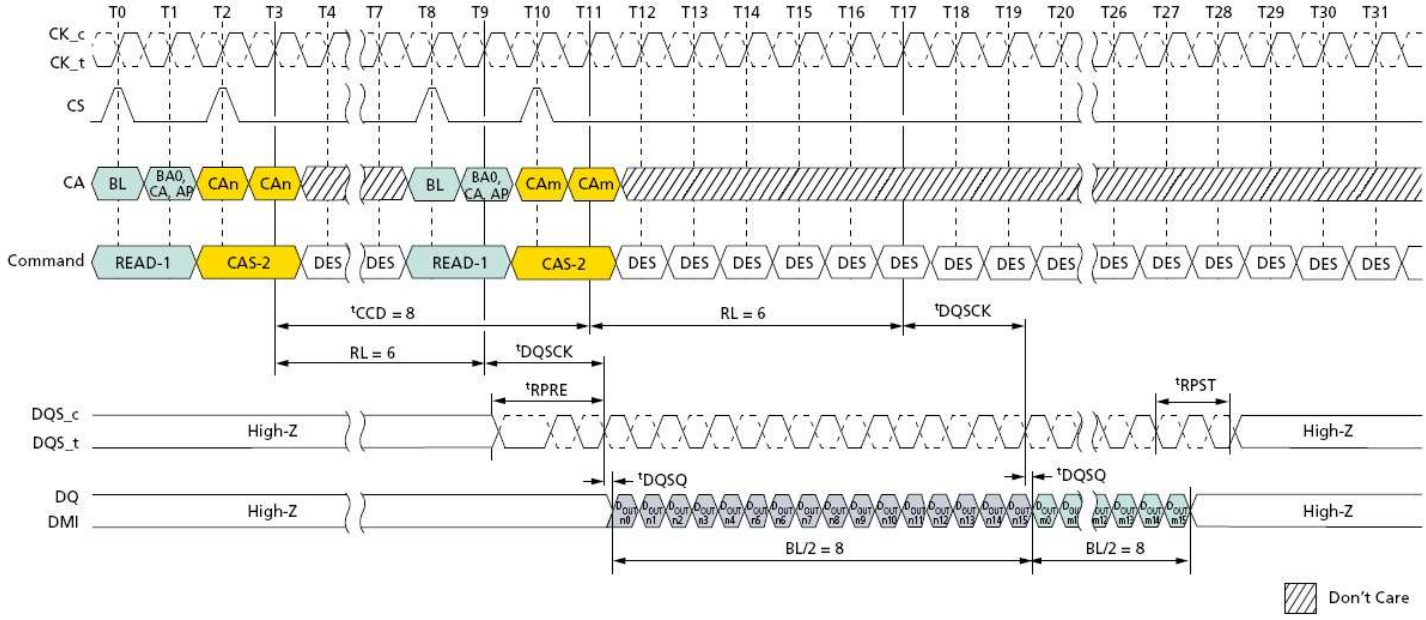
DQS will be driven with the following priority
1. Data clocking edges will always be driven
2. Postamble
3. Preamble

Essentially the data clocking, preamble, and postamble will be ordered such that alledges will be driven.

Additional examples of seamless and borderline non-overlapping cases have been includedfor clarity.

READ-to-READ Operations – Seamless

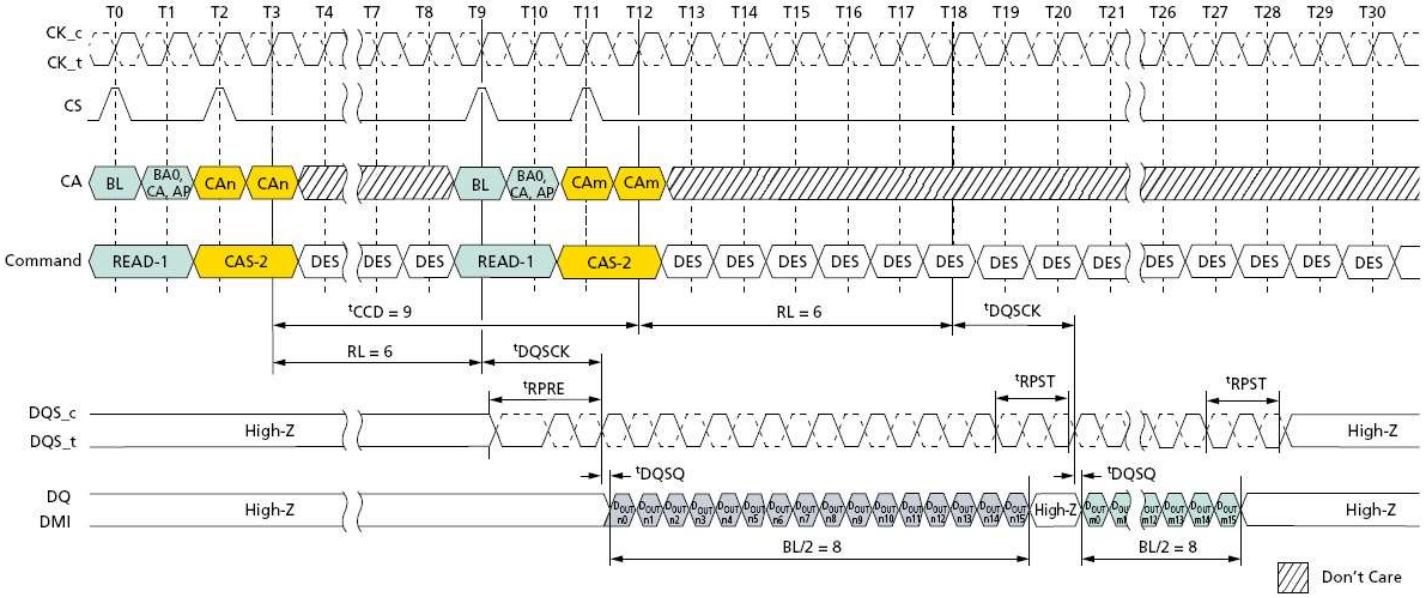
Figure 4-25: READ Operations: tCCD = MIN, Preamble = Toggle, 1.5nCK Postamble



Notes:
1. BL = 16 for column n and column m; RL = 6; Preamble = Toggle; Postamble = 1.5nCK.
2. DOUT n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid atthese times.

READ-to-READ Operations – Consecutive

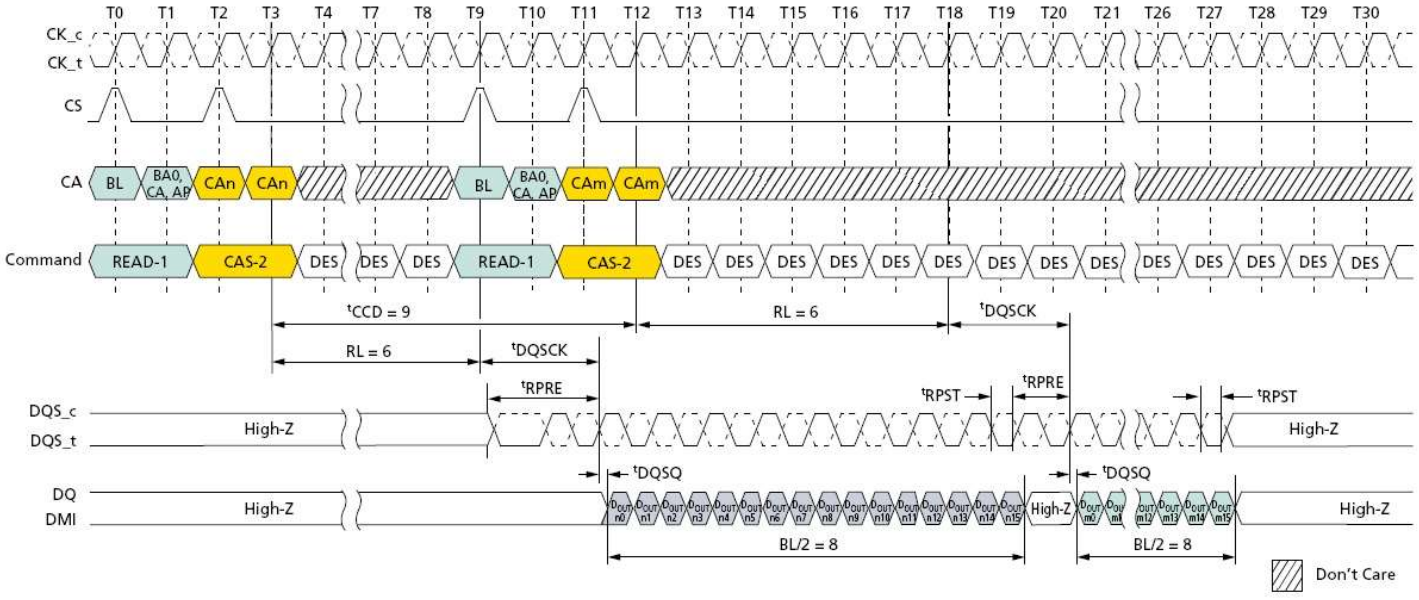
Figure 4-26: Seamless READ: tCCD = MIN + 1, Preamble = Toggle, 1.5nCK Postamble



Notes:

1. BL = 16 for column n and column m; RL = 6; Preamble = Toggle; Postamble = 1.5nCK.
2. D_{OUT} n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid atthese times.

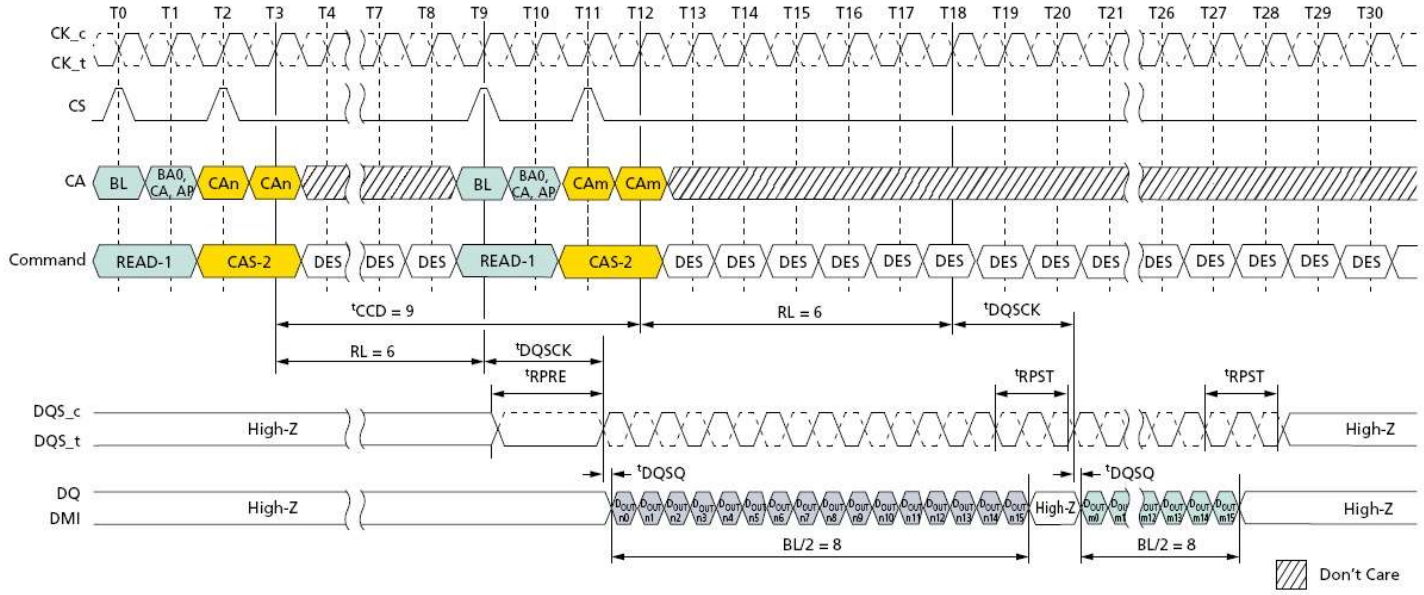
Figure 4-27: Consecutive READ: tCCD = MIN + 1, Preamble = Toggle, 0.5nCK Postamble



Notes:

1. BL = 16 for column n and column m; RL = 6; Preamble = Toggle; Postamble = 0.5nCK.
2. D_{OUT}n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid atthese times.

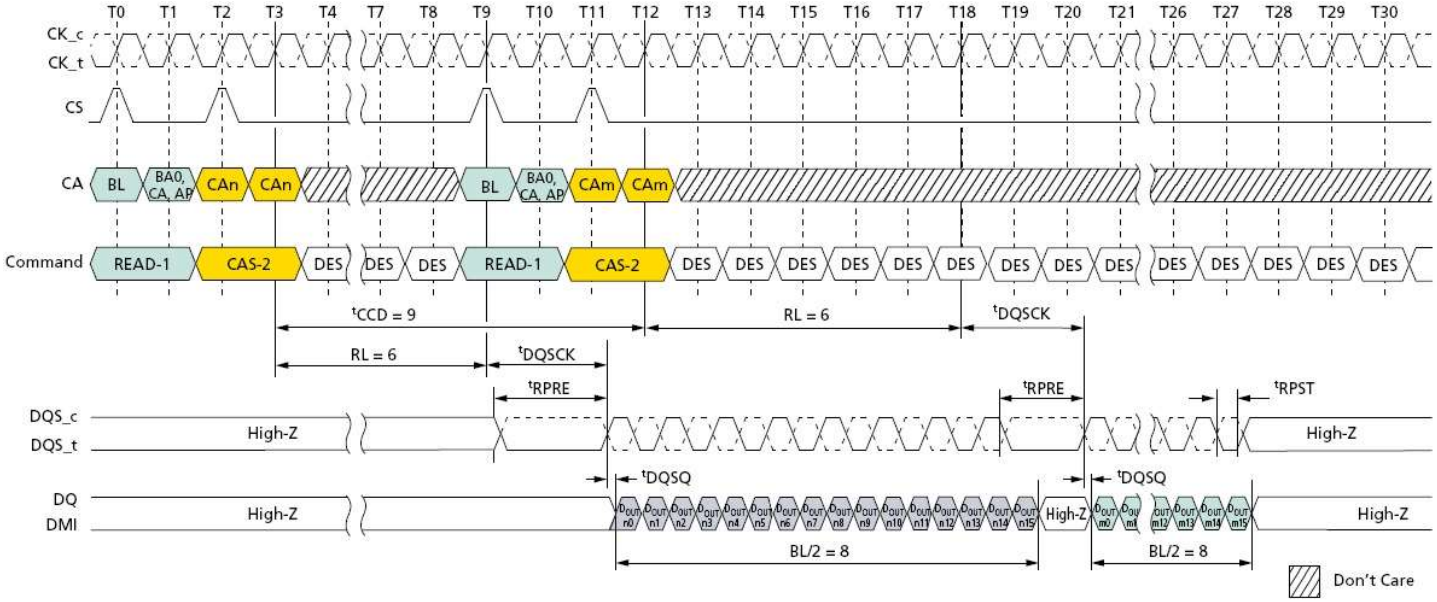
Figure 4-28: Consecutive READ: tCCD = MIN + 1, Preamble = Static, 1.5nCK Postamble



Notes:

1. BL = 16 for column n and column m; RL = 6; Preamble = Static; Postamble = 1.5nCK.
2. D_{OUT} n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid atthese times.

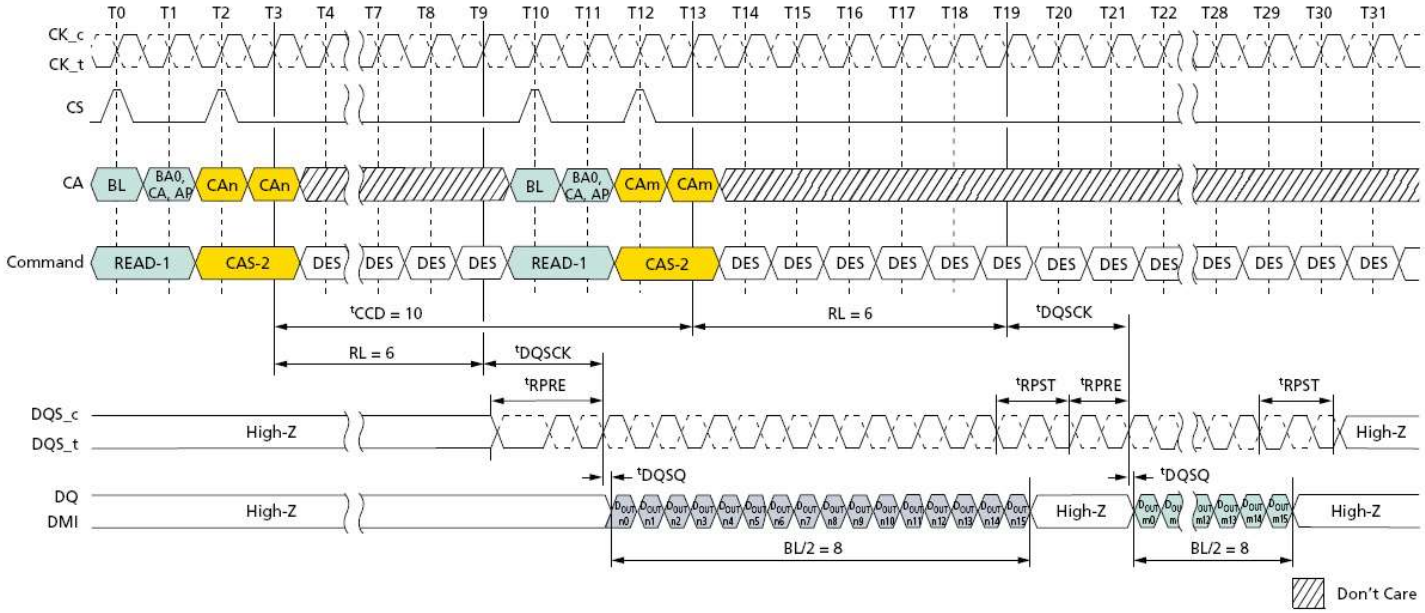
Figure 4-29: Consecutive READ: ^{t}CCD = MIN + 1, Preamble = Static, 0.5nCK Postamble



Notes:

1. BL = 16 for column n and column m; RL = 6; Preamble = Static; Postamble = 0.5nCK.
2. D_{OUT} n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid atthese times.

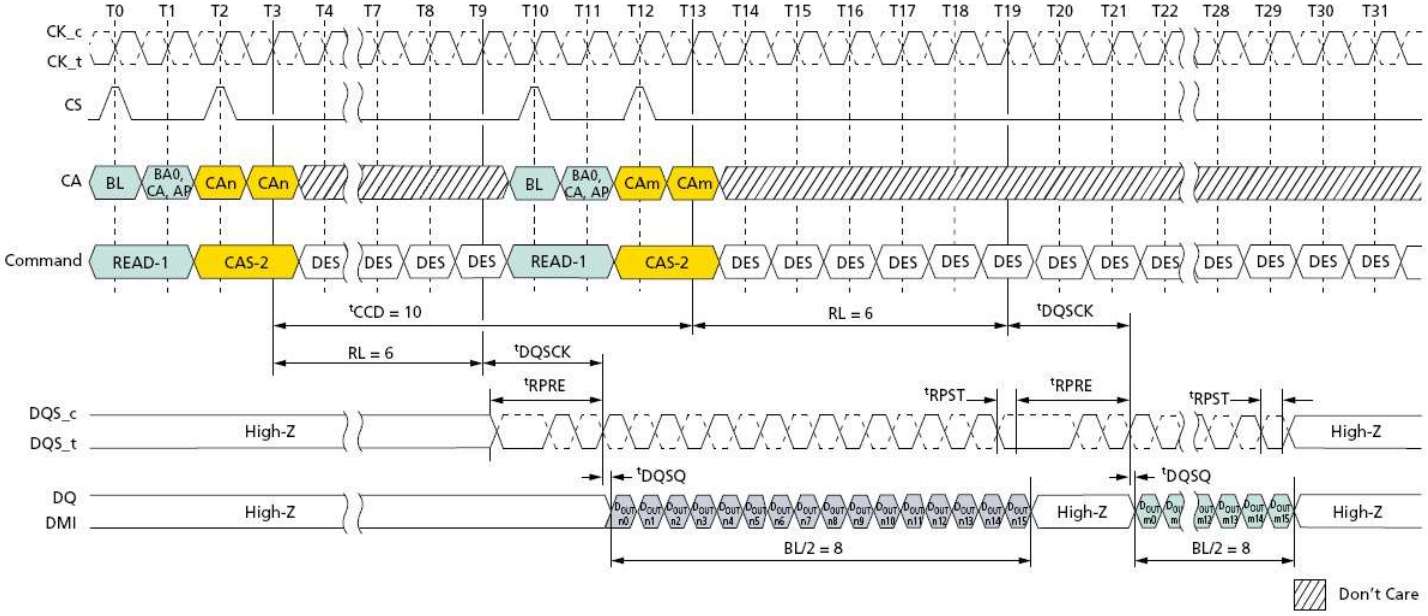
Figure 4-30: Consecutive READ: ^{t}CCD = MIN + 2, Preamble = Toggle, 1.5nCK Postamble



Notes:

1. BL = 16 for column n and column m; RL = 6; Preamble = Toggle; Postamble = 1.5nCK.
2. D_{OUT} n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid atthese times.

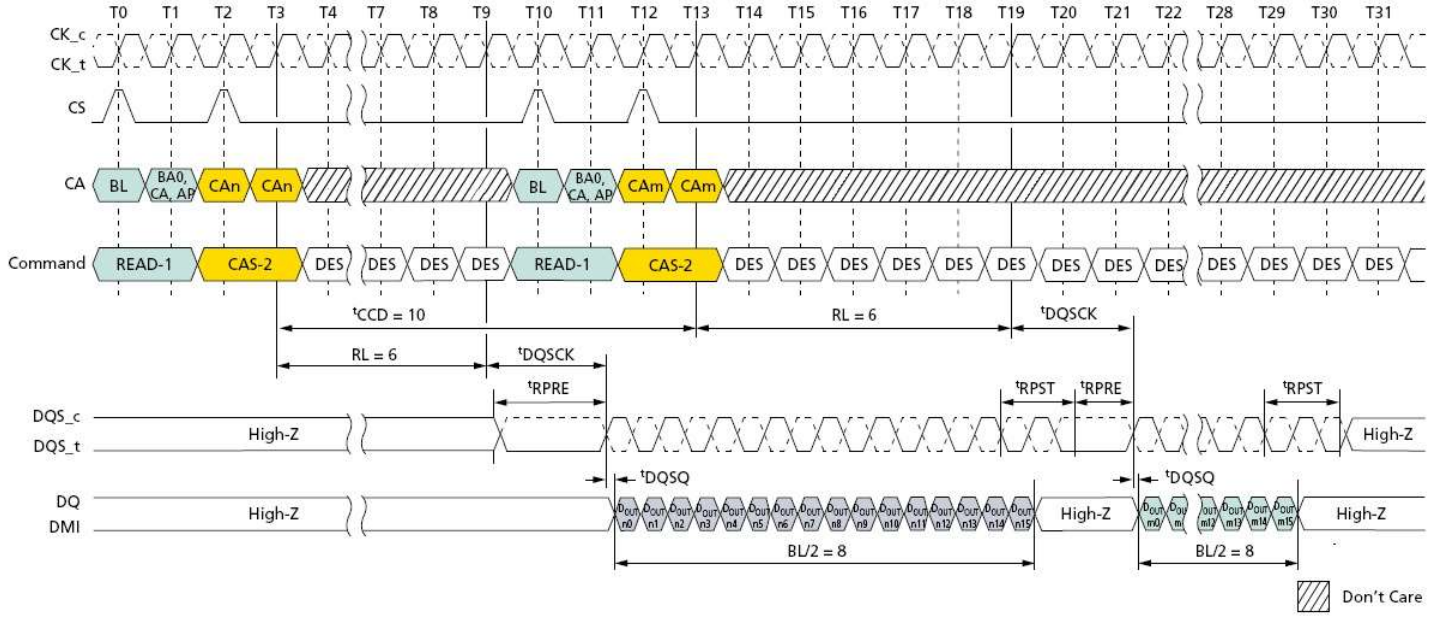
Figure 4-31: Consecutive READ: ^{t}CCD = MIN + 2, Preamble = Toggle, 0.5nCK Postamble



Notes:

1. BL = 16 for column n and column m; RL = 6; Preamble = Toggle; Postamble = 0.5nCK.
2. D_{OUT} n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid atthese times.

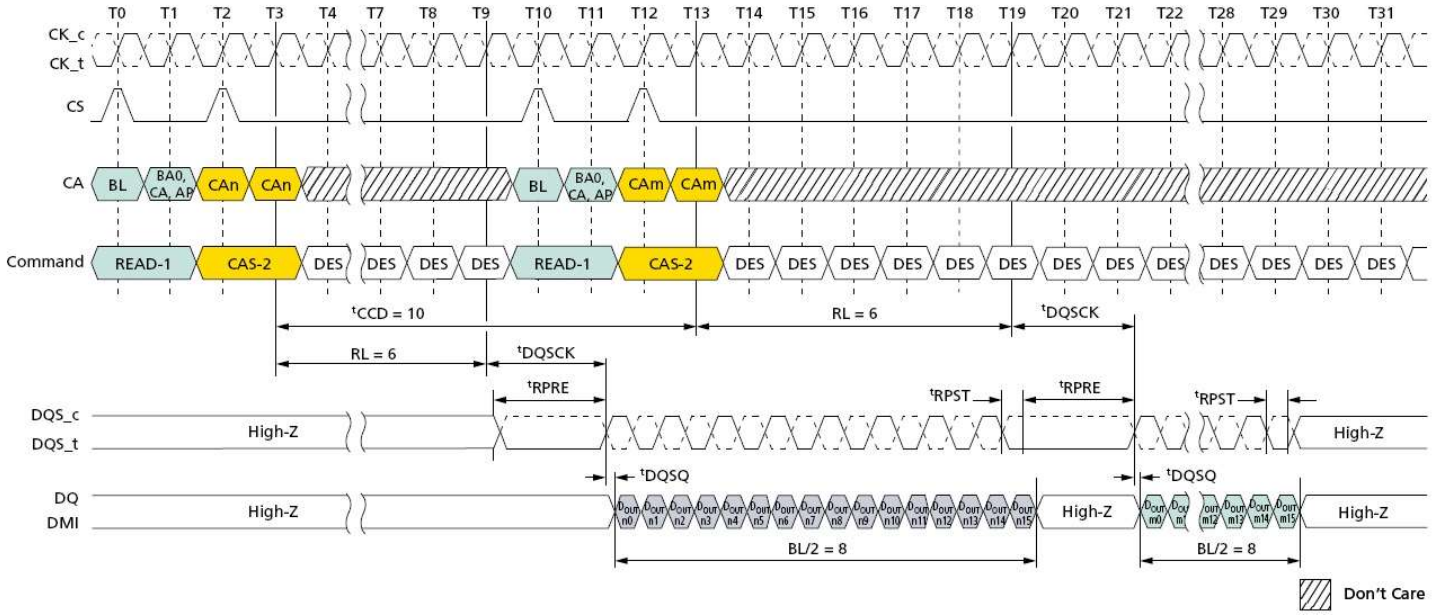
Figure 4-32: Consecutive READ: ^{t}CCD = MIN + 2, Preamble = Static, 1.5nCK Postamble



Notes:

1. BL = 16 for column n and column m; RL = 6; Preamble = Static; Postamble = 1.5nCK.
2. D_{OUT} n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid atthese times.

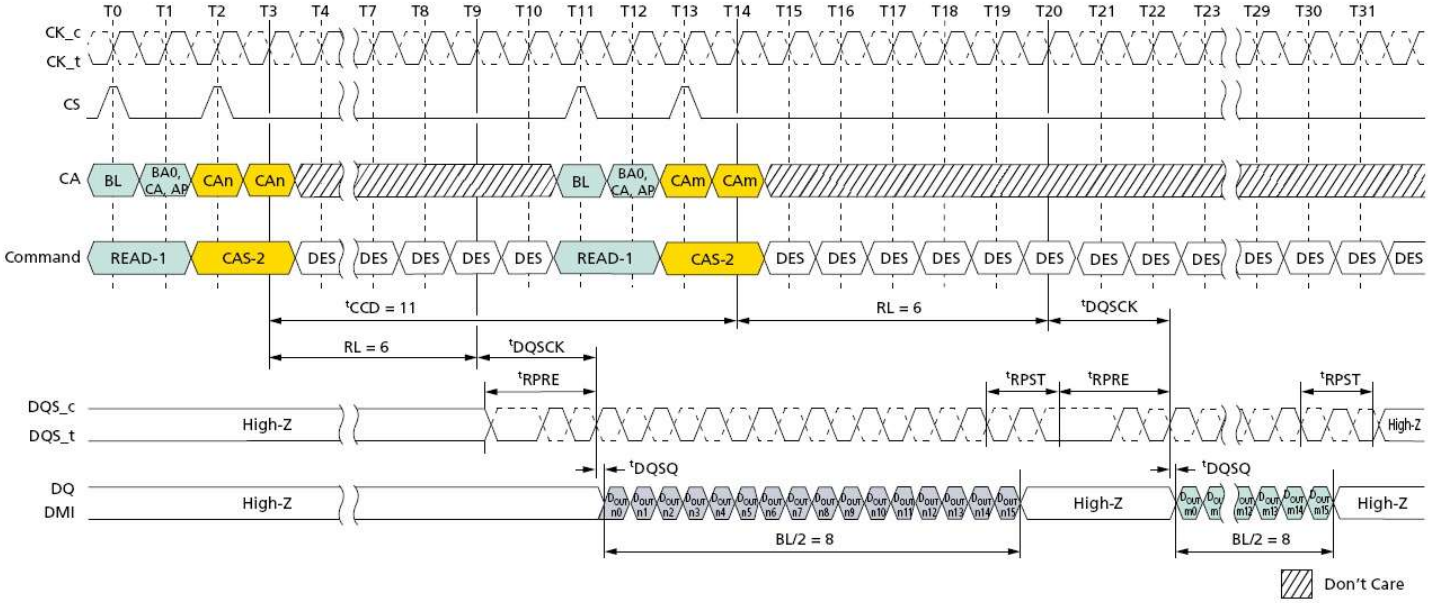
Figure 4-33: Consecutive READ: ^{t}CCD = MIN + 2, Preamble = Static, 0.5nCK Postamble



Notes:

1. BL = 16 for column n and column m; RL = 6; Preamble = Static; Postamble = 0.5nCK.
2. D_{OUT} n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid atthese times.

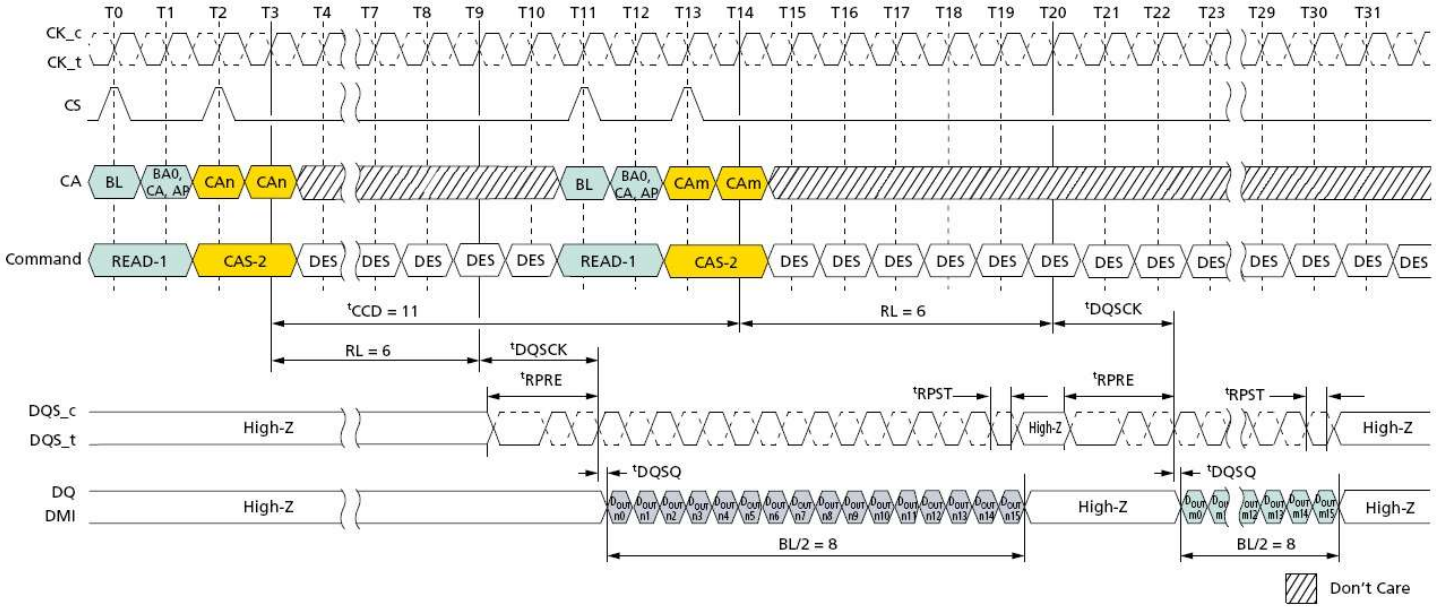
Figure 4-34: Consecutive READ: ^{t}CCD = MIN + 3, Preamble = Toggle, 1.5nCK Postamble



Notes:

1. BL = 16 for column n and column m; RL = 6; Preamble = Toggle; Postamble = 1.5nCK.
2. D_{OUT} n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid atthese times.

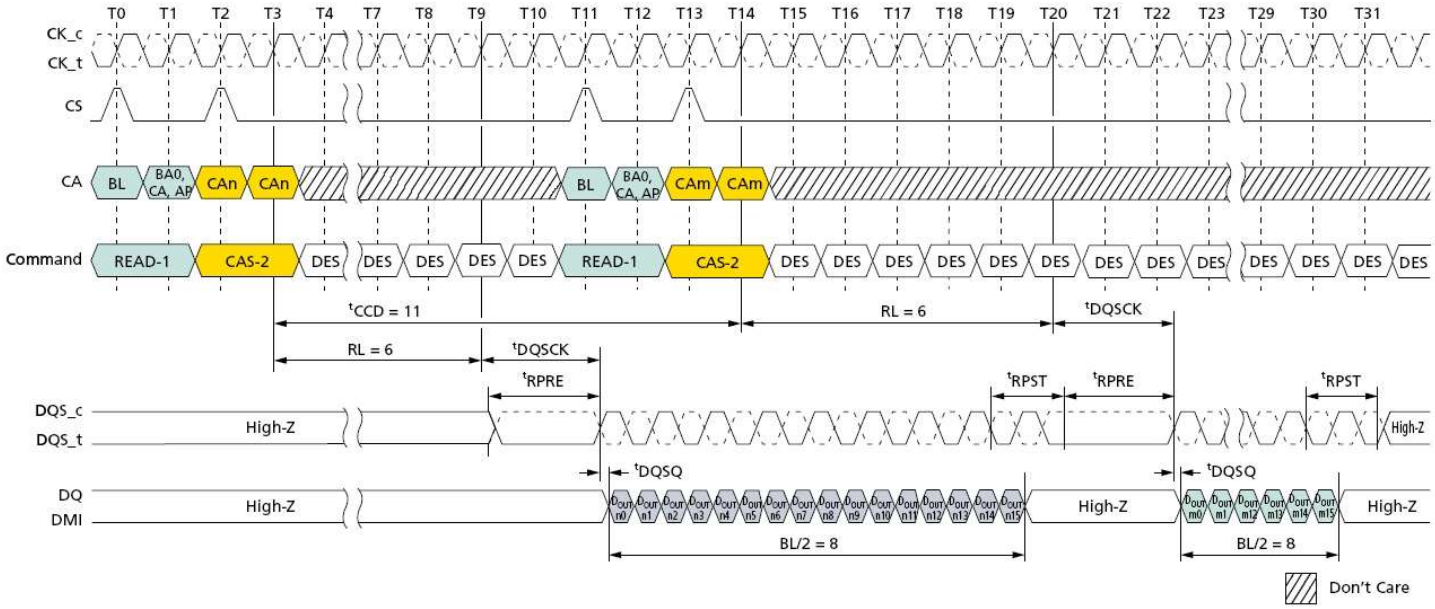
Figure 4-35: Consecutive READ: ^{t}CCD = MIN + 3, Preamble = Toggle, 0.5nCK Postamble



Notes:

1. BL = 16 for column n and column m; RL = 6; Preamble = Toggle; Postamble = 0.5nCK.
2. D_{OUT} n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid atthese times.

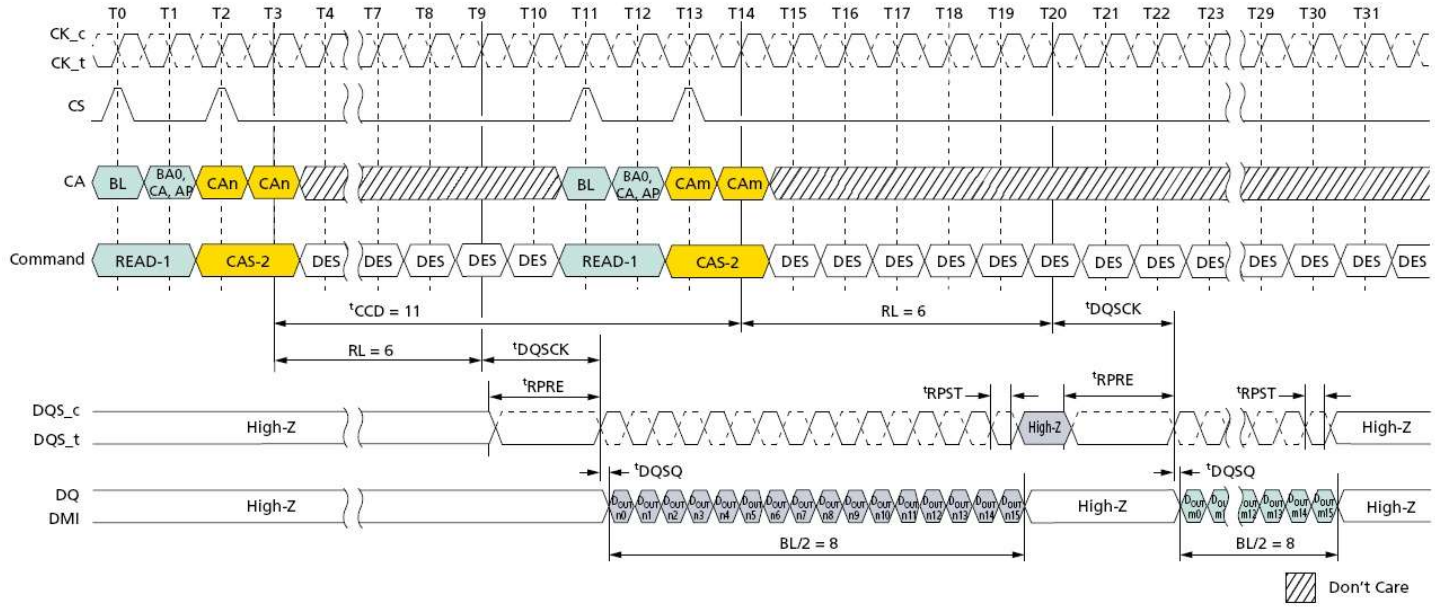
Figure 4-36: Consecutive READ: ^{t}CCD = MIN + 3, Preamble = Static, 1.5nCK Postamble



Notes:

1. BL = 16 for column n and column m; RL = 6; Preamble = Static; Postamble = 1.5nCK.
2. D_{OUT} n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid atthese times.

Figure 4-37: Consecutive READ: ^{t}CCD = MIN + 3, Preamble = Static, 0.5nCK Postamble

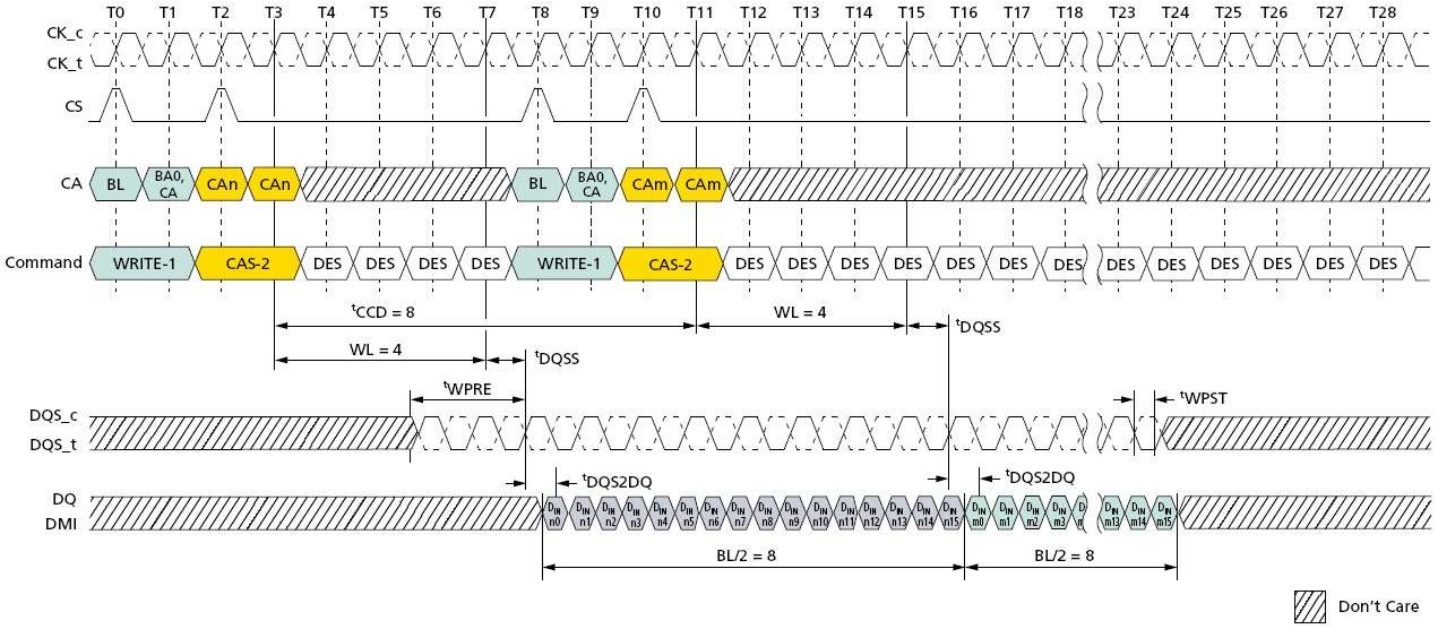


Notes:

1. BL = 16 for column n and column m; RL = 6, Preamble = Static; Postamble = 0.5nCK
2. D_{OUT} n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid atthese times.

WRITE-to-WRITE Operations – Seamless

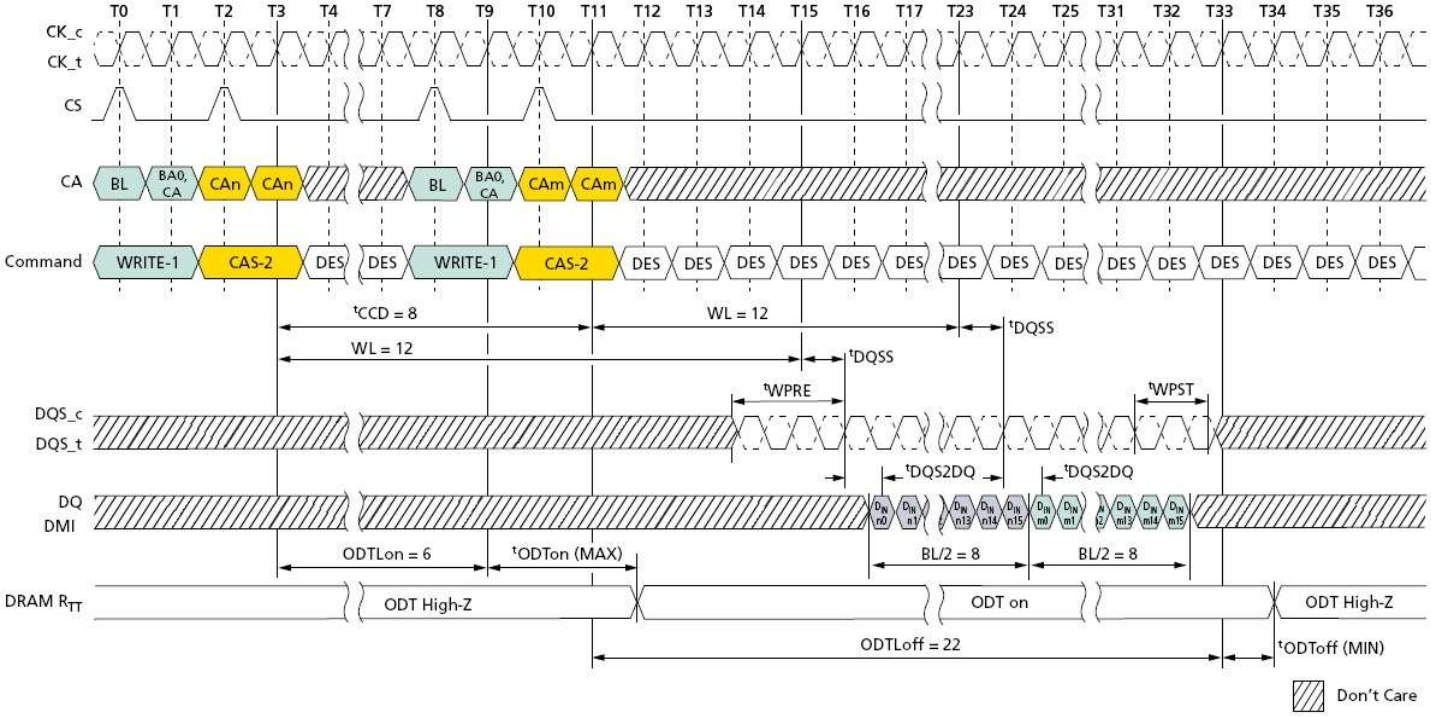
Figure 4-38: Seamless WRITE: ^{t}CCD = MIN, 0.5nCK Postamble



Notes:

1. BL = 16, Write postamble = 0.5nCK.
2. D_{IN} n/m = data-in from column n and column m.
3. The minimum number of clock cycles from the burst WRITE command to the burstWRITE command for any bank is BL/2.
4. DES commands are shown for ease of illustration; other commands may be valid atthese times.

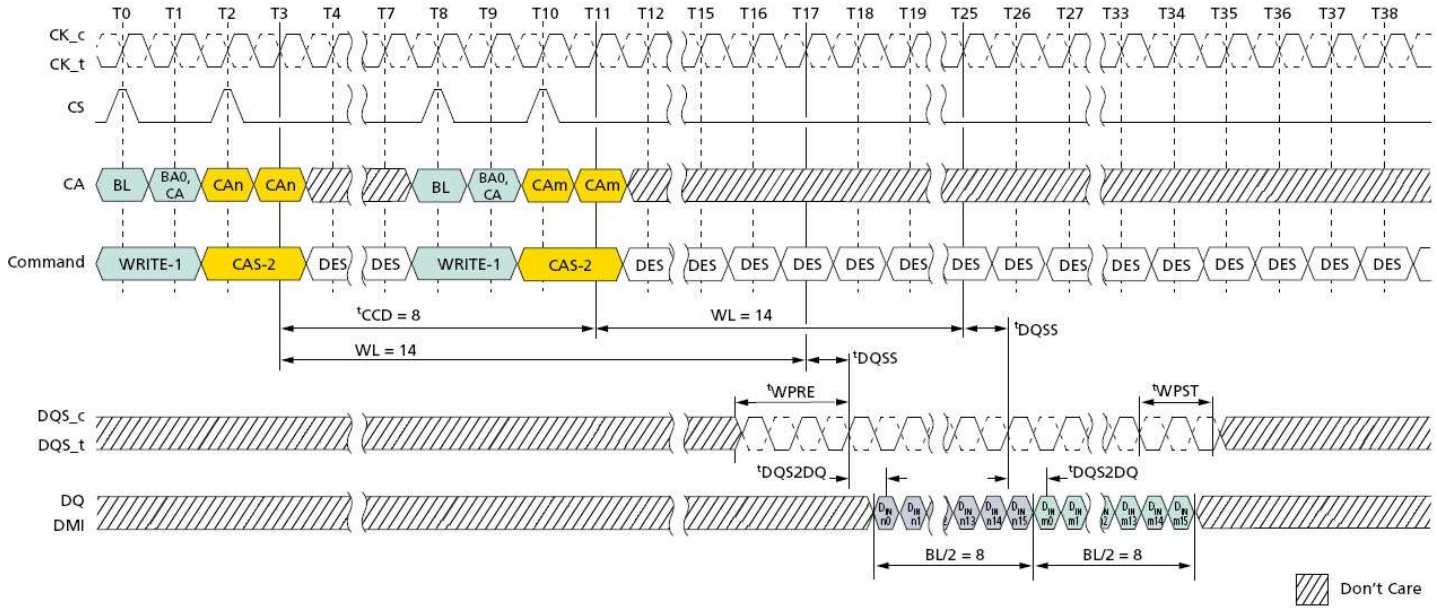
Figure 4-39: Seamless WRITE: tCCD = MIN, 1.5nCK Postamble, 533 MHz < Clock Frequency ≤ 800 MHz, ODT Worst Timing Case



Notes:

1. Clock frequency = 800 MHz, tCK(AVG) = 1.25ns.
2. BL = 16, Write postamble = 1.5nCK.
3. D_{IN} n/m = data-in from column n and column m.
4. The minimum number of clock cycles from the burst WRITE command to the burstWRITE command for any bank is BL/2.
5. DES commands are shown for ease of illustration; other commands may be valid atthese times.

Figure 4-40: Seamless WRITE: ^{t}CCD = MIN, 1.5nCK Postamble

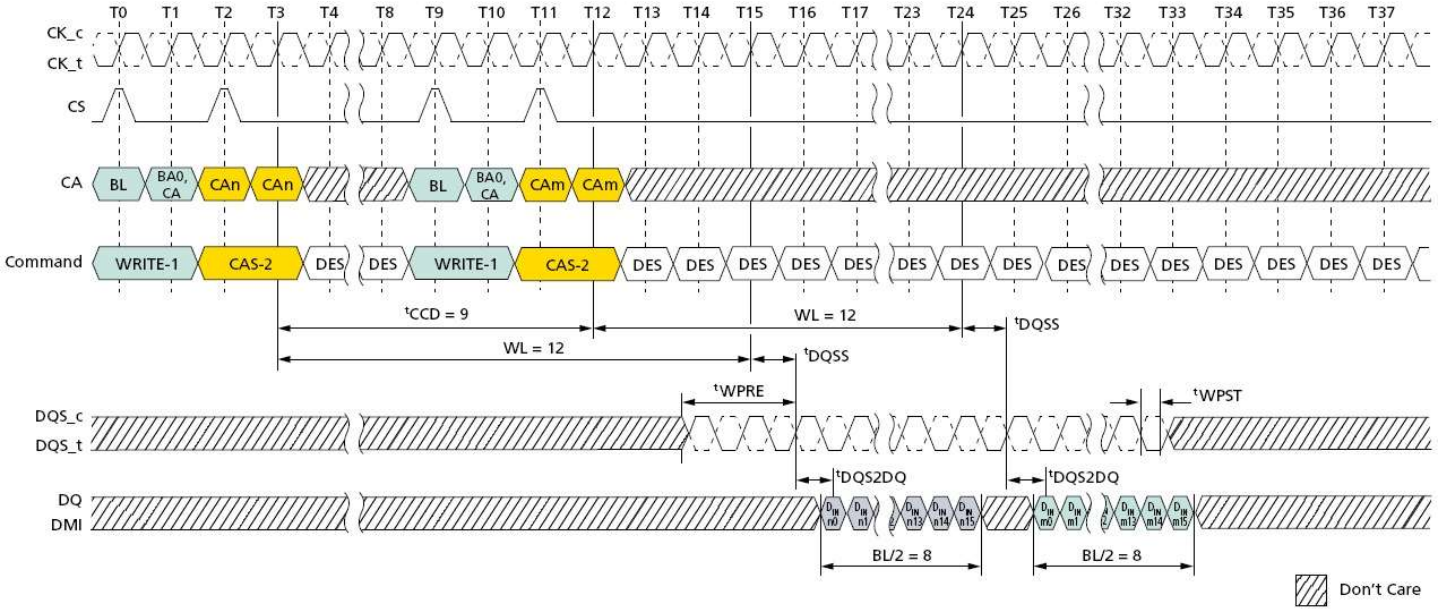


Notes:

1. BL = 16, Write postamble = 1.5nCK.
2. D_{IN} n/m = data-in from column n and column m.
3. The minimum number of clock cycles from the burst WRITE command to the burstWRITE command for any bank is BL/2.
4. DES commands are shown for ease of illustration; other commands may be valid atthese times.

WRITE-to-WRITE Operations – Consecutive

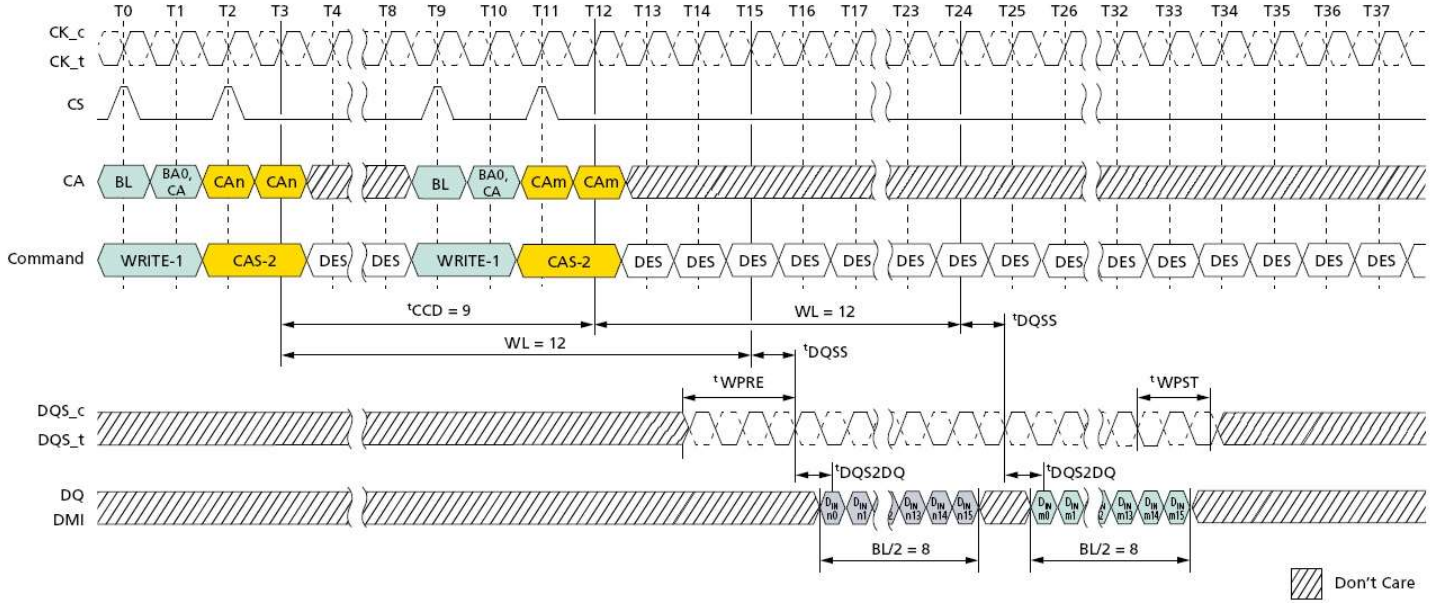
Figure 4-41: Consecutive WRITE: ^{t}CCD = MIN + 1, 0.5nCK Postamble



Notes:

1. BL = 16, Write postamble = 0.5nCK.
2. D_{IN} n/m = data-in from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid atthese times.

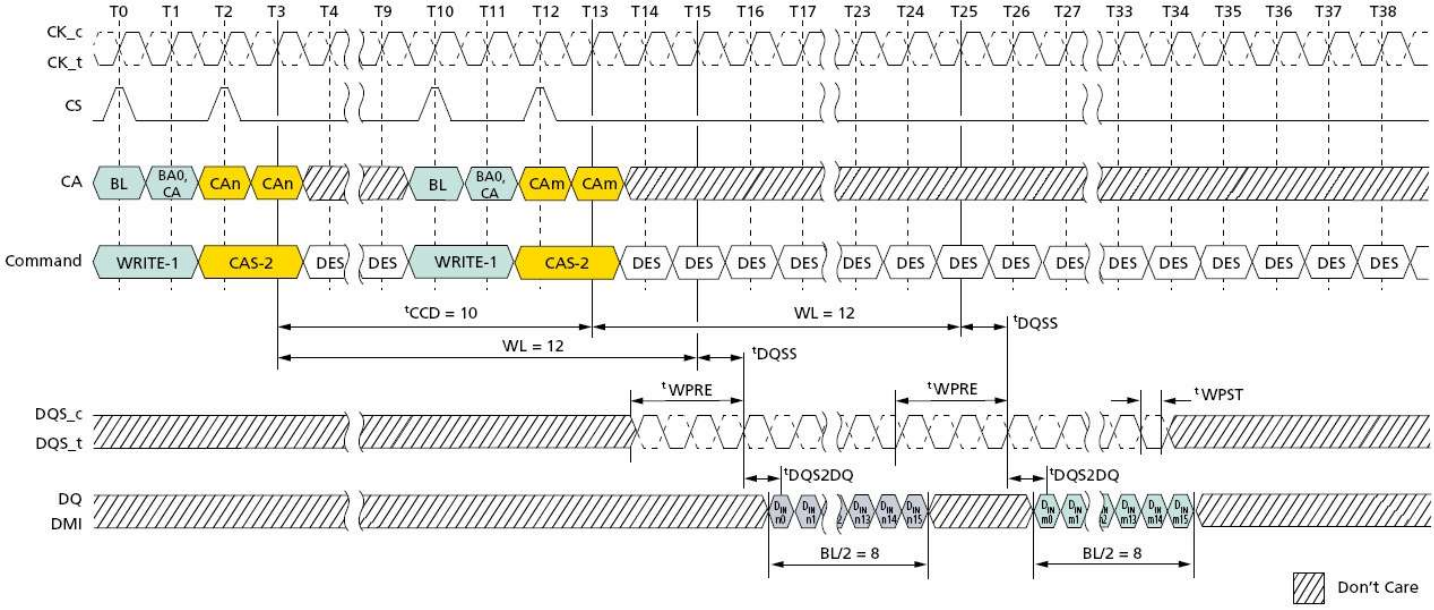
Figure 4-42: Consecutive WRITE: ^{t}CCD = MIN + 1, 1.5nCK Postamble



Notes:

1. LB = 16, Write postamble = 1.5nCK.
2. D_{IN} n/m = data-in from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid atthese times.

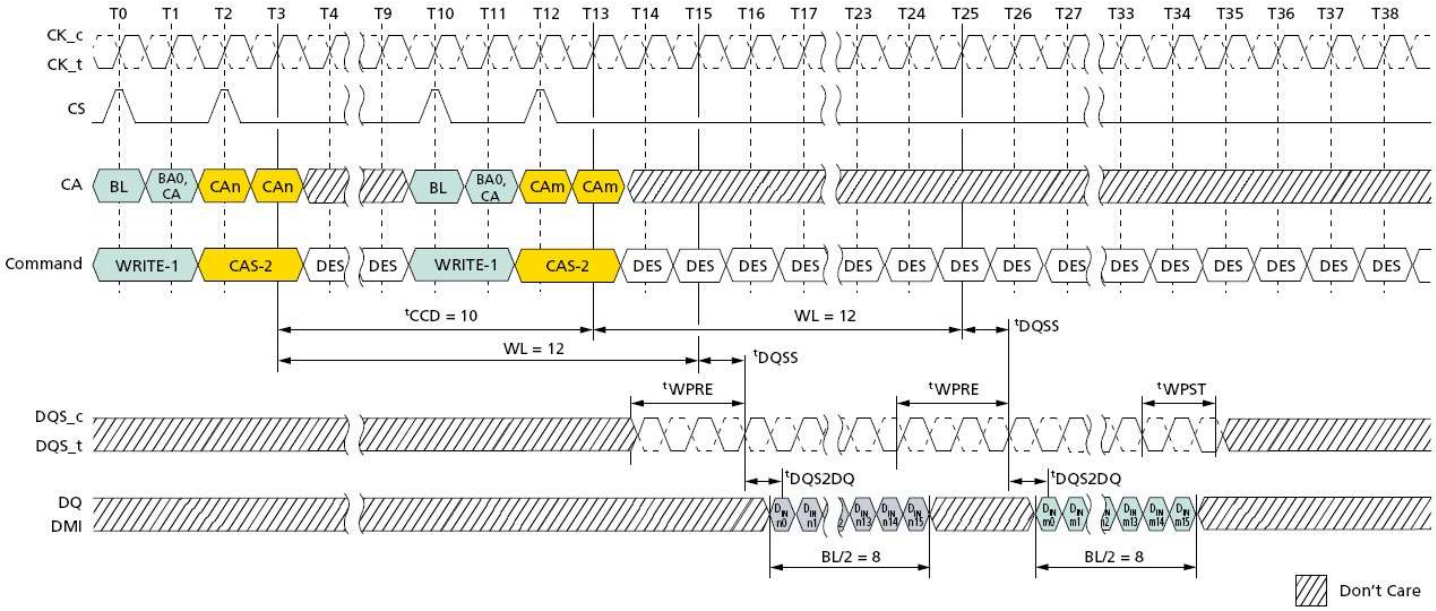
Figure 4-43: Consecutive WRITE: ^{t}CCD = MIN + 2, 0.5nCK Postamble



Notes:

1. BL = 16, Write postamble = 0.5nCK.
2. D_{IN} n/m = data-in from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid atthese times.

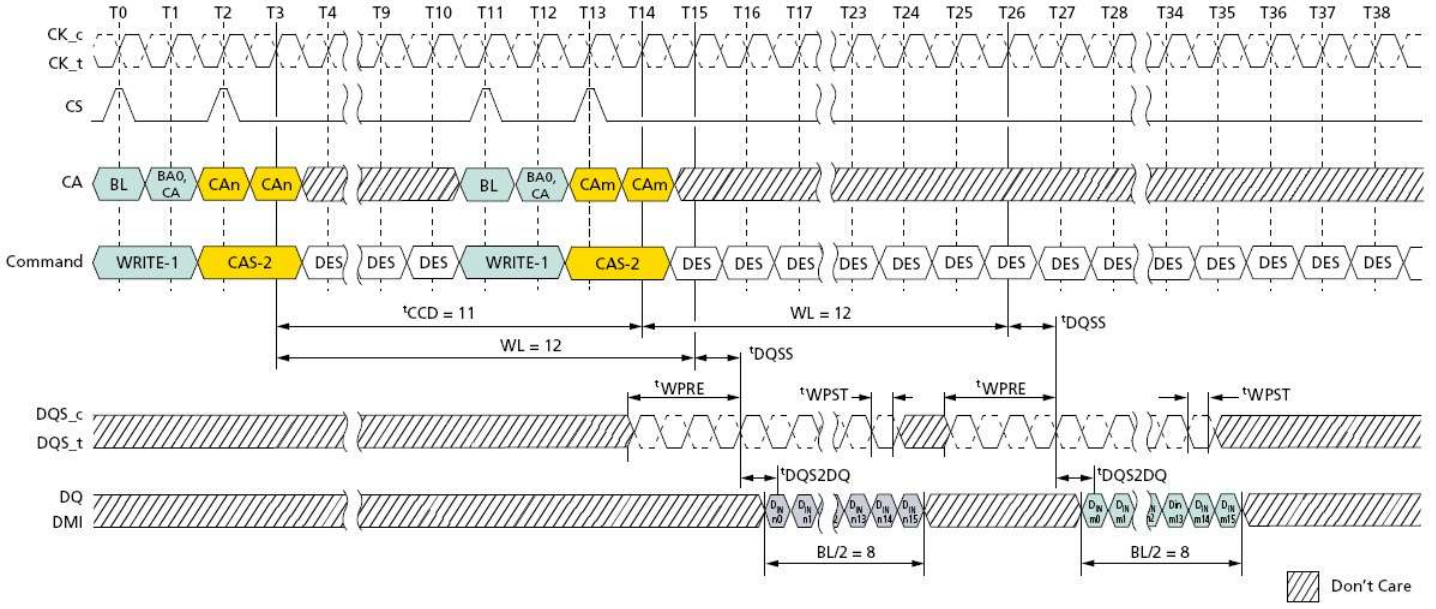
Figure 4-44: Consecutive WRITE: tCCD = MIN + 2, 1.5nCK Postamble



Notes:

1. BL = 16, Write postamble = 1.5nCK.
2. D_{IN} n/m = data-in from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid atthese times.

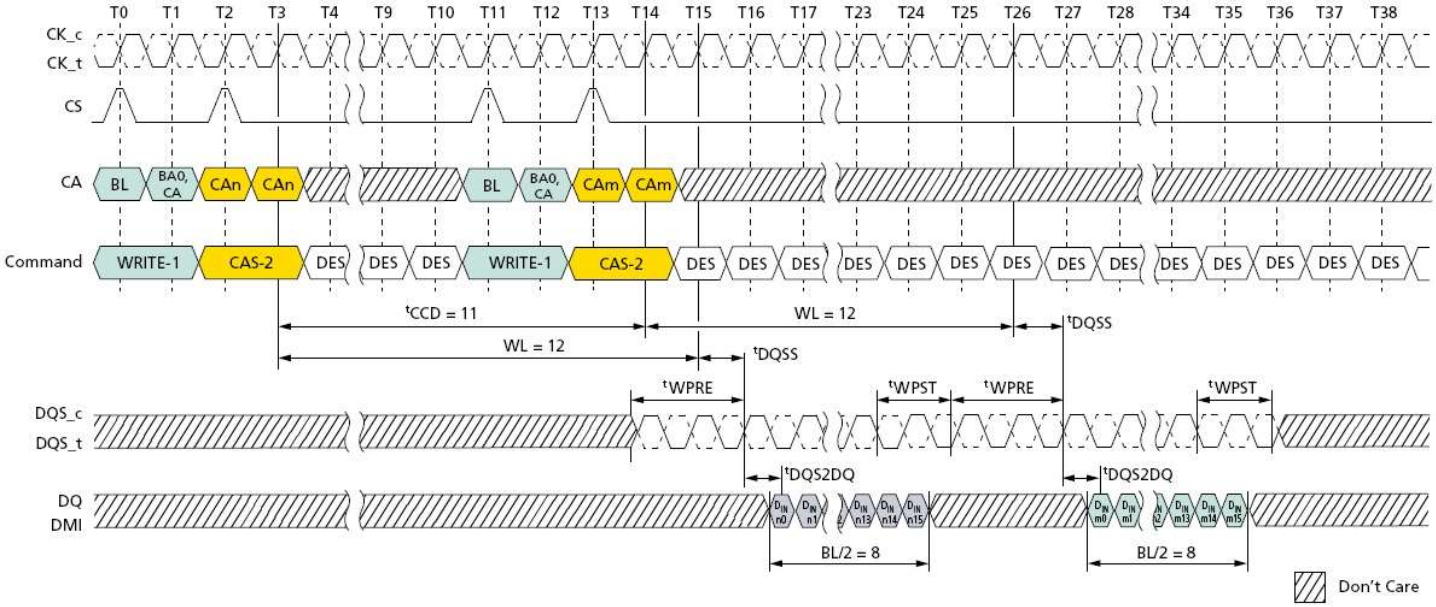
Figure 4-45: Consecutive WRITE: tCCD = MIN + 3, 0.5nCK Postamble



Notes:

1. BL = 16, Write postamble = 0.5nCK.
2. D_{IN} n/m = data-in from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid atthese times.

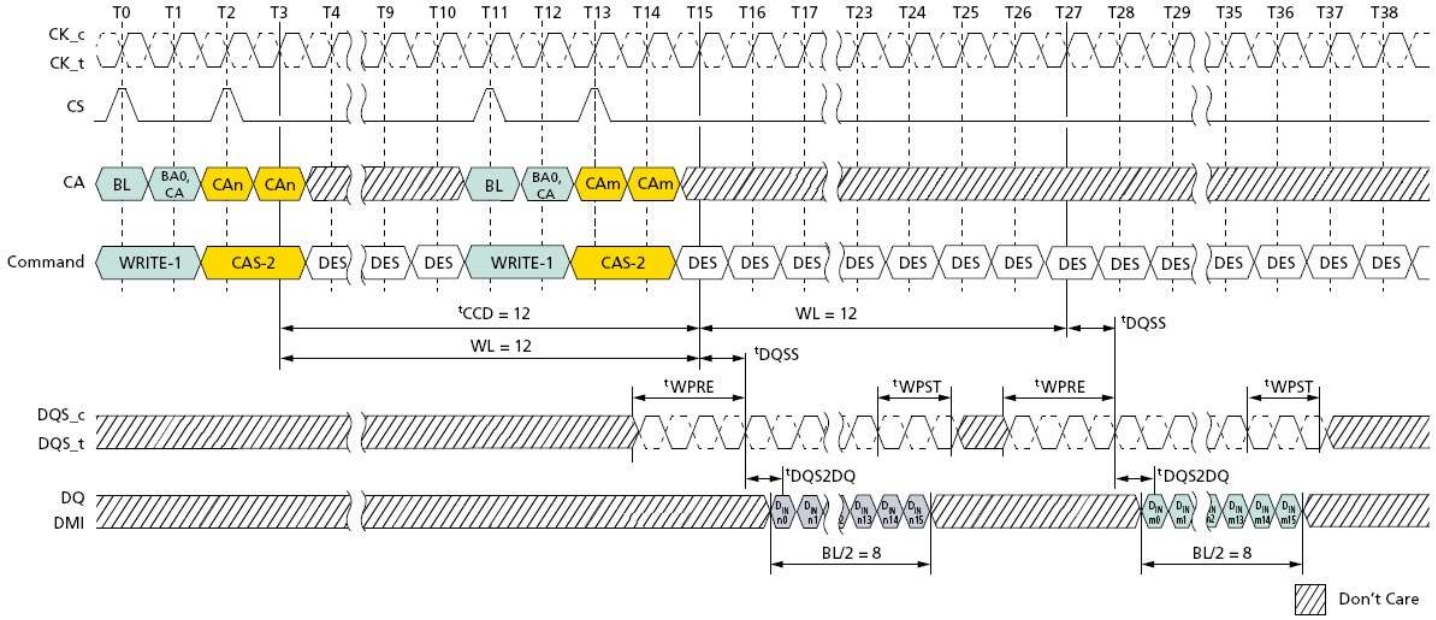
Figure 4-46: Consecutive WRITE: ^{t}CCD = MIN + 3, 1.5nCK Postamble



Notes:

1. BL = 16, Write postamble = 1.5nCK.
2. D_{IN} n/m = data-in from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid atthese times.

Figure 4-47: Consecutive WRITE: ^{t}CCD = MIN + 4, 1.5nCK Postamble



Notes:

1. BL = 16, Write postamble = 1.5nCK.
2. D_{IN} n/m = data-in from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid atthese times.

4.18 PRECHARGE Operation

The PRECHARGE command is used to precharge or close a bank that has been activated.The PRECHARGE command is initiated with CKE, CS, and CA[5:0] in the properstate (see Command Truth Table). The PRECHARGE command can be used to prechargeeach bank independently or all banks simultaneously. The all banks (AB) flagand the bank address bit are used to determine which bank(s) to precharge. The prechargedbank(s) will be available for subsequent row access ^{t}RPab after an all-bankPRECHARGE command is issued, or ^{t}RPpb after a single-bank PRECHARGE commandis issued.

To ensure that the device can meet the instantaneous current demands, the row prechargetime for an all-bank PRECHARGE (^{t}RPab) is longer than the per-bank prechargetime (^{t}RPpb).

Table 4-94: Precharge Bank Selection

AB (CA[5], R1)	BA2 (CA[2], R2)	BA1 (CA[1], R2)	BA0 (CA[0], R2)	Precharged Bank
0	0	0	0	Bank 0 only
0	0	0	1	Bank 1 only
0	0	1	0	Bank 2 only
0	0	1	1	Bank 3 only
0	1	0	0	Bank 4 only
0	1	0	1	Bank 5 only
0	1	1	0	Bank 6 only
0	1	1	1	Bank 7 only
1	Don't Care	Don't Care	Don't Care	All banks

Burst READ Operation Followed by Precharge

The PRECHARGE command can be issued as early as BL/2 clock cycles after a READcommand, but the PRECHARGE command cannot be issued until after ^{t}RAS is satisfied.A new bank ACTIVATE command can be issued to the same bank after the row prechargetime (^{t}RP) has elapsed. The minimum read-to-precharge time must also satisfy aminimum analog time from the second rising clock edge of the CAS-2 command. ^{t}RTPbegins BL/2 - 8 clock cycles after the READ command.

Figure 4-48: Burst READ Followed by Precharge – BL16, Toggling Preamble, 0.5nCK Postamble

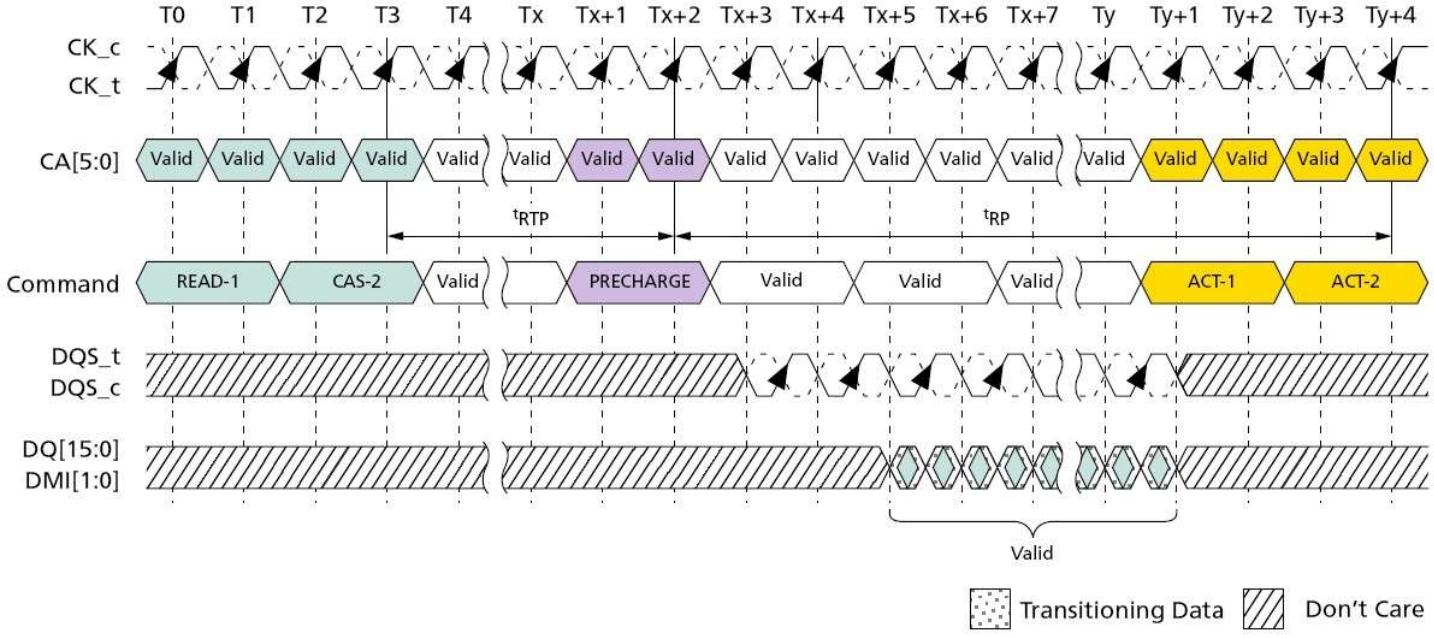
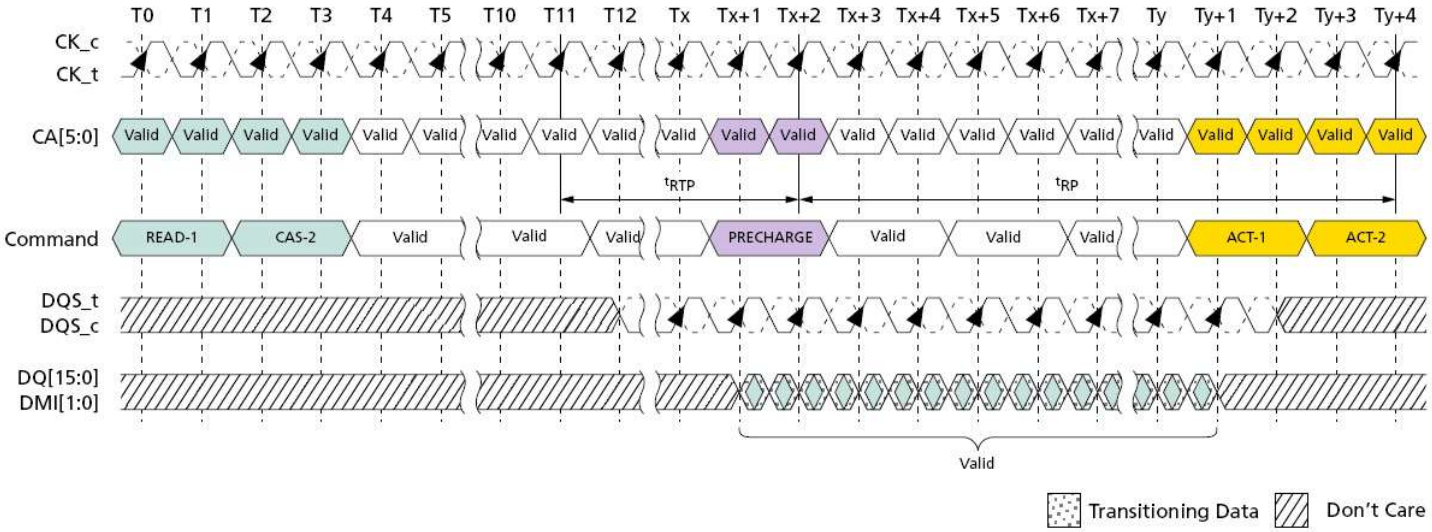


Figure 4-49: Burst READ Followed by Precharge – BL32, 2tCK, 0.5nCK Postamble

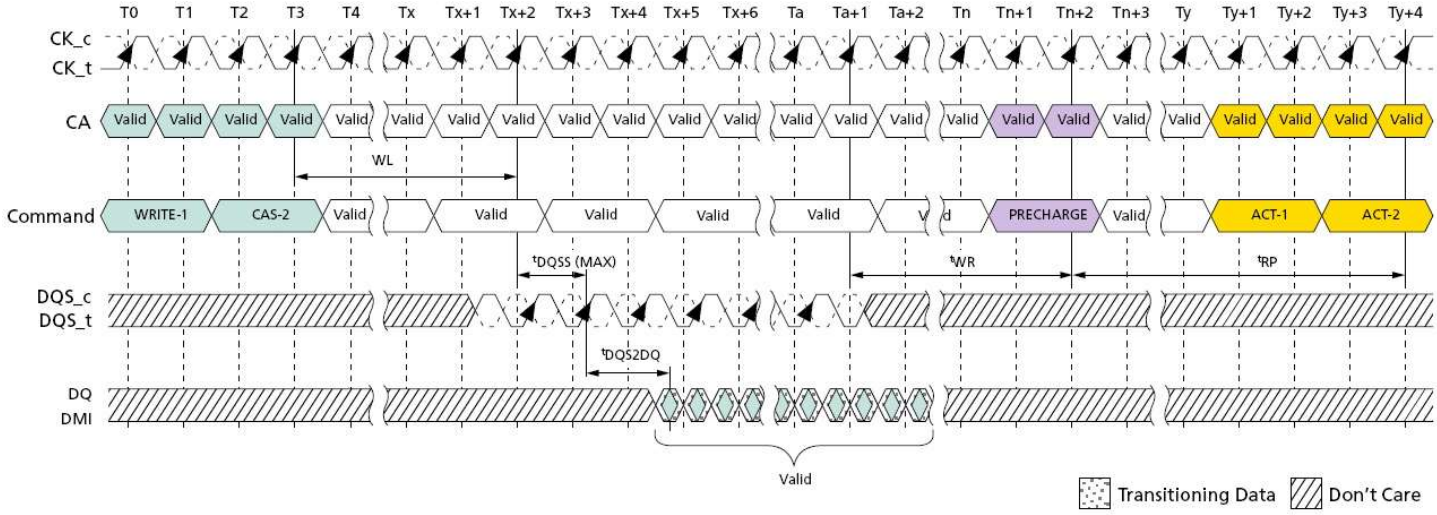


Burst WRITE Followed by Precharge

A write recovery time (^{t}WR) must be provided before a PRECHARGE command may beissued. This delay is referenced from the next rising edge of CK after the last valid DQSclock of the burst.

Devices write data to the memory array in prefetch multiples (prefetch = 16). An internalWRITE operation can only begin after a prefetch group has been clocked; therefore,^{t}WR starts at the prefetch boundaries. The minimum write-to-precharge time for commandsto the same bank is WL + BL/2 + 1 + RU(^{t}WR /^{t}CK) clock cycles.

Figure 4-50: Burst WRITE Followed by PRECHARGE – BL16, 2nCK Preamble, 0.5nCK Postamble



4.19 Auto Precharge

Before a new row can be opened in an active bank, the active bank must be prechargedusing either the PRECHARGE command or the auto precharge (AP) function. When aREAD or a WRITE command is issued to the device, the AP bit (CA5) can be set to enablethe active bank to automatically begin precharge at the earliest possible momentduring the burst READ or WRITE cycle.

If AP is LOW when the READ or WRITE command is issued, the normal READ or WRITEburst operation is executed, and the bank remains active at the completion of the burst.

If AP is HIGH when the READ or WRITE command is issued, the auto PRECHARGEfunction is engaged. This feature enables the PRECHARGE operation to be partially orcompletely hidden during burst READ cycles (dependent upon READ or WRITE latency),thus improving system performance for random data access.

Burst READ With Auto Precharge

If AP is HIGH when a READ command is issued, the READ with AUTO PRECHARGEfunction is engaged. The devices start an AUTO PRECHARGE operation on the risingedge of the clock at BL/2 after the second beat of the READ w/AP command, or BL/4 – 4+ RU (^{t}RTP/^{t}CK) clock cycles after the second beat of the READ w/AP command, whicheveris greater. Following an AUTO PRECHARGE operation, an ACTIVATE command canbe issued to the same bank if the following two conditions are both satisfied:

1. The RAS precharge time (^{t}RP) has been satisfied from the clock at which the autoprecharge began, and
2. The RAS cycle time (^{t}RC) from the previous bank activation has been satisfied.

Figure 4-51: Burst READ With Auto Precharge – BL16, Non-Toggling Preamble, 0.5nCK Postamble

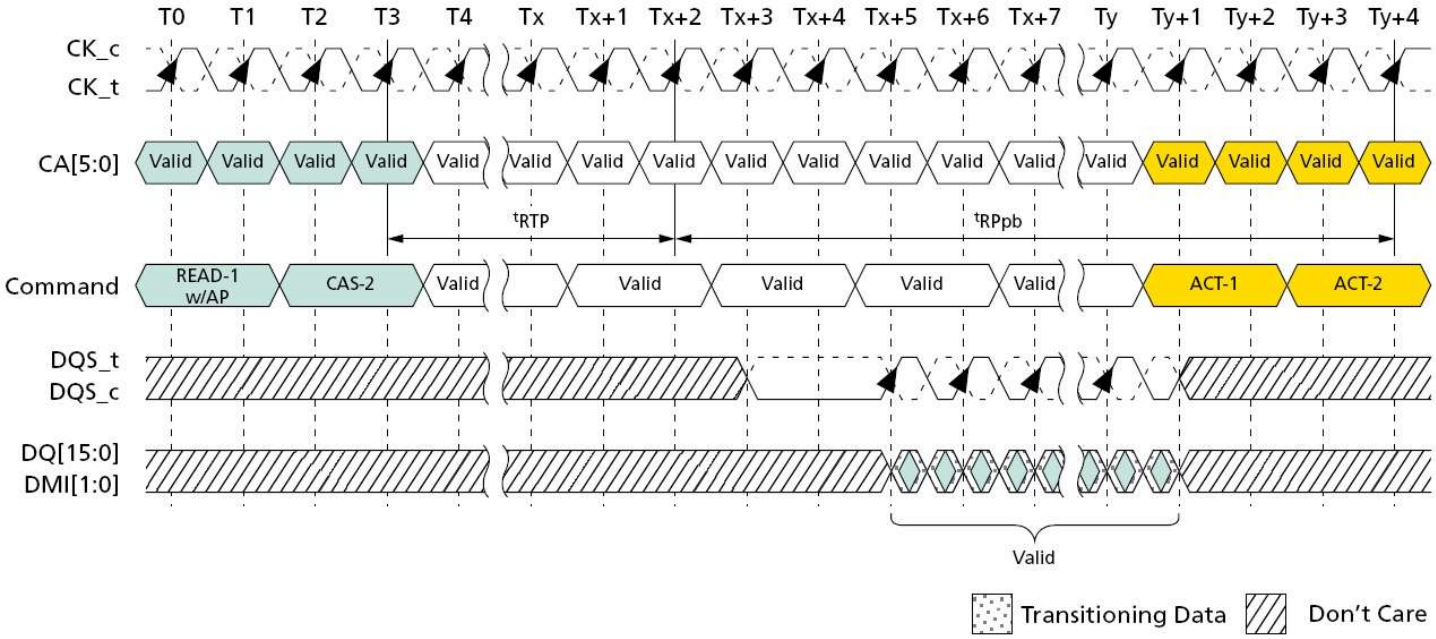
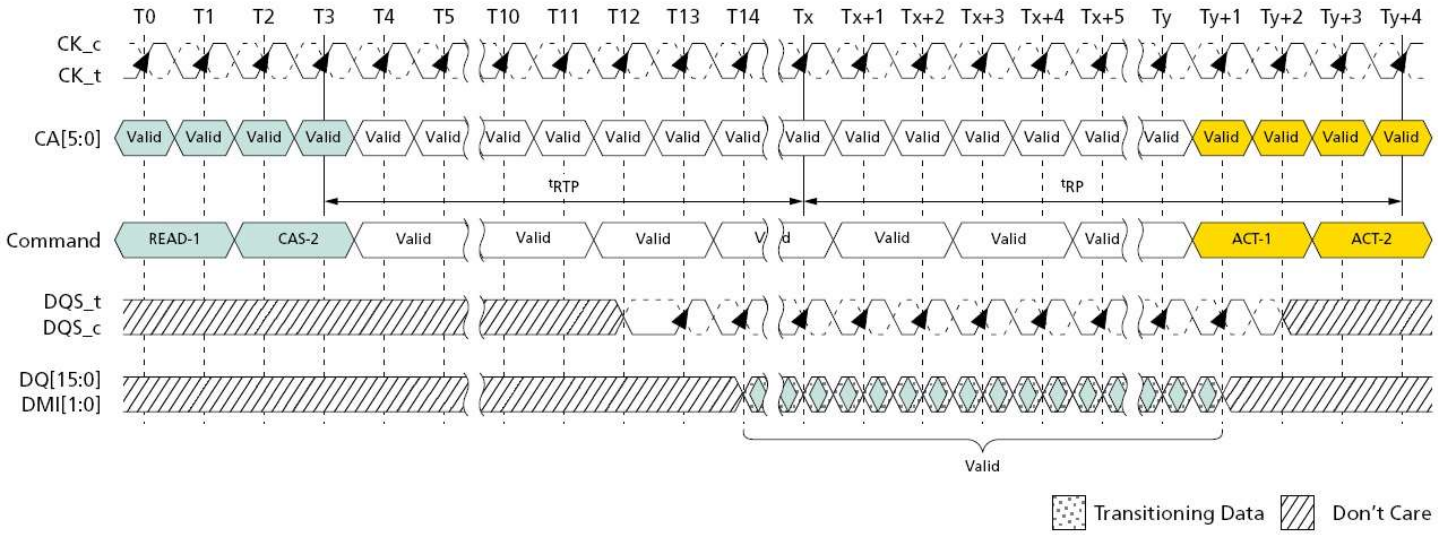


Figure 4-52: Burst READ With Auto Precharge – BL32, Toggling Preamble, 1.5nCK Postamble



Burst WRITE With Auto Precharge

If AP is HIGH when a WRITE command is issued, the WRITE with AUTO PRECHARGEfunction is engaged. The device starts an auto precharge on the rising edge ^{t}WR cyclesafter the completion of the burst WRITE.

Following a WRITE with AUTO PRECHARGE, an ACTIVATE command can be issued tothe same bank if the following conditions are met:

1. The RAS precharge time (^{t}RP) has been satisfied from the clock at which the autoprecharge began, and
2. The RAS cycle time (^{t}RC) from the previous bank activation has been satisfied.

Figure 4-53: Burst WRITE With Auto Precharge – BL16, 2nCK Preamble, 0.5nCK Postamble

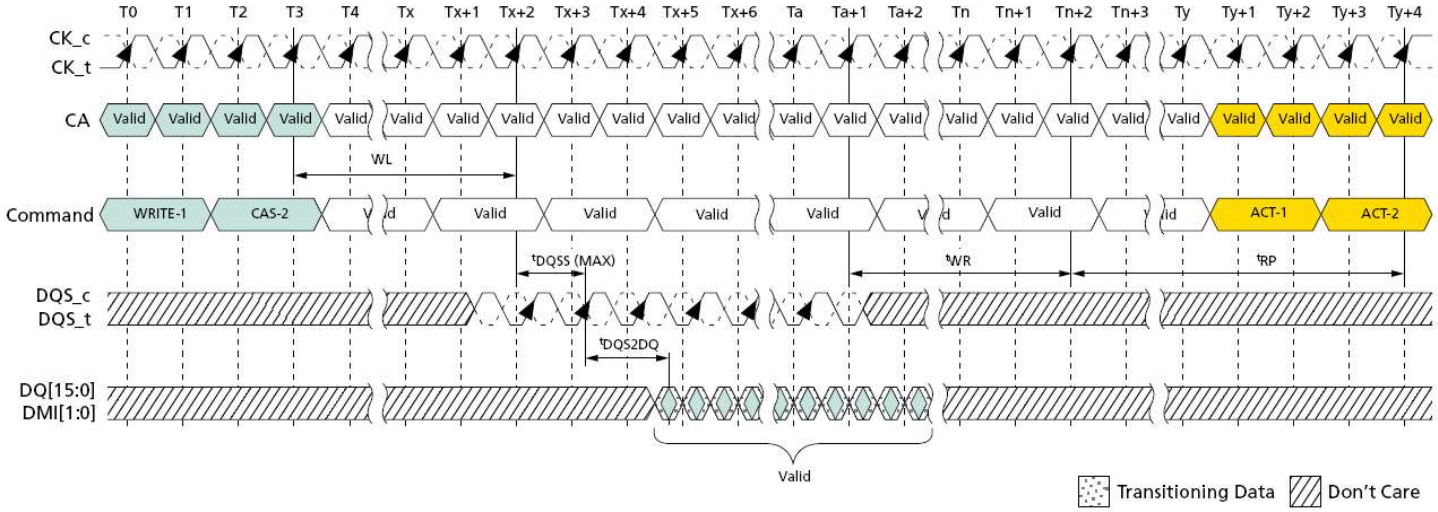


Table 4-95: Timing Between Commands (PRECHARGE and AUTO PRECHARGE): DQ ODT is Disable

From Command	To Command	Minimum Delay Between "From Command" and "To Command"	Unit	Notes
READ BL = 16	PRECHARGE (to same bank as READ)	^{t}RTP	^{t}CK	1, 6
	PRECHARGE ALL	^{t}RTP	^{t}CK	1, 6
READ BL = 32	PRECHARGE (to same bank as READ)	8^{t}CK + ^{t}RTP	^{t}CK	1, 6
	PRECHARGE ALL	8^{t}CK + ^{t}RTP	^{t}CK	1, 6
READ w/AP BL = 16	PRECHARGE (to same bank as READ w/AP)	*n*RTP	^{t}CK	1, 10
	PRECHARGE ALL	*n*RTP	^{t}CK	1, 10
	ACTIVATE (to same bank as READ w/AP)	*n*RTP + ^{t}RPpb	^{t}CK	1, 8, 10
	WRITE or WRITE w/AP (same bank)	Illegal	-	
	MASK-WR or MASK-WR w/AP (same bank)	Illegal	-	
	WRITE or WRITE w/AP (different bank)	RL + RU (^{t}DQSCK MAX/^{t}CK) + BL/2 + RD (^{t}RPST) - WL + ^{t}WPRE	^{t}CK	3, 4, 5
	MASK-WR or MASK-WR w/AP (different bank)	RL + RU (^{t}DQSCK MAX/^{t}CK) + BL/2 + RD (^{t}RPST) - WL + ^{t}WPRE	^{t}CK	3, 4, 5
	READ or READ w/AP (same bank)	Illegal	-	
	READ or READ w/AP (different bank)	BL/2	^{t}CK	3
READ w/AP BL = 32	PRECHARGE (to same bank as READ w/AP)	8^{t}CK + *n*RTP	^{t}CK	1, 10
	PRECHARGE ALL	8^{t}CK + *n*RTP	^{t}CK	1, 10
	ACTIVATE (to same bank as READ w/AP)	8^{t}CK + *n*RTP+ ^{t}RPpb	^{t}CK	1, 8, 10
	WRITE or WRITE w/AP (same bank)	Illegal	-	
	MASK-WR or MASK-WR w/AP (same bank)	Illegal	-	
	WRITE or WRITE w/AP (different bank)	RL + RU (^{t}DQSCK MAX/^{t}CK) + BL/2 + RD (^{t}RPST) - WL + ^{t}WPRE	^{t}CK	3, 4, 5
	MASK-WR or MASK-WR w/AP (different bank)	RL + RU (^{t}DQSCK MAX/^{t}CK) + BL/2 + RD (^{t}RPST) - WL + ^{t}WPRE	^{t}CK	3, 4, 5
	READ or READ w/AP (same bank)	Illegal	-	
	READ or READ w/AP (different bank)	BL/2	^{t}CK	3

Table 4-95: Timing Between Commands (PRECHARGE and AUTO PRECHARGE): DQ ODT is Disable (Continued)

From Command	To Command	Minimum Delay Between "From Command" and "To Command"	Unit	Notes
WRITE BL = 16 and 32	PRECHARGE (to same bank as WRITE)	WL + BL/2 + ^{t}WR + 1	^{t}CK	1, 7
	PRECHARGE ALL	WL + BL/2 + ^{t}WR + 1	^{t}CK	1, 7
MASK-WR BL = 16	PRECHARGE (to same bank as MASK-WR)	WL + BL/2 + ^{t}WR + 1	^{t}CK	1, 7
	PRECHARGE ALL	WL + BL/2 + ^{t}WR + 1	^{t}CK	1, 7
WRITE w/AP BL = 16 and 32	PRECHARGE (to same bank as WRITE w/AP)	WL + BL/2 + *n*WR + 1	^{t}CK	1, 11
	PRECHARGE ALL	WL + BL/2 + *n*WR + 1	^{t}CK	1, 11
	ACTIVATE (to same bank as WRITE w/AP)	WL + BL/2 + *n*WR + 1 + ^{t}RPpb	^{t}CK	1, 8, 11
	WRITE or WRITE w/AP (same bank)	Illegal	-	
	READ or READ w/AP (same bank)	Illegal	-	
	WRITE or WRITE w/AP (different bank)	BL/2	^{t}CK	3
	MASK-WR or MASK-WR w/AP (different bank)	BL/2	^{t}CK	3
	READ or READ w/AP (different bank)	WL + BL/2 + ^{t}WTR + 1	^{t}CK	3, 9
MASK-WR w/AP BL = 16	PRECHARGE (to same bank as MASK-WR w/AP)	WL + BL/2 + *n*WR +1	^{t}CK	1, 11
	PRECHARGE ALL	WL + BL/2 + *n*WR +1	^{t}CK	1, 11
	ACTIVATE (to same bank as MASK-WR w/AP)	WL + BL/2 + *n*WR +1 + ^{t}RPpb	^{t}CK	1, 8, 11
	WRITE or WRITE w/AP (same bank)	Illegal	-	3
	MASK-WR or MASK-WR w/AP (same bank)	Illegal	-	3
	WRITE or WRITE w/AP (different bank)	BL/2	^{t}CK	3
	MASK-WR or MASK-WR w/AP (different bank)	BL/2	^{t}CK	3
	READ or READ w/AP (same bank)	Illegal	-	3
	READ or READ w/AP (different bank)	WL + BL/2 + *n*WR +1	^{t}CK	3, 9
PRECHARGE	PRECHARGE (to same bank as PRECHARGE)	4	^{t}CK	1
	PRECHARGE ALL	4	^{t}CK	1
PRECHARGE ALL	PRECHARGE	4	^{t}CK	1
	PRECHARGE ALL	4	^{t}CK	1

Notes:

1. For a given bank, the precharge period should be counted from the latest PRECHARGEcommand, whether per-bank or all-bank, issued to that bank. The precharge period issatisfied tRP after that latest PRECHARGE command.
2. Any command issued during the minimum delay time as specified in the table above isillegal.
3. After READ w/AP, seamless READ operations to different banks are supported. AfterWRITE w/AP or MASK-WR w/AP, seamless WRITE operations to different banks are supported.READ, WRITE, and MASK-WR operations may not be truncated or interrupted.
4. ^{t}RPST values depend on MR1 OP[7] respectively.
5. ^{t}WPRE values depend on MR1 OP[2] respectively.
6. Minimum delay between "from command" and "to command" in clock cycle is calculatedby dividing tRTP (in ns) by ^{t}CK (in ns) and rounding up to the next integer: Minimumdelay [cycles] = roundup (^{t}RTP [ns]/^{t}CK [ns]).
7. Minimum delay between "from command" and "to command" in clock cycle is calculatedby dividing ^{t}WR (in ns) by ^{t}CK (in ns) and rounding up to the next integer: Minimumdelay [cycles] = roundup (WR [ns]/^{t}CK [ns]).
8. Minimum delay between "from command" and "to command" in clock cycle is calculatedby dividing ^{t}RPpb (in ns) by CK (in ns) and rounding up to the next integer: Minimumdelay [cycles] = roundup (^{t}RPpb [ns]/^{t}CK [ns]).
9. Minimum delay between "from command" and "to command" in clock cycle is calculatedby dividing ^{t}WTR (in ns) by ^{t}CK (in ns) and rounding up to the next integer: Minimumdelay [cycles] = roundup (^{t}WTR [ns]/^{t}CK [ns]).
10. For READ w/AP the value is nRTP, which is defined in mode register 2.
11. For WRITE w/AP the value is nWR, which is defined in mode register 1.

Table 4-96: Timing Between Commands (PRECHARGE and AUTO PRECHARGE): DQ ODT is Enable

From Command	To Command	Minimum Delay Between "From Command" and "To Command"	Unit	Notes
READ w/AP BL = 16	WRITE or WRITE w/AP (different bank)	RL + RU (^{t}DQSCK MAX/^{t}CK) + BL/2 + RD (^{t}RPST) - ODTLon - RD (^{t}ODTon MIN/^{t}CK) + 1	^{t}CK	2, 3
	MASK-WR or MASK-WR w/AP (different bank)	RL + RU (^{t}DQSCK MAX/^{t}CK) + BL/2 + RD (^{t}RPST) - ODTLon - RD (^{t}ODTon MIN/^{t}CK) + 1	^{t}CK	2, 3
READ w/AP BL = 32	WRITE or WRITE w/AP (different bank)	RL + RU (^{t}DQSCK MAX/^{t}CK) + BL/2 + RD (^{t}RPST) - ODTLon - RD (^{t}ODTon MIN/^{t}CK) + 1	^{t}CK	2, 3
	MASK-WR or MASK-WR w/AP (different bank)	RL + RU (^{t}DQSCK MAX/^{t}CK) + BL/2 + RD (^{t}RPST) - ODTLon - RD (^{t}ODTon MIN/^{t}CK) + 1	^{t}CK	2, 3

Notes:

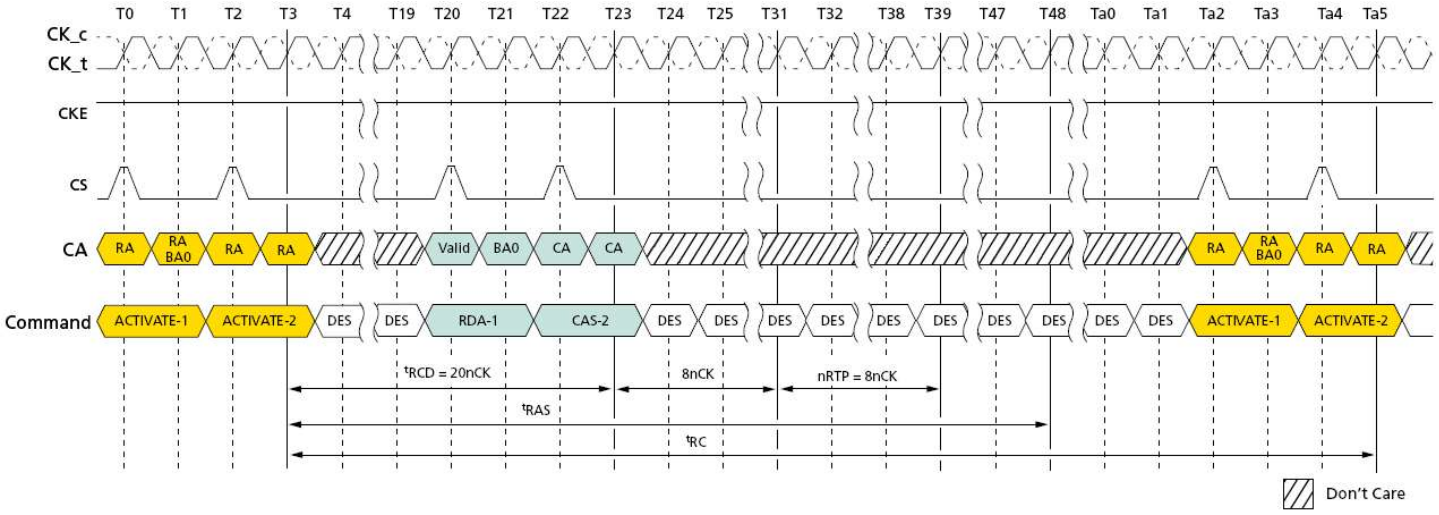
1. The rest of the timing about PRECHARGE and AUTO PRECHARGE is same as DQ ODT isdisable case.
2. After READ w/AP, seamless read operations to different banks are supported. READ,WRITE, and MASK-WR operations may not be truncated or interrupted.
3. ^{t}RPST values depend on MR1 OP[7] respectively.

RAS Lock Function

READ with AUTO PRECHARGE or WRITE/MASK WRITE with AUTO PRECHARGE commandsmay be issued after ^{t}RCD has been satisfied. The LPDDR4 SDRAM RAS lockoutfeature will schedule the internal precharge to assure that ^{t}RAS is satisfied. ^{t}RC needs tobe satisfied prior to issuing subsequent ACTIVATE commands to the same bank.

The figure below shows example of RAS lock function.

Figure 4-54: Command Input Timing with RAS Lock



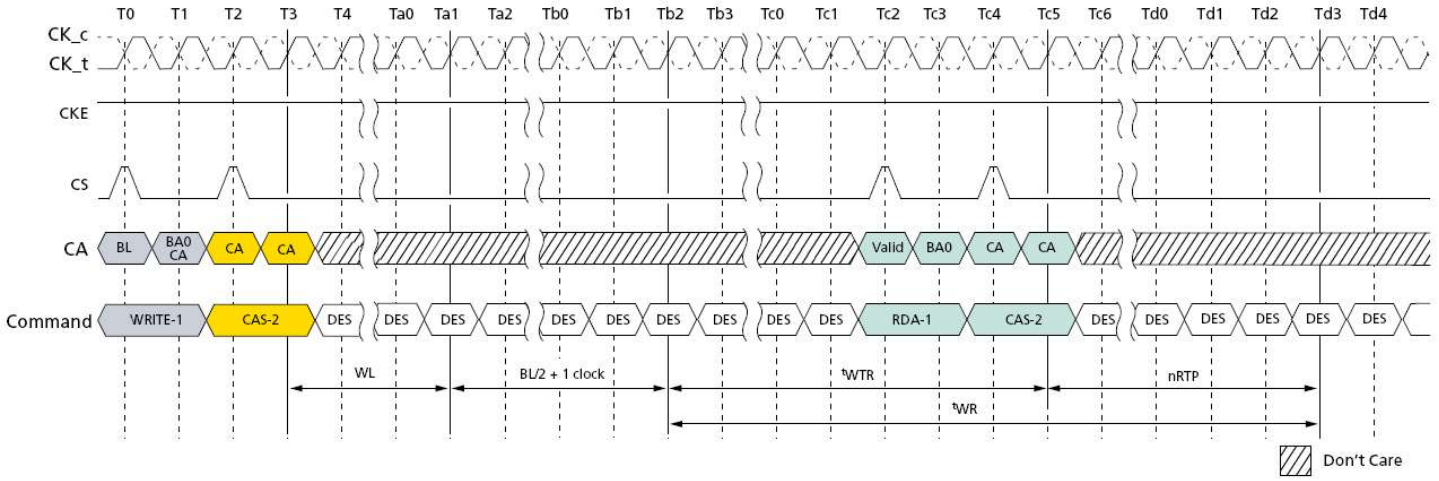
Notes:

1. ^{t}CK (AVG) = 0.938ns, Data rate = 2133 Mbps, ^{t}RCD (MIN) = MAX (18ns, 4nCK), ^{t}RAS (MIN)= MAX (42ns, 3nCK), nRTP = 8nCK, BL = 32.
2. ^{t}RCD = 20nCK comes from roundup (18ns/0.938ns).
3. DES commands are shown for ease of illustration; other commands may be valid atthese times.

Delay Time From WRITE-to-READ with Auto Precharge

In the case of WRITE command followed by READ with AUTO PRECHARGE, controllermust satisfy ^{t}WR for the WRITE command before initiating the device internal auto-precharge.It means that (^{t}WTR + nRTP) should be equal or longer than (^{t}WR) when BL settingis 16, as well as (^{t}WTR + nRTP + 8nCK) should be equal or longer than (^{t}WR) whenBL setting is 32. Refer to the following figure for details.

Figure 4-55: Delay Time From WRITE-to-READ with Auto Precharge



Notes:

1. Burst length at read = 16.
2. DES commands are shown for ease of illustration; other commands may be valid atthese times.

4.20 REFRESH Command

The REFRESH command is initiated with CS HIGH, CA0 LOW, CA1 LOW, CA2 LOW, CA3HIGH and CA4 LOW at the first rising edge of clock. Per bank REFRESH is initiated withCA5 LOW at the first rising edge of the clock. The all-bank REFRESH is initiated withCA5 HIGH at the first rising edge of clock.

A per bank REFRESH command (REFpb) is performed to the bank address as transferredon CA0, CA1, and CA2 on the second rising edge of the clock. Bank address BA0 istransferred on CA0, bank address BA1 is transferred on CA1, and bank address BA2 istransferred on CA2. A per bank REFRESH command (REFpb) to the eight banks can beissued in any order. For example, REFpb commands may be issued in the following order:1-3-0-2-4-7-5-6. After the eight banks have been refreshed using the per bank REFRESHcommand, the controller can send another set of per bank REFRESH commandsin the same order or a different order. One possible order can be a sequential roundrobin: 0-1-2-3-4-5-6-7. It is illegal to send a per bank REFRESH command to the samebank unless all eight banks have been refreshed using the per bank REFRESH command.The count of eight REFpb commands starts with the first REFpb command aftera synchronization event.

The bank count is synchronized between the controller and the device by resetting thebank count to zero. Synchronization can occur upon reset procedure or at every exitfrom self refresh. The REFab command also synchronizes the counter between the controllerand the device to zero. The device can be placed in self refresh, or a REFab commandcan be issued at any time without cycling through all eight banks using per bankREFRESH command. After the bank count is synchronized to zero, the controller canissue per bank REFRESH commands in any order, as described above.

A REFab command issued when the bank counter is not zero will reset the bank counterto zero and the device will perform refreshes to all banks as indicated by the row counter.If another REFRESH command (REFab or REFpb) is issued after the REFab commandthen it uses an incremented value of the row counter.
The table below shows examples of both bank and refresh counter increment behavior.

Table 4-97: Bank and Refresh Counter Increment Behavior

#	Command	BA0	BA1	BA2	Refresh Bank #	Bank Counter #	Ref. Conter # (Row Address #)
0	Reset, SRX, or REFab					To 0	–
1	REFpb	0	0	0	0	0 to 1	n
2	REFpb	0	0	1	1	1 to 2	
3	REFpb	0	1	0	2	2 to 3	
4	REFpb	0	1	1	3	3 to 4	
5	REFpb	1	0	0	4	4 to 5	
6	REFpb	1	0	1	5	5 to 6	
7	REFpb	1	1	0	6	6 to 7	
8	REFpb	1	1	1	7	7 to 0	
9	REFpb	1	1	0	6	0 to 1	n + 1
10	REFpb	1	1	1	7	1 to 2	
11	REFpb	0	0	1	1	2 to 3	
12	REFpb	0	1	1	3	3 to 4	
13	REFpb	1	0	1	5	4 to 5	
14	REFpb	1	1	0	2	5 to 6	
15	REFpb	1	0	0	0	6 to 7	
16	REFpb	1	0	0	4	7 to 0	
17	REFpb	0	0	0	0	0 to 1	n + 2
18	REFpb	0	0	1	1	1 to 2	
19	REFpb	0	1	0	2	2 to 3	
20	**REFpb**	**V**	**V**	**V**	**0 to 7**	**To 0**	**n + 2**
21	REFpb	1	1	0	6	0 to 1	n + 3
22	REFpb	1	1	1	7	1 to 2	
Snip							

A bank must be idle before it can be refreshed. The controller must track the bank beingrefreshed by the per bank REFRESH command.

The REFpb command must not be issued to the device until the following conditionshave been met:
- ^{t}RFCab has been satisfied after the prior REFab command
- ^{t}RFCpb has been satisfied after the prior REFpb command
- ^{t}RP has been satisfied after the prior PRECHARGE command to that bank
- ^{t}RRD has been satisfied after the prior ACTIVATE command (for example, after activatinga row in a different bank than the one affected by the REFpb command)

The target bank is inaccessible during per bank REFRESH cycle time (^{t}RFCpb). However,other banks within the device are accessible and can be addressed during the cycle.During the REFpb operation, any of the banks other than the one being refreshed canbe maintained in an active state or accessed by a READ or a WRITE command. Whenthe per bank REFRESH cycle has completed, the affected bank will be in the idle state.

After issuing REFpb, the following conditions must be met:
- ^{t}RFCpb must be satisfied before issuing a REFab command
- ^{t}RFCpb must be satisfied before issuing an ACTIVATE command to the same bank
- ^{t}RRD must be satisfied before issuing an ACTIVATE command to a different bank
- ^{t}RFCpb must be satisfied before issuing another REFpb command

An all-bank REFRESH command (REFab) issues a REFRESH command to every bank ina channel. All banks must be idle when REFab is issued (for example, by issuing a PRECHARGEALL command prior to issuing an all-bank REFRESH command). The REFabcommand must not be issued to the device until the following conditions have beenmet:
- ^{t}RFCab has been satisfied following the prior REFab command
- ^{t}RFCpb has been satisfied following the prior REFpb command
- ^{t}RP has been satisfied following the prior PRECHARGE command

When an all-bank REFRESH cycle has completed, all banks will be idle. After issuing REFab:
- RFCab latency must be satisfied before issuing an ACTIVATE command,
- RFCab latency must be satisfied before issuing a REFab or REFpb command

Table 4-98: REFRESH Command Timing Constraints

Symbol	Minimum Delay From…	To	Notes
^{t}RFCab	REFab	REFab	
		ACTIVATE command to any bank	
		REFab	
^{t}RFCpb	REFab	REFab	
		ACTIVATE command to same bank as REFpb	
		REFab	
^{t}RRD	REFpb	ACTIVATE command to a different bank than REFpb	
	ACTIVATE	REFab	1
		ACTIVATE command to a different bank than the prior ACTIVATE command	

Note:
1. A bank must be in the idle state before it is refreshed; therefore, REFab is prohibitedfollowing an ACTIVATE command. REFpb is supported only if it affects a bank that is inthe idle state.

Figure 4-56: All-Bank REFRESH Operation

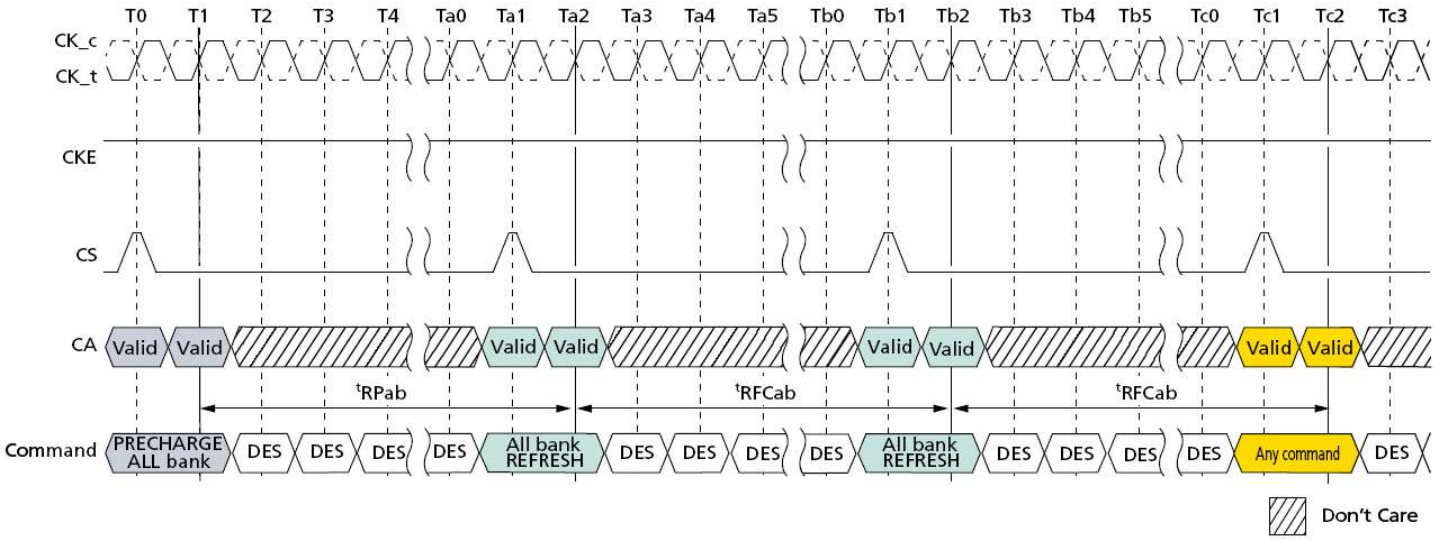
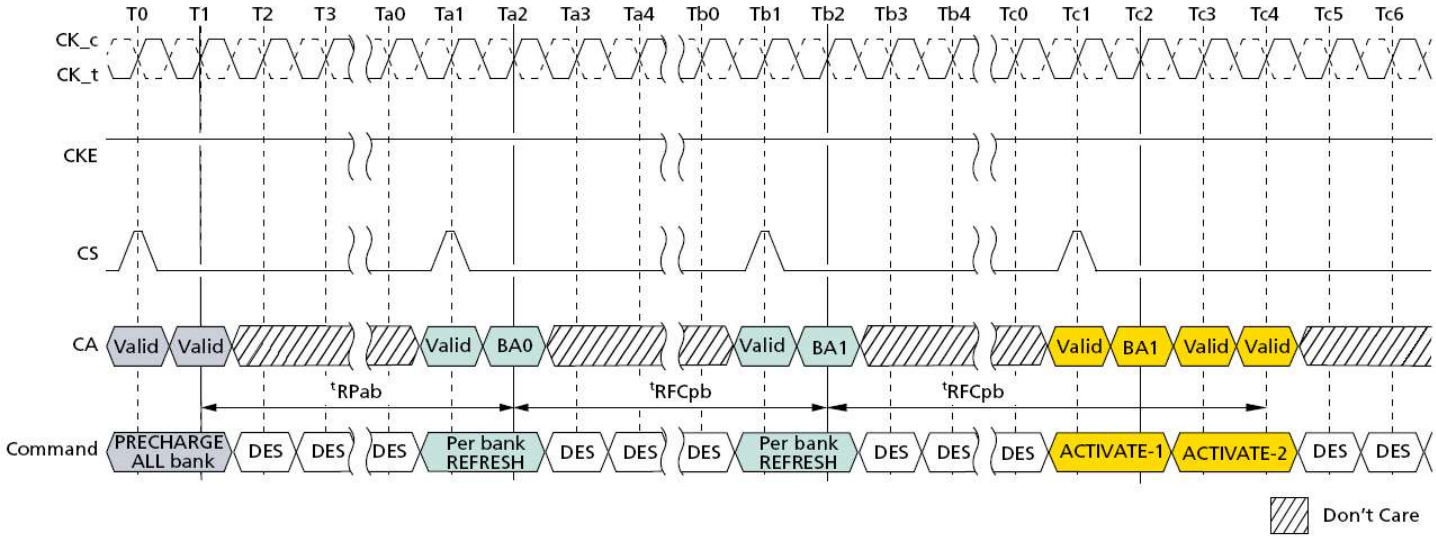


Figure 4-57: Per Bank REFRESH Operation



Notes:

1. In the beginning of this example, the REFpb bank is pointing to bank 0.
2. Operations to banks other than the bank being refreshed are supported during the^{t}RFCpb period.

In general, a REFRESH command needs to be issued to the device regularly every ^{t}REFIinterval. To allow for improved efficiency in scheduling and switching between tasks,some flexibility in the absolute refresh interval is provided. A maximum of eight REFRESHcommands can be postponed during operation of the device, but at no point intime are more than a total of eight REFRESH commands allowed to be postponed. Anda maximum number of pulled-in or postponed REF command is dependent on refreshrate. It is described in the table below. In the case where eight REFRESH commands arepostponed in a row, the resulting maximum interval between the surrounding REFRESHcommands is limited to 9 × tREFI. A maximum of eight additional REFRESHcommands can be issued in advance (pulled in), with each one reducing the number ofregular REFRESH commands required later by one. Note that pulling in more than eightREFRESH commands in advance does not reduce the number of regular REFRESHcommands required later; therefore, the resulting maximum interval between two surroundingREFRESH commands is limited to 9 ×^{t}REFI. At any given time, a maximum of16 REFRESH commands can be issued within 2 ×^{t}REFI.

Self refresh mode may be entered with a maximum of eight REFRESH commands beingpostponed. After exiting self refresh mode with one or more REFRESH commands postponed,additional REFRESH commands may be

postponed to the extent that the totalnumber of postponed REFRESH commands (before and after self refresh) will never exceedeight. During self refresh mode, the number of postponed or pulled-in REFRESHcommands does not change.

And for per bank refresh, a maximum of 8 x 8 per bank REFRESH commands can bepostponed or pulled in for scheduling efficiency. At any given time, a maximum of 2 x 8x 8 per bank REFRESH commands can be issued within 2 x ^{t}REFI.

Table 4-99: Legacy REFRESH Command Timing Constraints

MR4 OP[2:0]	Refresh Rate	Max. No. of pulled-in or postponed REFab	Max. Interval between Two REFab	Max. No. of REFab[1]	Per Bank Refresh
000b	Low Temp. Limit	N/A	N/A	N/A	N/A
001b	4 × ^{t}REFI	8	9 × 4 × ^{t}REFI	16	1/8 of REFab
010b	2 × ^{t}REFI	8	9 × 2 × ^{t}REFI	16	1/8 of REFab
011b	1 × ^{t}REFI	8	9 × ^{t}REFI	16	1/8 of REFab
100b	0.5 × ^{t}REFI	8	9 × 0.5 × ^{t}REFI	16	1/8 of REFab
101b	0.25 × ^{t}REFI	8	9 × 0.25 × ^{t}REFI	16	1/8 of REFab
110b	0.25 × ^{t}REFI	8	9 × 0.25 × ^{t}REFI	16	1/8 of REFab
111b	High Temp. Limit	N/A	N/A	N/A	N/A

Note:

1. Maximum number of REFab within MAX(2 ×^{t}REFI × refresh rate multiplier, 16 ×^{t}RFC).

Table 4-100: Modified REFRESH Command Timing Constraints

MR4 OP[2:0]	Refresh Rate	Max. No. of pulled-in or postponed REFab	Max. Interval between Two REFab	Max. No. of REFab[1]	Per Bank Refresh
000B	Low Temp. Limit	N/A	N/A	N/A	N/A
001B	4 × ^{t}REFI	2	3 × 4 × ^{t}REFI	4	1/8 of REFab
010B	2 × ^{t}REFI	4	5 × 2 × ^{t}REFI	8	1/8 of REFab
011B	1 × ^{t}REFI	8	9 × ^{t}REFI	16	1/8 of REFab
100B	0.5 × ^{t}REFI	8	9 × 0.5 × ^{t}REFI	16	1/8 of REFab
101B	0.25 × ^{t}REFI	8	9 × 0.25 × ^{t}REFI	16	1/8 of REFab
110B	0.25 × ^{t}REFI	8	9 × 0.25 × ^{t}REFI	16	1/8 of REFab
111B	High Temp. Limit	N/A	N/A	N/A	N/A

Notes:

1. For any thermal transition phase where refresh mode is transitioned to either 2 ×^{t}REFIor 4 ×^{t}REFI, LPDDR4 devices willsupport the previous postponed refresh requirementprovided the number of postponed refreshes is monotonically reduced to meet the newrequirement. However, the pulled-in REFRESH commands in previous thermal phase arenot applied in new thermal phase. Entering new thermal phase the controller mustcount the number of pulled-in REFRESH commands as zero, regardless of the number of remaining pulled-in REFRESH commands in the previous thermal phase.
2. LPDDR4 devices are refreshed properly if memory controller issues REFRESH commandswith same or shorter refresh period than reported by MR4 OP[2:0]. If a shorter refresh periodis applied, the corresponding requirements from this Table apply. For example, whenMR4 OP[2:0] = 001b, controller can be in any refresh rate from 4 ×^{t}REFI to 0.25 ×^{t}REFI.When MR4 OP[2:0] = 010b, the only prohibited refresh rate is 4 ×^{t}REFI.

Figure 4-58: Postponing REFRESH Commands (Example)

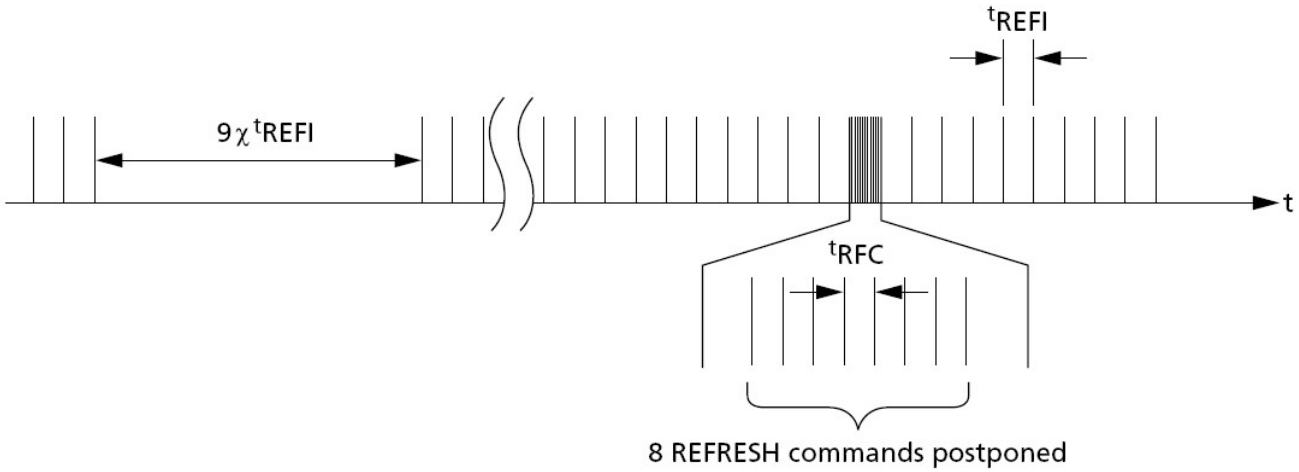
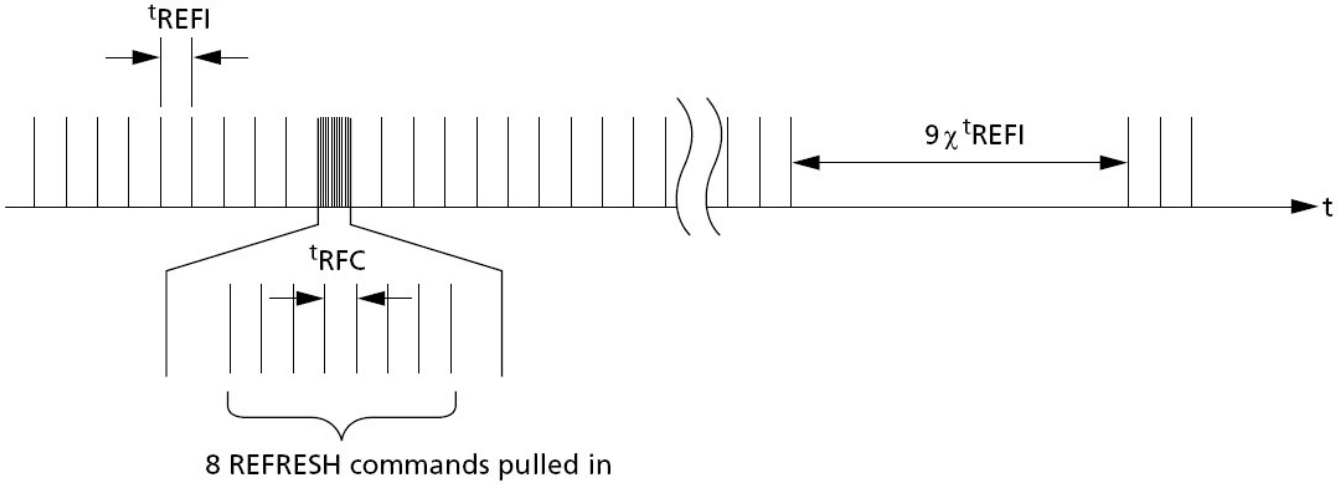


Figure 4-59: Pulling In REFRESH Commands (Example)



4.21 Refresh Requirement

Between the SRX command and SRE command, at least one extra REFRESH commandis required. After the SELF REFRESH EXIT command, in addition to the normal REFRESHcommand at tREFI interval, the device requires a minimum of one extra REFRESHcommand prior to the SELF REFRESH ENTRY command.

Table 4-101: Refresh Requirement Parameters

Parameter		Symbol	Density (per channel)					Unit
			4Gb	6Gb	8Gb	12Gb	16Gb	
Number of banks per channel		–	8					–
Refresh window (tREFW): (1 × Refresh)[3]		tREFW	32					ms
Required number of REFRESH commands in tREFW window		R	8192					–
Average refresh interval (1 × Refresh)[3]	REFab	tREFI	3904					µs
	REFpb	tREFIpb	488					ns
REFRESH cycle time (all banks)		tRFCab	180	280		380		ns
REFRESH cycle time (per bank)		tRFCpb	90	140		190		ns
Per bank refresh to per bank refresh time (different bank)		tPBR2PBR	90	90		90		ns

Notes:

1. Refresh for each channel is independent of the other channel on the die, or other channelsin a package. Power delivery in the user′ s system should be verified to make surethe DC operating conditions are maintained when multiple channels are refreshed simultaneously.
2. Self refresh abort feature is available for higher density devices starting with 6Gb densityper channel device and tXSR_abort(MIN) is defined as tRFCpb + 17.5ns.
3. Refer to MR4 OP[2:0] for detailed refresh rate and its multipliers.

4.22 SELF REFRESH Operation

Self Refresh Entry and Exit

The SELF REFRESH command can be used to retain data in the device without externalREFRESH commands. The device has a built-in timer to accommodate SELF REFRESHoperation. Self refresh is entered by the SELF REFRESH ENTRY command defined byhaving CS HIGH, CA0 LOW, CA1 LOW, CA2 LOW, CA3 HIGH, CA4 HIGH, and CA5 valid(valid meaning that it is at a logic level HIGH or LOW) for the first rising edge, and CSLOW, CA0 valid, CA1 valid, CA2 valid, CA3 valid, CA4 valid, and CA5 valid at the secondrising edge of clock. The SELF REFRESH command is only allowed when READ DATAburst is completed and the device is in the idle state.

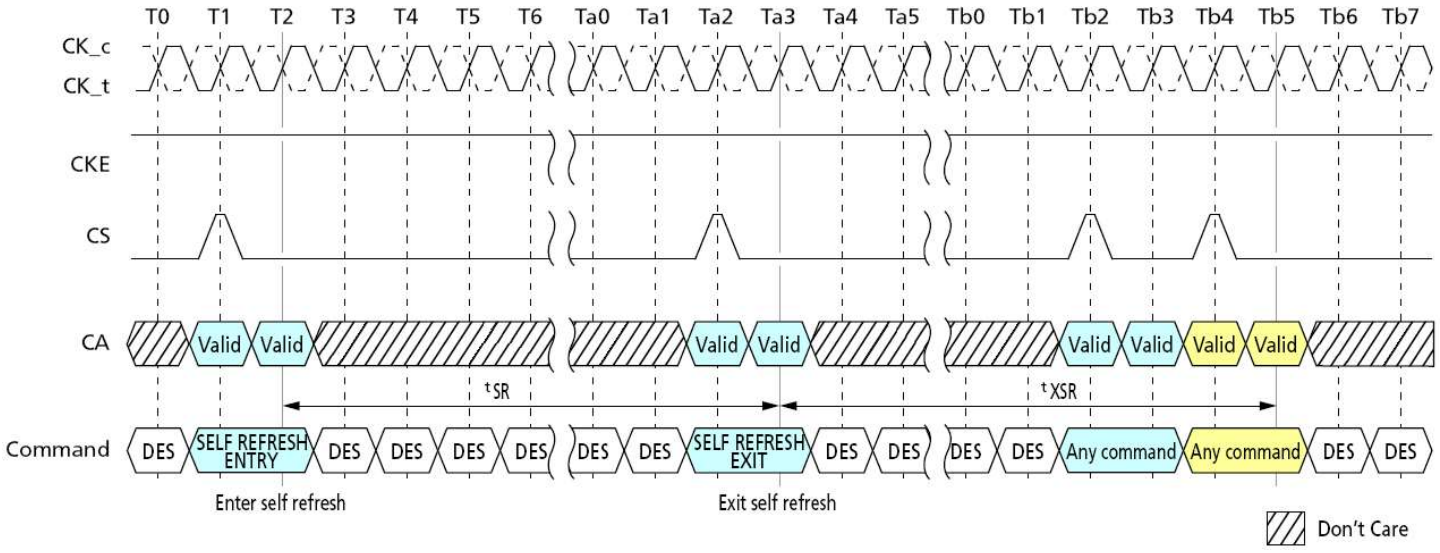
During self refresh mode, external clock input is needed and all input pins of the deviceare activated. The device can accept the following commands: MRR-1, CAS-2, DES, SRX,MPC, MRW-1, and MRW-2, except PASR bank/segment settingand SR abort setting.

The device can operate in self refresh mode within the standard and elevated temperatureranges. It also manages self refresh power consumption when the operating temperaturechanges: lower at low temperatures and higher at high temperatures.

For proper SELF REFRESH operation, power supply pins (V_{DD1}, V_{DD2}, and V_{DDQ}) mustbe at valid levels. V_{DDQ} can be turned off during self refresh with power-down after ^{t}CKELCK is satisfied. (Refer to the Self Refresh Entry/Exit Timing with Power-Down Entry/Exit figure.) Prior to exiting self refresh with power-down, V_{DDQ} must be withinspecified limits. The minimum time that the device must remain in self refresh mode is ^{t}SR (MIN). After self refresh exit is registered, only MRR-1, CAS-2, DES, MPC, MRW-1,and MRW-2 except PASR bank/segment mask settingand SR abort setting are allowed until ^{t}XSR is satisfied.

The use of self refresh mode introduces the possibility that an internally timed refreshevent can be missed when self refresh exit is registered. Upon exit from self refresh, it isrequired that at least one REFRESH command (8 per-bank or 1 all-bank) is issued beforeentry into a subsequent self refresh. This REFRESH command is not included in thecount of regular REFRESH commands required by the ^{t}REFI interval, and does notmodify the postponed or pulled-in refresh counts; the REFRESH command does counttoward the maximum refreshes permitted within 2 × ^{t}REFI.

Figure 4-60: Self Refresh Entry/Exit Timing



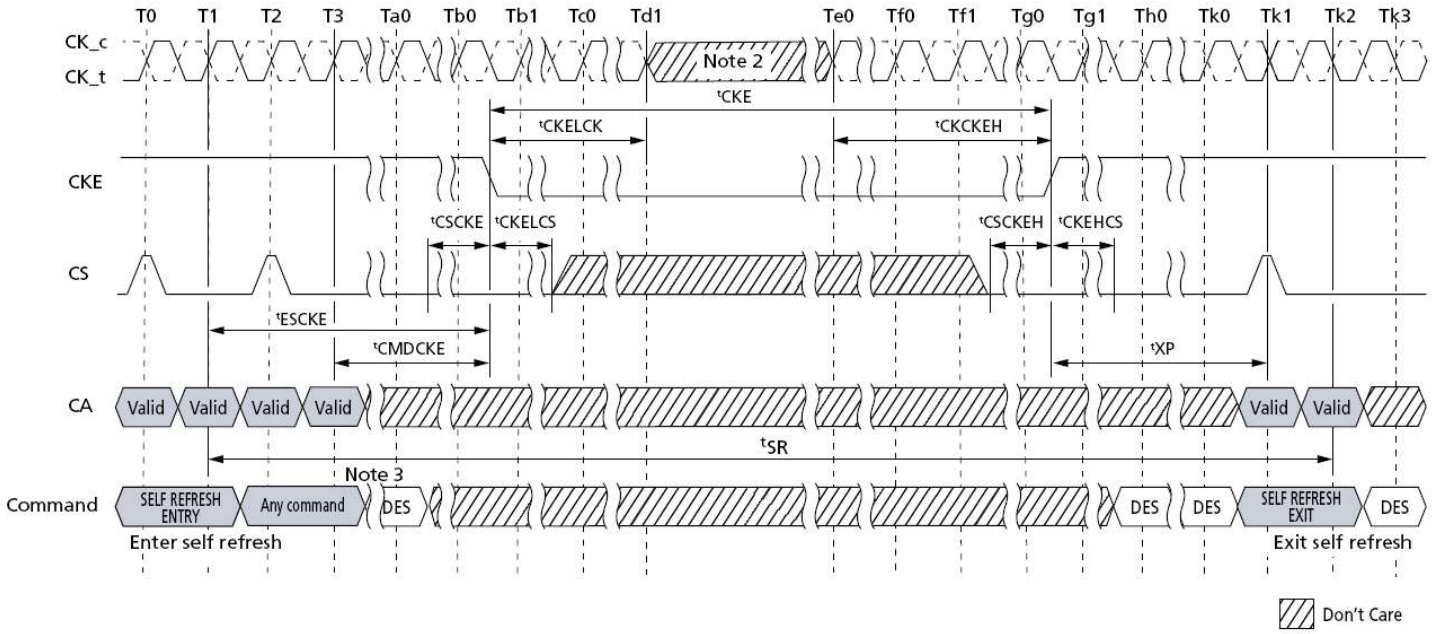
Notes:

1. MRR-1, CAS-2, DES, SRX, MPC, MRW-1, and MRW-2 commands (except PASR bank/segment setting) are allowed during self refresh.
2. DES commands are shown for ease of illustration; other commands may be valid atthese times.

Power-Down Entry and Exit During Self Refresh

Entering/exiting power-down mode is allowed during self refresh mode. The relatedtiming parameters between self refresh entry/exit and power-down entry/exit areshown below.

Figure 4-61: Self Refresh Entry/Exit Timing with Power-Down Entry/Exit



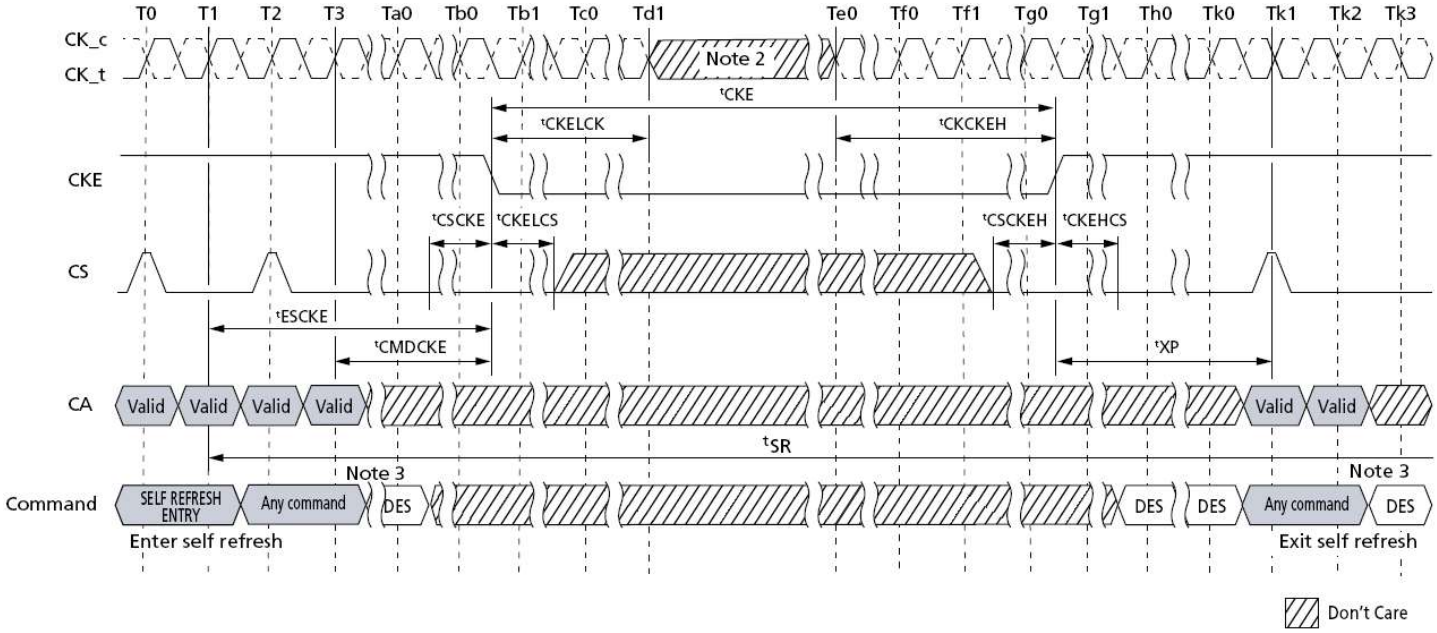
Notes:

1. MRR-1, CAS-2, DES, SRX, MPC, MRW-1, and MRW-2 commands (except PASR bank/segment mask setting and SR abort setting) are allowed during self refresh.
2. Input clock frequency can be changed, or the input clock can be stopped, or floated after ^{t}CKELCK satisfied and during power-down, provided that upon exiting power-down,the clock is stable and within specified limits for a minimum of ^{t}CKCKEH of stable clockprior to power-down exit and the clock frequency is between the minimum and maximumspecified frequency for the speed grade in use.
3. Two clock command for example.

Command Input Timing After Power-Down Exit

Command input timings after power-down exit during self refresh mode are shown below.

Figure 4-62: Command Input Timings after Power-Down Exit During Self Refresh



Notes:

1. MRR-1, CAS-2, DES, SRX, MPC, MRW-1, and MRW-2 commands (except PASR bank/segment setting) are allowed during self refresh.
2. Input clock frequency can be changed or the input clock can be stopped or floated after^{t}CKELCK satisfied and during power-down, provided that upon exiting power-down, theclock is stable and within specified limits for a minimum of ^{t}CKCKEH of stable clock priorto power-down exit and the clock frequency is between the minimum and maximumspecified frequency for the speed grade in use.
3. Two clock command for example.

Self Refresh Abort

If MR4 OP[3] is enabled, the device aborts any ongoing refresh during self refresh exitand does not increment the internal refresh counter. The controller can issue a validcommand after a delay of ^{t}XSR_abort instead of ^{t}XSR.

The value of ^{t}XSR_abort (MIN) is defined as ^{t}RFCpb + 17.5ns.

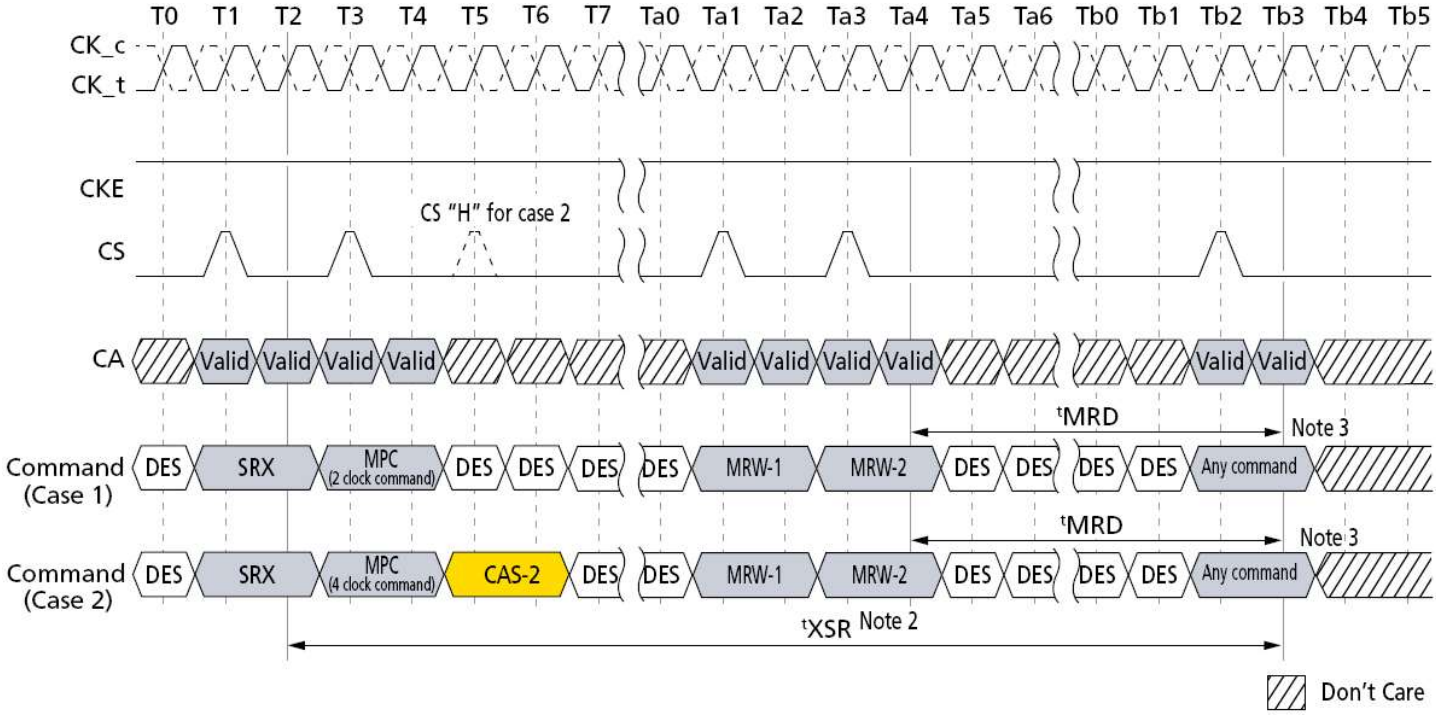
Upon exit from self refresh mode, the device requires a minimum of one extra refresh(eight per bank or one for the entire bank) before entering a subsequent self refreshmode. This requirement remains the same irrespective of the setting of the MR bit forself refresh abort.

Self refresh abort feature is valid for 6Gb density per channel and larger densities only.

MRR, MRW, MPC Commands During ^{t}XSR, ^{t}RFC

MODE REGISTER READ (MRR) command, MODE REGISTER WRITE (MRW) commandand MULTI PURPOSE command except PASR bank/segment mask setting and SR abort setting can be issued during ^{t}XSR period.

Figure 4-63: MRR, MRW, and MPC Commands Issuing Timing During ^{t}XSR

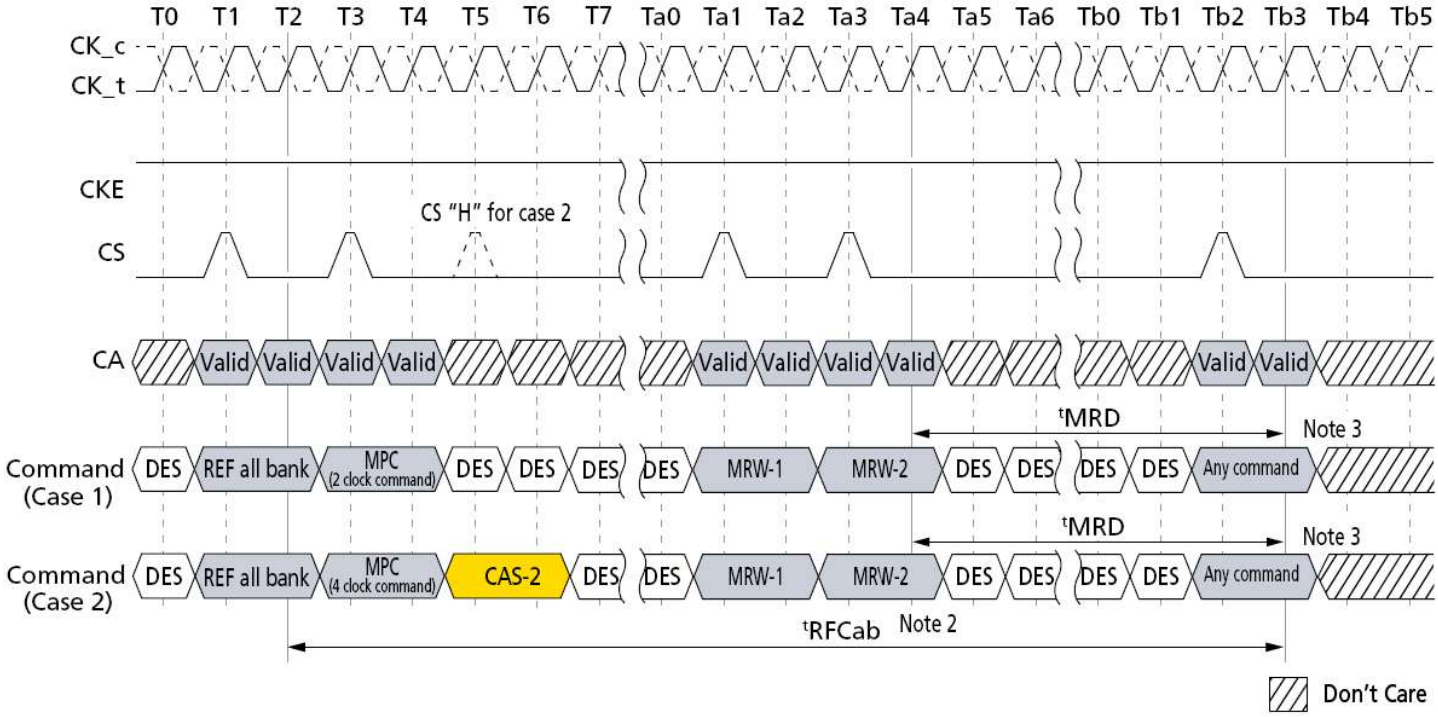


Notes:

1. MPC and MRW commands are shown. Any combination of MRR, MRW, and MPC is allowedduring ^{t}XSR period.
2. "Any command" includes MRR, MRW, and all MPC commands.

MRR, MRW, and MPC can be issued during ^{t}RFC period.

Figure 4-64: MRR, MRW, and MPC Commands Issuing Timing During tRFC



Notes:

1. MPC and MRW commands are shown. Any combination of MRR, MRW, and MPC is allowedduring ^{t}RFCab or ^{t}RFCpb period.
2. REFRESH cycle time depends on REFRESH command. In the case of per bank REFRESHcommand issued, REFRESH cycle time will be ^{t}RFCpb.
3. "Any command" includes MRR, MRW, and all MPC commands.

4.23 Power-Down Mode

Power-Down Entry and Exit

Power-down is asynchronously entered when CKE is driven LOW. CKE must not go LOWwhile the following operations are in progress:

- Mode register read
- Mode register write
- Read
- Write
- $V_{REF(CA)}$ range and value setting via MRW
- $V_{REF(DQ)}$ range and value setting via MRW
- Command bus training mode entering/exiting via MRW
- VRCG HIGH current mode entering/exiting via MRW

CKE can go LOW while any other operations such as row activation, precharge, autoprecharge, or refresh are in progress. The power-down IDD specification will not be applieduntil such operations are complete. Power-down entry and exit are shown below.

Entering power-down deactivates the input and output buffers, excluding CKE and RESET_n. To ensure that there is enough time to account for internal delay on the CKE signalpath, CS input is required stable LOW level and CA input level is "Don′ t Care" afterCKE is driven LOW, this timing period is defined as ^{t}CKELCS. Clock input is required afterCKE is driven LOW, this timing period is defined as ^{t}CKELCK. CKE LOW will result indeactivation of all input receivers except RESET_n after ^{t}CKELCK has expired. In powerdownmode, CKE must be held LOW; all other input signals except RESET_n are "Don'tCare." CKE LOW must be maintained until ^{t}CKE(MIN) is satisfied.

V_{DDQ} can be turned off during power-down after ^{t}CKELCK is satisfied. Prior to exitingpower-down, V_{DDQ} must be within its minimum/maximum operating range. No REFRESHoperations are performed in power-down mode except self refresh power-down.The maximum duration in non-self-refresh power-down mode is only limited by the refreshrequirements outlined in the REFRESH command section.

The power-down state is asynchronously exited when CKE is driven HIGH. CKE HIGHmust be maintained until ^{t}CKE(MIN) is satisfied. A valid, executable command can beapplied with power-down exit latency ^{t}XP after CKE goes HIGH. Power-down exit latencyis defined in the AC timing parameter table.

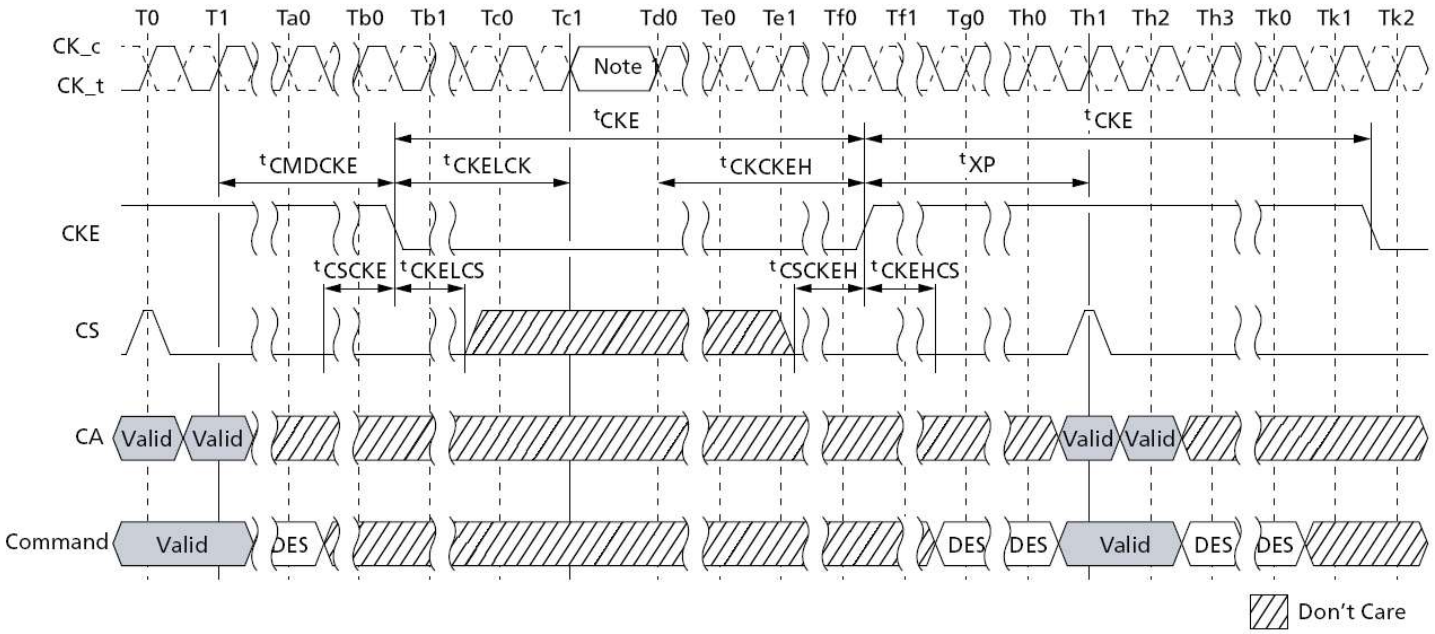
Clock frequency change or clock stop is inhibited during ^{t}CMDCKE, ^{t}CKELCK,^{t}CKCKEH, ^{t}XP, ^{t}MRWCKEL, and ^{t}ZQCKE periods.

If power-down occurs when all banks are idle, this mode is referred to as idle powerdown.if power-down occurs when there is a row active in any bank, this mode is referredto as active power-down. And If power-down occurs when self refresh is in progress,this mode is referred to as self refresh power-down in which the internal refresh is continuingin the same way as self refresh mode.

When CA, CK, and/or CS ODT is enabled via MR11 OP[6:4] and also via MR22 or CAODTpad setting, the rank providing ODT will continue to terminate the command busin all DRAM states including power-down when V_{DDQ} is stable and within its minimum/maximum operating range.

The LPDDR4 DRAM cannot be placed in power-down state during start DQS intervaloscillator operation.

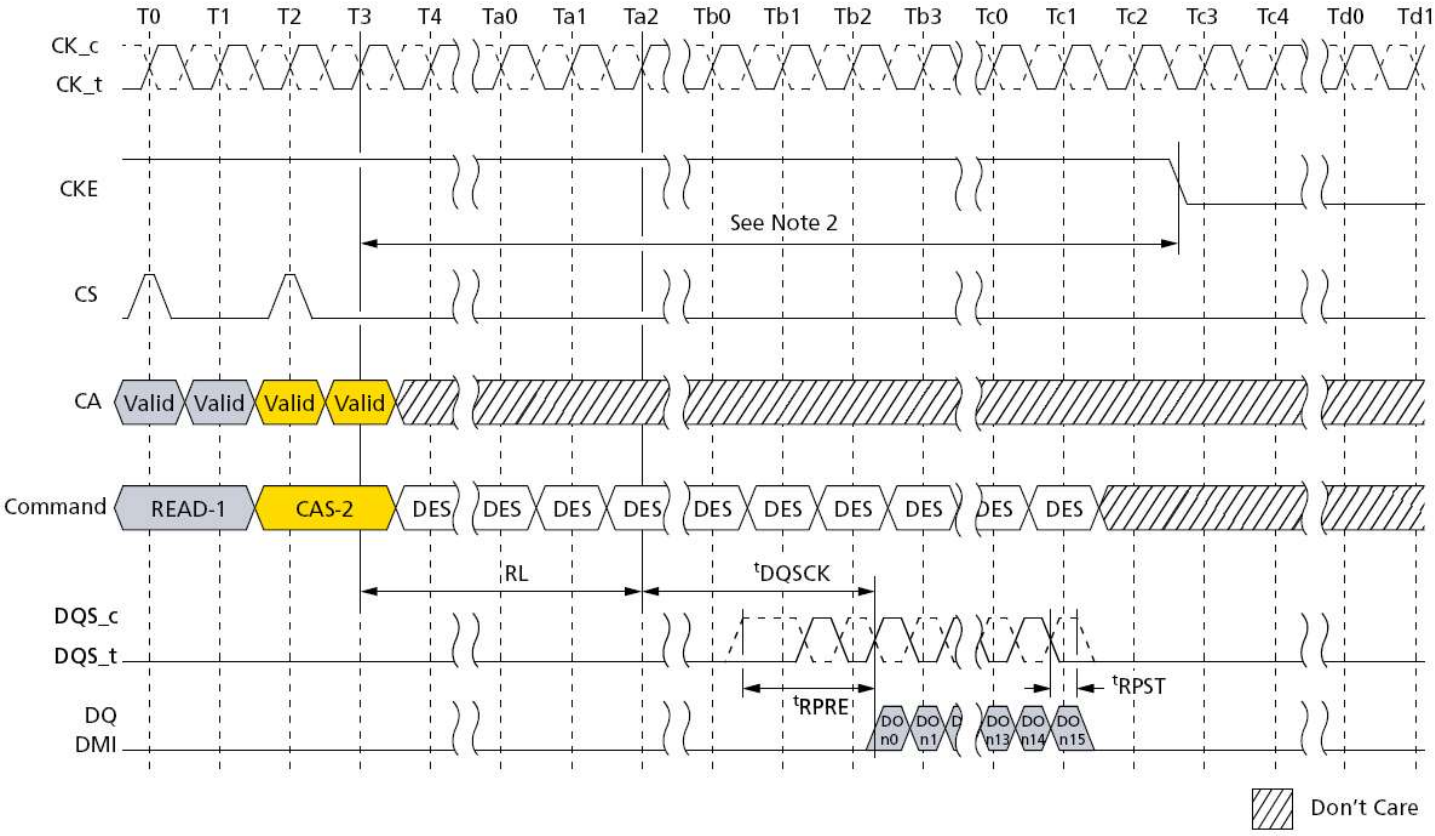
Figure 4-65: Basic Power-Down Entry and Exit Timing



Note:

1. Input clock frequency can be changed or the input clock can be stopped or floated duringpower-down, provided that upon exiting power-down, the clock is stable and withinspecified limits for a minimum of ^{t}CKCKEH of stable clock prior to power-down exit andthe clock frequency is between the minimum and maximum specified frequency for thespeed grade in use.

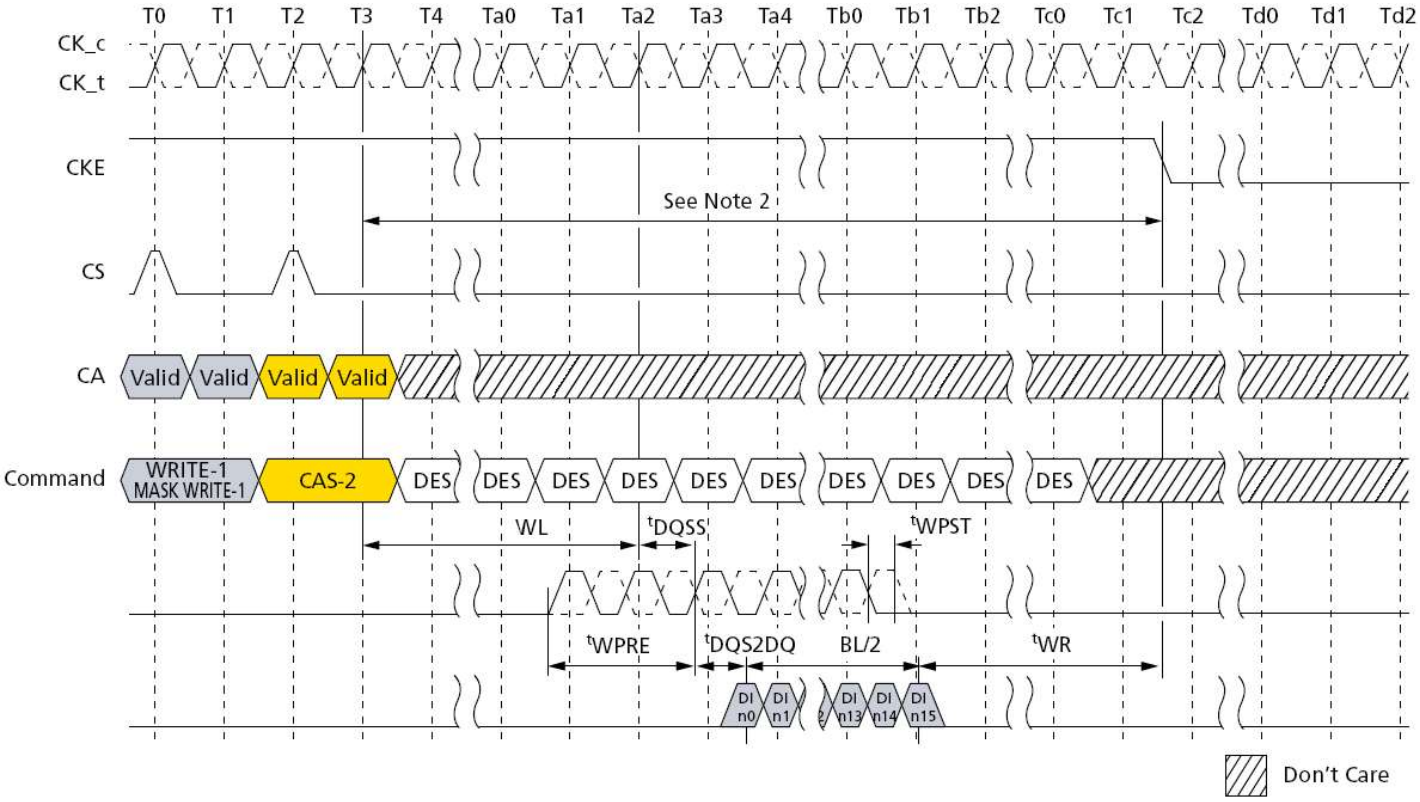
Figure 4-66: Read and Read with Auto Precharge to Power-Down Entry



Notes:

1. CKE must be held HIGH until the end of the burst operation.
2. Minimum delay time from READ command or READ with AUTO PRECHARGE commandto falling edge of CKE signal is as follows:
   When read postamble = 0.5nCK (MR1 OP[7] = [0]),
   (RL ×^{t}CK) + ^{t}DQSCK(MAX) + ((BL/2) ×^{t}CK) + 1^{t}CK
   When read postamble = 1.5nCK (MR1 OP[7] = [1]),
   (RL ×^{t}CK) + ^{t}DQSCK(MAX) + ((BL/2) ×^{t}CK) + 2^{t}CK

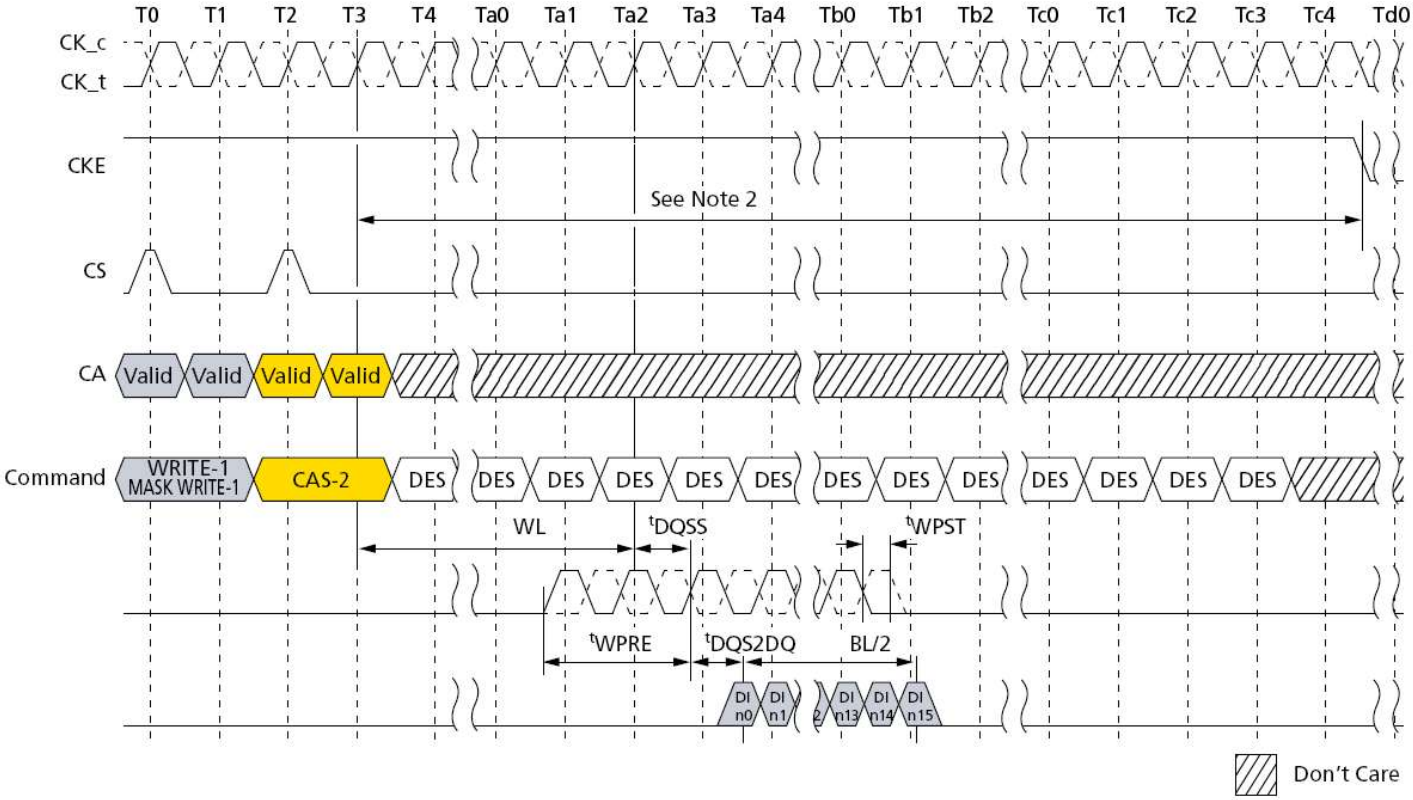
Figure 4-67: Write and Mask Write to Power-Down Entry



Notes:

1. CKE must be held HIGH until the end of the burst operation.
2. Minimum delay time from WRITE command or MASK WRITE command to falling edgeof CKE signal is as follows:
   (WL ×^{t}CK) + ^{t}DQSS(MAX) + ^{t}DQS2DQ(MAX) + ((BL/2) ×^{t}CK) + ^{t}WR
3. This timing is applied regardless of DQ ODT disable/enable setting: MR11 OP[2:0].
4. This timing diagram only applies to the WRITE and MASK WRITE commands without autoprecharge.

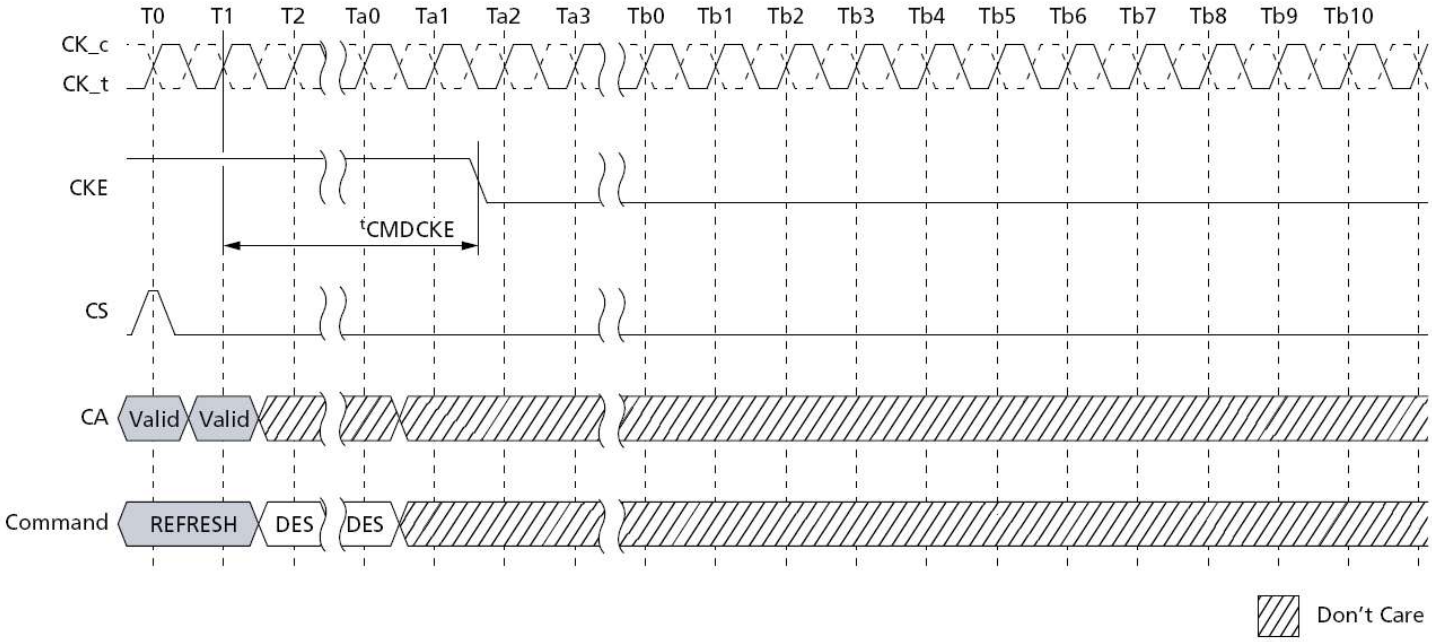
Figure 4-68: Write With Auto Precharge and Mask Write With Auto Precharge to Power-Down Entry



Notes:

1. CKE must be held HIGH until the end of the burst operation.
2. Delay time from WRITE with AUTO PRECHARGE command or MASK WRITE with AUTOPRECHARGE command to falling edge of CKE signal is more than
   (WL ×^{t}CK) + ^{t}DQSS(MAX) + ^{t}DQS2DQ(MAX) + ((BL/2) ×^{t}CK) + (nWR ×^{t}CK) + (2 ×^{t}CK)
3. This timing is applied regardless of DQ ODT disable/enable setting: MR11 OP[2:0].

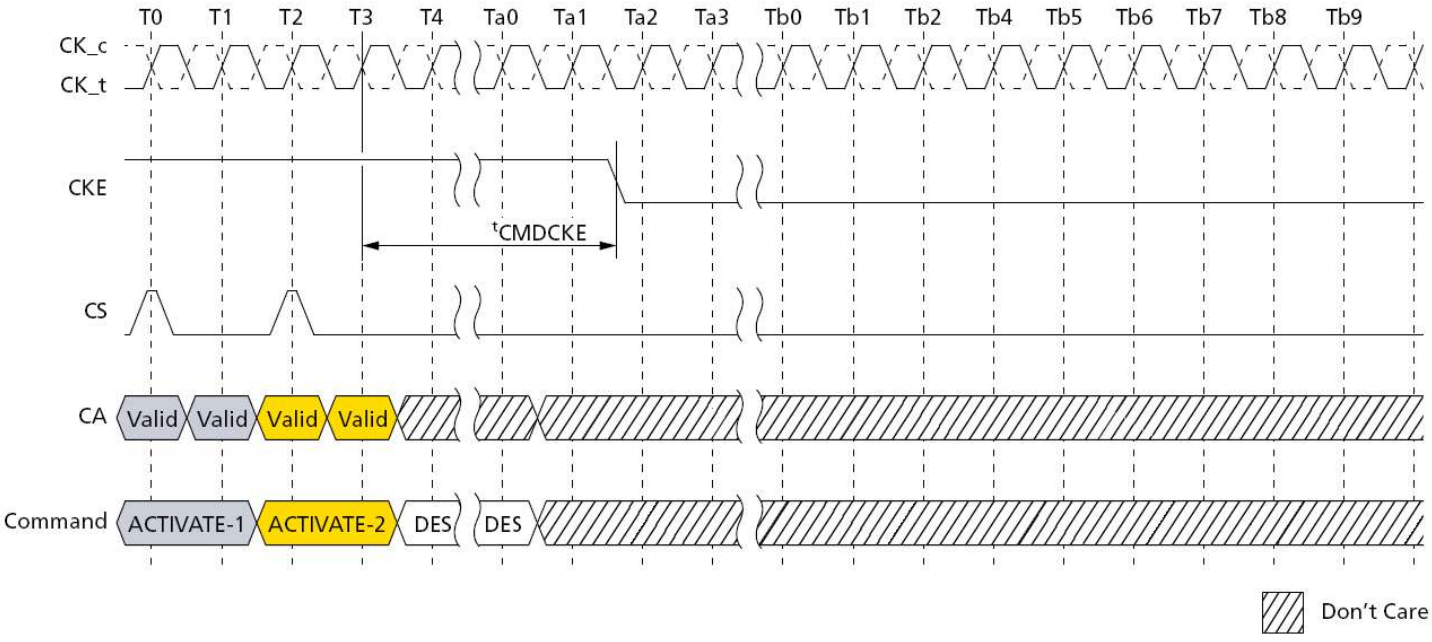
Figure 4-69: Refresh Entry to Power-Down Entry



Note:

1. CKE must be held HIGH until tCMDCKE is satisfied.

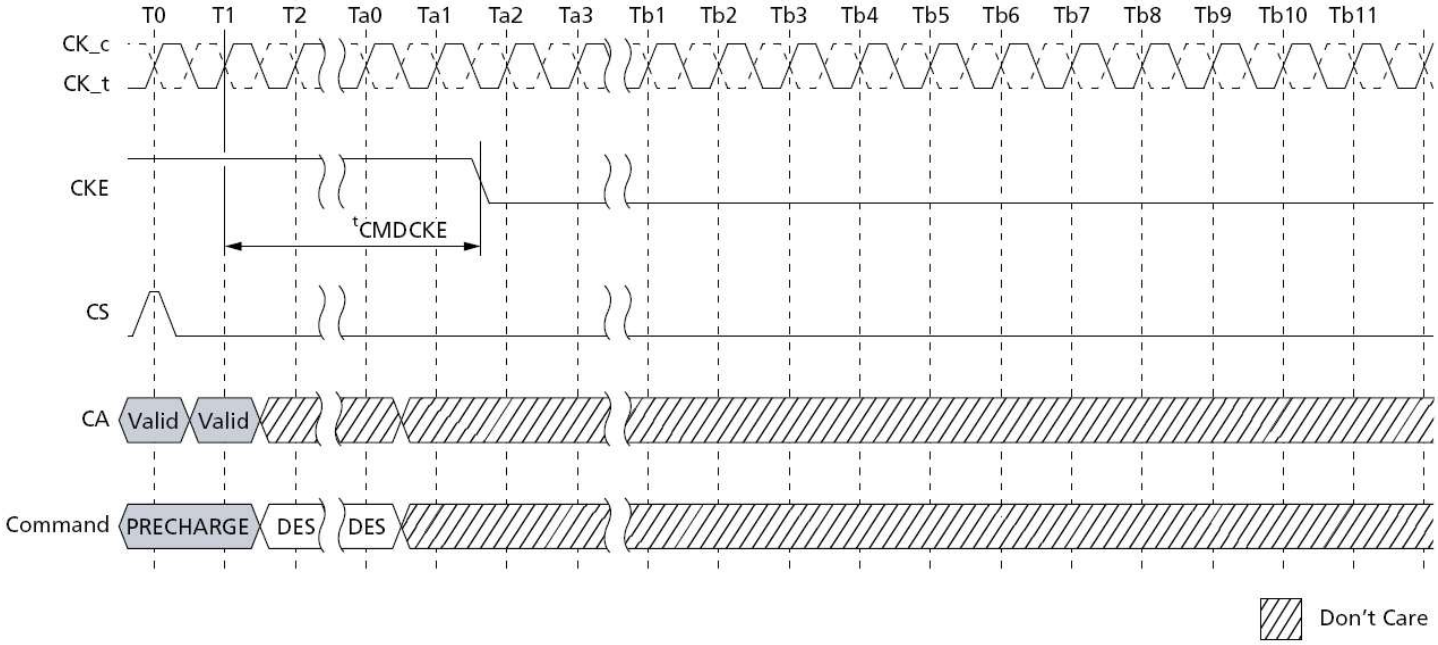
Figure 4-70: ACTIVATE Command to Power-Down Entry



Note:

1. CKE must be held HIGH until tCMDCKE is satisfied.

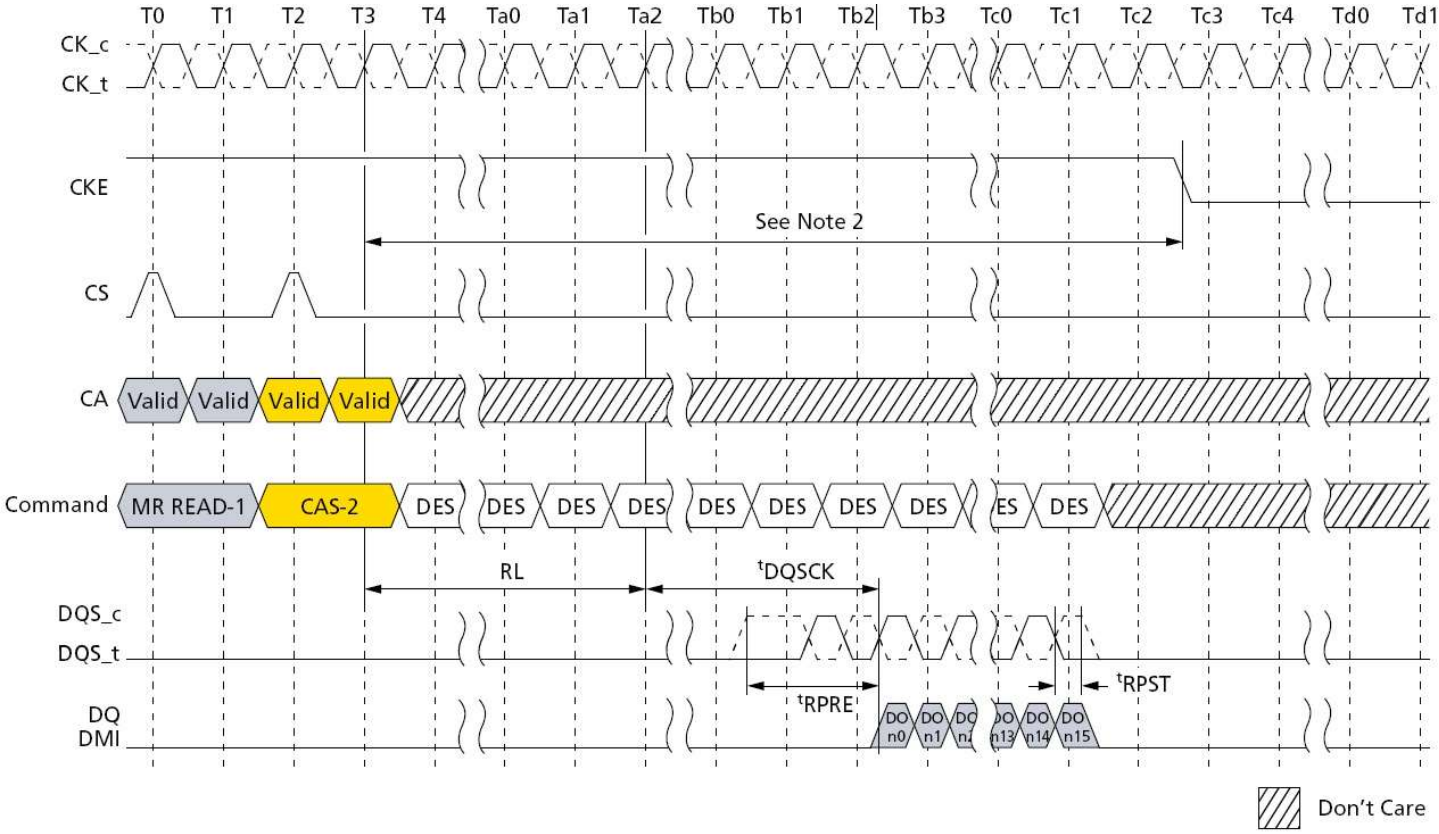
Figure 4-71: PRECHARGE Command to Power-Down Entry



Note:

1. CKE must be held HIGH until ᵗCMDCKE is satisfied.

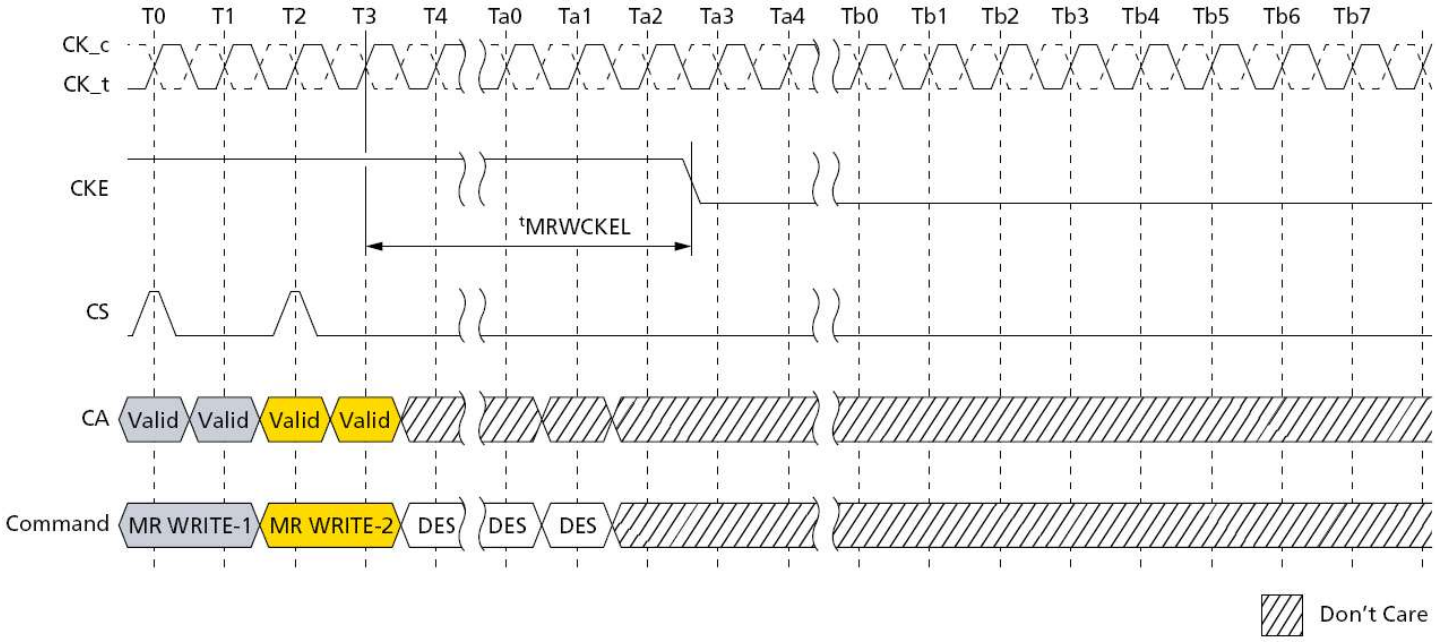
Figure 4-72: Mode Register Read to Power-Down Entry



Notes:

1. CKE must be held HIGH until the end of the burst operation.
2. Minimum delay time from MODE REGISTER READ command to falling edge of CKE signalis as follows:
   When read postamble = 0.5nCK (MR1 OP[7] = [0]),
   (RL ×^{t}CK) + ^{t}DQSCK(MAX) + ((BL/2) ×^{t}CK) + 1^{t}CK
   When read postamble = 1.5nCK (MR1 OP[7] = [1]),
   (RL ×^{t}CK) + ^{t}DQSCK(MAX) + ((BL/2) ×^{t}CK) + 2^{t}CK

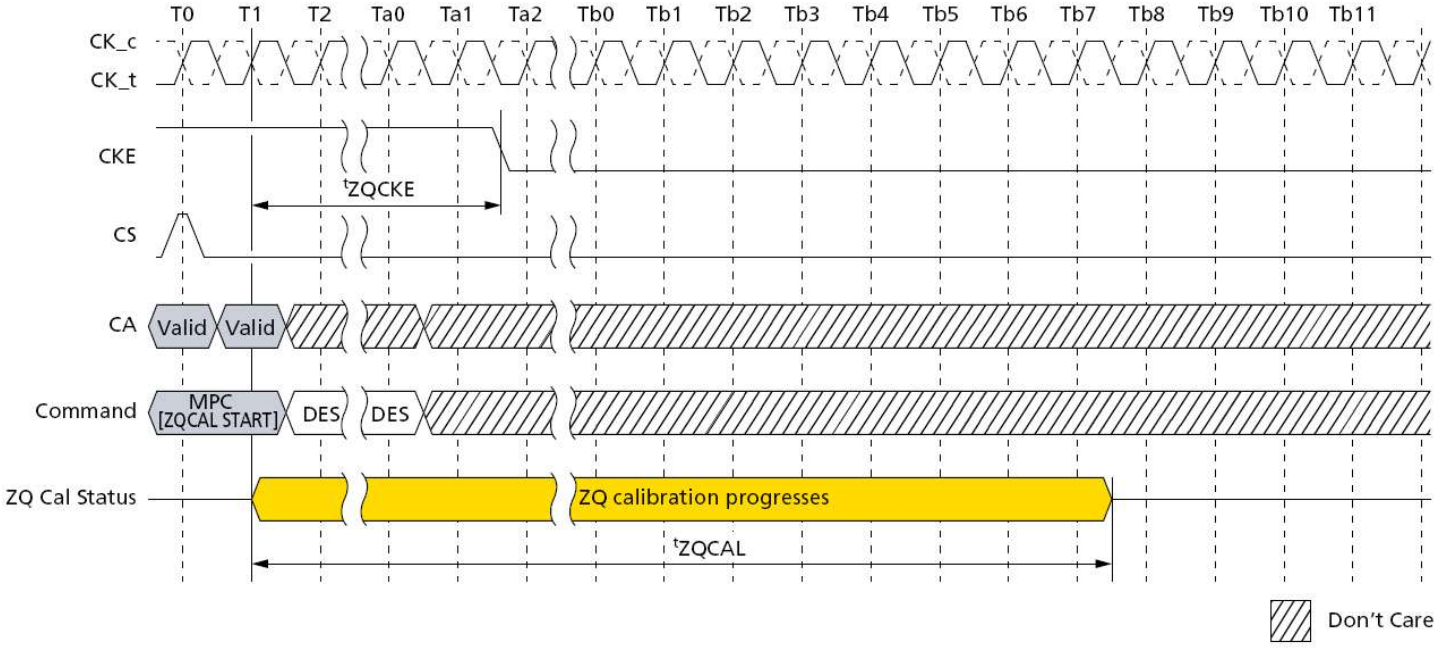
Figure4-73: Mode Register Write to Power-Down Entry



Notes:

1. CKE must be held HIGH until tMRWCKEL is satisfied.
2. This timing is the general definition for power-down entry after MODE REGISTER WRITEcommand. When a MODE REGISTER WRITE command changes a parameter or starts anoperation that requires special timing longer than tMRWCKEL, that timing must be satisfiedbefore CKE is driven LOW. Changing the $V_{REF(DQ)}$ value is one example, in this casethe appropriate tVREF-SHORT/MIDDLE/LONG must be satisfied.

Figure 4-74: MULTI PURPOSE Command for ZQCAL Start to Power-Down Entry



Note:

1. ZQ calibration continues if CKE goes LOW after tZQCKE is satisfied.

4.24 Input Clock Stop and Frequency Change

Clock Frequency Change – CKE LOW

During CKE LOW, the device supports input clock frequency changes under the followingconditions:
- ^{t}CK(abs) (MIN) is met for each clock cycle
- Refresh requirements apply during clock frequency change
- During clock frequency change, only REFab or REFpb commands may be executing
- Any ACTIVATE or PRECHARGE commands have completed prior to changing the frequency
- Related timing conditions, ^{t}RCD and tRP, have been met prior to changing the frequency
- The initial clock frequency must be maintained for a minimum of ^{t}CKELCK after CKEgoes LOW
- The clock satisfies ^{t}CH(abs) and ^{t}CL(abs) for a minimum of ^{t}CKCKEH prior to CKE goingHIGH

After the input clock frequency changes and CKE is held HIGH, additional MRW commandsmay be required to set the WR, RL, and so forth. These settings may require adjustmentto meet minimum timing requirements at the target clock frequency.

Clock Stop – CKE LOW

During CKE LOW, the device supports clock stop under the following conditions:
- CK_t and CK_c are don't care during clock stop
- Refresh requirements apply during clock stop
- During clock stop, only REFab or REFpb commands may be executing
- Any ACTIVATE or PRECHARGE commands have completed prior to stopping theclock
- Related timing conditions, ^{t}RCD and tRP, have been met prior to stopping the clock
- The initial clock frequency must be maintained for a minimum of ^{t}CKELCK after CKEgoes LOW
- The clock satisfies ^{t}CH(abs) and ^{t}CL(abs) for a minimum of ^{t}CKCKEH prior to CKE goingHIGH

Clock Frequency Change – CKE HIGH

During CKE HIGH, the device supports input clock frequency change under the followingconditions:
- ^{t}CK(abs) (MIN) is met for each clock cycle
- Refresh requirements apply during clock frequency change
- During clock frequency change, only REFab or REFpb commands may be executing
- Any ACTIVATE, READ, WRITE, PRECHARGE, MODE REGISTER WRITE, or MODEREGISTER READcommands (and any associated data bursts) have completed priorto changing the frequency
- Related timing conditions (^{t}RCD, ^{t}WR, ^{t}RP, ^{t}MRW, and ^{t}MRR) have been met prior tochanging the frequency
- During clock frequency change, CS is held LOW
- The device is ready for normal operation after the clock satisfies ^{t}CH(abs) and^{t}CL(abs) for a minimum of 2 ×^{t}CK + ^{t}XP

After the input clock frequency is changed, additional MRW commands may be requiredto set the WR, RL, and so forth. These settings may need to be adjusted to meetminimum timing requirements at the target clock frequency.

Clock Stop – CKE HIGH

During CKE HIGH, the device supports clock stop under the following conditions:
- CK_t is held LOW and CK_c is held HIGH during clock stop
- During clock stop, CS is held LOW
- Refresh requirements apply during clock stop
- During clock stop, only REFab or REFpb commands may be executing
- Any ACTIVATE, READ, WRITE, MPC (WRITE-FIFO, READ-FIFO, READ DQ CALIBRATION),PRECHARGE,MODE REGISTER WRITE, or MODE REGISTER READ commandshave completed, including any associateddata bursts and extra 4 clock cyclesmust be provided prior to stopping the clock
- Related timing conditions (tRCD, tWR, tRP, tMRW, tMRR, tZQLAT, and so forth) havebeen met prior to stoppingthe clock
- READ with AUTO PRECHARGE and WRITE with AUTO PRECHARGE commands needextra 4 clock cycles inaddition to the related timing constraints, nWR and nRTP, tocomplete the operations
- REFab, REFpb, SRE, SRX, and MPC[ZQCAL START] commands are required to haveextra 4 clock cycles priorto stopping the clock

- The device is ready for normal operation after the clock is restarted and satisfiestCH(abs) and tCL(abs) for aminimum of 2 ×tCK + tXP

4.25 MODE REGISTER READ Operation

The MODE REGISTER READ (MRR) command is used to read configuration and status data from the device registers. The MRR command is initiated with CS and CA[5:0] in the proper state as defined by the Command Truth Table. The mode register address operands (MA[5:0]) enable the user to select one of 64 registers. The mode register con- tents are available on the first four UI data bits of DQ[7:0] after RL × ^{t}CK + ^{t}DQSCK + ^{t}DQSQ following the MRR command. Subsequent data bits contain valid but undefined content. DQS is toggled for the duration of the MODE REGISTER READ burst. The MRR has a command burst length of 16. MRR operation must not be interrupted.

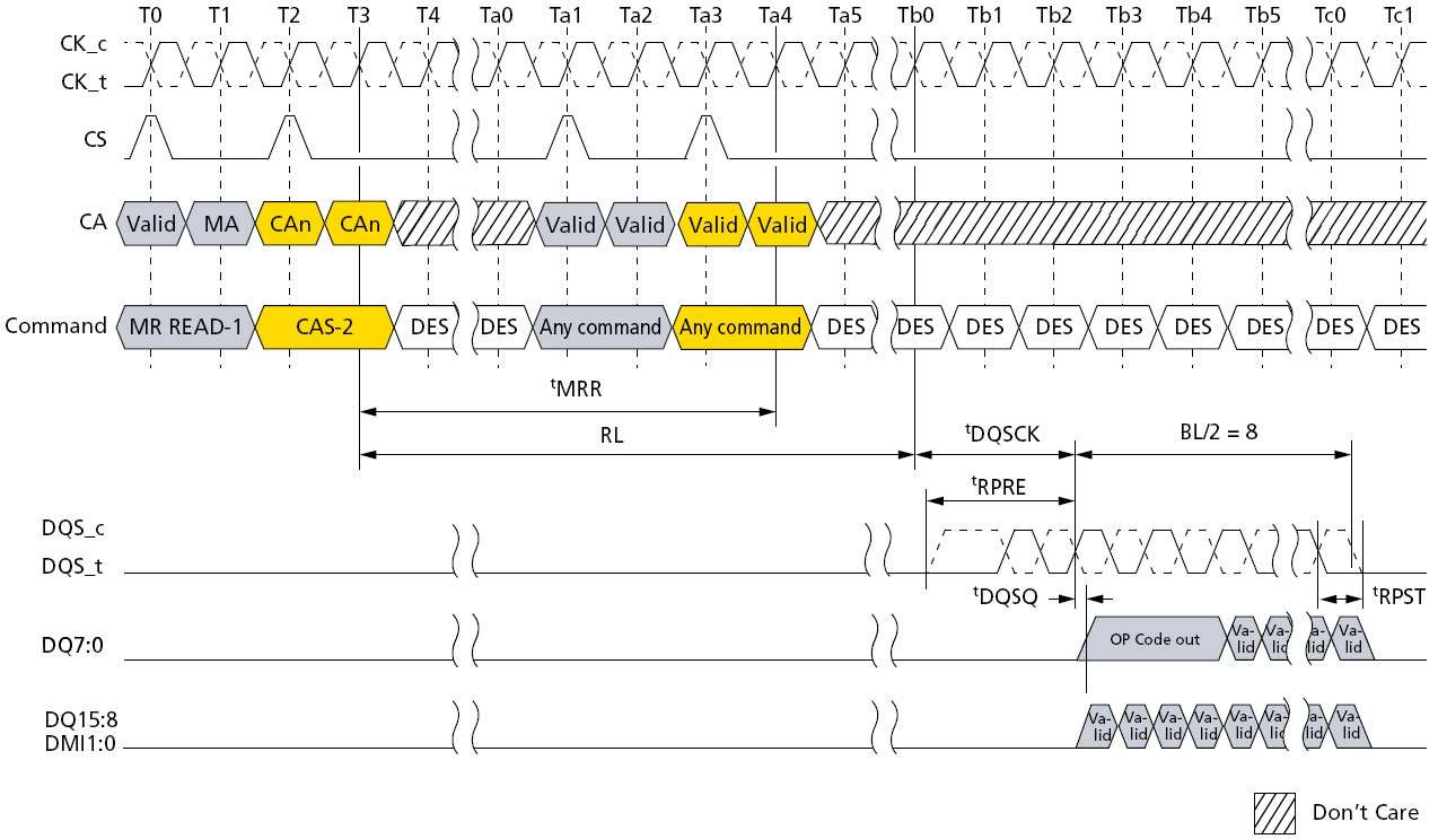
Table 4-102: MRR

UI	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DQ0	OP0				V											
DQ1	OP1				V											
DQ2	OP2				V											
DQ3	OP3				V											
DQ4	OP4				V											
DQ5	OP5				V											
DQ6	OP6				V											
DQ7	OP7				V											
DQ8–DQ15	V															
DMI0–DMI1	V															

Notes:

1. MRR data are extended to the first 4 UIs, allowing the LPDRAM controller to sample data easily.
2. DBI during MRR depends on mode register setting MR3 OP[6].
3. The read preamble and postamble of MRR are the same as for a normal read

Figure 4-75: MODE REGISTER READ Operation



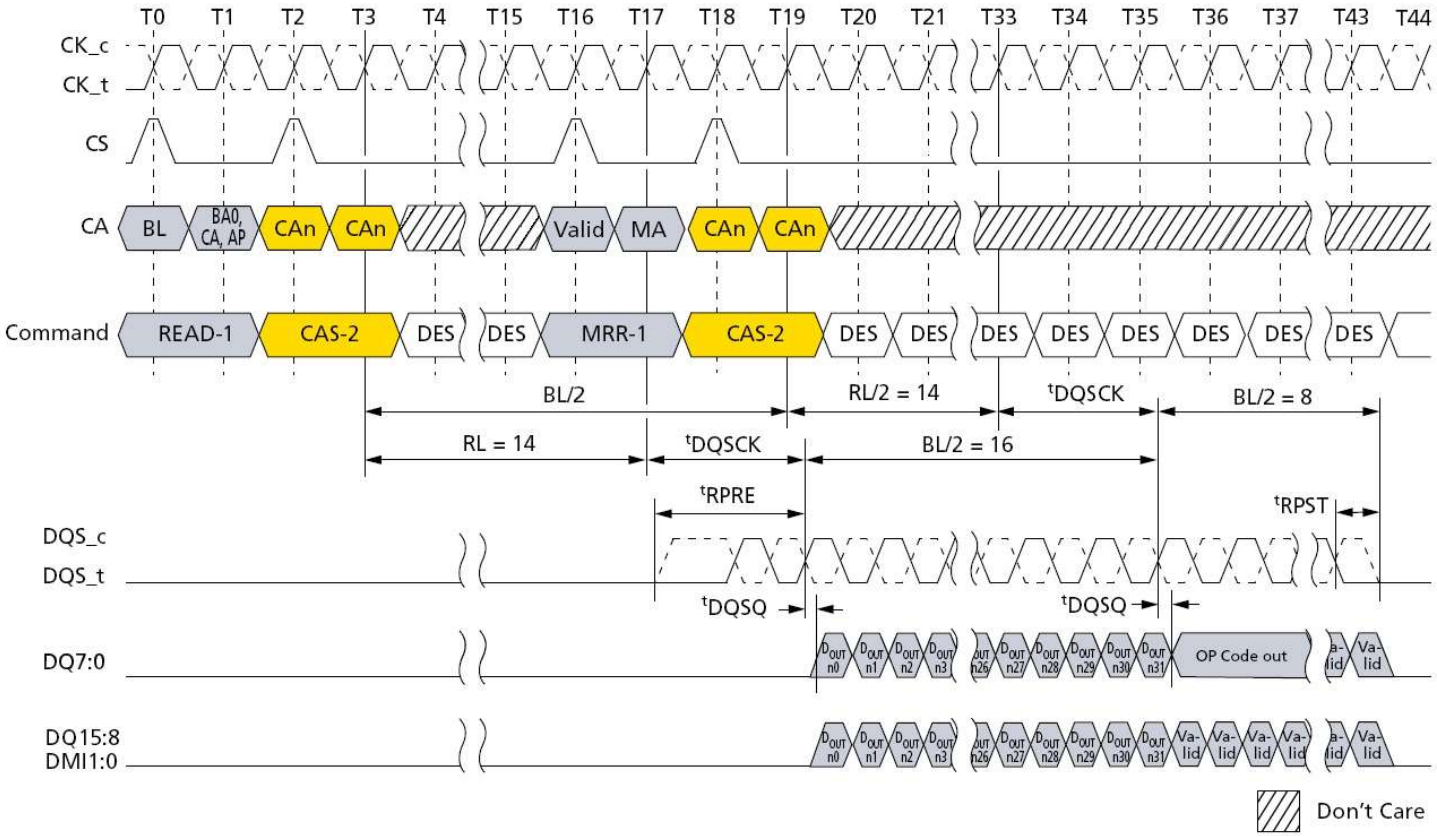
Notes:

1. Only BL = 16 is supported.
2. Only DESELECT is allowed during ^{t}MRR period.
3. There are some exceptions about issuing commands after ^{t}MRR. Refer to MRR/MRWTiming Constraints Table for detail.
4. DBI is disable mode.
5. DES commands except ^{t}MRR period are shown for ease of illustration; other commandsmay be valid at these times.
6. DQ/DQS: V_{SSQ} termination

MRR After a READ and WRITE Command

After a prior READ command, the MRR command must not be issued earlier than BL/2clock cycles, in a similar way WL + BL/2 + 1 + RU (^{t}WTR/^{t}CK) clock cycles after a PRIORWRITE, WRITE with AP, MASK WRITE, MASK WRITE with AP, and MPC[WRITE-FIFO]command in order to avoid the collision of READ and WRITE burst data on device internaldata bus.

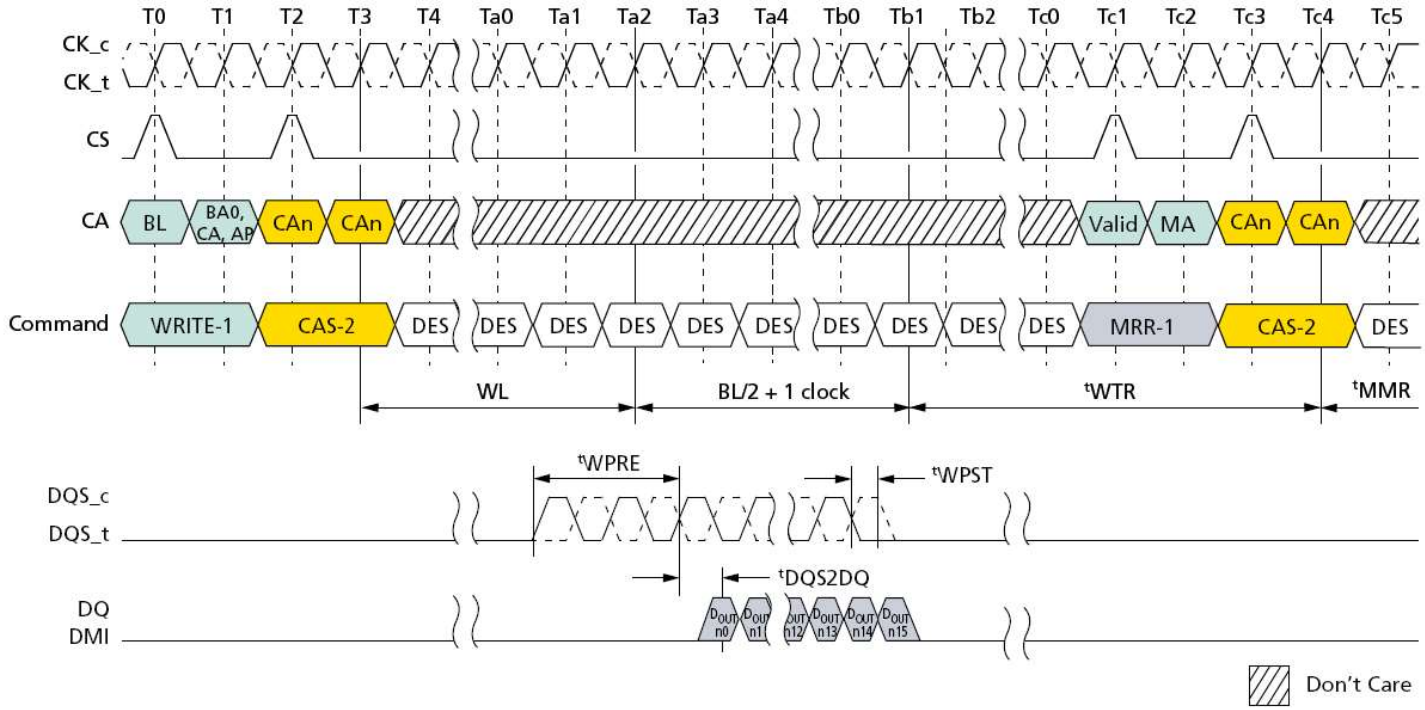
Figure 4-76: READ-to-MRR Timing



Notes:

1. The minimum number of clock cycles from the burst READ command to the MRR commandis BL/2.
2. Read BL = 32, MRR BL = 16, RL = 14, Preamble = Toggle, Postamble = 0.5nCK, DBI = Disable,DQ/DQS: V_{SSQ} termination.
3. D_{OUT} n = data-out to column n.
4. DES commands except ^{t}MRR period are shown for ease of illustration; other commandsmay be valid at these times.

Figure 4-77: WRITE-to-MRR Timing



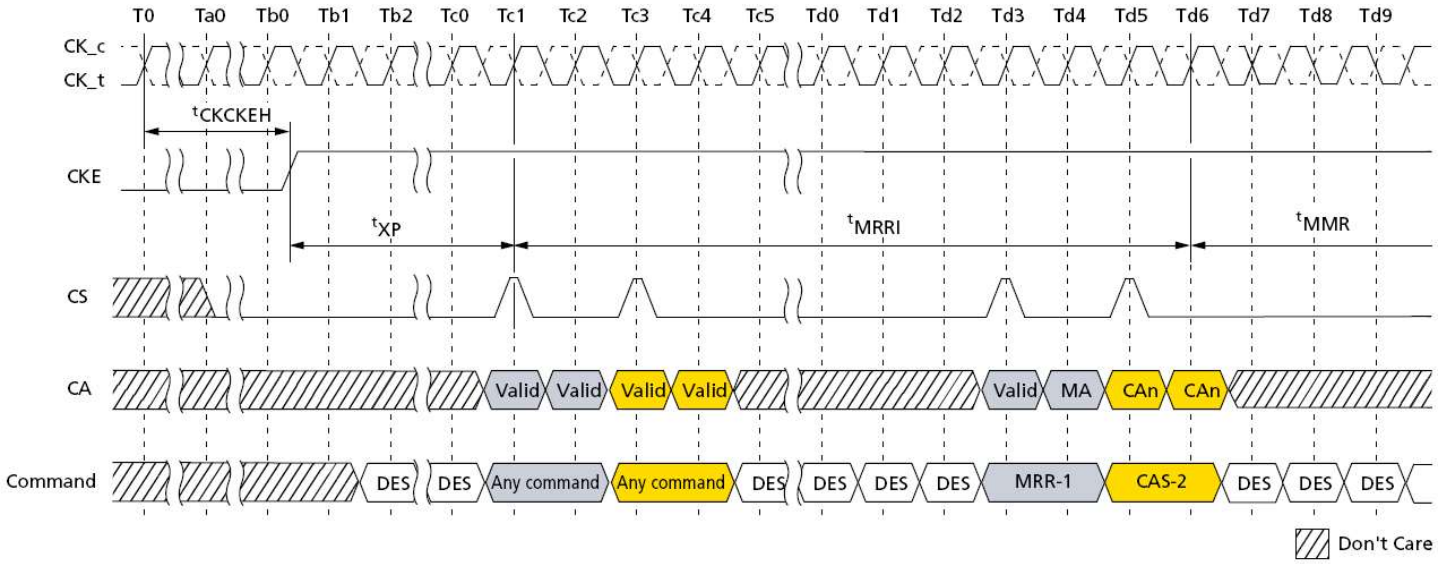
Notes:

1. Write BL=16, Write postamble = 0.5nCK, DQ/DQS: V_{SSQ} termination.
2. Only DES is allowed during ^{t}MRR period.
3. D_{OUT} n = data-out to column n.
4. The minimum number of clock cycles from the BURST WRITE command to MRR commandis WL + BL/2 + 1 + RU(^{t}WTR/^{t}CK).
5. ^{t}WTR starts at the rising edge of CK after the last latching edge of DQS.
6. DES commands except ^{t}MRR period are shown for ease of illustration; other commandsmay be valid at these times.

MRR After Power-Down Exit

Following the power-down state, an additional time, tMRRI, is required prior to issuingthe MODE REGISTER READ (MRR) command. This additional time (equivalent totRCD) is required in order to maximize power-down current savings by allowing morepower-up time for the MRR data path after exit from power-down mode.

Figure 4-78: MRR Following Power-Down



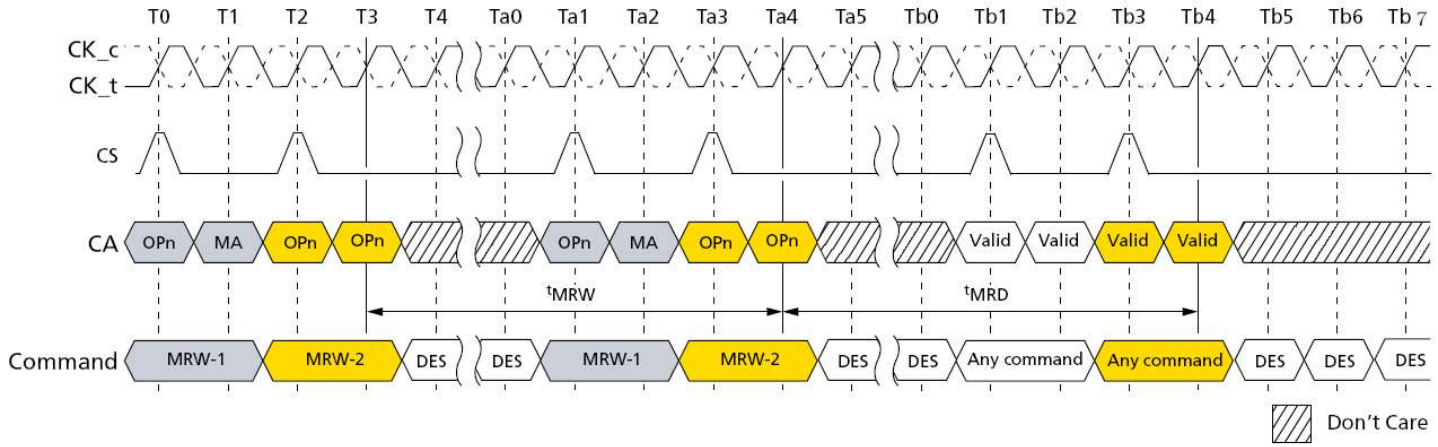
Notes:

1. Only DES is allowed during tMRR period.
2. DES commands except tMRR period are shown for ease of illustration; other commandsmay be valid at these times.

4.26 MODE REGISTER WRITE

The MODE REGISTER WRITE (MRW) writes configuration data to the mode registers.
The MRW command is initiated with CKE, CS, and CA[5:0] to valid levels at the risingedge of the clock. The mode register address and the data written to it is contained inCA[5:0] according to the Command Truth Table. The MRW command period is definedby tMRW. Mode register WRITEs to read-only registers have no impact on the functionalityof the device.

Figure 4-79: MODE REGISTER WRITE Timing



Mode Register Write States

MRW can be issued from either a bank-idle or a bank-active state. Certain restrictionsmay apply for MRW from an active state.

Table 4-103: Truth Table for MRR and MRW

Current State	Command	Intermediate State	Next State
All banks idle	MRR	Reading mode register, all banks idle	All banks idle
	MRW	Writing mode register, all banks idle	All banks idle
Bank(s) active	MRR	Reading mode register	Bank(s) active
	MRW	Writing mode register	Bank(s) active

Table 4-104: MRR/MRW Timing Constraints: DQ ODT is Disable

From Command	To Command	Minimum Delay Between "From Command" and "To Command"	Unit	Notes
MRR	MRR	^{t}MRR	–	
	RD/RDA	^{t}MRR	–	
	WR/WRA/MWR/MWRA	RL + RU(^{t}DQSCK(MAX)/^{t}CK) + BL/2 -WL + ^{t}WPRE + RD(^{t}RPST)	nCK	
	MRW	RL + RU(^{t}DQSCK(MAX)/^{t}CK) + BL/2 + 3	nCK	
RD/RDA	MRR	BL/2	nCK	
WR/WRA/MWR/ MWRA		WL + 1 + BL/2 + RU(^{t}WTR/^{t}CK)	nCK	
MRW		^{t}MRD	–	
POWER-DOWN EXIT		^{t}XP + ^{t}MRRI	–	
MRW	RD/RDA	^{t}MRD	–	
	WR/WRA/MWR/MWRA	^{t}MRD	–	
	MRW	^{t}MRW	–	
RD/ RD-FIFO/ READ DQ CAL	MRW	RL + BL/2 + RU(^{t}DQSCK(MAX)/^{t}CK) + RD(^{t}RPST) + MAX(RU(7.5ns/^{t}CK), 8nCK)	nCK	
RD with AUTO PRECHARGE		RL + BL/2 + RU(^{t}DQSCK(MAX)/^{t}CK) + RD(^{t}RPST) + MAX(RU(7.5ns/^{t}CK), 8nCK)+ nRTP - 8	nCK	
WR/ MWR/ WR-FIFO		WL + 1 + BL/2 + MAX(RU(7.5ns/^{t}CK), 8nCK)	nCK	
WR/MWR with AUTO PRECHARGE		WL + 1 + BL/2 + MAX(RU(7.5ns/^{t}CK), 8nCK)+ nWR	nCK	

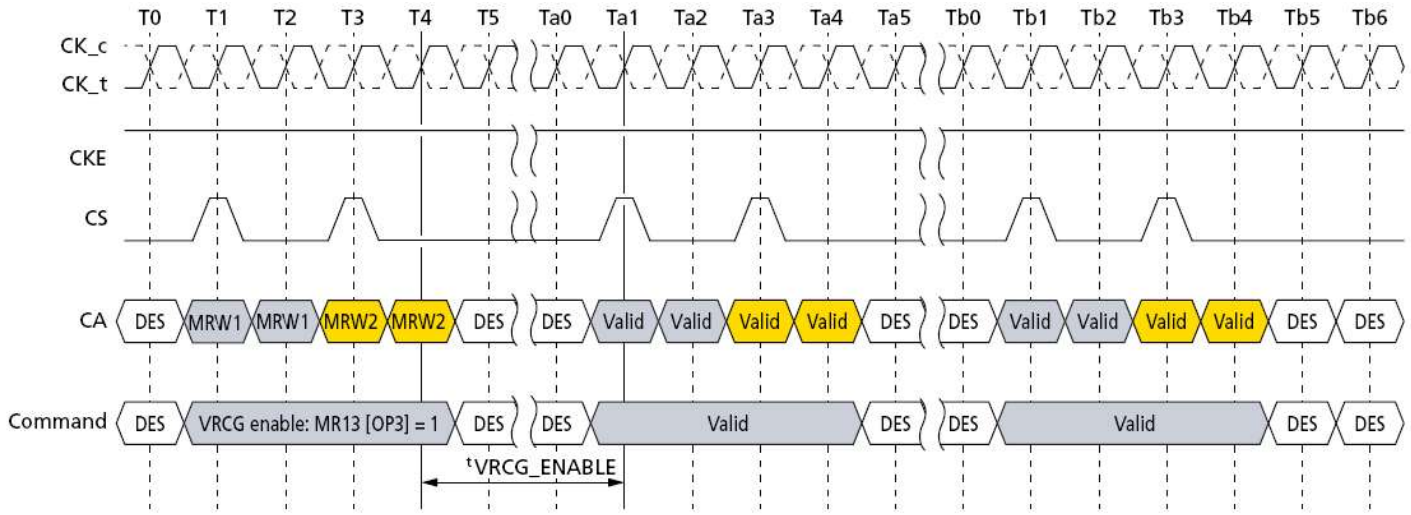
Table 4-105: MRR/MRW Timing Constraints: DQ ODT is Enable

From Command	To Command	Minimum Delay Between "From Command" and "To Command"	Unit	Notes
MRR	MRR	^{t}MRR	–	
	RD/RDA	^{t}MRR	–	
	WR/WRA/MWR/MWRA	RL + RU(^{t}DQSCK(MAX)/^{t}CK) + BL/2 -ODTLon - RD(^{t}ODTon(MIN)/^{t}CK) + RD(^{t}RPST) + 1	nCK	
	MRW	RL + RU(^{t}DQSCK(MAX)/^{t}CK) + BL/2 + 3	nCK	
RD/RDA	MRR	BL/2	nCK	
WR/WRA/MWR/ MWRA		WL + 1 + BL/2 + RU(^{t}WTR/^{t}CK)	nCK	
MRW		^{t}MRD	–	
POWER-DOWN EXIT		^{t}XP + ^{t}MRRI	–	
MRW	RD/RDA	^{t}MRD	–	
	WR/WRA/MWR/MWRA	^{t}MRD	–	
	MRW	^{t}MRW	–	
RD/ RD-FIFO/ READ DQ CAL	MRW	RL + BL/2 + RU(^{t}DQSCK(MAX)/^{t}CK) + RD(^{t}RPST) + MAX(RU(7.5ns/^{t}CK), 8nCK)	nCK	
RD with AUTO PRECHARGE		RL + BL/2 + RU(^{t}DQSCK(MAX)/^{t}CK) + RD(^{t}RPST) + MAX(RU(7.5ns/^{t}CK), 8nCK)+ nRTP - 8	nCK	
WR/ MWR/ WR-FIFO		WL + 1 + BL/2 + MAX(RU(7.5ns/^{t}CK), 8nCK)	nCK	
WR/MWR with AUTO PRECHARGE		WL + 1 + BL/2 + MAX(RU(7.5ns/^{t}CK), 8nCK)+ nWR	nCK	

4.27 V_{REF} Current Generator (VRCG)

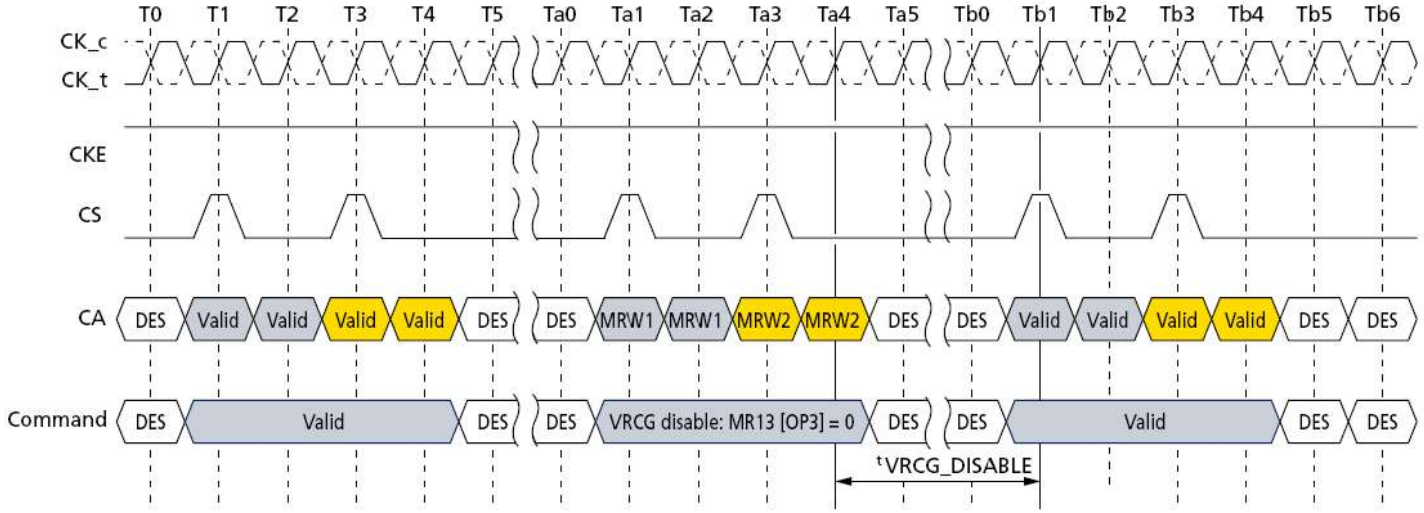
LPDDR4 SDRAM V_{REF} current generators (VRCG) incorporate a high current mode toreduce the settling time of the internal $V_{REF(DQ)}$ and $V_{REF(CA)}$ levels during training andwhen changing frequency set points during operation. The high current mode is enabledby setting MR13[OP3] = 1. Only DESELECT commands may be issued until ^{t}VRCG_ENABLE is satisfied. ^{t}VRCG_ENABLE timing is shown below.

Figure 4-80: VRCG Enable Timing



VRCG high current mode is disabled by setting MR13[OP3] = 0. Only DESELECT commandsmay be issued until ^{t}VRCG_DISABLE is satisfied. ^{t}VRCG_DISABLE timing isshown below.

Figure 4-81: VRCG Disable Timing



Note that LPDDR4 SDRAM devices support $V_{FER(CA)}$ and $V_{REF(DQ)}$ range and valuechanges without enabling VRCG high current mode.

Table 4-106: VRCG Enable/Disable Timing

Parameter	Symbol	Min	Max	Unit
V_{REF} high current mode enable time	^{t}VRCG_ENABLE	–	200	ns
V_{REF} high current mode disable time	^{t}VRCG_DISABLE	–	100	ns

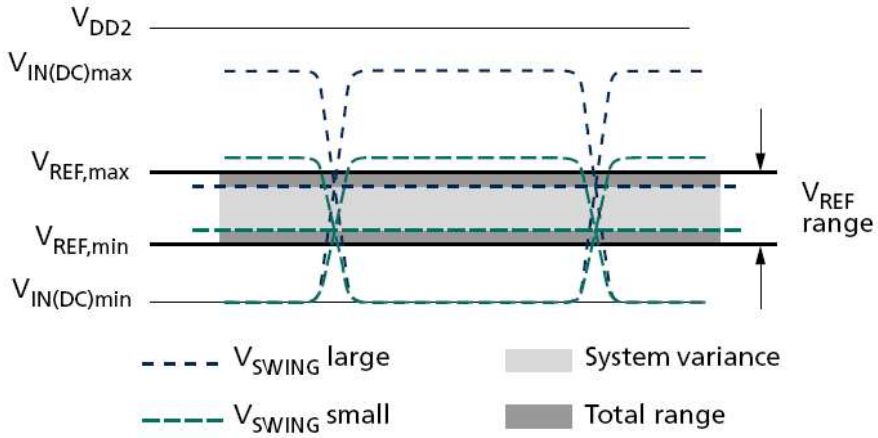
4.28 VREF Training

$V_{REF(CA)}$ Training

The device's internal $V_{REF(CA)}$ specification parameters are operating voltage range, stepsize, V_{REF} step time, V_{REF} full-range step time, and V_{REF} valid level.

The voltage operating range specifies the minimum required V_{REF} setting range forLPDDR4 devices. The minimum range is defined by V_{REF},max and V_{REF},min.

Figure 4-82: V_{REF} Operating Range ($V_{REF,max}$, $V_{REF,min}$)

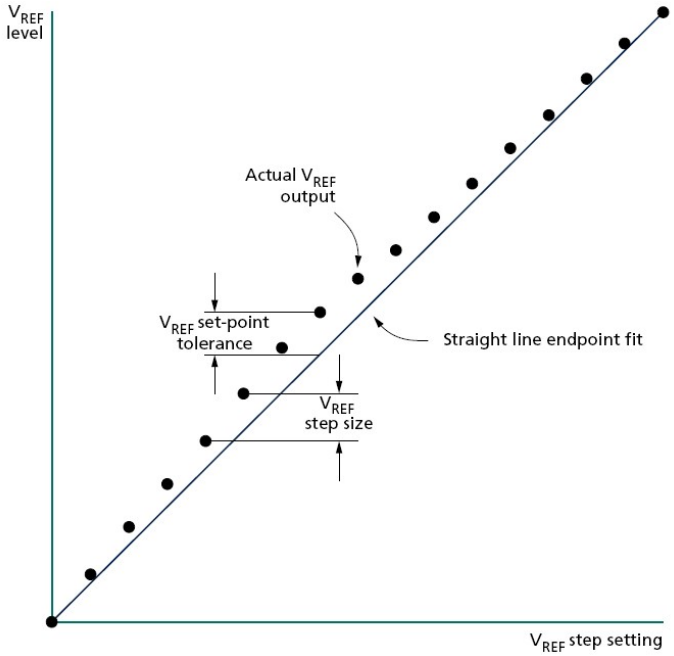


The V_{REF} step size is defined as the step size between adjacent steps. However, for a givendesign, the device has one value for V_{REF} step size that falls within the given range.

The V_{REF} set tolerance is the variation in the V_{REF} voltage from the ideal setting. This accountsfor accumulated error over multiple steps. There are two ranges for V_{REF} set toleranceuncertainty. The range of V_{REF} set tolerance uncertainty is a function of thenumber of steps n.

The V_{REF} set tolerance is measured with respect to the ideal line that is based on the twoendpoints, where the endpoints are at the minimum and maximum V_{REF} values for aspecified range.

Figure 4-83: V_{REF} Set-Point Tolerance and Step Size



The V_{REF} increment/decrement step times are defined by $^{t}V_{REF}$_TIME-SHORT,$^{t}V_{REF}$_TIME-MIDDLE, and$^{t}V_{REF}$_TIME-LONG. The parameters are defined from TS toTE as shown below, where TE is referenced to when the V_{REF} voltage is at the final DClevel within the V_{REF} valid tolerance (V_{REF,val_tol}).

The V_{REF} valid level is defined by V_{REF,val_tol} to qualify the step time TE (see the followingfigures). This parameter is used to ensure an adequate RC time constant behavior of thevoltage level change after any V_{REF} increment/decrement adjustment. This parameter isonly applicable for LPDDR4 component level validation/characterization.

$^{t}V_{REF}$_TIME-SHORT is for a single step size increment/decrement change in the V_{REF}voltage.

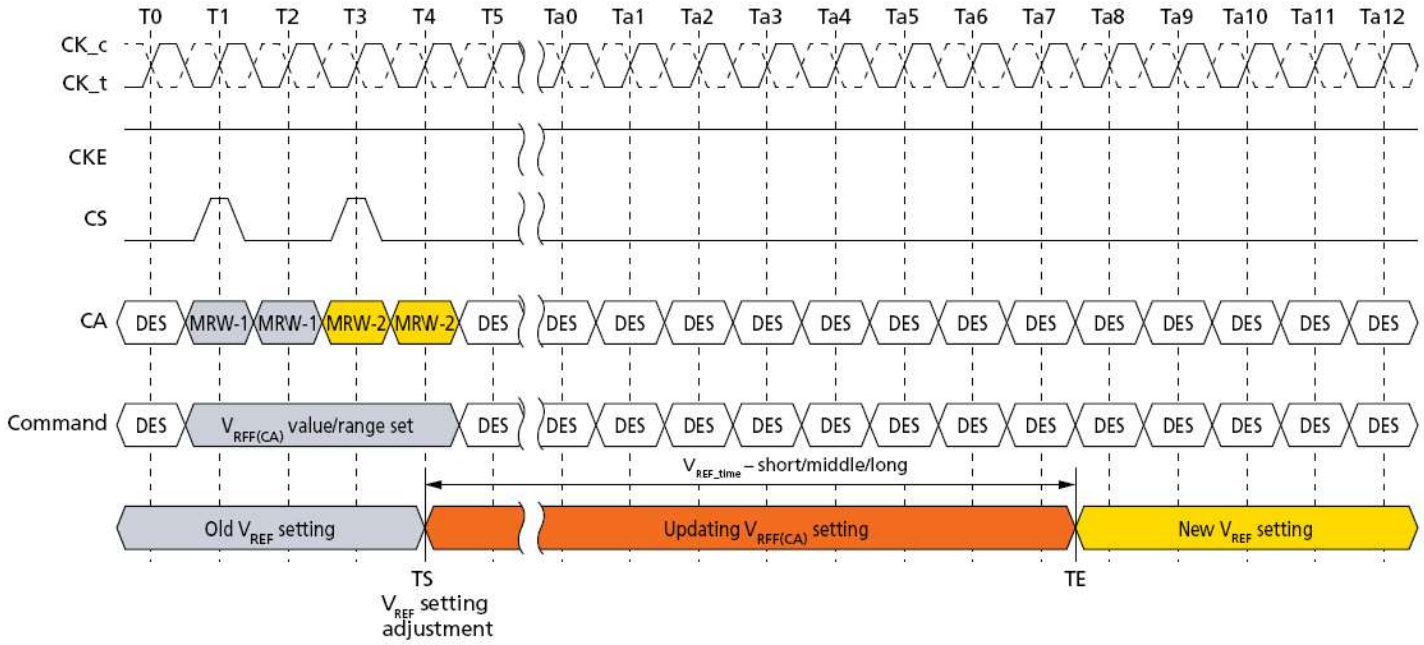
$^{t}V_{REF}$_TIME-MIDDLE is at least two stepsizes increment/decrement change within thesame $V_{REF(CA)}$ range in V_{REF} voltage.

$^{t}V_{REF}$_TIME-LONG is the time including up to $V_{REF,min}$ to $V_{REF,max}$ or $V_{REF,max}$ to $V_{REF,min}$change across the $V_{REF(CA)}$ range in V_{REF} voltage.

TS is referenced to MRW command clock.

TE is referenced to $V_{REF\_val\_tol}$.

Figure 4-84: $^{t}V_{ref}$ for Short, Middle, and Long Timing Diagram



Notes:
1. TS is referenced to MRW command clock.
2. TE is referenced to V_{RFF,VAL_TOL}.

The MRW command to the mode register bits are as follows;
MR12 OP[5:0] : $V_{REF(CA)}$ Setting
MR12 OP[6] : $V_{REF(CA)}$ Range

The minimum time required between two V_{REF} MRW commands is $^{t}V_{REF}$_TIME-SHORTfor a single step and $^{t}V_{REF}$_TIME-MIDDLE for a full voltage range step.

Figure 4-85: $V_{REF(CA)}$ Single-Step Increment

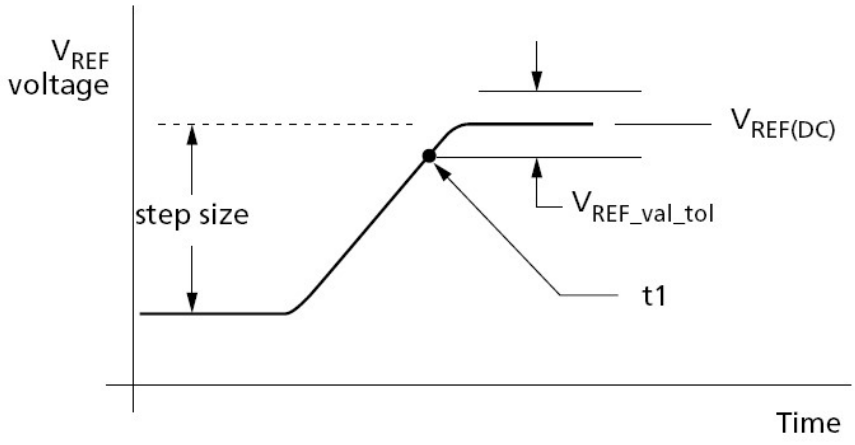


Figure 4-86: $V_{REF(CA)}$ Single-Step Decrement

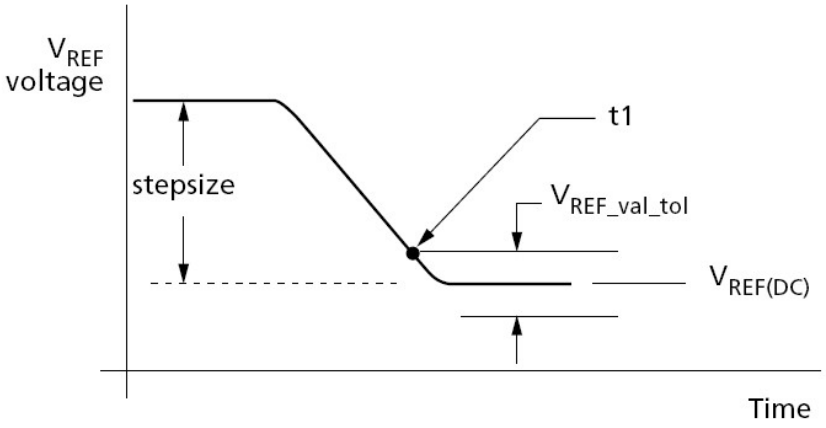


Figure 4-87: $V_{REF(CA)}$ Full Step from $V_{REF,min}$ to $V_{REF,max}$

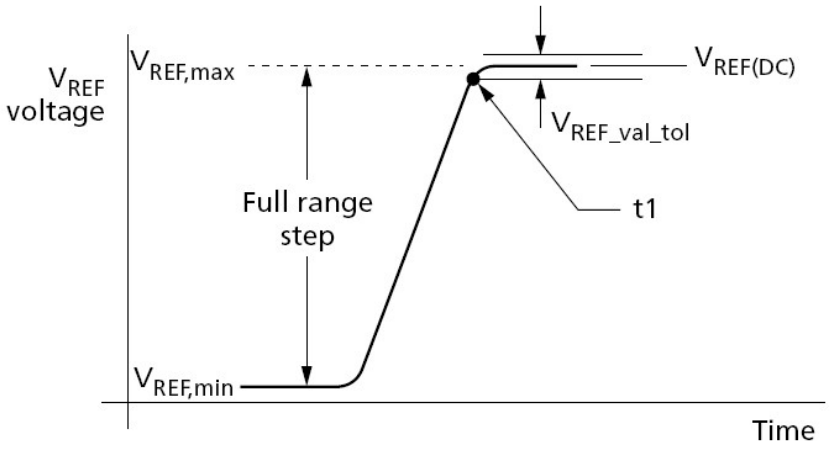
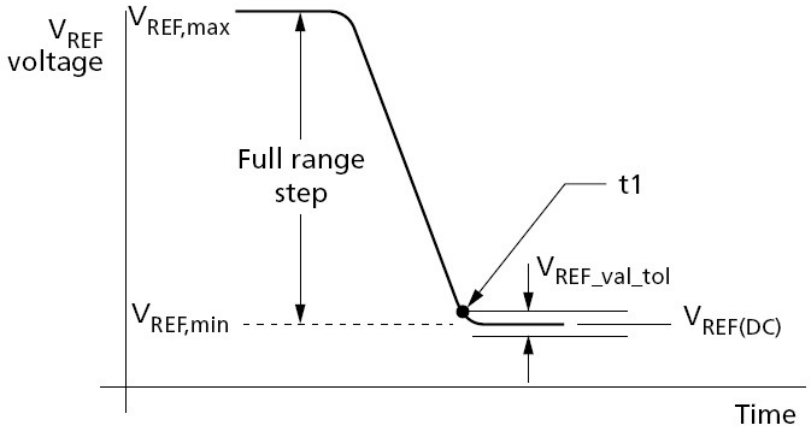


Figure 4-88: $V_{REF(CA)}$ Full Step from $V_{REF,max}$ to $V_{REF,min}$



The following table contains the CA internal V_{REF} specification that will be characterizedat the component level for compliance.

Table 4-107: Internal $V_{REF(CA)}$ Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes
$V_{REF(CA),max\_r0}$	$V_{REF(CA)}$ range-0 MAX operat-ing point	–	–	44.9%	V_{DDQ}	1, 11
$V_{REF(CA),min\_r0}$	$V_{REF(CA)}$ range-0 MIN operat-ing point	15.0%	–	–	V_{DDQ}	1, 11
$V_{REF(CA),max\_r1}$	$V_{REF(CA)}$ range-1 MAX operat-ing point	–	–	62.9%	V_{DDQ}	1, 11
$V_{REF(CA),min\_r1}$	$V_{REF(CA)}$ range-1 MIN operat-ing point	32.9%	–	–	V_{DDQ}	1, 11
$V_{REF(CA),step}$	$V_{REF(CA)}$ step size	0.50%	0.60%	0.70%	V_{DDQ}	2
$V_{REF(CA),set\_tol}$	$V_{REF(CA)}$ set tolerance	–11	0	11	mV	3, 4, 6
		–1.1	0	1.1	mV	3, 5, 7
$^{t}V_{REF}$_TIME-SHORT	$V_{REF(CA)}$ step time	–	–	100	ns	8
$^{t}V_{REF}$_TIME-MIDDLE		–	–	200	ns	12
$^{t}V_{REF}$_TIME-LONG		–	–	250	ns	9
$^{t}V_{REF\_time\_weak}$		–	–	1	ms	13, 14
$V_{REF(CA)\_val\_tol}$	$V_{REF(CA)}$ valid tolerance	–0.10%	0.00%	0.10%	V_{DDQ}	10

Notes:

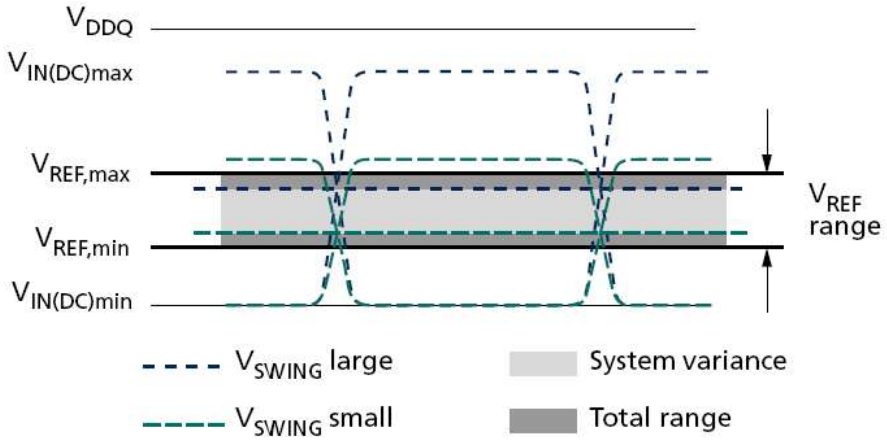
1. $V_{REF(CA)}$ DC voltage referenced to $V_{DD2(DC)}$.
2. $V_{REF(CA)}$ step size increment/decrement range. $V_{REF(CA)}$ at DC level.
3. $V_{REF(CA),new} = V_{REF(CA),old} + n \times V_{REF(CA),step}$; n = number of steps; if increment, use "+"; ifdecrement, use "–".
4. The minimum value of $V_{REF(CA)}$ setting tolerance = $V_{REF(CA),new}$ - 11mV. The maximum valueof $V_{REF(CA)}$ setting tolerance = $V_{REF(CA),new}$ + 11mV. For n > 4.
5. The minimum value of $V_{REF(CA)}$ setting tolerance = $V_{REF(CA),new}$ - 1.1mV. The maximumvalue of $V_{REF(CA)}$ setting tolerance = $V_{REF(CA),new}$ + 1.1mV. For n ≤ 4.
6. Measured by recording the minimum and maximum values of the $V_{REF(CA)}$ output overthe range, drawing a straight line between those points and comparing all other$V_{REF(CA)}$ output settings to that line.
7. Measured by recording the minimum and maximum values of the $V_{REF(CA)}$ output acrossfour consecutive steps (n = 4), drawing a straight line between those points and comparingall other $V_{REF(CA)}$ output settings to that line.
8. Time from MRW command to increment or decrement one step size for $V_{REF(CA)}$.
9. Time from MRW command to increment or decrement $V_{REF,min}$ to $V_{REF,max}$ or $V_{REF,max}$ to$V_{REF,min}$ change across the $V_{REF(CA)}$ range in V_{REF} voltage.
10. Only applicable for DRAM component level test/characterization purposes. Not applicablefor normal mode of operation. V_{REF} valid is to qualify the step times which will becharacterized at the component level.
11. DRAM range-0 or range-1 set by MR12 OP[6].
12. Time from MRW command to increment or decrement more than one step size up to afull range of V_{REF} voltage within the same $V_{REF(CA)}$ range.
13. Applies when VRCG high current mode is not enabled, specified by MR13 [OP3] = 0b.
14. $^{t}V_{REF\_time\_weak}$ covers all $V_{REF(CA)}$ range and value change conditions are applied to$^{t}V_{REF}$_TIME-SHORT/MIDDLE/LONG.

$V_{REF(DQ)}$ Training

The device's internal $V_{REF(DQ)}$ specification parameters are operating voltage range, stepsize, V_{REF} step tolerance, V_{REF} step time and V_{REF} valid level.

The voltage operating range specifies the minimum required V_{REF} setting range forLPDDR4 devices. The minimum range is defined by $V_{REF,max}$ and $V_{REF,min}$.

Figure 4-89: V_{REF} Operating Range ($V_{REF,max}$, $V_{REF,min}$)

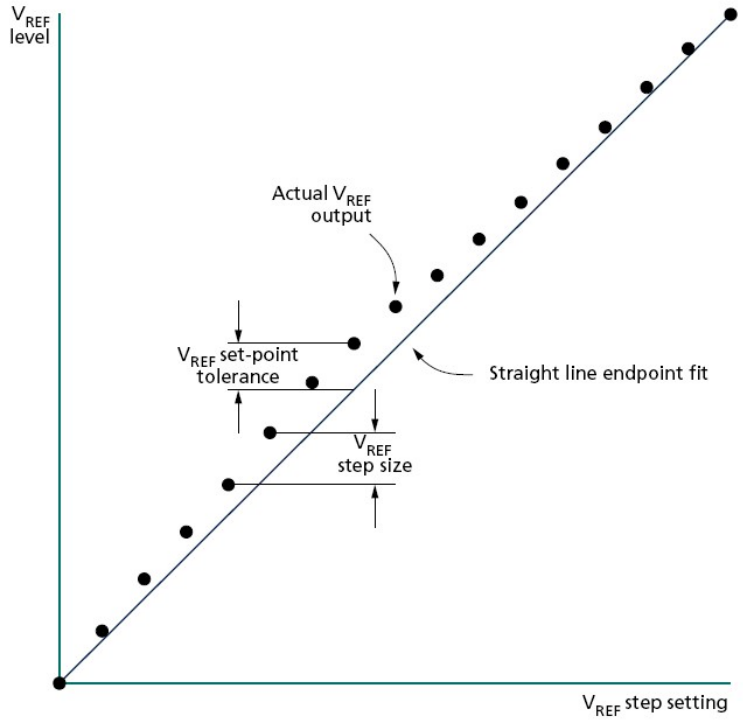


The V_{REF} step size is defined as the step size between adjacent steps. However, for a givendesign, the device has one value for V_{REF} step size that falls within the given range.

The V_{REF} set tolerance is the variation in the V_{REF} voltage from the ideal setting. This accountsfor accumulated error over multiple steps. There are two ranges for V_{REF} set toleranceuncertainty. The range of V_{REF} set tolerance uncertainty is a function of thenumber of steps n.

The V_{REF} set tolerance is measured with respect to the ideal line that is based on the twoendpoints, where the endpoints are at the minimum and maximum V_{REF} values for aspecified range.

Figure 4-90: V_{REF} Set Tolerance and Step Size



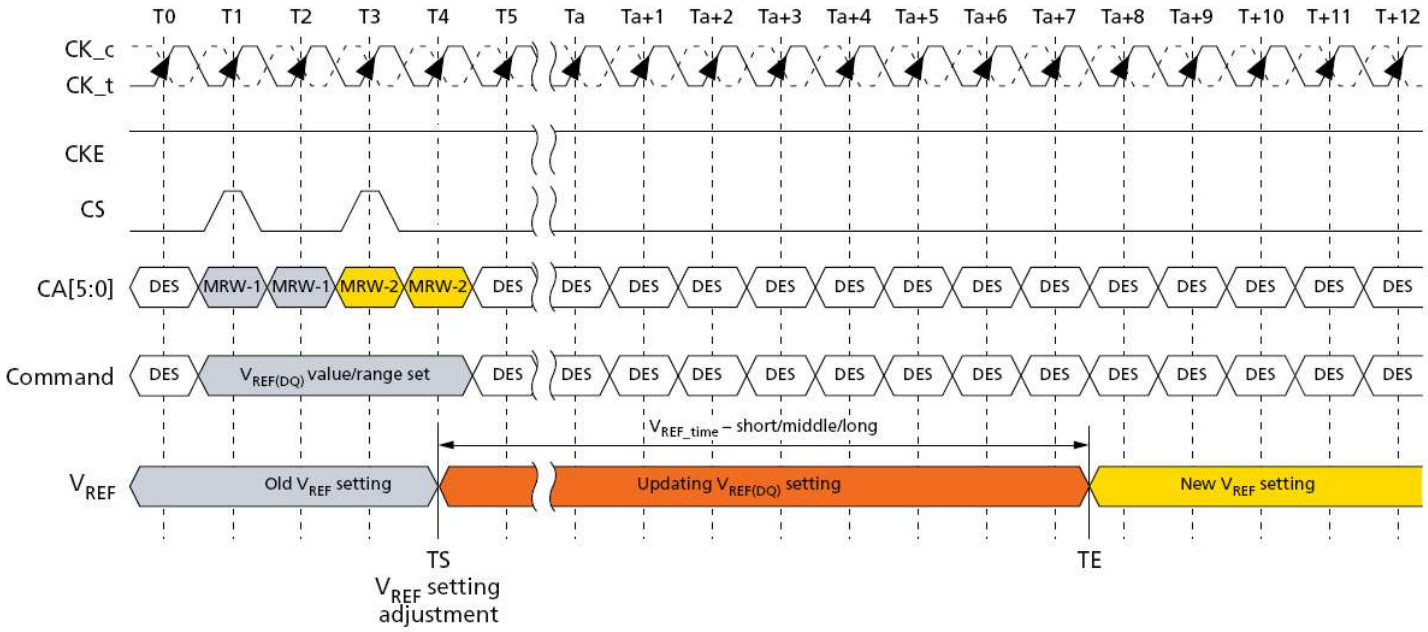
The V_{REF} increment/decrement step times are defined by $^{t}V_{REF}$_TIME-SHORT,$^{t}V_{REF}$_TIME-MIDDLE and $^{t}V_{REF}$_TIME-LONG. The $^{t}V_{REF}$_TIME-SHORT, $^{t}V_{REF}$_TIMEMIDDLEand $^{t}V_{REF}$_TIME-LONG times are defined from TS to TE in the following figurewhere TE is referenced to when the V_{REF} voltage is at the final DC level within the V_{REF}valid tolerance (V_{REF,VAL_TOL}).

The V_{REF} valid level is defined by V_{REF,VAL_TOL} to qualify the step time TE (see the figurebelow). This parameter is used to ensure an adequate RC time constant behavior of thevoltage level change after any V_{REF} increment/decrement adjustment.This parameter isonly applicable for DRAM component level validation/characterization.
$^{t}V_{REF}$_TIME-SHORT is for a single step size increment/decrement change in the V_{REF}voltage.

$^{t}V_{REF}$_TIME-MIDDLE is at least two step sizes of increment/decrement change in the$V_{REF(DQ)}$ range in the V_{REF}voltage.

$^{t}V_{REF}$_TIME-LONG is the time including and up to the full range of V_{REF} (MIN to MAX orMAX to MIN) across the $V_{REF(DQ)}$ range in V_{REF} voltage.

Figure 4-91: $V_{REF(DQ)}$ Transition Time for Short, Middle, or Long Changes



Notes:
1. TS is referenced to MRW command clock.
2. TE is referenced to V_{REF,VAL_TOL}.

The MRW command to the mode register bits are defined as:
MR14 OP[5:0]: $V_{REF(DQ)}$ setting
MR14 OP[6]: $V_{REF(DQ)}$ range

The minimum time required between two V_{REF} MRW commands is $^{t}V_{REF}$_TIME-SHORTfor a single step and $^{t}V_{REF}$_TIME-MIDDLE for a full voltage range step.

Figure 4-92: $V_{REF(DQ)}$ Single-Step Size Increment

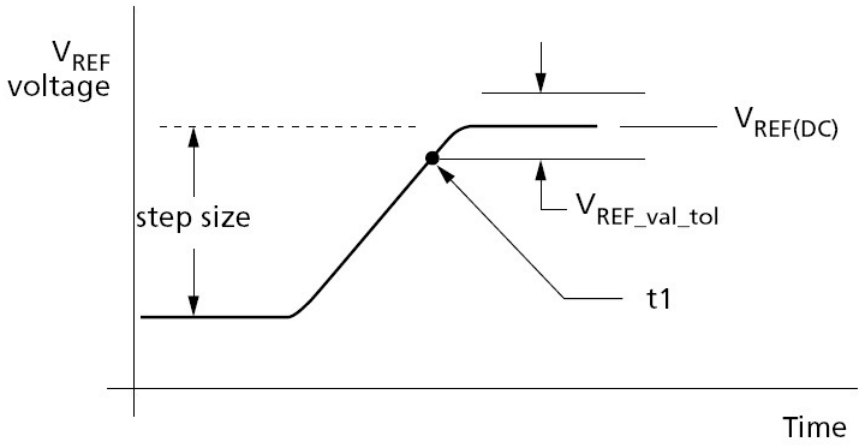


Figure 4-93: $V_{REF(DQ)}$ Single-Step Size Decrement

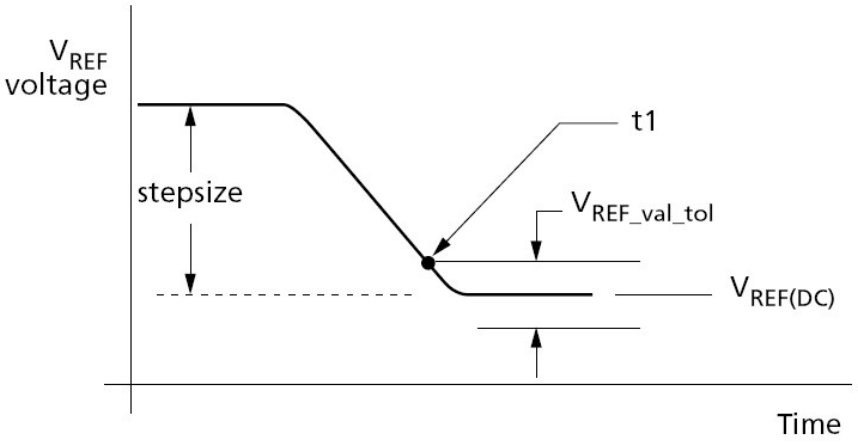


Figure 4-94: $V_{REF(DQ)}$ Full Step from $V_{REF,min}$ to $V_{REF,max}$

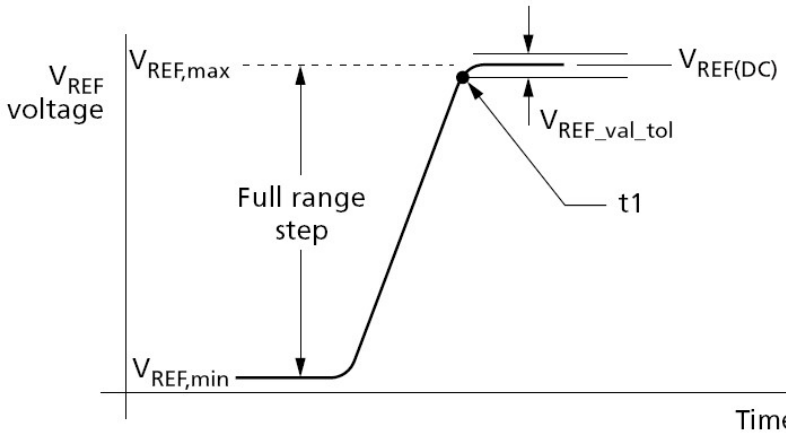
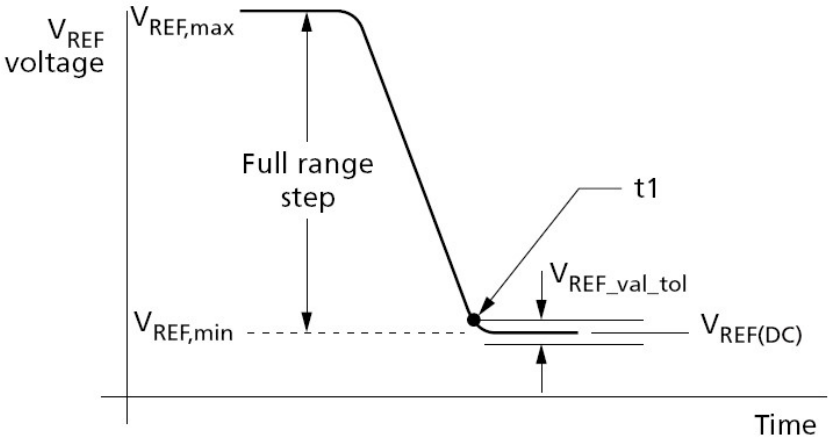


Figure 4-95: $V_{REF(DQ)}$ Full Step from $V_{REF,max}$ to $V_{REF,min}$



The following table contains the DQ internal V_{REF} specification that will be characterizedat the component level for compliance.

Table 4-108: Internal $V_{REF(DQ)}$ Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes
$V_{REF(DQ),max\_r0}$	V_{REF} MAX operating point Range-0	–	–	44.9%	V_{DDQ}	1, 11
$V_{REF(DQ),min\_r0}$	V_{REF} MIN operating point Range-0	15.0%	–	–	V_{DDQ}	1, 11
$V_{REF(DQ),max\_r1}$	V_{REF} MAX operating point Range-1	–	–	62.9%	V_{DDQ}	1, 11
$V_{REF(DQ),min\_r1}$	V_{REF} MIN operating point Range-1	32.9%	–	–	V_{DDQ}	1, 11
$V_{REF(DQ),step}$	$V_{REF(DQ)}$ step size	0.50%	0.60%	0.70%	V_{DDQ}	2
$V_{REF(DQ),set\_tol}$	$V_{REF(DQ)}$ set tolerance	–11	0	11	mV	3, 4, 6
		-1.1	0	1.1	mV	3, 5, 7
$^{t}V_{REF}$_TIME-SHORT	$V_{REF(DQ)}$ step time	–	–	100	ns	8
$^{t}V_{REF}$_TIME-MIDDLE		–	–	200	ns	12
$^{t}V_{REF}$_TIME-LONG		–	–	250	ns	9
$^{t}V_{REF\_time\_weak}$		–	–	1	ms	13, 14
$V_{REF(DQ)\_val\_tol}$	$V_{REF(DQ)}$ valid tolerance	–0.10%	0.00%	0.10%	V_{DDQ}	10

Notes:

1. $V_{REF(DQ)}$ DC voltage referenced to $V_{DDQ(DC)}$.
2. $V_{REF(DQ)}$ step size increment/decrement range. $V_{REF(DQ)}$ at DC level.
3. $V_{REF(DQ),new} = V_{REF(DQ),old} + n \times V_{REF(DQ),step}$; n = number of steps; if increment, use "+"; ifdecrement, use "–".
4. The minimum value of $V_{REF(DQ)}$ setting tolerance = $V_{REF(DQ),new}$ - 11mV. The maximumvalue of $V_{REF(DQ)}$ setting tolerance = $V_{REF(DQ),new}$ + 11mV. For n > 4.
5. The minimum value of $V_{REF(DQ)}$setting tolerance = $V_{REF(DQ),new}$ - 1.1mV. The maximumvalue of $V_{REF(DQ)}$ setting tolerance = $V_{REF(DQ),new}$ + 1.1mV. For n ≤ 4.
6. Measured by recording the minimum and maximum values of the $V_{REF(DQ)}$ output overthe range, drawing a straight linebetween those points and comparing all other$V_{REF(DQ)}$ output settings to that line.
7. Measured by recording the minimum and maximum values of the $V_{REF(DQ)}$ output acrossfour consecutive steps (n = 4), drawing a straight line between those points and comparingall other $V_{REF(DQ)}$ output settings to that line.
8. Time from MRW command to increment or decrement one step size for $V_{REF(DQ)}$.
9. Time from MRW command to increment or decrement $V_{REF,min}$ to $V_{REF,max}$ or $V_{REF,max}$ to$V_{REF,min}$ change across the $V_{REF(DQ)}$ Range in $V_{REF(DQ)}$ Voltage.

10. Only applicable for DRAM component level test/characterization purposes. Not applicablefor normal mode of operation. V_{REF} valid is to qualify the step times which will becharacterized at the component level.
11. DRAM range-0 or range-1 set by MR14 OP[6].
12. Time from MRW command to increment or decrement more than one step size up to afull range of V_{REF} voltage within the same $V_{REF(DQ)}$ range.
13. Applies when VRCG high current mode is not enabled, specified by MR13 [OP3] = 0.
14. $^{t}V_{REF}$_time_weak covers all $V_{REF(DQ)}$ Range and Value change conditions are applied to$^{t}V_{REF}$_TIME-SHOR/MIDDLE/LONG.

4.29 Command Bus Training

Command Bus Training Mode

The command bus must be trained before enabling termination for high-frequency operation.The device provides an internal $V_{REF(CA)}$ that defaults to a level suitable for unterminated,low-frequency operation, but the$V_{REF(CA)}$must be trained to achieve suitablereceiver voltage margin for terminated, high-frequency operation.

The training mode described here centers the internal $V_{REF(CA)}$ in the CA data eye and atthe same time allows for timing adjustments of the CS and CA signals to meet setup/hold requirements. Because it can be difficult to capture commands prior to trainingthe CA inputs, the training mode described here uses a minimum of external commandsto enter, train, and exit the CA bus training mode.

The die has a bond-pad (ODT_CA) to control the command bus termination for multirankoperation. Other mode register bits are provided to fine tune termination controlin a variety of system configuration. See On-Die Termination for more information.

The device uses frequency set points to enable multiple operating settings for the die.

The device defaults to FSP-OP[0] at power-up, which has the default settings to operatein un-terminated, low-frequency environments. Prior to training, the terminationshould be enabled for one die in each channel by setting MR13 OP[6] = 1b (FSP-WR[1])and setting all other mode register bits for FSP-OP[1] to the desired settings for highfrequencyoperation. Upon training entry, the device will automatically switch to FSPOP[1] and use the high-frequency settings during training (See the Command BusTraining Entry Timing figure for more information on FSP-OP register sets). Upon trainingexit, the device will automatically switch back to FSP-OP[0], returning to a "knowngood"state for unterminated, low-frequency operation.

To enter command bus training mode, issue a MRW-1 command followed by a MRW-2command to set MR13 OP[0] = 1b (command bus training mode enabled).

After time ^{t}MRD, CKE may be set LOW, causing the device to switch to FSP-OP[1], andcompleting the entry into command bus training mode.

A status DQS_t, DQS_c, DQ, and DMI are as noted below; the DQ ODT state will be followedby FREQUENCY SET POINT function except in the case of output pins.

- DQS_t[0], DQS_c[0] become input pins for capturing DQ[6:0] levels by toggling.
- DQ[5:0] become input pins for setting $V_{REF(CA)}$ level.
- DQ[6] becomes an input pin for setting $V_{REF(CA)}$ range.
- DQ[7] and DMI[0] become input pins, and their input level is valid or floating.
- DQ[13:8] become output pins to feedback, capturing value via the command bus usingthe CS signal.
- DQS_t[1], DQS_c[1], DMI[1], and DQ[15:14] become output pins or are disabled,meaning the device may be driven to a valid level or may be left floating.

At time ^{t}CAENT later, the device may change its $V_{REF(CA)}$ range and value using inputsignals DQS_t[0], DQS_c[0], and DQ[6:0] from existing value that is set via MR12OP[6:0]. The mapping between MR12 OP code and DQs is shown below. At least one$V_{REF(CA)}$ setting is required before proceeding to the next training step.

Table 4-109: Mapping MR12 Op Code and DQ Numbers

	Mapping						
MR12 OP code	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQ number	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0

The new $V_{REF(CA)}$ value must "settle" for time ^{t}VREFCA_Long before attempting to latchCA information.

Note:
If DQ ODT is enabled in MR11-OP[2:0], then the SDRAM will terminate the DQlanes during command bus training whenentering $V_{REF(CA)}$ range and values onDQ[6:0].
To verify that the receiver has the correct $V_{REF(CA)}$ setting, and to further train the CA eyerelative to clock (CK), values latchedat the receiver on the CA bus are asynchronouslyoutput to the DQ bus.

To exit command bus training mode, drive CKE HIGH, and after time ^{t}VREFCA_Long,issue the MRW-1 command followed bythe MRW-2 command to set MR13 OP[0] = 0b.After time tMRW, the device is ready for normal operation. After training exit, the
devicewill automatically switch back to the FSP-OP registers that were in use prior to training.

Command bus training (CBT) may be executed from the idle or self refresh state. Whenexecuting CBT within the self refreshstate, the device must not be in a power-downstate (for example, CKE must be HIGH prior to training entry). CBT entry and exitis thesame, regardless of the state from which CBT is initiated.

Training Sequence for Single-Rank Systems

The sequence example shown here assumes an initial low-frequency, non-terminatingoperating point training a high-frequency, terminating operating point. The **bold text**shows high-frequency instructions. Any operating point may be trained from anyknown good operating point.

1. Set MR13 OP[6] = 1b to enable writing to frequency set point 1 (FSP-WR[1]) (orFSP-OP[0]).
2. Write FSP-WR[1] (or FSP-WR[0]) registers for all channels to set up high-frequencyoperating parameters.
3. Issue MRW-1 and MRW-2 commands to enter command bus training mode.
4. Drive CKE LOW, **and change CK frequency to the high-frequency operatingpoint.**
5. **Perform command bus training ($V_{REF(CA)}$, CS, and CA).**
6. **Exit training by driving CKE HIGH**, change CK frequency to the low-frequencyoperating point, and issueMRW-1 and MRW-2 commands. When CKE is drivenHIGH, the device will automatically switch back to theFSP-OP registers that werein use prior to training (trained values are not retained).
7. Write the trained values to FSP-WR[1] (or FSP-WR[0]) by issuing MRW-1 andMRW-2 commands to the SDRAMand setting all applicable mode register parameters.
8. Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[1](or FSP-OP[0]), to turn ontermination, **and change CK frequency to the high-frequencyoperating point. At this point the commandbus is trained and you mayproceed to other training or normal operation.**

Training Sequence for Multiple-Rank Systems

The sequence example shown here is assuming an initial low-frequency operatingpoint, training a high-frequency operating point. The **bold text** shows high-frequencyinstructions. Any operating point may be trained from any known good operating point.

1. Set MR13 OP[6] = 1b to enable writing to frequency set point 1 (FSP-WR[1]) (orFSP-WR[0]).
2. Write FSP-WR[1] (or FSP-WR[0]) registers for all channels and ranks to set uphigh-frequency operatingparameters.
3. Read MR0 OP[7] on all channels and ranks to determine which die are terminating,signified by MR0 OP[7] = 1b.
4. Issue MRW-1 and MRW-2 commands to enter command bus training mode onthe terminating rank.
5. Drive CKE LOW on the terminating rank (or all ranks), **and change CK frequencyto the high-frequencyoperating point.**
6. **Perform command bus training on the terminating rank ($V_{REF(CA)}$, CS, and CA).**

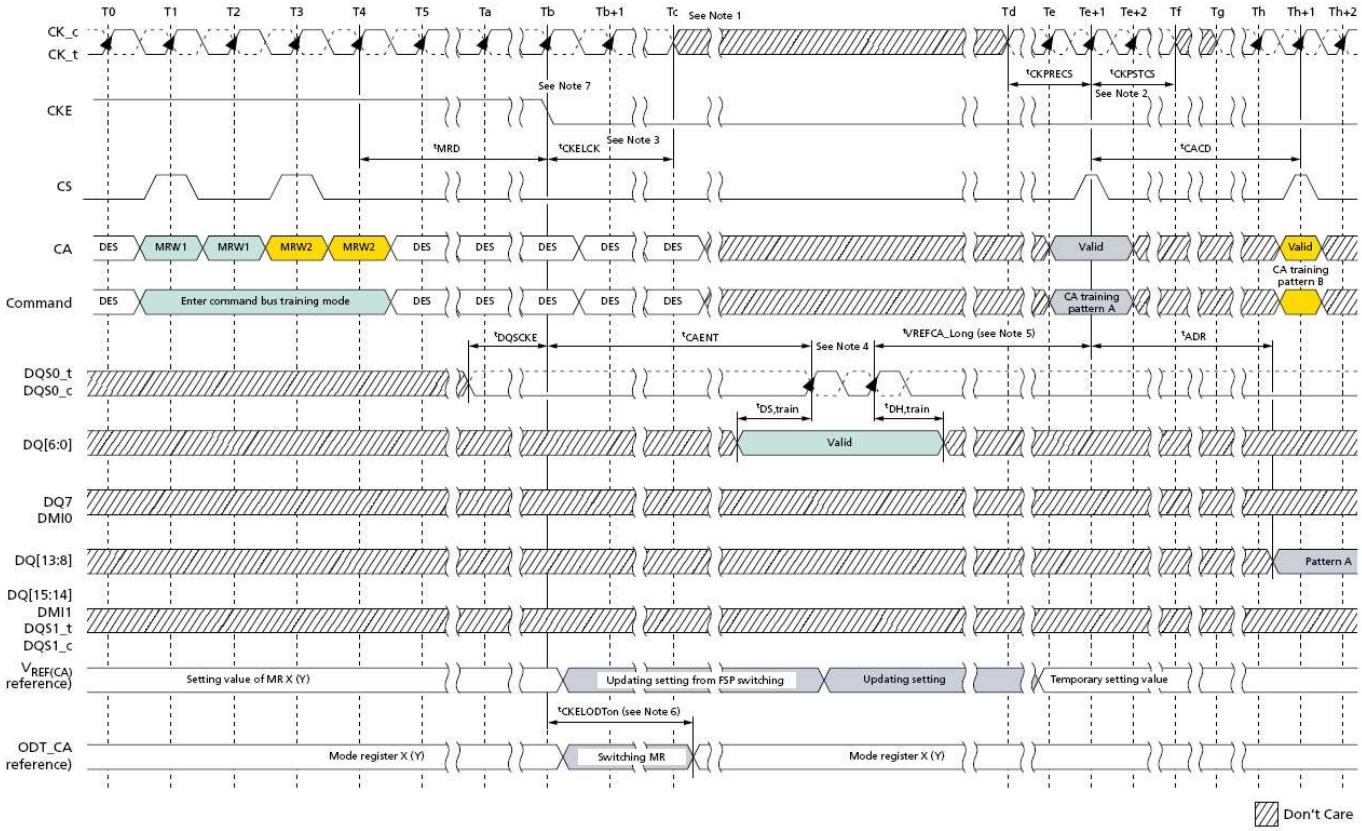
7. **Exit training by driving CKE HIGH**, change CK frequency to the low-frequencyoperating point, and issueMRW-1 and MRW-2 commands to write the trainedvalues to FSP-WR[1] (or FSP-WR[0]). When CKE is drivenHIGH, the SDRAM willautomatically switch back to the FSP-OP registers that were in use prior to training(trainedvalues are not retained by the device).
8. Issue MRW-1 and MRW-2 commands to enter training mode on the non-terminatingrank (but keep CKE HIGH).
9. Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[1](or FSP-OP[0]), to turn ontermination, **and change CK frequency to the high-frequencyoperating point.**
10. **Drive CKE LOW on the non-terminating (or all) ranks. The non-terminatingrank(s) will now be usingFSP-OP[1] (or FSP-OP[0]).**
11. **Perform command bus training on the non-terminating rank ($V_{REF(CA)}$), CS, andCA).**
12. **Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSPOP[0] (or FSP-OP[1]) to turnoff termination.**
13. **Exit training by driving CKE HIGH on the non-terminating rank**, change CK frequencyto the low-frequencyoperating point, and issue MRW-1 and MRW-2 commands.When CKE is driven HIGH, the device willautomatically switch back tothe FSP-OP registers that were in use prior to training (that is, trained values arenotretained by the device).
14. Write the trained values to FSP-WR[1] (or FSP-WR[0]) by issuing MRW-1 andMRW-2 commands and setting allapplicable mode register parameters.
15. Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[1](or FSP-OP[0]), to turn ontermination, **and change CK frequency to the high-frequencyoperating point. At this point the commandbus is trained for both ranksand the user may proceed to other training or normal operation.**

Relation Between CA Input Pin and DQ Output Pin

Table 4-110: Mapping of CA Input Pin and DQ Output Pin

	Mapping					
CA number	CA5	CA4	CA3	CA2	CA1	CA0
DQ number	DQ13	DQ12	DQ11	DQ10	DQ9	DQ8

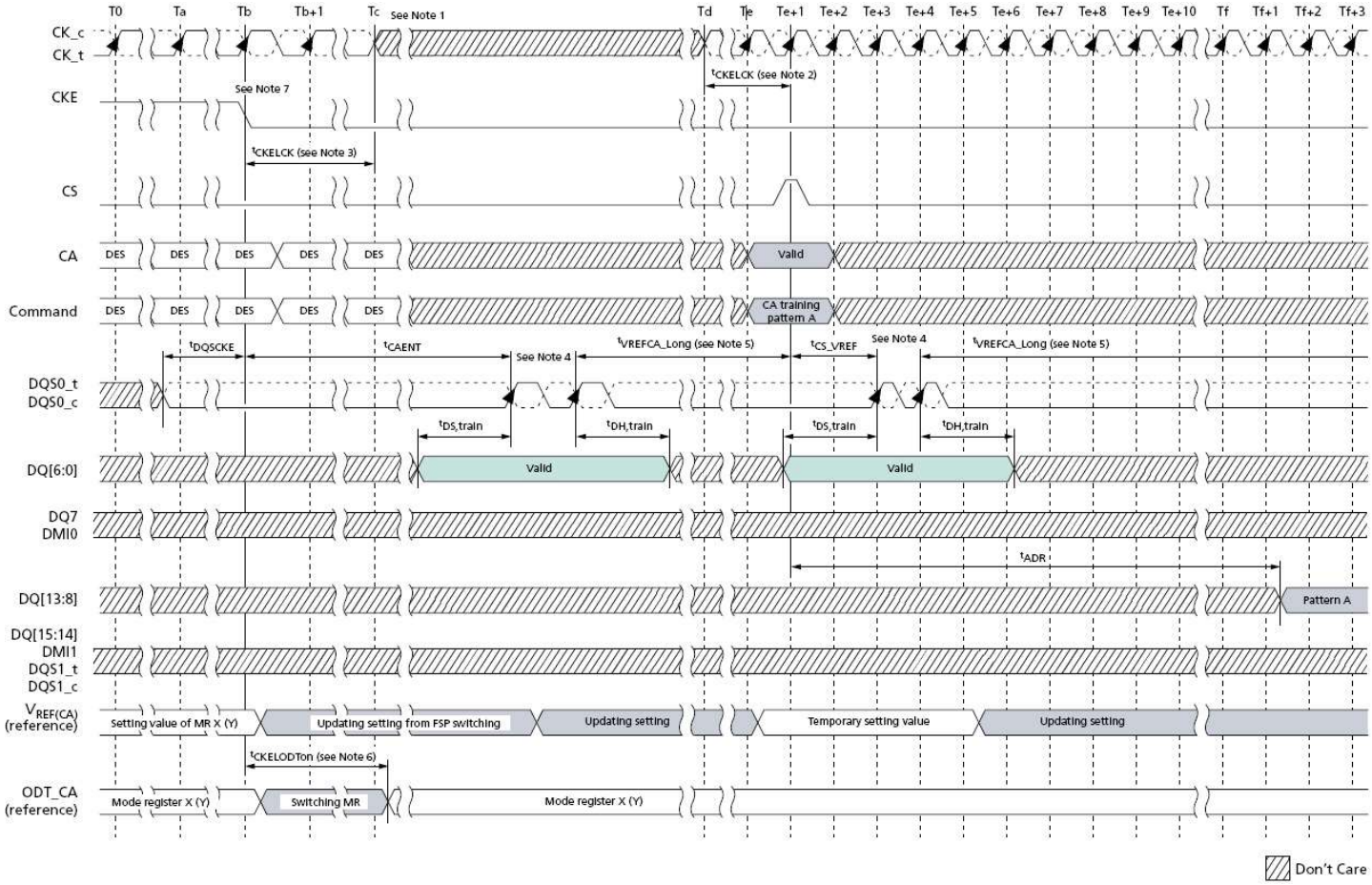
Figure 4-96: Command Bus Training Mode Entry – CA Training Pattern I/O with $V_{REF(CA)}$ Value Update



Notes:

1. After ^{t}CKELCK, the clock can be stopped or the frequency changed any time.
2. The input clock condition should be satisfied ^{t}CKPRECS and ^{t}CKPSTCS.
3. Continue to drive CK, and hold CA and CS LOW, until ^{t}CKELCK after CKE is LOW (whichdisables command decoding).
4. The device may or may not capture the first rising edge of DQS_t/DQS_c due to an unstablefirst rising edge. Therefore, atleast two consecutive pulses of DQS signal input isrequired every for DQS input signal while capturing DQ[6:0] signals. Thecaptured valueof the DQ[6:0] signal level by each DQS edge may be overwritten at any time and thedevice will temporarilyupdate the $V_{REF(CA)}$ setting of MR12 after time ^{t}VREFCA_Long.
5. ^{t}VREFCA_Long may be reduced to ^{t}VREFCA_Short if the following conditions are met: 1)The new V_{REF} setting is a singlestep above or below the old V_{REF} setting; 2) The DQSpulses a single time, or the new V_{REF} setting value on DQ[6:0] is static and meets^{t}DS,train/ ^{t}DH,train for every DQS pulse applied.
6. When CKE is driven LOW, the device will switch its FSP-OP registers to use the alternate(non-active) set. For example, if the device is currently using FSP-OP[0], then it willswitch to FSP-OP[1] when CKE is driven LOW. All operating parameters should be writtento the alternate mode registers before entering command bus training to ensurethat ODT settings, RL/WL/nWR setting, and so forth, are set to the correct values.
7. When CKE is driven LOW in command bus training mode, the device will change operationto the alternate FSP, that is, theinverse of the FSP programmed in the FSP-OP moderegister.

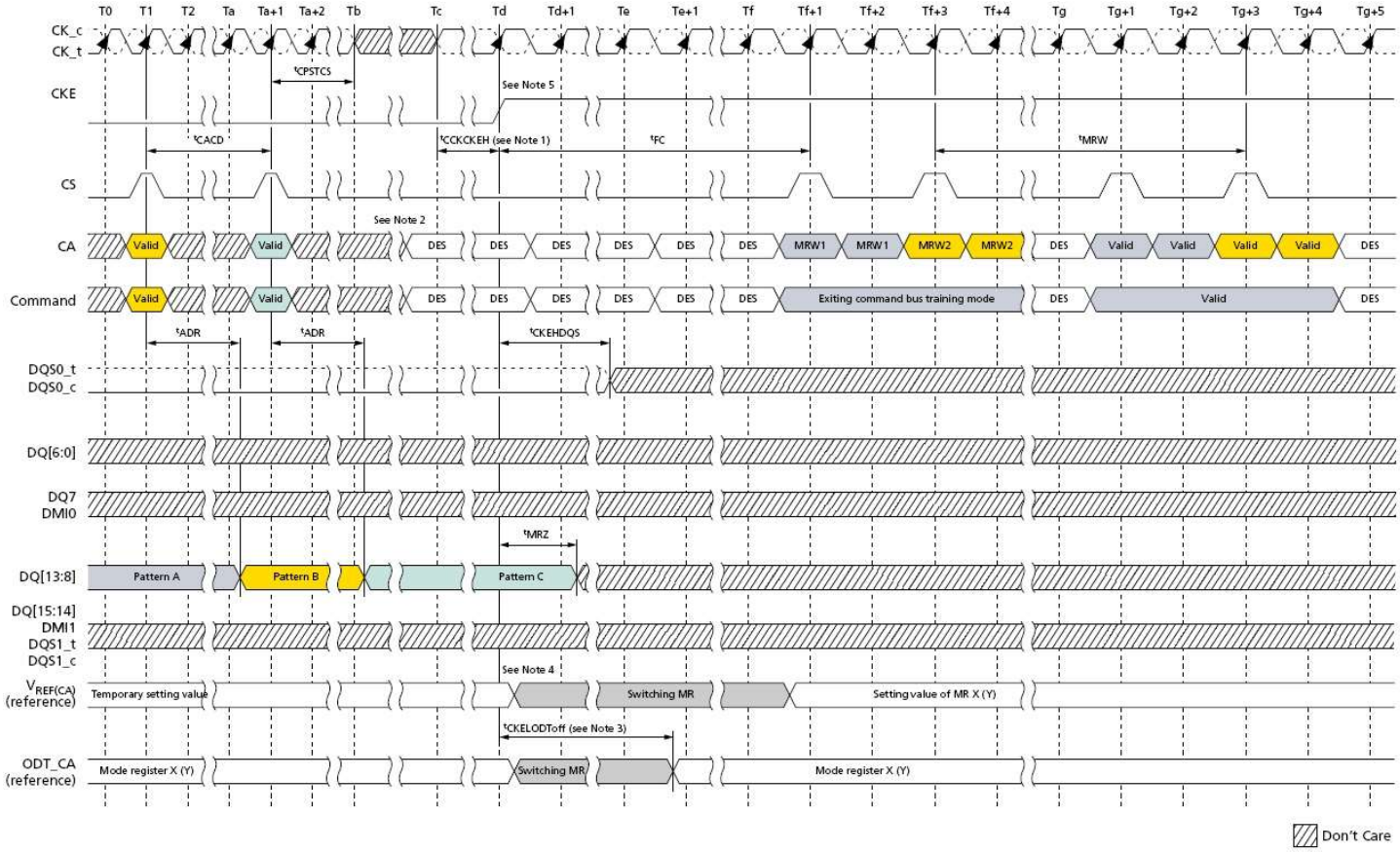
Figure 4-97: Consecutive $V_{REF(CA)}$ Value Update



Notes:

1. After tCKELCK, the clock can be stopped or the frequency changed any time.
2. The input clock condition should be satisfied tCKPRECS and tCKPSTCS.
3. Continue to drive CK, and hold CA and CS LOW, until tCKELCK after CKE is LOW (whichdisables command decoding).
4. The device may or may not capture the first rising edge of DQS_t/DQS_c due to an unstablefirst rising edge. Therefore, atleast two consecutive pulses of DQS signal input isrequired every for DQS input signal while capturing DQ[6:0] signals. Thecaptured valueof the DQ[6:0] signal level by each DQS edge may be overwritten at any time and thedevice will temporarilyupdate the $V_{REF(CA)}$ setting of MR12 after time tVREFCA_Long.
5. tVREFCA_Long may be reduced to tVREFCA_Short if the following conditions are met: 1)The new V_{REF} setting is a singlestep above or below the old V_{REF} setting; 2) The DQSpulses a single time, or the new V_{REF} setting value on DQ[6:0] is static and meetstDS,train/ tDH,train for every DQS pulse applied.
6. When CKE is driven LOW, the device will switch its FSP-OP registers to use the alternate(non-active) set. For example, if the device is currently using FSP-OP[0], then it willswitch to FSP-OP[1] when CKE is driven LOW. All operating parameters should be writtento the alternate mode registers before entering command bus training to ensurethat ODT settings, RL/WL/nWR setting, and so forth, are set to the correct values.
7. When CKE is driven LOW in command bus training mode, the device will change operationto the alternate FSP, that is, theinverse of the FSP programmed in the FSP-OP moderegister.

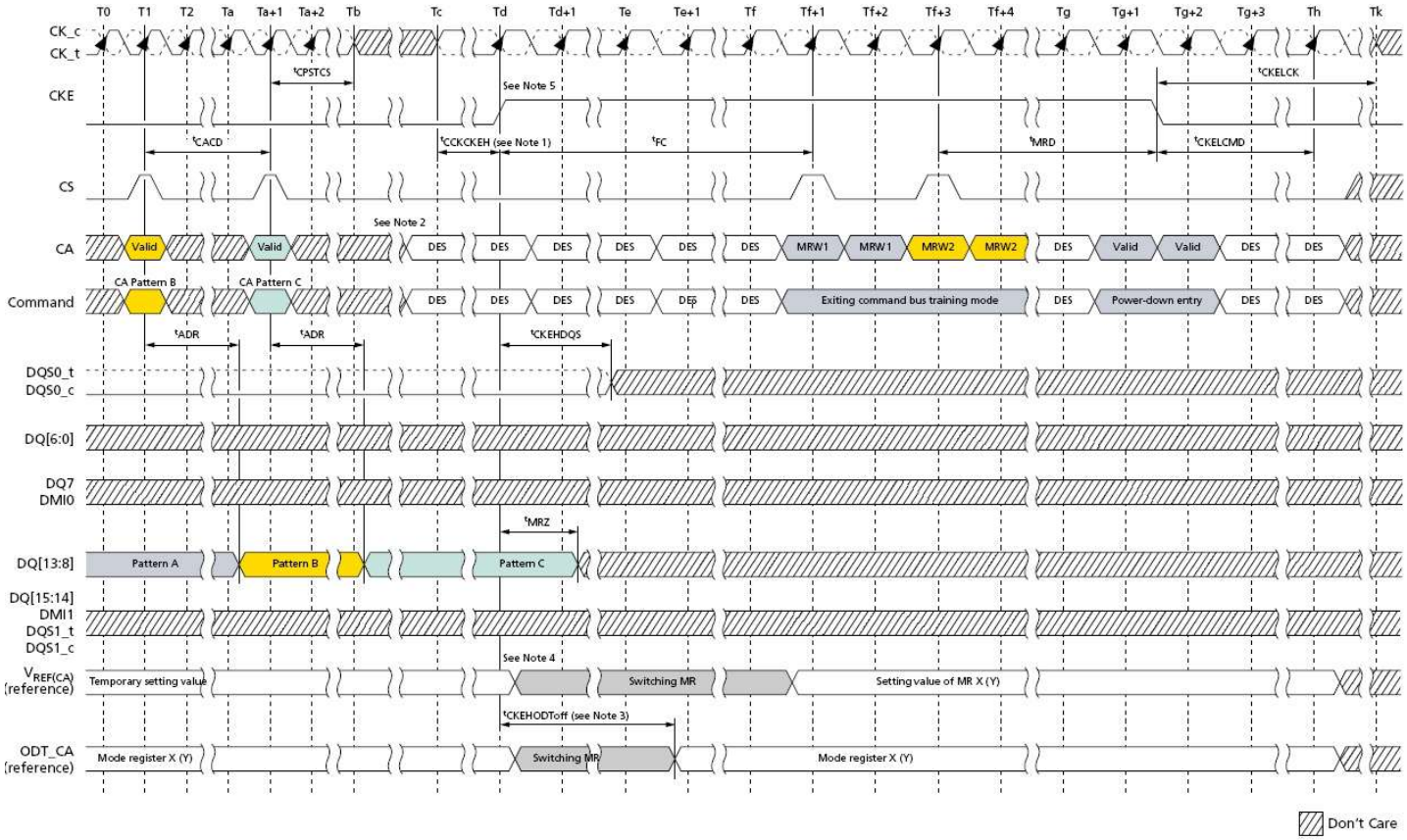
Figure 4-98: Command Bus Training Mode Exit with Valid Command



Notes:

1. The clock can be stopped or the frequency changed any time before ^{t}CKCKEH. CK mustmeet ^{t}CKCKEH before CKE isdriven HIGH. When CKE is driven HIGH, the clock frequencymust be returned to the original frequency (that is, thefrequency corresponding to theFSP at command bus training mode entry.
2. CS and CA[5:0] must be deselected (LOW) ^{t}CKCKEH before CKE is driven HIGH.
3. When CKE is driven HIGH, ODT_CA will revert to the state/value defined by FSP-OP priorto command bus training modeentry, that is, the original frequency set point (FSP-OP,MR13-OP[7]). For example, if the device was using FSP-OP[1] fortraining, then it willswitch to FSP-OP[0] when CKE is driven HIGH.
4. Training values are not retained by the device and must be written to the FSP-OP registerset before returning to operation atthe trained frequency. For example, $V_{REF(CA)}$ willreturn to the value programmed in the original set point.
5. When CKE is driven HIGH, the device will revert to the FSP in operation at command bustraining mode entry.

Figure 4-99: Command Bus Training Mode Exit with Power-Down Entry



Notes:

1. The clock can be stopped or the frequency changed any time before ^{t}CKCKEH. CK mustmeet ^{t}CKCKEH before CKE isdriven HIGH. When CKE is driven HIGH, the clock frequencymust be returned to the original frequency (that is, thefrequency corresponding to theFSP at command bus training mode entry.
2. CS and CA[5:0] must be deselected (LOW) ^{t}CKCKEH before CKE is driven HIGH.
3. When CKE is driven HIGH, ODT_CA will revert to the state/value defined by FSP-OP priorto command bus training modeentry, that is, the original frequency set point (FSP-OP,MR13-OP[7]). For example, if the device was using FSP-OP[1] fortraining, then it willswitch to FSP-OP[0] when CKE is driven HIGH.
4. Training values are not retained by the device and must be written to the FSP-OP registerset before returning to operation atthe trained frequency. For example, $V_{REF(CA)}$ willreturn to the value programmed in the original set point.
5. When CKE is driven HIGH, the device will revert to the FSP in operation at command busraining mode entry.

4.30 Write Leveling

Mode Register Write-WR Leveling Mode

To improve signal-integrity performance, the device provides a write leveling feature tcompensate for CK-to-DQS timing skew, affecting timing parameters such as ^{t}DQSS^{t}DSS, and ^{t}DSH. The memory controller uses the write leveling feature to receive feedbacfrom the device, enabling it to adjust the clock-to-data strobe signal relationshipfor each DQS_t/DQS_c signal pair. The device samples the clock state with the risinedge of DQS signals and asynchronously feeds back to the memory controller. Thmemory controller references this feedback to adjust the clock-to-data strobe signal relationshipfor each DQS_t/DQS_c signal pair.

All data bits (DQ[7:0] for DQS[0] and DQ[15:8] for DQS[1]) carry the training feedback tthe controller. Both DQS signals in each channel must be leveled independently. Writeleveling entry/exit is independent between channels for dual channel devices.

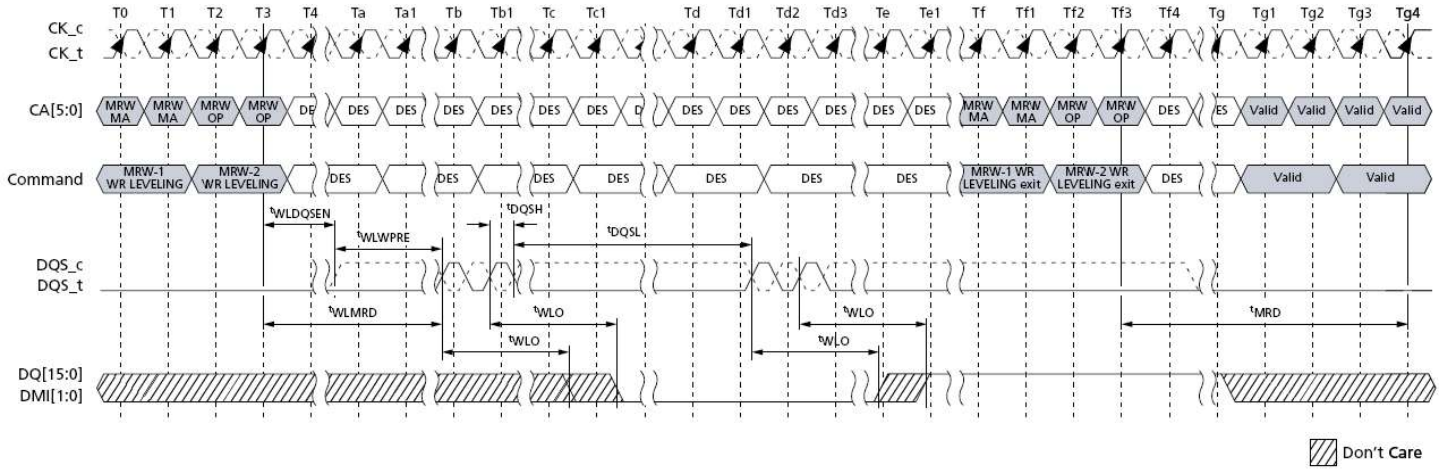
The device enters write leveling mode when mode register MR2-OP[7] is set HIGH.When entering write leveling mode, the state of the DQ pins is undefined. During writleveling mode, only DESELECT commands, or a MRW command to exit the WRITLEVELING operation, are allowed. Depending on the absolute values of tQSL and tQSin the application, the value of tDQSS may have to be better than the limits provided inthe AC Timing Parameters section in order to satisfy the ^{t}DSS and tDSH specifications.Upon completion of the WRITE LEVELING operation, the device exits write levelinmode when MR2-OP[7] is reset LOW.

Write leveling should be performed before write training (DQS2DQ training).

Write Leveling Procedure

1. Enter write leveling mode by setting MR2-OP[7]=1.
2. Once in write leveling mode, DQS_t must be driven LOW and DQS_c HIGH after adelay of ^{t}WLDQSEN.
3. Wait for a time ^{t}WLDQSEN before providing the first DQS signal input. The delaytime ^{t}WLMRD(MAX) iscontroller-dependent.
4. The device may or may not capture the first rising edge of DQS_t due to an unstablefirst rising edge; therefore, atleast two consecutive pulses of DQS signal inputis required for every DQS input signal during write training mode.The capturedclock level for each DQS edge is overwritten, and the device provides asynchronousfeedback on allDQ bits after time tWLO.
5. The feedback provided by the device is referenced by the controller to incrementor decrement the DQS_t and/orDQS_c delay settings.
6. Repeat steps 4 and 5 until the proper DQS_t/DQS_c delay is established.
7. Exit write leveling mode by setting MR2-OP[7] = 0.

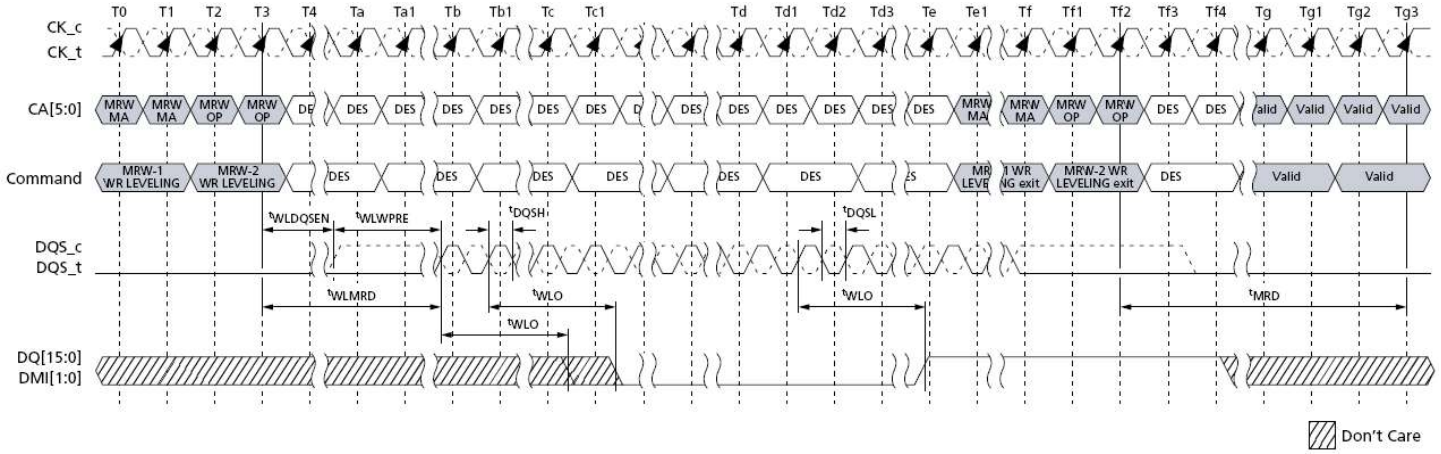
Figure 4-100: Write Leveling Timing – ^{t}DQSL (MAX)



Note:

1. Clock can be stopped except during DQS toggle period (CK_t = LOW, CK_c = HIGH).However, a stable clock prior to sampling is required to ensure timing accuracy.

Figure 4-101: Write Leveling Timing – ^{t}DQSL (MIN)



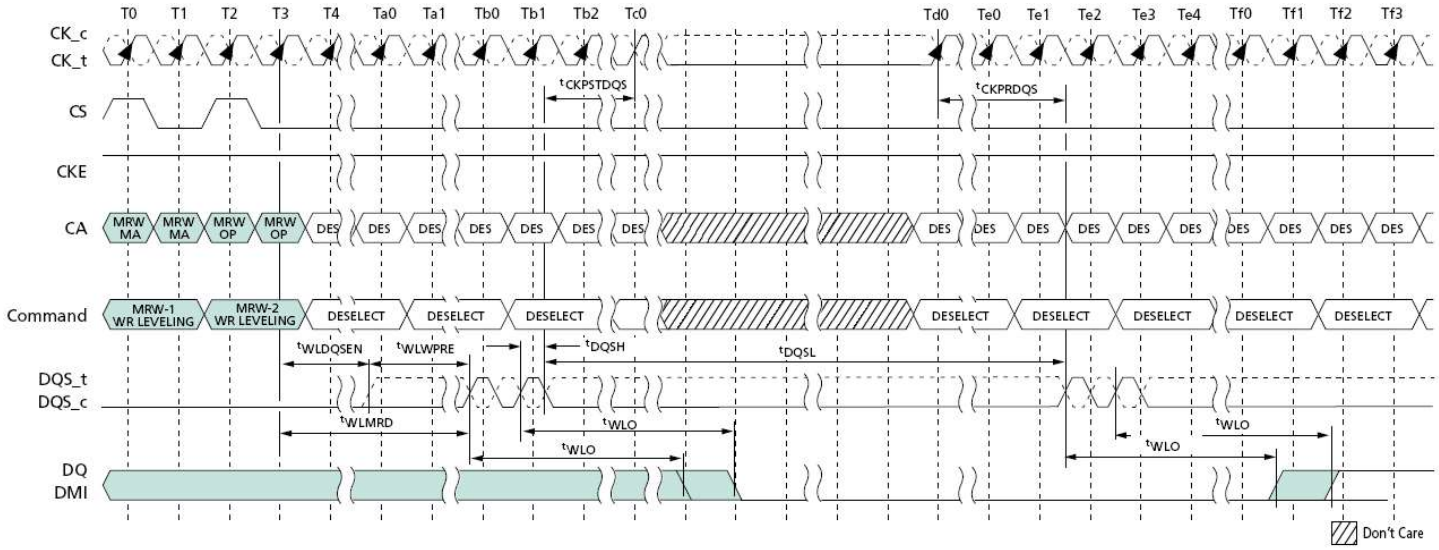
Note:

1. Clock can be stopped except during DQS toggle period (CK_t = LOW, CK_c = HIGH).However, a stable clock prior to sampling is required to ensure timing accuracy.

Input Clock Frequency Stop and Change

The input clock frequency can be stopped or changed from one stable clock rate to anotherstable clock rate during write leveling mode. The frequency stop or change timingis shown below.

Figure 4-102: Clock Stop and Timing During Write Leveling



Notes:

1. CK_t is held LOW and CK_c is held HIGH during clock stop.
2. CS will be held LOW during clock clock stop.

Table 4-111: Write Leveling Timing Parameters

Parameter	Symbol	Min/Max	Value	Units
DQS_t/DQS_c delay after write leveling mode is programmed	tWLDQSEN	MIN	20	tCK
		MAX	–	
Write preamble for write leveling	tWLWPRE	MIN	20	tCK
		MAX	–	
First DQS_t/DQS_c edge after write leveling mode is programmed	tWLMRD	MIN	40	tCK
		MAX	–	
Write leveling output delay	tWLO	MIN	0	ns
		MAX	20	
MODE REGISTER SET command delay	tMRD	Refer to Mode Register Timing Parameter Table		
Valid clock requirement before DQS toggle	tCKPRDQS	MIN	MAX (7.5ns, 4nCK)	–
		MAX	–	
Valid clock requirement after DQS toggle	tCKPSTDQS	MIN	MAX (7.5ns, 4nCK)	–
		MAX	–	

Table 4-112: Write Leveling Setup and Hold Timing

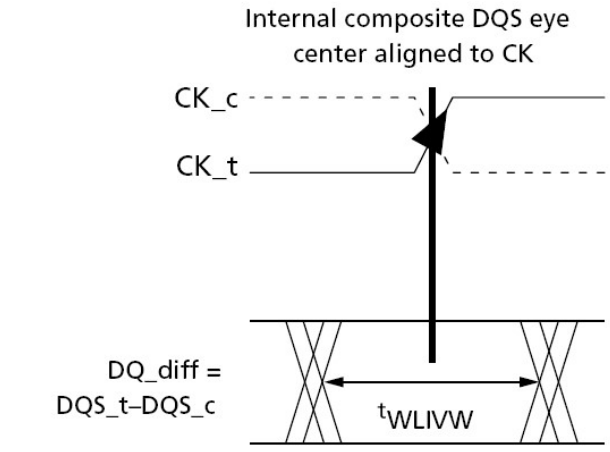
Parameter	Symbol	Min/Max	Data Rate			Unit
			1600	2400	3200	
Writ1e leveling hold time	^{t}WLH	MIN	150	100	75	ps
Write leveling setup time	^{t}WLS	MIN	150	100	75	ps
Write leveling input validwindow	^{t}WLIVW	MIN	240	160	120	ps

Notes:

1. In addition to the traditional setup and hold time specifications, there is value in a invalidwindow-based specification for writeleveling training. As the training is based oneach device, worst case process skews for setup and hold do not make sense toclosetiming between CK and DQS.
2. ^{t}WLIVW is defined in a similar manner to TdIVW_total, except that here it is a DQS invalidwindow with respect to CK. Thiswould need to account for all voltage and temperature(VT) drift terms between CK and DQS within the device that affect thewrite levelinginvalid window.

The figure below shows the DQS input mask for timing with respect to CK. The “total”mask (^{t}WLIVW) defines the time the input signal must not encroach in order for theDQS input to be successfully captured by CK. The mask is a receiver property and it isnot the valid data-eye.

Figure 4-103: DQS_t/DQS_c to CK_t/CK_c Timings at the Pins Referenced from the Internal Latch



4.31 MULTIPURPOSE Operation

The device uses the MULTIPURPOSE command to issue a NO OPERATION (NOP) commandand to access various training modes. The MPC command is initiated with CS,and CA[5:0] asserted to the proper state at the rising edge of CK, as defined by the CommandTruth Table. The MPC command has seven operands (OP[6:0]) that are decodedto execute specific commands in the SDRAM. OP[6] is a special bit that is decoded onthe first rising CK edge of the MPC command. When OP[6] = 0, the device executes aNOP command, and when OP[6] = 1, the device further decodes one of several trainingcommands.

When OP[6] = 1 and the training command includes a READ or WRITE operation, theMPC command must be followed immediately by a CAS-2 command. For training commandsthat read or write, READ latency (RL) and WRITE latency (WL) are counted fromthe second rising CK edge of the CAS-2 command with the same timing relationship asa typical READ or WRITE command. The operands of the CAS-2 command following aMPC READ/WRITE command must be driven LOW. The following MPC commandsmust be followed by a CAS-2 command:

- WRITE-FIFO
- READ-FIFO
- READ DQ CALIBRATION

All other MPC commands do not require a CAS-2 command, including the following:

- NOP
- START DQS OSCILLATOR
- STOP DQS OSCILLATOR
- ZQCAL START
- ZQCAL LATCH

Table 4-113: MPC Command Definition

SDR Command	SDR Command Pins			SDR CA Pins						CK_t Edge	Notes
	CKE										
	CK_t (n-1)	CK_t(n)	CS	CA0	CA1	CA2	CA3	CA4	CA5		
MPC (Train, NOP)	H	H	H	L	L	L	L	L	OP6	↑	1, 2
			L	OP0	OP1	OP2	OP3	OP4	OP5	↓	

Notes:

1. See the Command Truth Table for more information.
2. MPC commands for READ or WRITE TRAINING operations must be immediately followedby the CAS-2 command, consecutively, without any other commands in between. TheMPC command must be issued before issuing the CAS-2command.

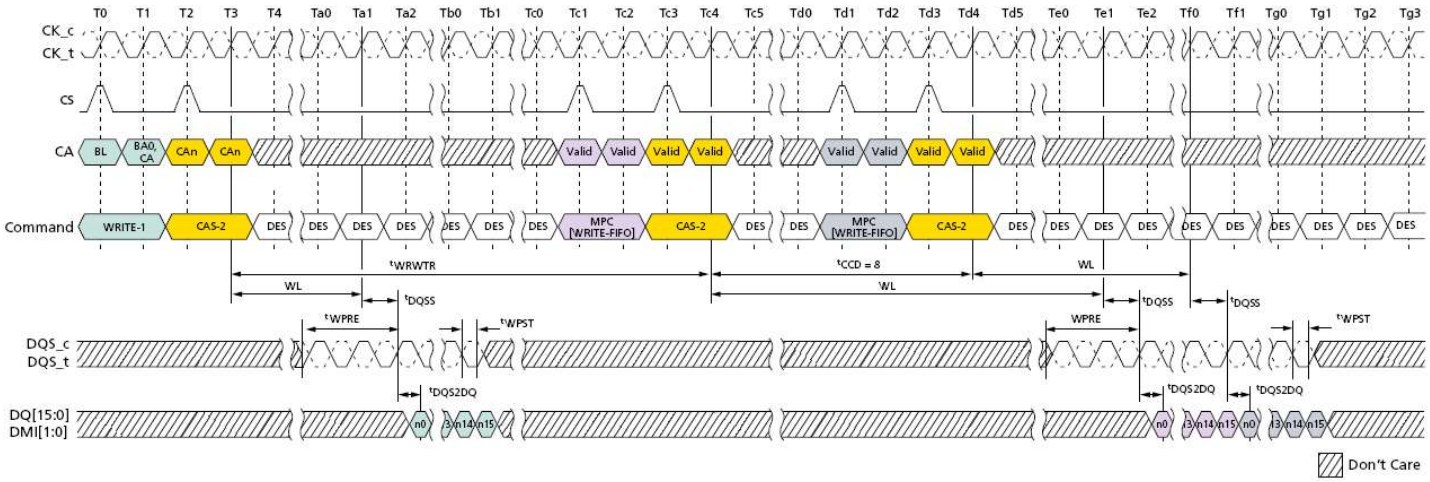
Table 4-114: MPC Commands

Function	Operand	Data
Training Modes	OP[6:0]	**0XXXXXXb:** NOP **1000001b:** READ-FIFO: READ-FIFO supports only BL16 operation **1000011b:** READ DQ CALIBRATION (MR32/MR40) **1000101b:** RFU **1000111b:** WRITE-FIFO: WRITE-FIFO supports only BL16 operation **1001001b:** RFU **1001011b:** START DQS OSCILLATOR **1001101b:** STOP DQS OSCILLATOR **1001111b:** ZQCAL START **1010001b:** ZQCAL LATCH **All Others:** Reserved

Notes:

1. See command truth table for more information.
2. MPC commands for READ or WRITE TRAINING operations must be immediately followedby CAS-2 commandconsecutively without any other commands in-between. MPC commandmust be issued first before issuing the CAS-2command.
3. WRITE-FIFO and READ-FIFO commands will only operate as BL16, ignoring the burstlength selected by MR1 OP[1:0].

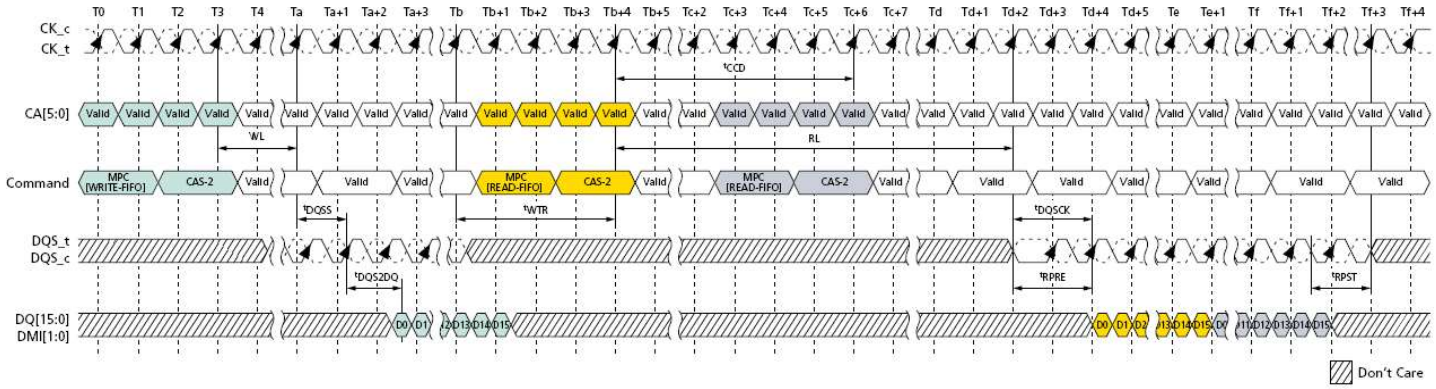
Figure 4-104: WRITE-FIFO – ^{t}WPRE = 2nCK, ^{t}WPST = 0.5nCK



Notes:

1. MPC[WRITE-FIFO] can be executed with a single bank or multiple banks active, duringrefresh or during self refresh, withCKE HIGH.
2. Write-1 to MPC is shown as an example of command-to-command timing for MPC. Timingfrom Write-1 toMPC[WRITE-FIFO] is ^{t}WRWTR.
3. Seamless MPC[WRITE-FIFO] commands may be executed by repeating the command every^{t}CCD time.
4. MPC[WRITE-FIFO] uses the same command-to-data timing relationship (WL, ^{t}DQSS,^{t}DQS2DQ) as a WRITE-1 command.
5. A maximum of five MPC[WRITE-FIFO] commands may be executed consecutively withoutcorrupting FIFO data. The sixthMPC[WRITE-FIFO] command will overwrite the FIFO datafrom the first command. If fewer than five MPC[WRITE-FIFO]commands are executed,then the remaining FIFO locations will contain undefined data.
6. For the CAS-2 command following an MPC command, the CAS-2 operands must be drivenLOW.
7. To avoid corrupting the FIFO contents, MPC[READ-FIFO] must immediately followMPC[WRITE-FIFO]/CAS-2 without anyother commands in-between. See Write Trainingsection for more information on FIFO pointer behavior.

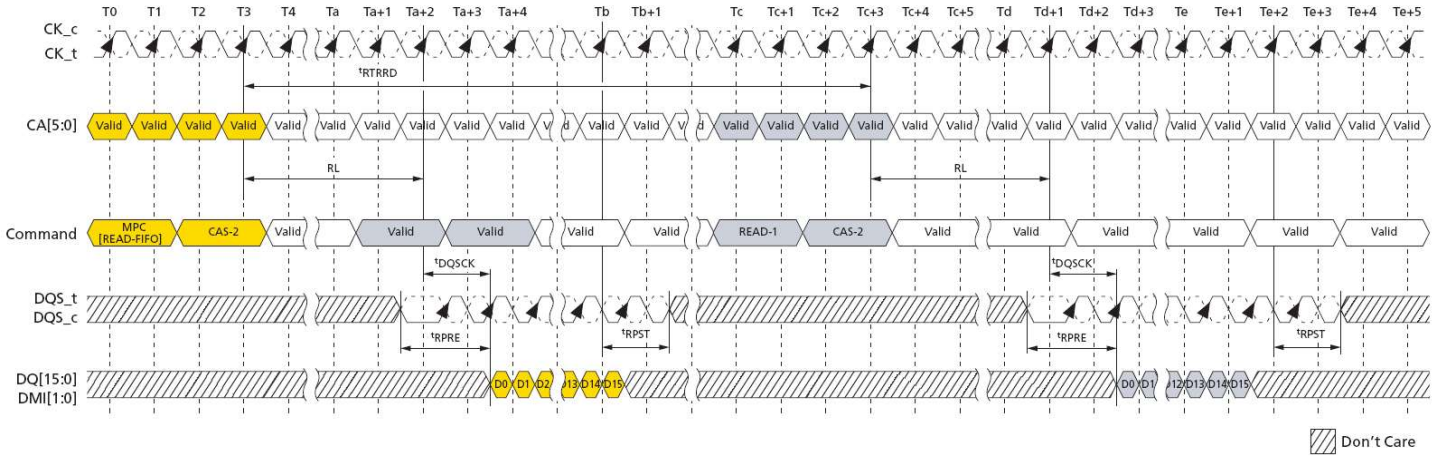
Figure 4-105: READ-FIFO – tWPRE = 2nCK, tWPST = 0.5nCK, tRPRE = Toggling, tRPST = 1.5nCK



Notes:

1. MPC[WRITE-FIFO] can be executed with a single bank or multiple banks active, duringrefresh or during self refresh withCKE HIGH.
2. Seamless MPC[READ-FIFO] commands may be executed by repeating the command everytCCD time.
3. MPC[READ-FIFO] uses the same command-to-data timing relationship (RL, tDQSCK) as aREAD-1 command.
4. Data may be continuously read from the FIFO without any data corruption. After fiveMPC[READ-FIFO] commands, the FIFOpointer will wrap back to the first FIFO and continueadvancing. If fewer than five MPC[WRITE-FIFO] commands wereexecuted, thenthe MPC[READ-FIFO] commands to those FIFO locations will return undefined data. SeeWrite Training formore information on the FIFO pointer behavior.
5. For the CAS-2 command immediately following an MPC command, the CAS-2 operandsmust be driven LOW.
6. DMI[1:0] signals will be driven if WR-DBI, RD-DBI, or DM is enabled in the mode registers.See Write Training for moreinformation on DMI behavior.

Figure 4-106: READ-FIFO – ^{t}RPRE = Toggling, ^{t}RPST = 1.5nCK



Notes:

1. MPC[WRITE-FIFO] can be executed with a single bank or multiple banks active, duringrefresh or during self refresh withCKE HIGH.
2. MPC[READ-FIFO] to READ-1 operation is shown as an example of command-to-commandtiming for MPC. Timing fromMPC[READ-FIFO] command to read is tRTRRD.
3. Seamless MPC[READ-FIFO] commands may be executed by repeating the command every^{t}CCD time.
4. MPC[READ-FIFO] uses the same command-to-data timing relationship (RL, ^{t}DQSCK) as aREAD-1 command.
5. Data may be continuously read from the FIFO without any data corruption. After fiveMPC[READ-FIFO] commands, the FIFOpointer will wrap back to the first FIFO and continueadvancing. If fewer than five MPC[WRITE-FIFO] commands areexecuted, then theMPC[READ-FIFO] commands to those FIFO locations will return undefined data. SeeWrite Training formore information on the FIFO pointer behavior.
6. For the CAS-2 command immediately following an MPC command, the CAS-2 operandsmust be driven LOW.
7. DMI[1:0] signals will be driven if WR-DBI, RD-DBI, or DM is enabled in the mode registers.See Write Training for moreinformation on DMI behavior.

Table 4-115: Timing Constraints for Training Commands

Previous Command	Next Command	Minimum Delay	Unit	Notes
WR/MWR	MPC[WRITE-FIFO]	^{t}WRWTR	nCK	1
	MPC[READ-FIFO]	Not allowed	–	2
	MPC[READ DQ CALIBRATION]	WL + RU(^{t}DQSS(MAX)/^{t}CK) + BL/2 + RU(^{t}WTR/^{t}CK)	nCK	
RD/MRR	MPC[WRITE-FIFO]	^{t}RTRRD	nCK	3
	MPC[READ-FIFO]	Not allowed	–	2
	MPC[READ DQ CALIBRATION]	^{t}RTRRD	nCK	3
MPC[WRITE-FIFO]	WR/MWR	Not allowed	–	2
	MPC[WRITE-FIFO]	^{t}CCD	nCK	
	RD/MRR	Not allowed	–	2
	MPC[READ-FIFO]	WL + RU(^{t}DQSS(MAX)/^{t}CK) + BL/2 + RU(^{t}WTR/^{t}CK)	nCK	
	MPC[READ DQ CALIBRATION]	Not allowed		2
MPC[READ-FIFO]	WR/MWR	^{t}RTRRD	nCK	3
	MPC[WRITE-FIFO]	^{t}RTW	nCK	4
	RD/MRR	^{t}RTRRD	nCK	3
	MPC[READ-FIFO]	^{t}CCD	nCK	
	MPC[READ DQ CALIBRATION]	^{t}RTRRD	nCK	3
MPC[READ DQ CALIBRATION]	WR/MWR	^{t}RTRRD	nCK	3
	MPC[WRITE-FIFO]	^{t}RTRRD	nCK	3
	RD/MRR	^{t}RTRRD	nCK	3
	MPC[READ-FIFO]	Not allowed	–	2
	MPC[READ DQ CALIBRATION]	^{t}CCD	nCK	

Notes:

1. ^{t}WRWTR = WL + BL/2 + RU(^{t}DQSS(MAX)/ ^{t}CK) + MAX(RU(7.5ns/^{t}CK), 8nCK).
2. No commands are allowed between MPC[WRITE-FIFO] and MPC[READ-FIFO] except theRW commands related to trainingparameters.
3. ^{t}RTRRD = RL + RU(^{t}DQSCK(MAX)/^{t}CK) + BL/2 + RD(^{t}RPST) + MAX(RU(7.5ns/^{t}CK), 8nCK).
4. In case of DQ ODT disable MR11 OP[2:0] = 000b,
^{t}RTW = RL + RU(tDQSCK(MAX)/^{t}CK) + BL/2 - WL + tWPRE + RD(^{t}RPST).
In case of DQ ODT enable MR11 OP[2:0] ≠ 000b,
^{t}RTW = RL + RU(tDQSCK(MAX)/^{t}CK) + BL/2 + RD(^{t}RPST) - ODTLon - RD(^{t}ODTon(MIN)/^{t}CK)+ 1.

4.32 Read DQ Calibration Training

The READ DQ CALIBRATION TRAINING function outputs a 16-bit, user-defined patternon the DQ pins. Read DQ calibration is initiated by issuing a MPC[READ DQ CALIBRATION]command followed by a CAS-2 command, which causes the device to drivethe contents of MR32, followed by the contents of MR40 on each of DQ[15:0] and DMI[1:0]. The pattern can be inverted on selected DQ pins according to user-definedinvert masks written to MR15 and MR20.

Read DQ Calibration Training Procedure

1. Issue MRW commands to write MR32 (first eight bits), MR40 (second eight bits),MR15 (eight-bit invert mask forbyte 0), and MR20 (eight-bit invert mask for byte1).
   In the alternative, this step could be replaced with the default pattern:
   - MR32 default = 5Ah
   - MR40 default = 3Ch
   - MR15 default = 55h
   - MR20 default = 55h

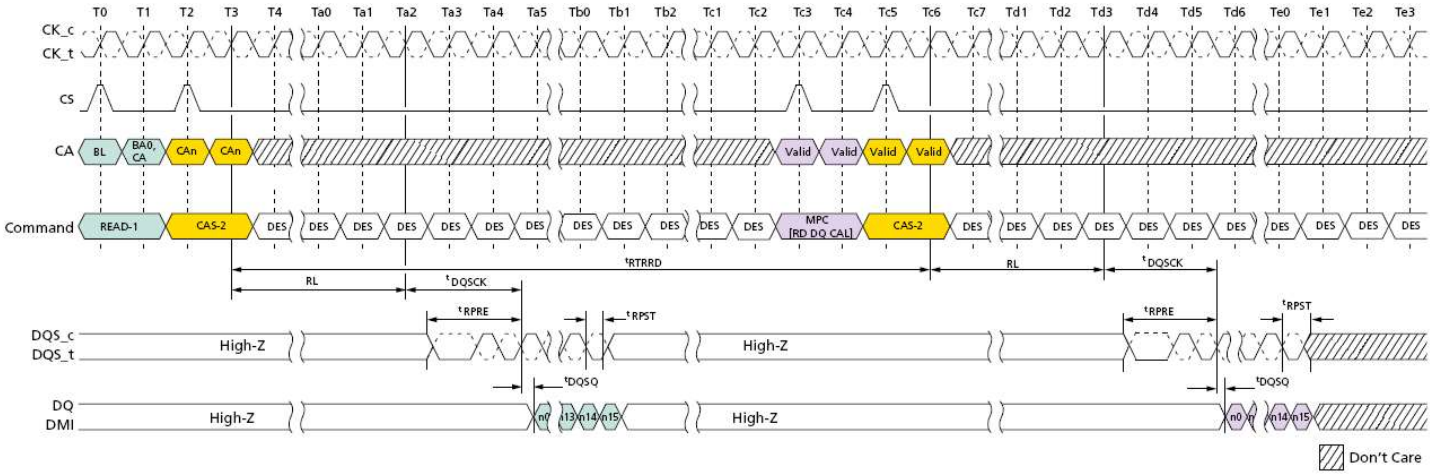
2. Issue an MPC command, followed immediately by a CAS-2 command.
   - Each time an MPC command, followed by a CAS-2, is received by the device, a16-bit data burst will drive theeight bits programmed in MR32 followed by theeight bits programmed in MR40 on all I/O pins after the currentlyset RL.
   - The data pattern will be inverted for I/O pins with a 1 programmed in the correspondinginvert mask moderegister bit (see table below).
   - The pattern is driven on the DMI pins, but no DATA BUS INVERSION function isenabled, even if read DBI isenabled in the mode register.
   - The MPC command can be issued every ^{t}CCD seamlessly, and ^{t}RTRRD delay isrequired between ARRAYREAD command and the MPC command as well thedelay required between the MPC command and an ARRAYREAD.
   - The operands received with the CAS-2 command must be driven LOW.

3. DQ
   Read DQ calibration training can be performed with any or no banks active duringrefresh or during self refreshwith CKE HIGH.

Table 4-116: Invert Mask Assignments

DQ pin	0	1	2	3	DMI0	4	5	6	7
MR15 bit	0	1	2	3	N/A	4	5	6	7
DQ pin	8	9	10	11	DMI1	12	13	14	15
MR20 bit	0	1	2	3	N/A	4	5	6	7

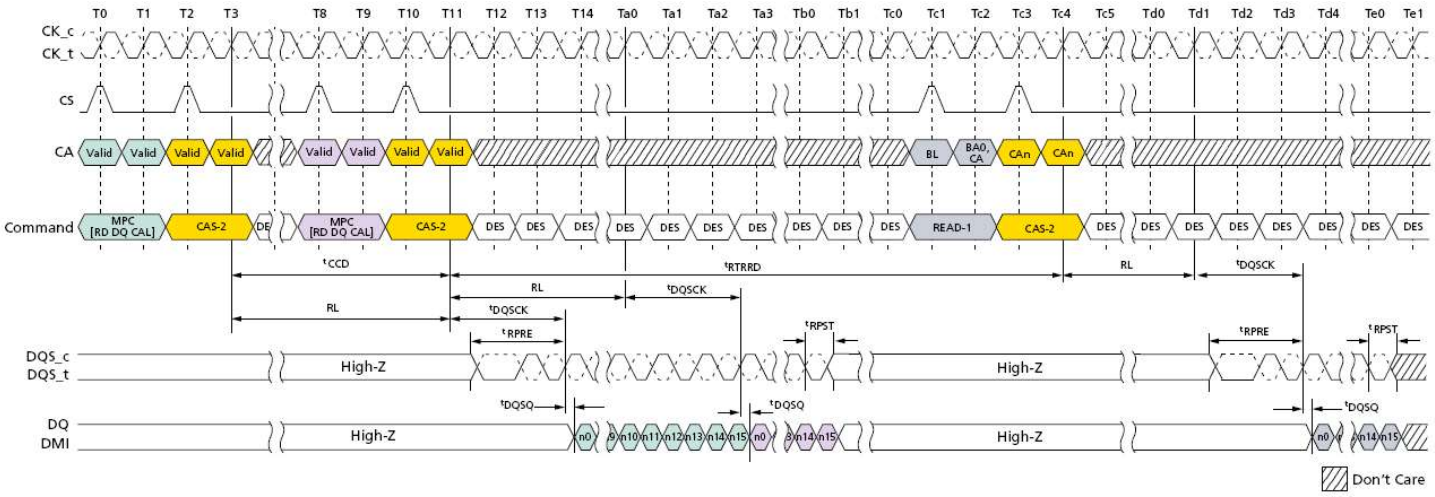
Figure 4-107: Read DQ Calibration Training Timing: Read-to-Read DQ Calibration



Notes:

1. Read-1 to MPC operation is shown as an example of command-to-command timing. Timingfrom Read-1 to MPC commandis tRTRRD.
2. MPC uses the same command-to-data timing relationship (RL, tDQSCK, tDQSQ) as aRead-1 command.
3. BL = 16, Read preamble: Toggle, Read postamble: 0.5nCK.
4. DES commands are shown for ease of illustration; other commands may be valid atthese times.

Figure 4-108: Read DQ Calibration Training Timing: Read DQ Calibration to Read DQ Calibration/Read



Notes:

1. MPC[READ DQ CALIBRATION] to MPC[READ DQ CALIBRATION] operation is shown as anexample of command-to-command timing.
2. MPC[READ DQ CALIBRATION] to READ-1 operation is shown as an example of command-to-command timing.
3. MPC[READ DQ CALIBRATION] uses the same command-to-data timing relationship (RL,tDQSCK, tDQSQ) as a READ-1 command.
4. Seamless MPC[READ DQ CALIBRATION] commands may be executed by repeating thecommand every tCCD time.
5. Timing from MPC[READ DQ CALIBRATION] command to READ-1 is tRTRRD.
6. BL = 16, Read preamble: Toggle, Read postamble: 0.5nCK.
7. DES commands are shown for ease of illustration; other commands may be valid atthese times.

Read DQ Calibration Training Example

An example of read DQ calibration training output is shown in table below. This showsthe 16-bit data pattern that will be driven on each DQ in byte 0 when one READ DQCALIBRATION TRAINING command is executed. This output assumes the followingmode register values are used:

- MR32 = 1CH
- MR40 = 59H
- MR15 = 55H
- MR20 = 55H

Table 4-117: Read DQ Calibration Bit Ordering and Inversion Example

Pin	Bit Sequence →																
	Invert	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DQ0	Yes	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQ1	No	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQ2	Yes	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQ3	No	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DMI0	Never	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQ4	Yes	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQ5	No	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQ6	Yes	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQ7	No	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQ8	Yes	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQ9	No	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQ10	Yes	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQ11	No	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DMI1	Never	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQ12	Yes	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQ13	No	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQ14	Yes	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQ15	No	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0

Notes:

1. The patterns contained in MR32 and MR40 are transmitted on DQ[15:0] and DMI[1:0]when read DQ calibration is initiatedvia a MPC[READ DQ CALIBRATION] command. Thepattern transmitted serially on each data lane, organized little endiansuch that the loworderbit in a byte is transmitted first. If the data pattern is 27H, then the first bit transmittedwith is a 1,followed by 1, 1, 0, 0, 1, 0, and 0. The bit stream will be 00100111 →.
2. MR15 and MR20 may be used to invert the MR32/MR40 data pattern on the DQ pins.See MR15 and MR20 for moreinformation. Data is never inverted on the DMI[1:0] pins.
3. DMI [1:0] outputs status follows MR Setting vs. DMI Status table.
4. No DATA BUS INVERSION (DBI) function is enacted during read DQ calibration, even ifDBI is enabled in MR3-OP[6].

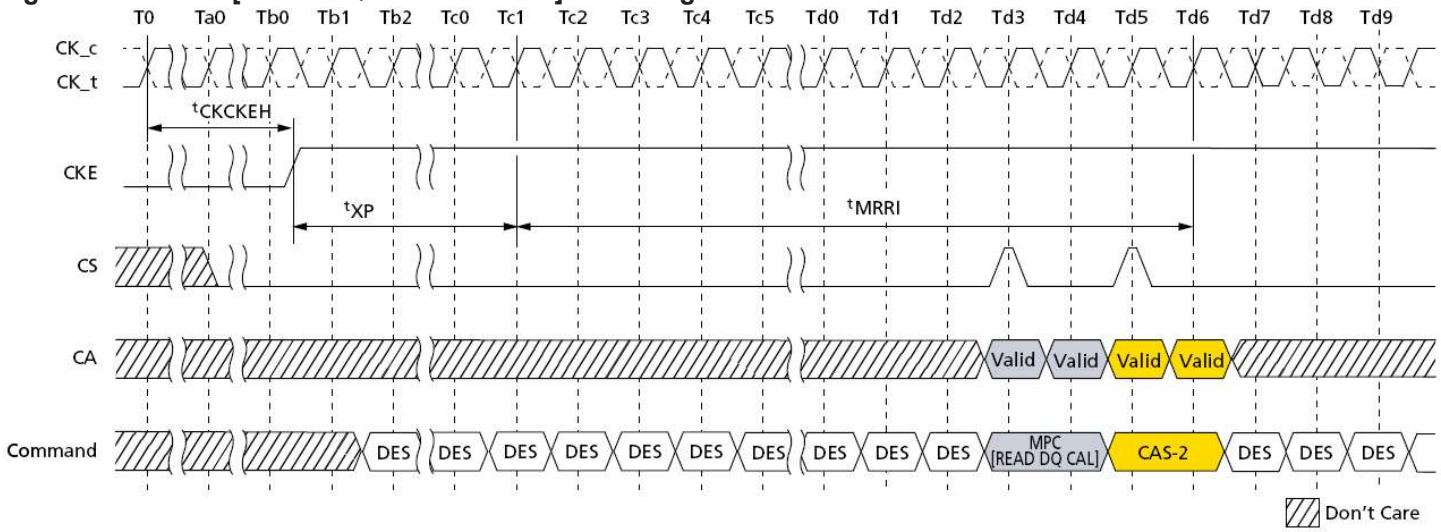
Table 4-118: MR Setting vs. DMI Status

DM Function MR13 OP[5]	WRITE DBIdc Function MR3 OP[7]	READ DBIdc Function MR3 OP[6] DMI	Status
1: Disable	0: Disable	0: Disable	High-Z
1: Disable	1: Enable	0: Disable	The data pattern is transmitted
1: Disable	0: Disable	1: Enable	The data pattern is transmitted
1: Disable	1: Enable	1: Enable	The data pattern is transmitted
0: Enable	0: Disable	0: Disable	The data pattern is transmitted
0: Enable	1: Enable	0: Disable	The data pattern is transmitted
0: Enable	0: Disable	1: Enable	The data pattern is transmitted
0: Enable	1: Enable	1: Enable	The data pattern is transmitted

MPC[READ DQ CALIBRATION] After Power-Down Exit

Following the power-down state, an additional time, ^{t}MRRI, is required prior to issuingthe MPC[READ DQ CALIBRATION] command. This additional time (equivalent to^{t}RCD) is required in order to be able to maximize power-down current savings by allowingmore power-up time for the read DQ data in MR32 and MR40 data path after exitfrom standby, power-down mode.

Figure 4-109: MPC[READ DQ CALIBRATION] Following Power-Down State



4.33 Write Training

The device uses an unmatched DQS-DQ path to enable high-speed performance andsave power. As a result, the DQS strobe must be trained to arrive at the DQ latch centeralignedwith the data eye. The DQ receiver is located at the DQ pad and has a shorterinternal delay than the DQS signal. The DQ receiver will latch the data present on the DQ bus when DQS reaches the latch, and training is accomplished by delaying the DQsignals relative to DQS such that the data eye arrives at the receiver latch centered onthe DQS transition.

Two modes of training are available:
• Command-based FIFO WR/RD with user patterns
• An internal DQS clock-tree oscillator, which determines the need for, and the magnitudeof, required training

The command-based FIFO WR/RD uses the MPC command with operands to enablethis special mode of operation. When issuing the MPC command, if CA[5] is set LOW(OP[6] = 0), then the device will perform a NOP command. When CA[5] is set HIGH, theCA[4:0] pins enable training functions or are reserved for future use (RFU). MPC commandsthat initiate a read or write to the device must be followed immediately by aCAS-2 command. See the MPC Operation section for more information.

To perform write training, the controller can issue an MPC[WRITE-FIFO] commandwith OP[6:0] set, followed immediately by a CAS-2 command (CAS-2 operands shouldbe driven LOW) to initiate a WRITE-FIFO. Timings for MPC[WRITE-FIFO] are identicalto WRITE commands, with WL timed from the second rising clock edge of the CAS-2command. Up to five consecutive MPC[WRITE-FIFO] commands with user-definedpatterns may be issued to the device, which will store up to 80 values (BL16 × 5) per pinthat can be read back via the MPC[READ-FIFO] command. (The WRITE/READ-FIFOPOINTER operation is described in a different section.

After writing data with the MPC[WRITE-FIFO] command, the data can be read backwith the MPC[READ-FIFO] command and results can be compared with "expected" datato determine whether further training (DQ delay) is needed. MPC[READ-FIFO] is initiatedby issuing an MPC command, as described in the MPC Operation section, followedimmediately by a CAS-2 command (CAS-2 operands must be driven LOW). Timingsfor the MPC[READ-FIFO] command are identical to READ commands, with RLtimed from the second rising clock edge of the CAS-2 command.

READ-FIFO is nondestructive to the data captured in the FIFO; data may be read continuouslyuntil it is disturbed by another command, such as a READ, WRITE, or anotherMPC[WRITE-FIFO]. If fewer than five WRITE-FIFO commands are executed, unwrittenregisters will have undefined (but valid) data when read back.

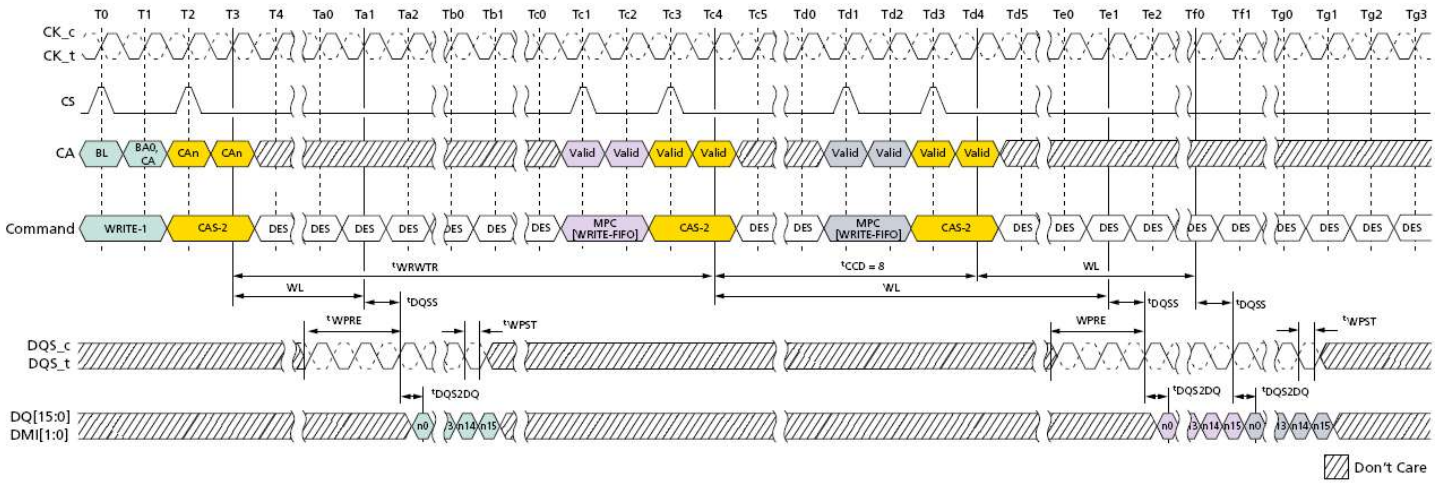
For example: If five WRITE-FIFO commands are executed sequentially, then a series ofREAD-FIFO commands will read valid data from FIFO[0], FIFO[1]….FIFO[4] and thenwrap back to FIFO[0] on the next READ-FIFO. However, if fewer than five WRITE-FIFOcommands are executed sequentially (example = 3), then a series of READ-FIFO commandswill return valid data for FIFO[0], FIFO[1], and FIFO[2], but the next two READFIFOcommands will return undefined data for FIFO[3] and FIFO[4] before wrappingback to the valid data in FIFO[0].

The READ-FIFO pointer and WRITE-FIFO pointer are reset under the following conditions:
• Power-up initialization
• RESET_n asserted
• Power-down entry
• Self refresh power-down entry

The MPC[WRITE-FIFO] command advances the WRITE-FIFO pointer, and theMPC[READ-FIFO] advances the READ-FIFO pointer. Also any normal (non-FIFO) READoperation (RD, RDA) advances both WRITE-FIFO pointer and READ-FIFO pointer. Issuing(non-FIFO) READ operation command is inhibited during write training period. To keep the pointers aligned, the SoC memory controller must adhere to the following restrictionat the end of Write training period:
b = a + (n × c)

Where:
'a' is the number of MPC[WRITE-FIFO] commands
'b' is the number of MPC[READ-FIFO] commands
'c' is the FIFO depth (= 5 for LPDDR4)
'n' is a positive integer, ≥0

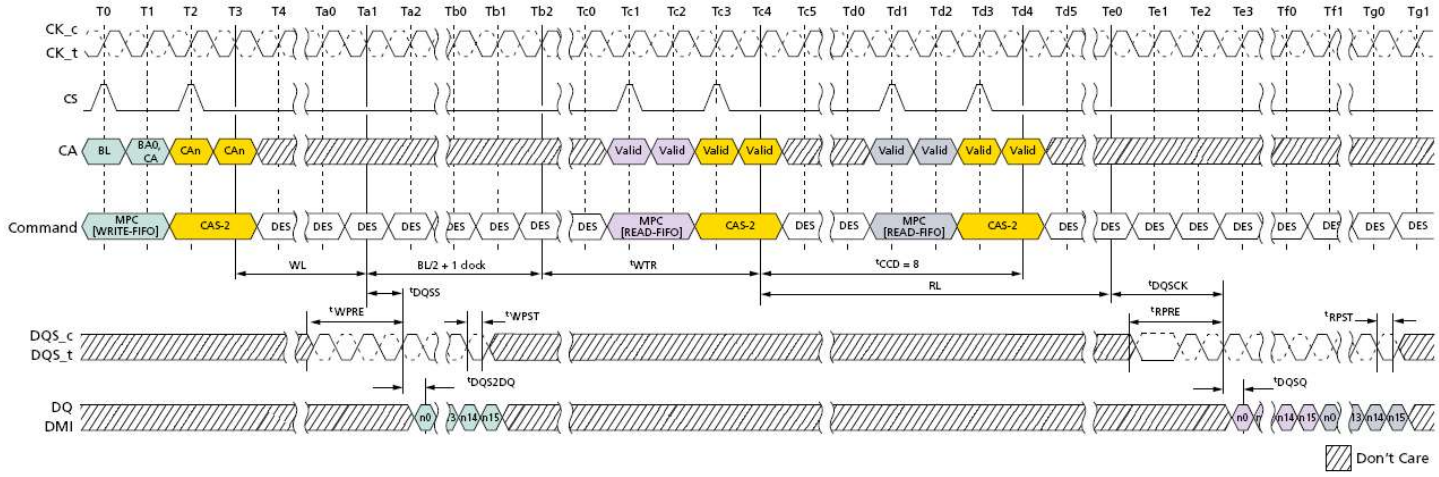
Figure 4-110: WRITE-to-MPC[WRITE-FIFO] Operation Timing



Notes:

1. MPC[WRITE-FIFO] can be executed with a single bank or multiple banks active duringREFRESH or during SELF REFRESH with CKE HIGH.
2. Write-1 to MPC is shown as an example of command-to-command timing for MPC. Timingfrom Write-1 to MPC[WRITE-FIFO] is ^{t}WRWTR.
3. Seamless MPC[WR-FIFO] commands may be executed by repeating the command every^{t}CCD time.
4. MPC[WRITE-FIFO] uses the same command-to-data timing relationship (WL, ^{t}DQSS,^{t}DQS2DQ) as a WRITE-1 command.
5. A maximum of five MPC[WRITE-FIFO] commands may be executed consecutively withoutcorrupting FIFO data. The sixthMPC[WRITE-FIFO] command will overwrite the FIFO datafrom the first command. If fewer than five MPC[WRITE-FIFO]commands are executed,then the remaining FIFO locations will contain undefined data.
6. For the CAS-2 command following an MPC command, the CAS-2 operands must be drivenLOW.
7. To avoid corrupting the FIFO contents, MPC[READ-FIFO] must immediately followMPC[WRITE-FIFO]/CAS-2 without anyother commands disturbing FIFO pointers in between.FIFO pointers are disturbed by CKE LOW, WRITE, MASKED WRITE,READ, READDQ CALIBRATION, and MRR.
8. BL = 16, Write postamble = 0.5nCK.
9. DES commands are shown for ease of illustration; other commands may be valid atthese times.

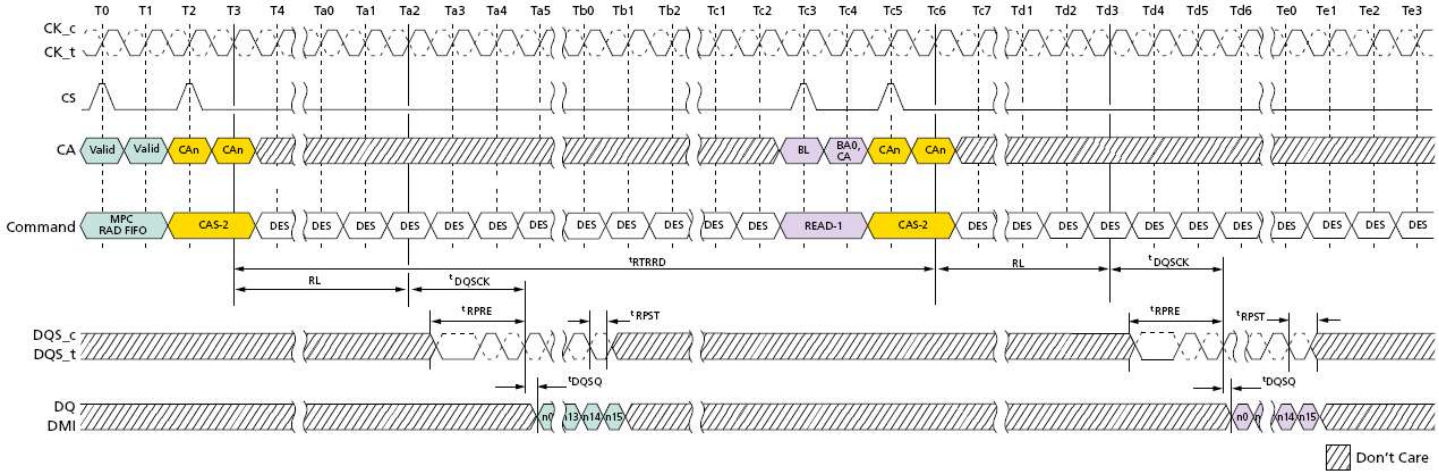
Figure 4-111: MPC[WRITE-FIFO]-to-MPC[READ-FIFO] Timing



Notes:

1. MPC[WRITE-FIFO] can be executed with a single bank or multiple banks active during refreshor during self refresh with CKE HIGH.
2. MPC[WRITE-FIFO] to MPC[READ-FIFO] is shown as an example of command-to-commandtiming for MPC. Timing from MPC[WRITE-FIFO] to MPC[READ-FIFO] is specified in thecommand-to-command timing table.
3. Seamless MPC[READ-FIFO] commands may be executed by repeating the command every^{t}CCD time.
4. MPC[READ-FIFO] uses the same command-to-data timing relationship (RL, ^{t}DQSCK,^{t}DQSQ) as a READ-1 command.
5. Data may be continuously read from the FIFO without any data corruption. After fiveMPC[READ-FIFO] commands, the FIFO pointer will wrap back to the first FIFO and continueadvancing. If fewer than five MPC[WRITE-FIFO] commands were executed, thenthe MPC[READ-FIFO] commands to those FIFO locations will return undefined data. SeeWrite Training for more information on the FIFO pointer behavior.
6. For the CAS-2 command immediately following an MPC command, the CAS-2 operandsmust be driven LOW.
7. DMI[1:0] signals will be driven if WR-DBI, RD-DBI, or DM is enabled in the mode registers.See Write Training section for more information on DMI behavior.
8. BL = 16, Write postamble = 0.5nCK, Read preamble: Toggle, Read postamble: 0.5nCK.
9. DES commands are shown for ease of illustration; other commands may be valid atthese times.

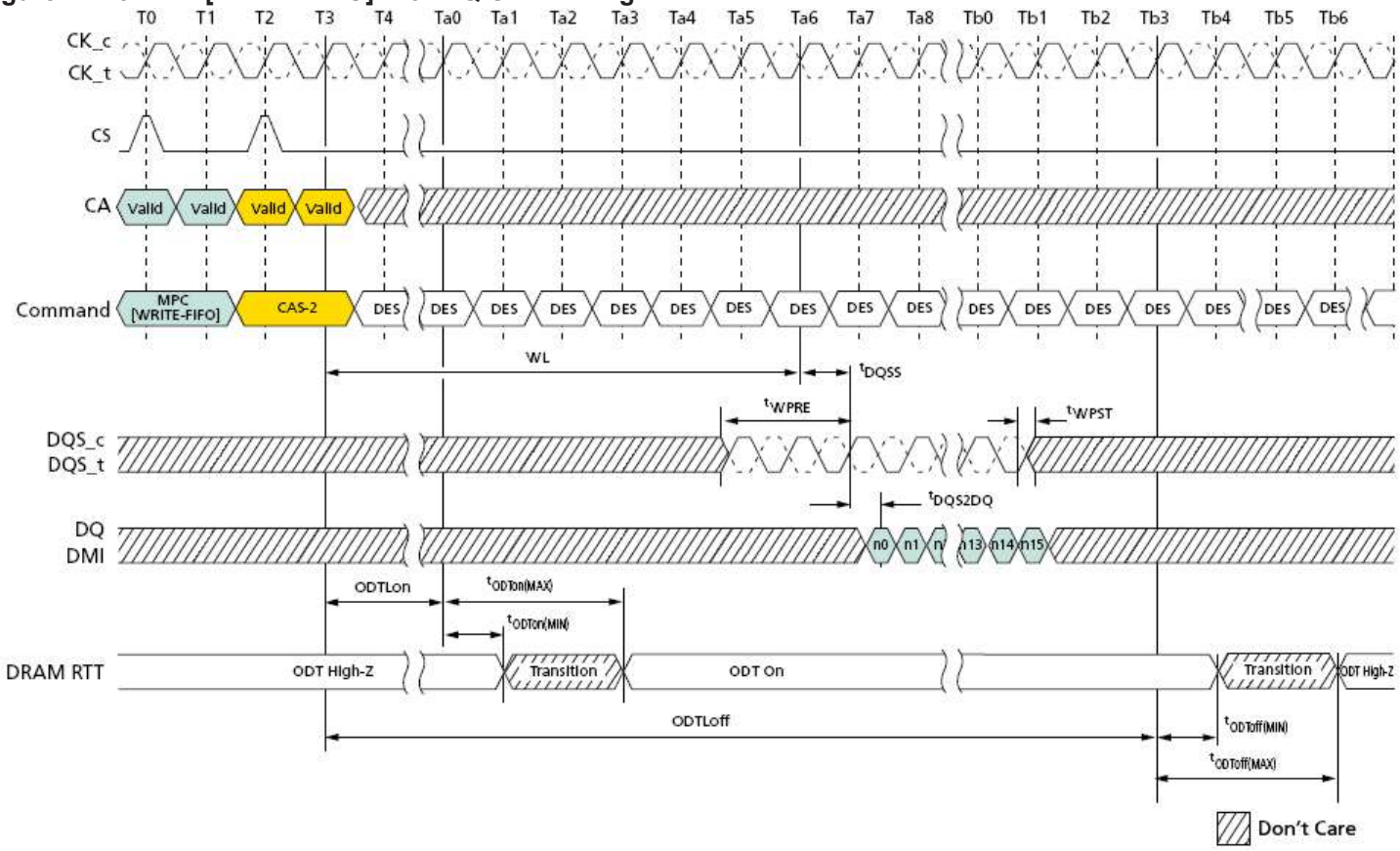
Figure 4-112: MPC[READ-FIFO] to Read Timing



Notes:

1. MPC[WRITE-FIFO] can be executed with a single bank or multiple banks active during refreshor during self refresh with CKE HIGH.
2. MPC[READ-FIFO] to READ-1 operation is shown as an example of command-to-commandtiming for MPC. Timing from MPC[READ-FIFO] command to READ is ^{t}RTRRD.
3. Seamless MPC[READ-FIFO] commands may be executed by repeating the command every^{t}CCD time.
4. MPC[READ-FIFO] uses the same command-to-data timing relationship (RL, ^{t}DQSCK,^{t}DQSQ) as a READ-1 command.
5. Data may be continuously read from the FIFO without any data corruption. After fiveMPC[READ-FIFO] commands, the FIFO pointer will wrap back to the first FIFO and continueadvancing. If fewer than five MPC[WRITE-FIFO] commands were executed, thenthe MPC[READ-FIFO] commands to those FIFO locations will return undefined data. SeeWrite Training for more information on the FIFO pointer behavior.
6. For the CAS-2 command immediately following an MPC command, the CAS-2 operandsmust be driven LOW.
7. DMI[1:0] signals will be driven if WR-DBI, RD-DBI, or DM is enabled in the mode registers.See Write Training for more information on DMI behavior.
8. BL = 16, Read preamble: Toggle, Read postamble: 0.5nCK
9. DES commands are shown for ease of illustration; other commands may be valid atthese times.

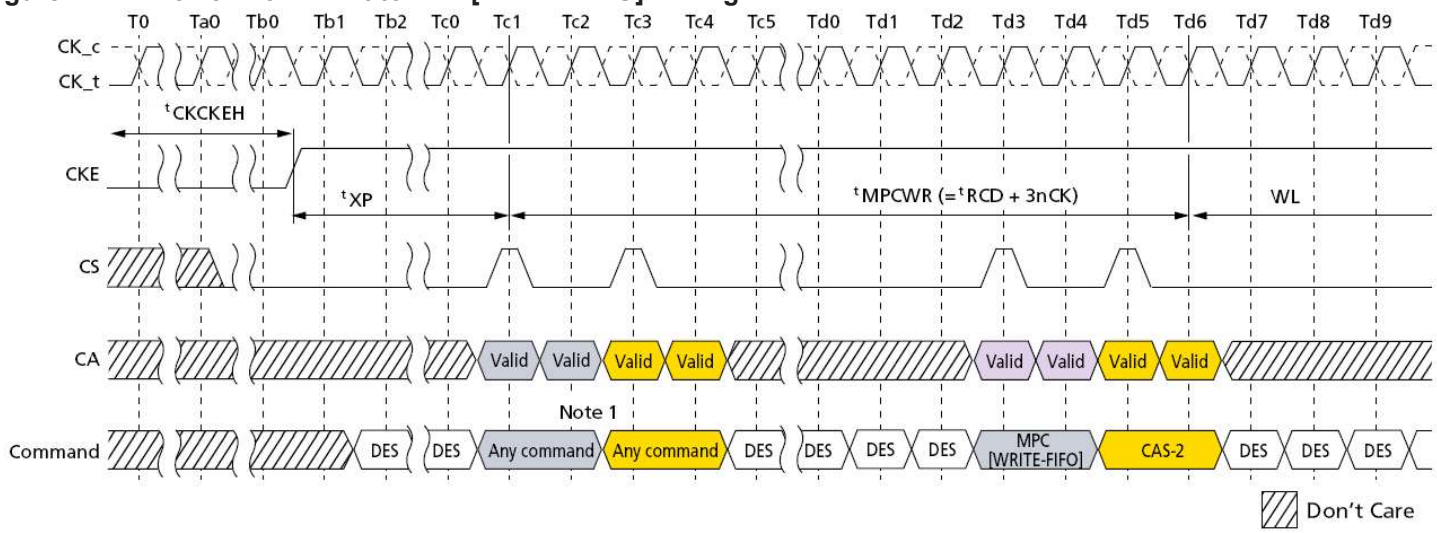
Figure 4-113: MPC[WRITE-FIFO] with DQ ODT Timing



Notes:

1. MPC[WRITE-FIFO] can be executed with a single bank or multiple banks active during refreshor during self refresh with CKE HIGH.
2. MPC[WRITE-FIFO] uses the same command-to-data/ODT timing relationship (RL, ^{t}DQSCK,^{t}DQS2DQ, ODTLon, ODTLoff, ^{t}ODTon, ^{t}ODToff) as a WRITE-1 command.
3. For the CAS-2 command immediately following an MPC command, the CAS-2 operandsmust be driven LOW.
4. BL = 16, Write postamble = 0.5nCK.
5. DES commands are shown for ease of illustration; other commands may be valid atthese times.

Figure 4-114: Power-Down Exit to MPC[WRITE-FIFO] Timing



Notes:

1. Any commands except MPC[WRITE-FIFO] and other exception commands defined othersection in this document (for example. MPC[READ DQ CALIBRATION]).
2. DES commands are shown for ease of illustration; other commands may be valid atthese times.

Table 4-119: MPC[WRITE-FIFO] AC Timing

Parameter	Symbol	MIN/MAX	Value	Unit
Additional time after tXP has expired until MPC[WRITE-FIFO] command may be issued	tMPCWR	MIN	tRCD + 3nCK	–

Internal Interval Timer

As voltage and temperature change on the device, the DQS clock-tree delay will shift,requiring retraining. The device includes an internal DQS clock-tree oscillator to measurethe amount of delay over a given time interval (determined by the controller), allowingthe controller to compare the trained delay value to the delay value seen at a latertime. The DQS oscillator will provide the controller with important information regardingthe need to retrain and the magnitude of potential error.

The DQS interval oscillator is started by issuing an MPC command with OP[5:0] =101011b, which will start an internal ring oscillator that counts the number of time asignal propagates through a copy of the DQS clock tree.

The DQS oscillator may be stopped by issuing an MPC[STOP DQS OSCILLATOR] commandwith OP[6:0] set, as described in MPC Operation, or the controller may instructthe SDRAM to count for a specific number of clocks anthen stop automatically (SeeMR23 for more information). If MR23 is set to automatically stop the DQS oscillator,then the MPC[STOP DQS OSCILLATOR] command should not be used (illegal). Whenthe DQS oscillator is stopped by either method, the result of the oscillator counter is automaticallystored in MR18 and MR19.

The controller may adjust the accuracy of the result by running the DQS interval oscillatorfor shorter (less accurate) or longer (more accurate) duration. The accuracy of theresult for a given temperature and voltage is determined by the following equation,where run time = total time between START and STOP commands and DQS delay = thevalue of the DQS clock tree delay (tDQS2DQ MIN/MAX):

$$\text{DQS oscillator granularity error} = \frac{2 \times (\text{DQS delay})}{\text{run time}}$$

Additional matching error must be included, which is the difference between DQStraining circuit and the actual DQS clock tree across voltage and temperature. Thematching error is vendor specific. Therefore, the total accuracy of the DQS oscillatorcounter is given by:

DQS oscillator accuracy = 1 - granularity error - matching error

For example, if the total time between START and STOP commands is 100ns, and themaximum DQS clock tree delay is 800ps (^{t}DQS2DQ MAX), then the DQS oscillator granularityerror is:

$$\text{DQS oscillator granularity error} = \frac{2 \times (0.8\text{ns})}{100\text{ns}} = 1.6\%$$

This equates to a granularity timing error of 12.8ps. Assuming a circuit matching errorof 5.5ps across voltage and temperature, the accuracy is:

$$\text{DQS oscillator accuracy} = 1 - \frac{12.8 + 5.5}{800} = 97.7\%$$

For example, running the DQS oscillator for a longer period improves the accuracy. Ifthe total time between START and STOP commands is 500ns, and the maximum DQSclock tree delay is 800ps (tDQS2DQ MAX), then the DQS oscillator granularity error is:

$$\text{DQS oscillator granularity error} = \frac{2 \times (0.8\text{ns})}{500\text{ns}} = 0.32\%$$

This equates to a granularity timing error or 2.56ps. Assuming a circuit matching errorof 5.5ps across voltage and temperature, the accuracy is:

$$\text{DQS oscillator accuracy} = 1 - \frac{2.56 + 5.5}{800} = 99.0\%$$

The result of the DQS interval oscillator is defined as the number of DQS clock tree delaysthat can be counted within the run time, determined by the controller. The result isstored in MR18-OP[7:0] and MR19-OP[7:0].

MR18 contains the least significant bits (LSB) of the result, and MR19 contains the mostsignificant bits (MSB) of the result. MR18 and MR19 are overwritten by the SDRAMwhen a MPC[STOP DQS OSCILLATOR] command is received.

The SDRAM counter will count to its maximum value (= 2^16) and stop. If the maximumvalue is read from the mode registers, the memory controller must assume thatthe counter overflowed the register and therefore discard the result. The longest runtime for the oscillator that will not overflow the counter registers can be calculated asfollows:

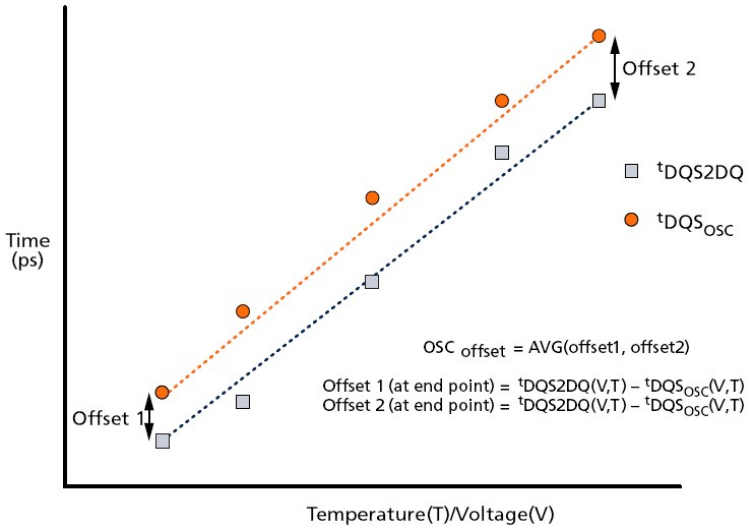
Longest runtime interval = 216 x ^{t}DQS2DQ(MIN) = 216 × 0.2ns = 13.1µs

DQS Interval Oscillator Matching Error

The interval oscillator matching error is defined as the difference between the DQStraining ckt (interval oscillator) and the actual DQS clock tree across voltage and temperature.

Parameters:
^{t}DQS2DQ: Actual DQS clock tree delay
^{t}DQS$_{OSC}$: Training ckt (interval oscillator) delay
OSC$_{Offset}$: Average delay difference over voltage and temperature (shown below)
OSC$_{Match}$: DQS oscillator matching error

Figure 4-115: Interval Oscillator Offset – OSCoffset



OSC_{Match} :

$$OSC_{Match} = [\ ^{t}DQS2DQ(V,T) - ^{t}DQS_{OSC}(V,T) - OSC_{offset}\ ]$$

$^{t}DQS_{OSC}$:

$$^{t}DQS_{OSC}(V,T) = [\ \frac{Runtime}{2 \times Count}\ ]$$

Table 4-120: DQS Oscillator Matching Error Specification

Parameter	Symbol	MIN	MAX	Unit	Notes
DQS oscillator matching error	OSC_{Match}	–20	20	ps	1, 2, 3, 4, 5, 6, 7, 8
DQS oscillator offset	OSC_{offset}	–100	100	ps	2, 4. 7

Notes:

1. The OSC_{Match} is the matching error per between the actual DQS and DQS interval oscillatorover voltage and temperature.
2. This parameter will be characterized or guaranteed by design.
3. The OSC_{Match} is defined as the following:

$$OSC_{Match} = [\ ^{t}DQS2DQ_{(V,T)} - ^{t}DQS_{OSC(V,T)} - OSC_{offset}\ ]$$

Where $^{t}DQS2DQ_{(V,T)}$ and $^{t}DQS_{OSC(V,T)}$ are determined over the same voltage and temperatureconditions.

4. The runtime of the oscillator must be at least 200ns for determining $^{t}DQS_{OSC}(V,T)$.

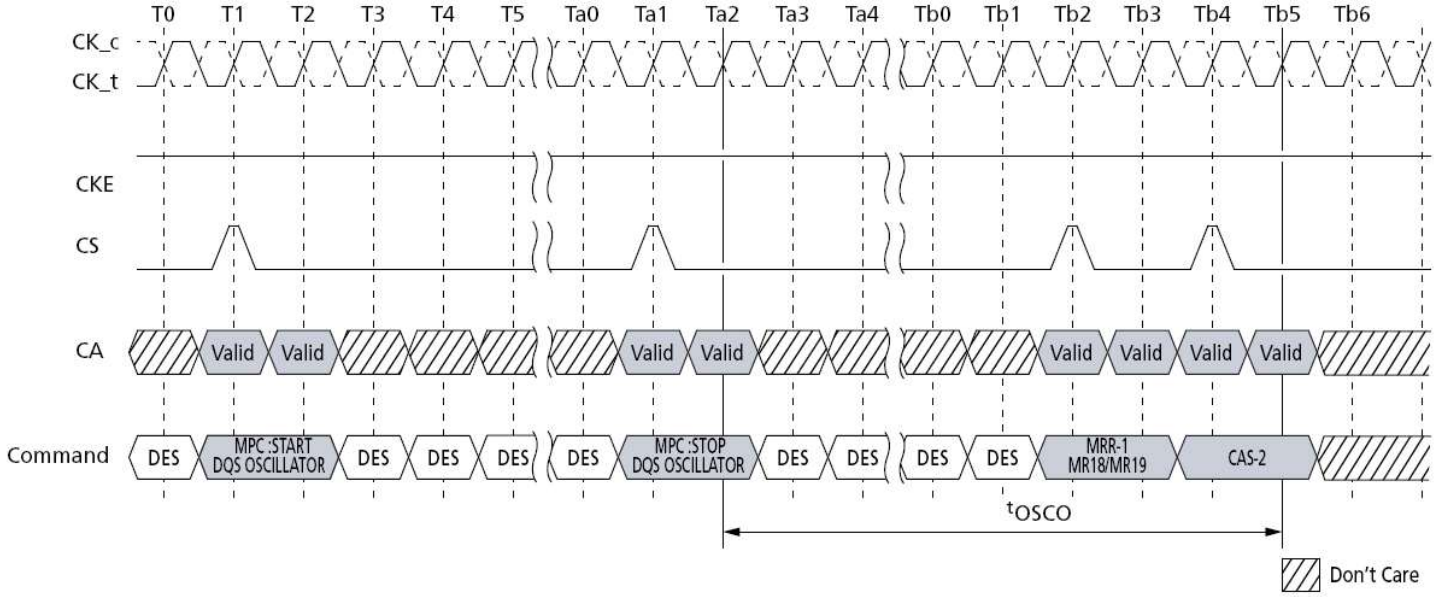
$$^{t}DQS_{OSC}(V,T) = [\ \frac{Runtime}{2 \times Count}\ ]$$

5. The input stimulus for $^{t}DQS2DQ$ will be consistent over voltage and temperature conditions.
6. The OSCoffset is the average difference of the endpoints across voltage and temperature.
7. These parameters are defined per channel.
8. $^{t}DQS2DQ(V,T)$ delay will be the average of DQS-to-DQ delay over the runtime period.

OSC Count Readout Time

OSC Stop to its counting value readout timing is shown in following figures.

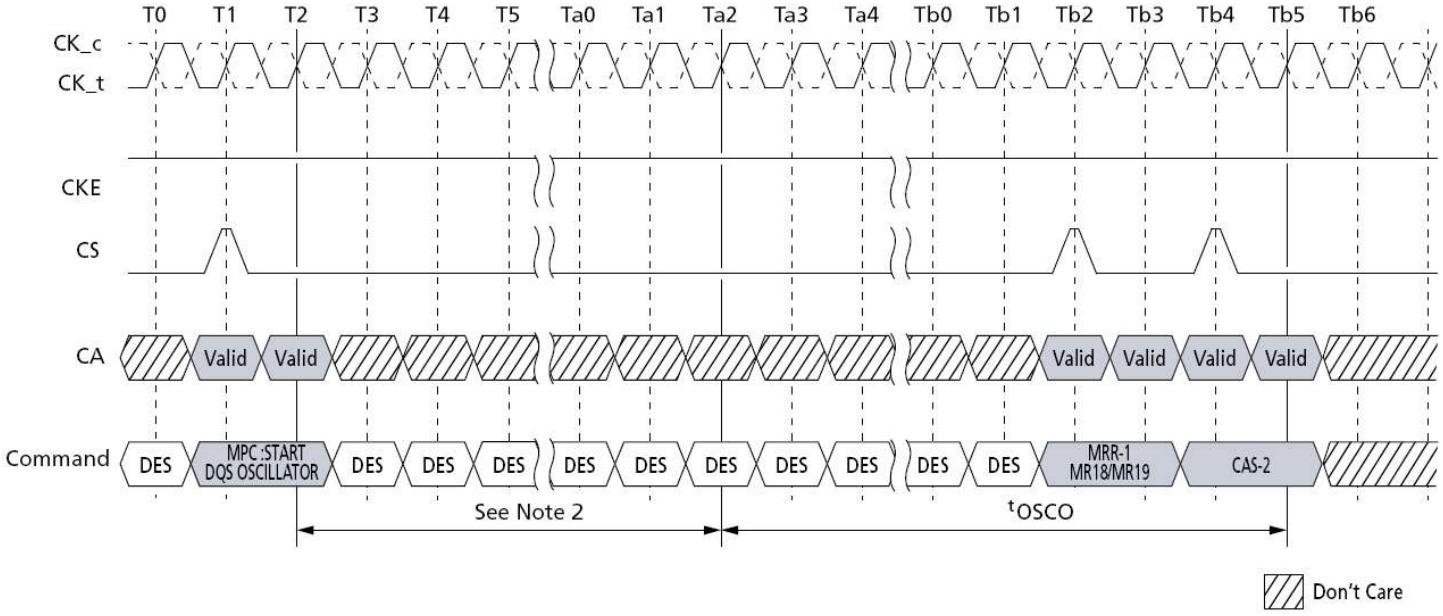
Figure 4-116: In Case of DQS Interval Oscillator is Stopped by MPC Command



Note:

1. DQS interval timer run time setting:MR23 OP[7:0] = 00000000b.

Figure 4-117: In Case of DQS Interval Oscillator is Stopped by DQS Interval Timer



Notes:

1. DQS interval timer run time setting: MR23 OP[7:0] ≠ 00000000b.
2. Setting counts of MR23.

Table 4-121: DQS Interval Oscillator AC Timing

Parameter	Symbol	MIN/MAX	Value	Unit
Delay time from OSC stop to mode registerreadout	tOSCO	MIN	MAX (40ns,8nCK)	ns

Note:

1. START DQS OSCILLATOR command is prohibited until tOSCO(MIN) is satisfied.

4.34 Thermal Offset

Because of tight thermal coupling, hot spots on an SOC can induce thermal gradientsacross the device. Because these hot spots may not be located near the thermal sensor,the temperature compensated self refresh (TCSR) circuit may not generate enough refreshcycles to guarantee memory retention. To address this shortcoming, the controllercan provide a thermal offset that the memory can use to adjust its TCSR circuit to ensurereliable operation.

This thermal offset is provided through MR4 OP[6:5] to either or both channels (dualchannel devices). This temperature offset may modify refresh behaviour for the channelto which the offset is provided. It will take a maximum of 200µs to have the change reflectedin MR4 OP[2:0] for the channel to which the offset is provided. If the inducedthermal gradient from the device temperature sensor location to the hot spot locationof the controller is greater than 15°C, self refresh mode will not reliably maintain memorycontents.

To accurately determine the temperature gradient between the memory thermal sensorand the induced hot spot, the memory thermal sensor location must be provided to thecontroller.

4.35 Temperature Sensor

The device has a temperature sensor that can be read from MR4. This sensor can beused to determine the appropriate refresh rate, to determine whether AC timing de-ratingis required at an elevated temperature range, and to monitor the operating temperature.Either the temperature sensor or the device T_{OPER} can be used to determine if operatingtemperature requirements are being met.

The device monitors device temperature and updates MR4 according to ^{t}TSI. Upon exitingself refresh or power-down, the device temperature status bits shall be no older than^{t}TSI.

When using the temperature sensor, the actual device case temperature may be higherthan the T_{OPER} specification that applies to standard or elevated temperature ranges.For example, T_{CASE} may be above 85°C when MR4[2:0] = b011. The device enables a 2°Ctemperature margin between the point when the device updates the MR4 value and thepoint when the controller reconfigures the system accordingly. When performing tightthermal coupling of the device to external hot spots, the maximum device temperaturemay be higher than indicated by MR4.

To ensure proper operation when using the temperature sensor, consider the following:
- TempGradient is the maximum temperature gradient experienced by the device at thetemperature of interest over a range of 2°C.
- ReadInterval is the time period between MR4 reads from the system.
- TempSensorInterval (^{t}TSI) is the maximum delay between the internal updates ofMR4.
- SysRespDelay is the maximum time between a read of MR4 and a response from thesystem.

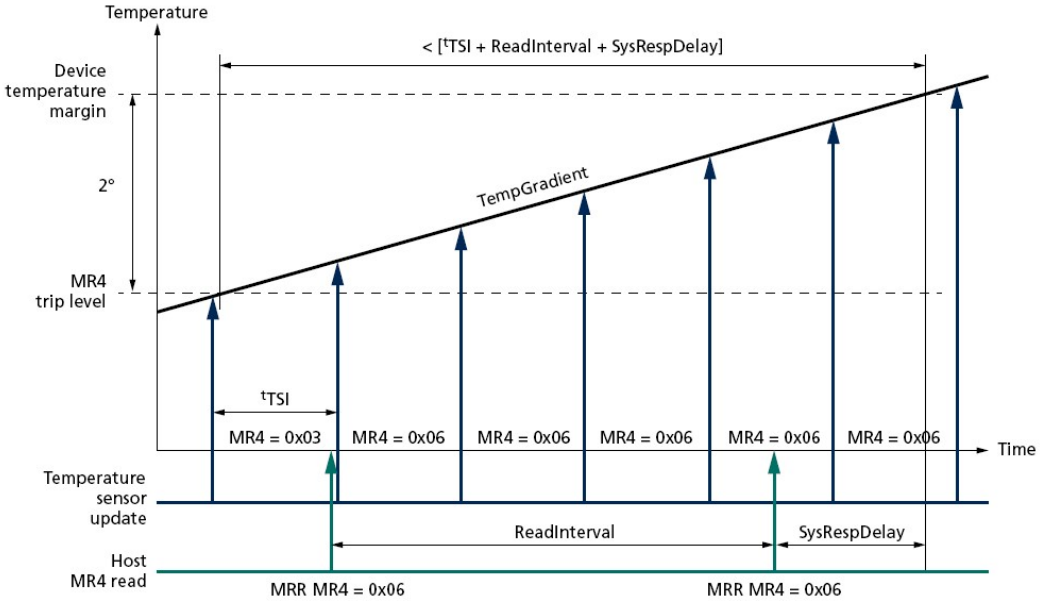
In order to determine the required frequency of polling MR4, the system uses the Temp-Gradient and the maximum response time of the system in the following equation:
TempGradient × (ReadInterval + ^{t}TSI + SysRespDelay) ≤ 2°C

Table 4-122: Temperature Sensor

Parameter	Symbol	MIN/MAX	Value	Unit
System temperature gradient	TempGradient	MAX	System Dependent	°C/s
MR4 read interval	ReadInterval	MAX	System Dependent	ms
Temperature sensor interval	^{t}TSI	MAX	32	ms
System response delay	SysRespDelay	MAX	System Dependent	ms
Device temperature margin	TempMargin	MAX	2	°C

For example, if TempGradient is 10°C/s and the SysRespDelay is 1ms:
(10°C/s) x (ReadInterval + 32ms + 1ms) ≤ 2°C
In this case, ReadInterval shall be no greater than 167ms.

Figure 4-118: Temperature Sensor Timing



4.36 ZQ Calibration

The MPC command is used to initiate ZQ calibration, which calibrates the output driverimpedance and CA/DQ ODT impedance across process, temperature, and voltage. ZQcalibration occurs in the background of device operation and is designed to eliminateany need for coordination between channels (that is, it allows for channel independence).ZQ calibration is required each time that the PU-Cal value (MR3-OP[0]) ischanged. Additional ZQ CALIBRATION commands may be required as the voltage andtemperature change in the system environment. CA ODT values (MR11-OP[6:4]) andDQ ODT values (MR11-OP[2:0]) may be changed without performing ZQ calibration, aslong as the PU-Cal value doesn′ t change.

There are two ZQ calibration modes initiated with the MPC command: ZQCAL STARTand ZQCAL LATCH. ZQCAL START initiates the calibration procedure, and ZQCALLATCH captures the result and loads it into the drivers.
A ZQCAL START command may be issued anytime the device is not in a power-downstate. A ZQCAL LATCH command may be issued anytime outside of power-down after ^{t}ZQCAL has expired and all DQ bus operations have completed. The CA bus must maintaina deselect state during ^{t}ZQLAT to allow CA ODT calibration settings to be updated.The DQ calibration value will not be updated until ZQCAL LATCH is performed and ^{t}ZQLAT has been met. The following mode register fields that modify I/O parameterscannot be changed following a ZQCAL START command and before ^{t}ZQCAL has expired:

- PU-Cal (pull-up calibration V_{OH} point)
- PDDS (pull-down drive strength and Rx termination)
- DQ ODT (DQ ODT value)
- CA ODT (CA ODT value)

ZQCAL Reset

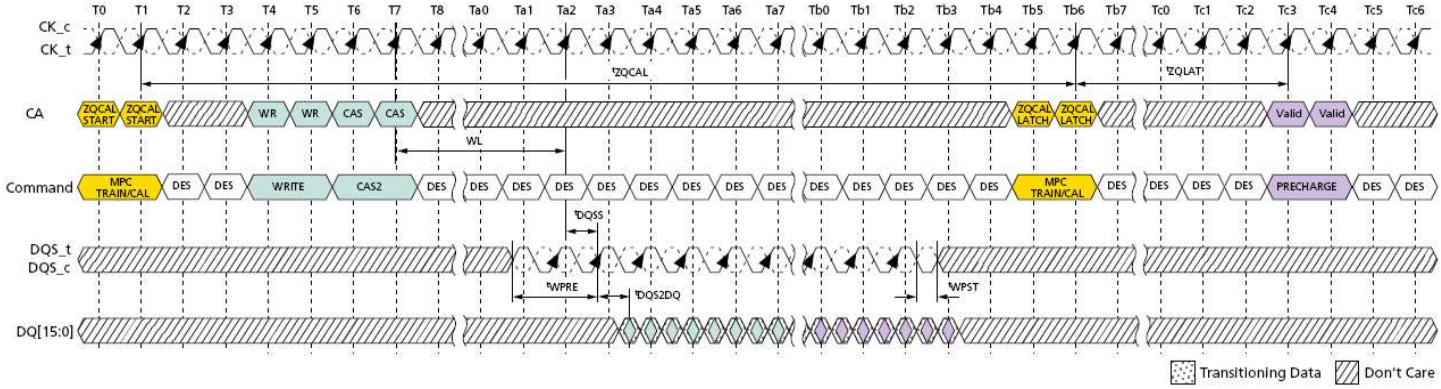
The ZQCAL RESET command resets the output impedance calibration to a default accuracyof ±30% across process, voltage, and temperature. This command is used to ensureoutput impedance accuracy to ±30% when ZQCAL START and ZQCAL LATCH commandsare not used.

The ZQCAL RESET command is executed by writing MR10-OP[0] = 1B.

Table 4-123: ZQ Calibration Parameters

Parameter	Symbol	MIN/MAX	Value	Unit
ZQCAL START to ZQCAL LATCH command interval	^{t}ZQCAL	MIN	1	μs
ZQCAL LATCH to next valid command interval	^{t}ZQLAT	MIN	MAX (30ns, 8nCK)	ns
ZQCAL RESET to next valid command interval	^{t}ZQRESET	MIN	MAX (50ns, 3nCK)	ns

Figure 4-119: ZQCAL Timing



Notes:

1. WRITE and PRECHARGE operations are shown for illustrative purposes. Any single ormultiple valid commands may be executed within the ^{t}ZQCAL time and prior to latchingthe results.
2. Before the ZQCAL LATCH command can be executed, any prior commands that utilizethe DQ bus must have completed. WRITE commands with DQ termination must be givenenough time to turn off the DQ ODT before issuing the ZQCAL LATCH command. Seethe ODT section for ODT timing.

Multichannel Considerations

The device includes a single ZQ pin and associated ZQ calibration circuitry. Calibrationvalues from this circuit will be used by both channels according to the following protocol:

- The ZQCAL START command can be issued to either or both channels.
- The ZQCAL START command can be issued when either or both channels are executingother commands, andother commands can be issued during ^{t}ZQCAL.
- The ZQCAL START command can be issued to both channels simultaneously.
- The ZQCAL START command will begin the calibration unless a previously requestedZQ calibration is inprogress.
- If the ZQCAL START command is received while a ZQ calibration is in progress, thecommand will be ignored andthe in-progress calibration will not be interrupted.
- The ZQCAL LATCH command is required for each channel.
- The ZQCAL LATCH command can be issued to both channels simultaneously.
- The ZQCAL LATCH command will latch results of the most recent ZQCAL STARTcommand provided ^{t}ZQCAL hasbeen met.
- ZQCAL LATCH commands that do not meet ^{t}ZQCAL will latch the results of the mostrecently completed ZQcalibration.
- The ZQRESET MRW commands will only reset the calibration values for the channelissuing the command.

In compliance with complete channel independence, either channel may issue ZQCALSTART and ZQCAL LATCH commands as needed without regard to the state of the otherchannel.

ZQ External Resistor, Tolerance, and Capacitive Loading

To use the ZQ CALIBRATION function, a 240 ohm, ±1% tolerance external resistor mustbe connected between the ZQ pin and V_{DDQ}.

If the system configuration shares the CA bus to form a x32 (or wider) channel, the ZQpin of each die's x16 channel must use a separate ZQCAL resistor.

If the system configuration has more than one rank, and if the ZQ pins of both ranks areattached to a single resistor, then the SDRAM controller must ensure that the ZQCAL'sdon't overlap.

The total capacitive loading on the ZQ pin must be limited to 25pF. For example, if a systemconfiguration shares a CA bus between n channels to form an n x16 wide bus, andno means are available to control the ZQCAL separately for each channel (that is, separateCS, CKE, or CK), then each x16 channel must have a separate ZQCAL resistor. For ax32, two-rank system, each x16 channel must have its own ZQCAL resistor, but theZQCAL resistor can be shared between ranks on each x16 channel. In this configuration,the CS signal can be used to ensure that the ZQCAL commands for Rank[0] and Rank[1]don't overlap.

4.37 Frequency Set Points

Frequency set points enable the CA bus to be switched between two differing operatingfrequencies with changes in voltage swings and termination values, without ever beingin an untrained state, which could result in a loss of communication to the device. Thisis accomplished by duplicating all CA bus mode register parameters, as well as othermode register parameters commonly changed with operating frequency.

These duplicated registers form two sets that use the same mode register addresses,with read/write access controlled by MR bit FSP-WR (frequency set point write/read)and the operating point controlled by MR bit FSP-OP (FREQUENCY SET POINT operation).Changing the FSP-WR bit enables MR parameters to be changed for an alternatefrequency set-point without affecting the current operation.

Once all necessary parameters have been written to the alternate set point, changingthe FSP-OP bit will switch operation to use all of the new parameters simultaneously(within tFC), eliminating the possibility of a loss of communication that could becaused by a partial configuration change.

Parameters that have two physical registers controlled by FSP-WR and FSP-OP includethose in the following table.

Table 4-124: Mode Register Function with Two Physical Registers

MR Number	Operand	Function	Notes
MR1	OP[1:0]	BL (Burst length)	
	OP[2]	WR-PRE (Write preamble length)	
	OP[3]	RD-PRE (Read preamble type)	
	OP[6:4]	nWR (Write-recovery for AUTO PRECHARGE command)	
	OP[7]	RD-PST (Read postamble length)	
MR2	OP[2:0]	RL (READ latency)	
	OP[5:3]	WL (WRITE latency)	
	OP[6]	WLS (WRITE latency set)	
MR3	OP[0]	PU-CAL (Pull-up calibration point)	1
	OP[1]	WR-PST (Write postamble length)	
	OP[5:3]	PDDS (Pull-down drive strength)	
	OP[6]	DBI-RD (DBI-read enable)	
	OP[7]	DBI-WR (DBI-write enable)	
MR11	OP[2:0]	DQ ODT (DQ bus receiver on-die termination)	
	OP[6:4]	CA ODT (CA bus receiver on-die termination)	
MR12	OP[5:0]	$V_{REF(CA)}$ ($V_{REF(CA)}$ setting)	
	OP[6]	VR_{CA} ($V_{REF(CA)}$ range)	
MR14	OP[5:0]	$V_{REF(DQ)}$ ($V_{REF(DQ)}$ setting)	
	OP[6]	VR_{DQ} ($V_{REF(DQ)}$ range)	
MR22	OP[2:0]	SOC ODT (Controller ODT value for V_{OH} calibration)	
	OP[3]	ODTE-CK (CK ODT enabled for non-terminating rank)	
	OP[4]	ODTE-CS (CS ODT enable for non-terminating rank)	
	OP[5]	ODTD-CA (CA ODT termination disable)	

Note:

1. For dual-channel devices, PU-CAL setting is required as the same value for both Ch.Aand Ch.B before issuing ZQCAL START command. See Mode Register Definition sectionfor more details.

The table below shows how the two mode registers for each of the parameters in theprevious table can be modified by setting the appropriate FSP-WR value and how deviceoperation can be switched between operating points by setting the appropriate FSP-OPvalue. The FSP-WR and FSP-OP functions operate completely independently.

Table 4-125: Relation Between MR Setting and DRAM Operation

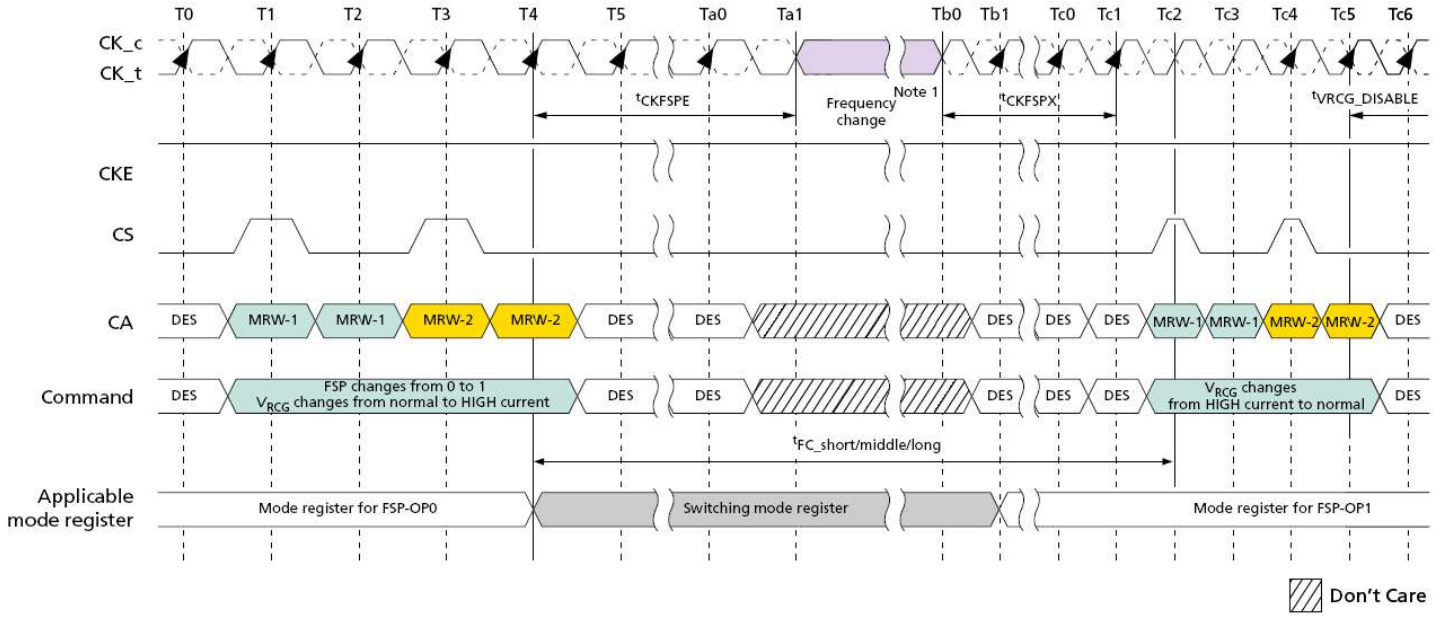
Function	MR# and Operand	Data	Operation	Notes
FSP-WR	MR13 OP[6]	0 (default)	Data write to mode register N for FSP-OP[0] by MRW command.	1
			Data read from mode register N for FSP-OP[0] by MRR command.	
		1	Data write to mode register N for FSP-OP[1] by MRW command.	
			Data read from mode register N for FSP-OP[1] by MRR command.	
FSP-OP	MR13 OP[7]	0 (default)	DRAM operates with mode register N for FSP-OP[0] setting.	2
		1	DRAM operates with mode register N for FSP-OP[1] setting.	

Notes:
1. FSP-WR stands for frequency set point write/read.
2. FSP-OP stands for frequency set point operating point.

Frequency Set Point Update Timing

The frequency set point update timing is shown below. When changing the frequencyset point via MR13 OP[7], the V_{RCG} setting: MR13 OP[3] have to be changed into V_{REF}fast response (high current) mode at the same time. After frequency change time (^{t}FC) issatisfied. V_{RCG} can be changed into normal operation mode via MR13 OP[3].

Figure 4-120: Frequency Set Point Switching Timing



Note:
1. For frequency change during frequency set point switching, refer to input Clock Stopand Frequency Change section.

Table 4-126: Frequency Set Point AC Timing

Parameter	Symbol	Min/ Max	Data Rate		Unit	Notes
			1600	3200		
Frequency set point switching time	^{t}FC_short	MIN	200		ns	1
	^{t}FC_middle	MIN	200		ns	
	^{t}FC_long	MIN	250		ns	
Valid clock requirement after entering FSPchange	^{t}CKFSPE	MIN	MAX(7.5ns, 4nCK)		–	
Valid clock requirement before first valid commandafter FSP change	tCKFSPX	MIN	MAX(7.5ns, 4nCK)		–	

Note:

1. Frequency set point switching time depends on value of $V_{REF(CA)}$ setting: MR12 OP[5:0]and $V_{REF(CA)}$ range: MR12 OP[6] of FSP-OP 0 and 1. The details are shown in table below.Additionally change of frequency set point may affect $V_{REF(DQ)}$ setting. Settling time of$V_{REF(DQ)}$ level is the same as $V_{REF(CA)}$ level.

Table 4-127: ^{t}FC Value Mapping

Application	Step Size		Range	
	From FSP-OP0	To FSP-OP1	From FSP-OP0	To FSP-OP1
^{t}FC_short	Base	A single step size incre-ment/decrement	Base	No change
^{t}FC_middle	Base	Two or more step size in-crement/decrement	Base	No change
FC_long	–	–	Base	Change

Note:

1. As well as change from FSP-OP1 to FSP-OP0.

Table 4-128: tFC Value Mapping: Example

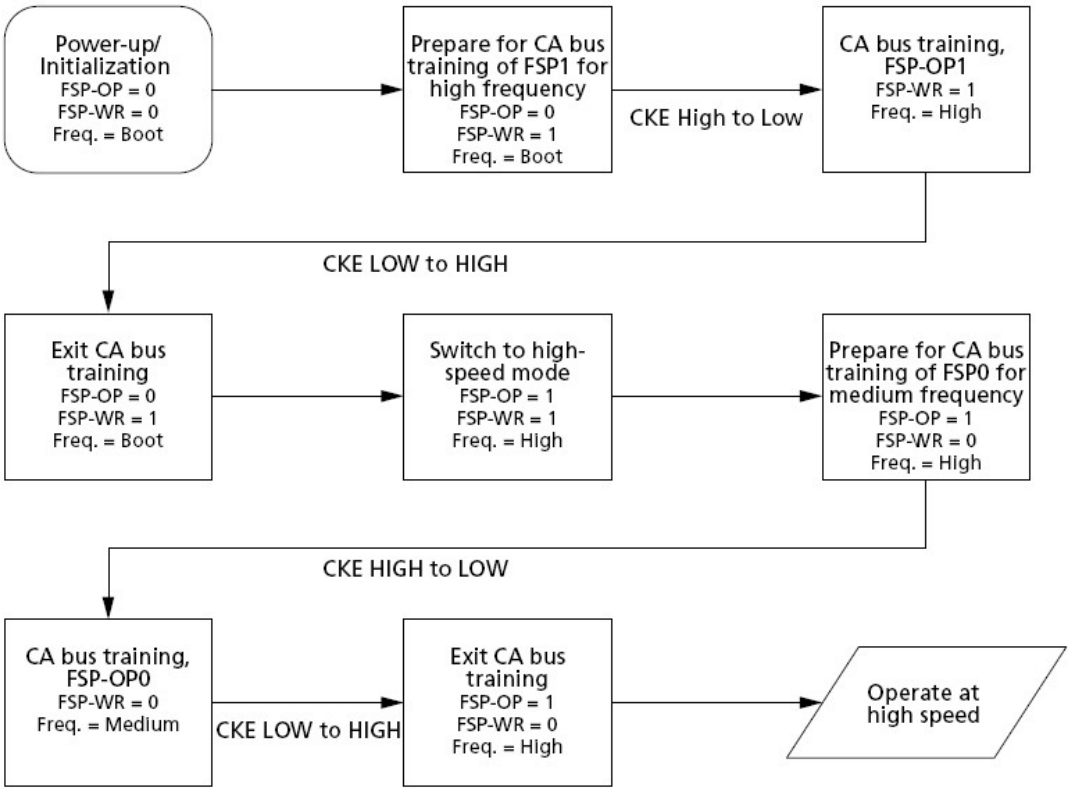
Case	From/To	FSP-OP: MR13 OP[7]	$V_{REF(CA)}$ Setting: MR12: OP[5:0]	$V_{REF(CA)}$ Range: MR12 OP[6]	Application	Notes
1	From	0	001100	0	^{t}FC_short	1
	To	1	001101	0		
2	From	0	001100	0	^{t}FC_middle	2
	To	1	001110	0		
3	From	0	Don't Care	0	^{t}FC_long	3
	To	1	Don't Care	1		

Notes:

1. A single step size increment/decrement for $V_{REF(CA)}$ setting value.
2. Two or more step size increment/decrement for $V_{REF(CA)}$ setting value.
3. $V_{REF(CA)}$ range is changed. In this case, changing $V_{REF(CA)}$ setting doesn't affect ^{t}FC value.

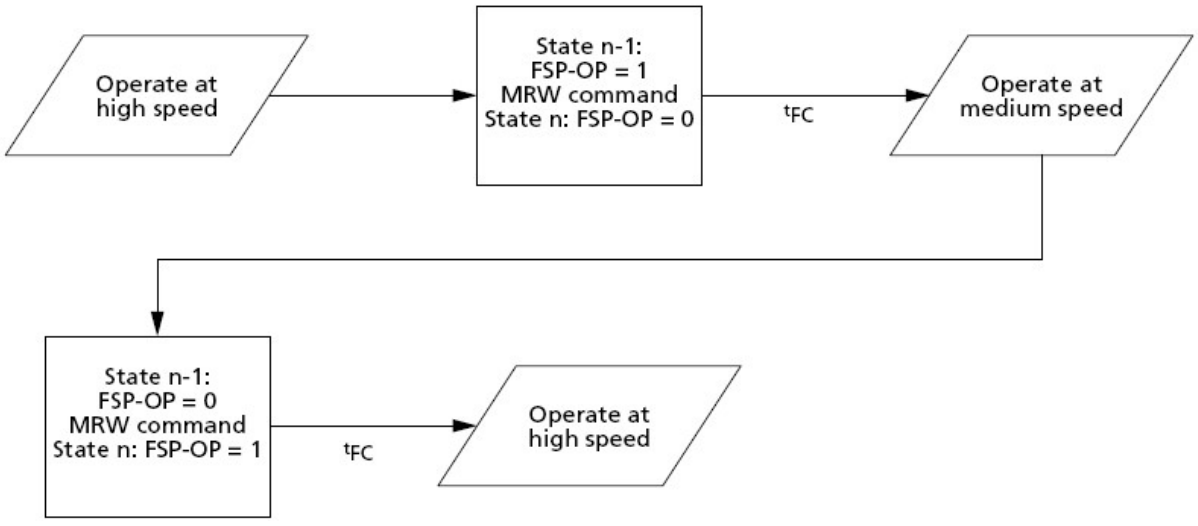
The LPDDR4 SDRAM defaults to FSP-OP[0] at power-up. Both set points default to settingsneeded to operate in un-terminated, low-frequency environments. To enable thedevice to operate at higher frequencies, Command bus training mode should be utilizedto train the alternate frequency set point. See Command Bus Training section formore details on this training mode.

Figure 4-121: Training for Two Frequency Set Points



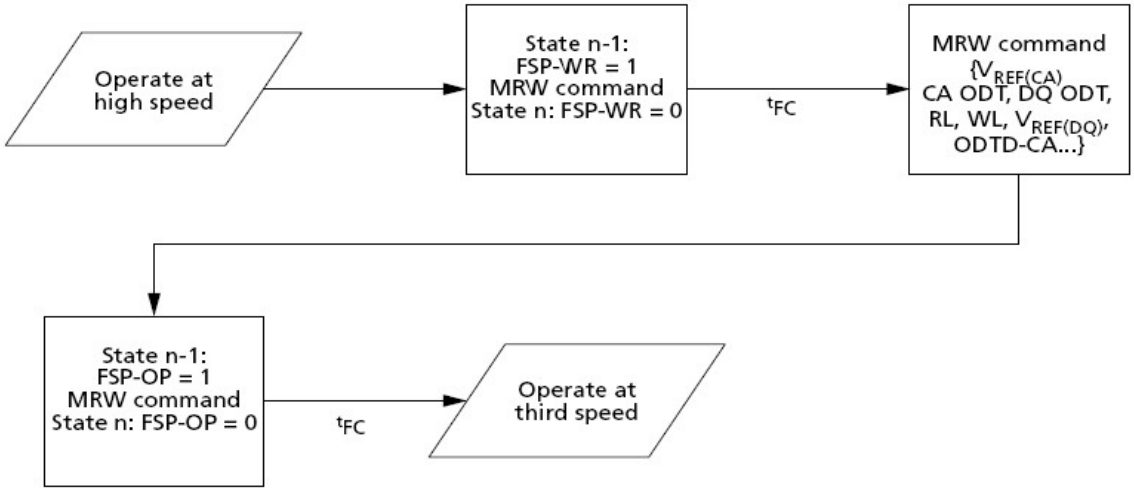
Once both of the frequency set points have been trained, switching between points canbe performed with a single MRW followed by waiting for time ^{t}FC.

Figure 4-122: Example of Switching Between Two Trained Frequency Set Points



Switching to a third (or more) set point can be accomplished if the memory controllerhas stored the previously-trained values (in particular the $V_{REF(CA)}$ calibration value)and rewrites these to the alternate set point before switching FSP-OP.

Figure 4-123: Example of Switching to a Third Trained Frequency Set Point



4.38 Pull-Up and Pull-Down Characteristics and Calibration

Table 4-129: Pull-Down Driver Characteristics – ZQ Calibration

R_{ONPD},nom	Register	Min	Nom	Max	Unit
40 Ohm	R_{ON40PD}	0.90	1.0	1.10	$R_{ZQ}/6$
48 Ohm	R_{ON48PD}	0.90	1.0	1.10	$R_{ZQ}/5$
60 Ohm	R_{ON60PD}	0.90	1.0	1.10	$R_{ZQ}/4$
80 Ohm	R_{ON80PD}	0.90	1.0	1.10	$R_{ZQ}/3$
120 Ohm	$R_{ON120PD}$	0.90	1.0	1.10	$R_{ZQ}/2$
240 Ohm	$R_{ON240PD}$	0.90	1.0	1.10	$R_{ZQ}/1$

Note:
1. All value are after ZQ calibration. Without ZQ calibration, R_{ONPD} values are ±30%.

Table 4-130: Pull-Up Characteristics – ZQ Calibration

V_{OHPU},nom	V_{OH},nom	Min	Nom	Max	Unit
$V_{DDQ}/0.5$	300	0.90	1.0	1.10	V_{OH},nom
$V_{DDQ}/0.6$	360	0.90	1.0	1.10	V_{OH},nom

Notes:
1. All value are after ZQ calibration. Without ZQ calibration, R_{ONPD} values are ±30%.
2. V_{OH},nom (mV) values are based on a nominal V_{DDQ} = 0.6V.

Table 4-131: Valid Calibration Points

V_{OHPU}	ODT Value					
	240	120	80	60	48	40
$V_{DDQ}/0.5$	Valid	Valid	Valid	Valid	Valid	Valid
$V_{DDQ}/0.6$	DNU	Valid	DNU	Valid	DNU	DNU

Notes:
1. Once the output is calibrated for a given $V_{OH(nom)}$ calibration point, the ODT value maybe changed without recalibration.
2. If the $V_{OH(nom)}$ calibration point is changed, then recalibration is required.
3. DNU = Do not use.

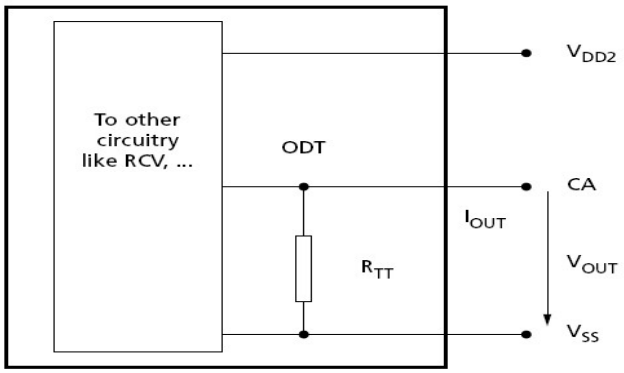
4.39 On-Die Termination for the Command/Address Bus

The on-die termination (ODT) feature allows the device to turn on/off termination resistancefor CK_t, CK_c, CS, and CA[5:0] signals without the ODT control pin. The ODTfeature is designed to improve signal integrity of the memory channel by allowing theDRAM controller to turn on and off termination resistance for any target DRAM devicesvia the mode register setting.

A simple functional representation of the DRAM ODT feature is shown below.

Figure 4-124: ODT for CA

$$R_{TT} = \frac{V_{OUT}}{|I_{OUT}|}$$



ODT Mode Register and ODT State Table

ODT termination values are set and enabled via MR11. The CA bus (CK_t, CK_c, CS,CA[5:0]) ODT resistance values are set by MR11 OP[6:4]. The default state for the CA isODT disabled.

ODT is applied on the CA bus to the CK_t, CK_c, CS, and CA signals. Generally only onetermination load will be present even if multiple devices are sharing the command signals.In contrast to LPDDR4 where the ODT_CA input is used in combination withmode registers. Before enabling CA termination via MR11, all ranks should have appropriate MR22 terminationsettingsrogrammed. In a multi rank system, the terminating rank should betrained first, followed by the non-terminating rank(s).

Table 4-132: Command Bus ODT State

CA ODT MR11[6:4]	ODTD-CA MR22 OP[5]	ODTE-CK MR22 OP[3]	ODTE-CS MR22 OP[4]	ODT State for CA	ODT State for CK	ODT State for CS
Disabled[1]	Valid[2]	Valid[2]	Valid[2]	Off	Off	Off
Valid[2]	0	0	0	On	On	On
Valid[2]	0	0	1	On	On	Off
Valid[2]	0	1	0	On	Off	On
Valid[2]	0	1	1	On	Off	Off
Valid[2]	1	0	0	Off	On	On
Valid[2]	1	0	1	Off	On	Off
Valid[2]	1	1	0	Off	Off	On
Valid[2]	1	1	1	Off	Off	Off

Notes:
1. Default value.
2. Valid = 0 or 1.

ODT Mode Register and ODT Characteristics

Table 4-133: ODT DC Electrical Characteristics for DQ Bus

RZQ = 240Ω ±1% over entire operating range after calibration

MR11 OP[6:4]	R_{TT}	VOUT	Min	Nom	Max	Unit	Notes
001b	240Ω	$V_{OL(DC)}$ = 0.2 × V_{DDQ}	0.8	1.0	1.1	R_{ZQ}/1	1, 2
		$V_{OM(DC)}$ = 0.50 ×V_{DDQ}	0.9	1.0	1.1		
		$V_{OH(DC)}$ = 0.75 ×V_{DDQ}	0.9	1.0	1.3		
010b	120Ω	$V_{OL(DC)}$ = 0.2 × V_{DDQ}	0.8	1.0	1.1	R_{ZQ}/2	1, 2
		$V_{OM(DC)}$ = 0.50 ×V_{DDQ}	0.9	1.0	1.1		
		$V_{OH(DC)}$ = 0.75 ×V_{DDQ}	0.9	1.0	1.3		
011b	80Ω	$V_{OL(DC)}$ = 0.2 × V_{DDQ}	0.8	1.0	1.1	R_{ZQ}/3	1, 2
		$V_{OM(DC)}$ = 0.50 ×V_{DDQ}	0.9	1.0	1.1		
		$V_{OH(DC)}$ = 0.75 ×V_{DDQ}	0.9	1.0	1.3		
100b	60Ω	$V_{OL(DC)}$ = 0.2 × V_{DDQ}	0.8	1.0	1.1	R_{ZQ}/4	1, 2
		$V_{OM(DC)}$ = 0.50 ×V_{DDQ}	0.9	1.0	1.1		
		$V_{OH(DC)}$ = 0.75 ×V_{DDQ}	0.9	1.0	1.3		
101b	48Ω	$V_{OL(DC)}$ = 0.2 × V_{DDQ}	0.8	1.0	1.1	R_{ZQ}/5	1, 2
		$V_{OM(DC)}$ = 0.50 ×V_{DDQ}	0.9	1.0	1.1		
		$V_{OH(DC)}$ = 0.75 ×V_{DDQ}	0.9	1.0	1.3	R_{ZQ}/6	1, 2
110b	40Ω	$V_{OL(DC)}$ = 0.2 × V_{DDQ}	0.8	1.0	1.1	R_{ZQ}/6	1, 2
		$V_{OM(DC)}$ = 0.50 ×V_{DDQ}	0.9	1.0	1.1		
		$V_{OH(DC)}$ = 0.75 ×V_{DDQ}	0.9	1.0	1.3		
Mismatch, CA -CA within clockgroup		0.5 × V_{DDQ}	–	–	2	%	1, 2, 3

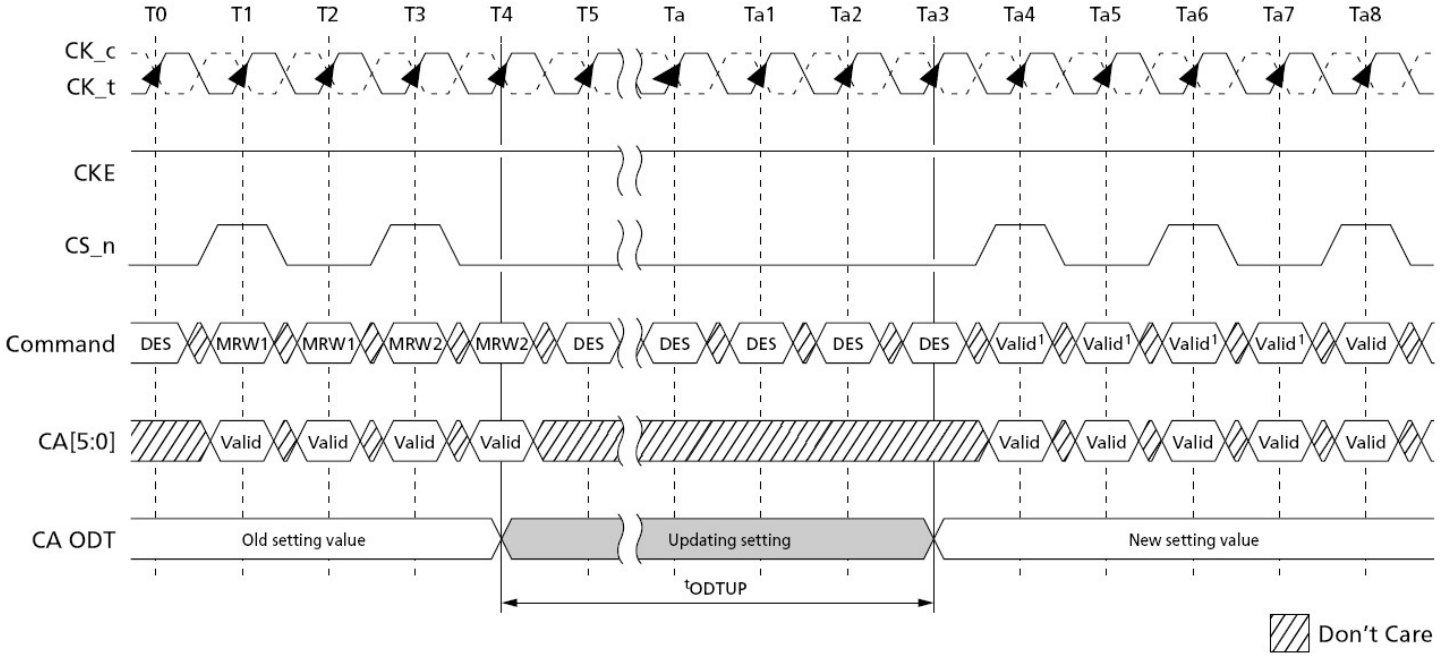
Notes:

1. The tolerance limits are specified after calibration with stable temperature and voltage. To understand the behavior of the tolerance limits when voltage or temperature changes after calibration, see the section on voltage and temperature sensitivity.
2. Pull-down ODT resistors are recommended to be calibrated at 0.50 × V_{DDQ}. Other calibration points may be required to achieve the linearity specification shown above, for example, calibration at 0.75 × V_{DDQ} and 0.20 × V_{DDQ}.
3. CA to CA mismatch within clock group variation for a given component including CK_t, CK_c ,and CS (characterized).

$$\text{CA-to-CA mismatch} = \frac{R_{ODT}(MAX) - R_{ODT}(MIN)}{R_{ODT}(AVG)}$$

ODT for CA Update Time

Figure 4-125: ODT for CA Setting Update Timing in 4-Clock Cycle Command



4.40 DQ On-Die Termination

On-die termination (ODT) is a feature that allows the device to turn on/off terminationresistance for each DQ, DQS, and DMI signal without the ODT control pin. The ODTfeature is designed to improve signal integrity of the memory channel by allowing theDRAM controller to turn on and off termination resistance for any target DRAM devicesduring WRITE or MASK WRITE operation.

The ODT feature is off and cannot be supported in power-down and self refresh modes.

The switch is enabled by the internal ODT control logic, which uses the WRITE-1 orMASK WRITE-1 command and other mode register control information. The value ofRTT is determined by the MR bits.

$$R_{TT} = \frac{V_{OUT}}{|I_{OUT}|}$$

Figure 4-126: Functional Representation of DQ ODT

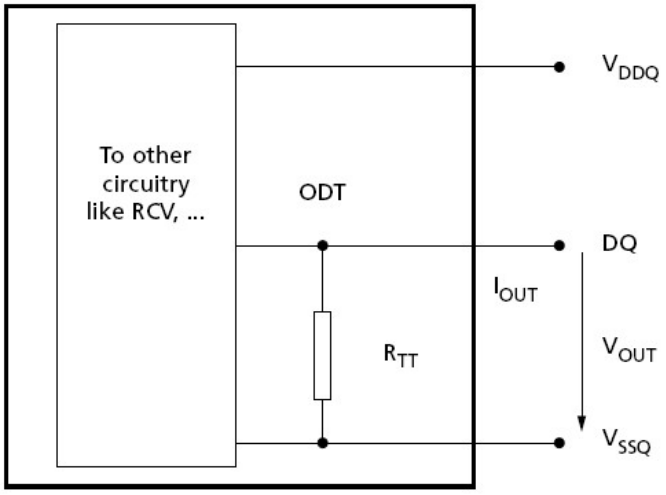


Table 4-134: ODT DC Electrical Characteristics for DQ Bus

R_{ZQ} = 240Ω ±1% over entire operating range after calibration

MR11 OP[6:4]	R_{TT}	V_{OUT}	Min	Nom	Max	Unit	Notes
001b	240Ω	$V_{OL(DC)}$ = 0.2 × V_{DDQ}	0.8	1.0	1.1	R_{ZQ}/1	1, 2
		$V_{OM(DC)}$ = 0.50× V_{DDQ}	0.9	1.0	1.1		
		$V_{OH(DC)}$ = 0.75 × V_{DDQ}	0.9	1.0	1.3		
010b	120Ω	$V_{OL(DC)}$ = 0.2 × V_{DDQ}	0.8	1.0	1.1	R_{ZQ}/2	1, 2
		$V_{OM(DC)}$ = 0.50× V_{DDQ}	0.9	1.0	1.1		
		$V_{OH(DC)}$ = 0.75 × V_{DDQ}	0.9	1.0	1.3		
011b	80Ω	$V_{OL(DC)}$ = 0.2 × V_{DDQ}	0.8	1.0	1.1	R_{ZQ}/3	1, 2
		$V_{OM(DC)}$ = 0.50× V_{DDQ}	0.9	1.0	1.1		
		$V_{OH(DC)}$ = 0.75 × V_{DDQ}	0.9	1.0	1.3		
100b	60Ω	$V_{OL(DC)}$ = 0.2 × V_{DDQ}	0.8	1.0	1.1	R_{ZQ}/4	1, 2
		$V_{OM(DC)}$ = 0.50× V_{DDQ}	0.9	1.0	1.1		
		$V_{OH(DC)}$ = 0.75 × V_{DDQ}	0.9	1.0	1.3		
101b	48Ω	$V_{OL(DC)}$ = 0.2 × V_{DDQ}	0.8	1.0	1.1	R_{ZQ}/5	1, 2
		$V_{OM(DC)}$ = 0.50× V_{DDQ}	0.9	1.0	1.1		
		$V_{OH(DC)}$ = 0.75 × V_{DDQ}	0.9	1.0	1.3		
110b	40Ω	$V_{OL(DC)}$ = 0.2 × V_{DDQ}	0.8	1.0	1.1	R_{ZQ}/6	1, 2
		$V_{OM(DC)}$ = 0.50× V_{DDQ}	0.9	1.0	1.1		
		$V_{OH(DC)}$ = 0.75 × V_{DDQ}	0.9	1.0	1.3		
Mismatch, CA -CA within clock group		0.50 × V_{DDQ}	–	–	2	%	1, 2, 3

Notes:

1. The ODT tolerance limits are specified after calibration with stable temperature andvoltage. To understand the behavior of the tolerance limits when voltage or temperaturechanges after calibration, see the following section on voltage and temperaturesensitivity.
2. Pull-down ODT resistors are recommended to be calibrated at 0.50 × V_{DDQ}. Other calibrationpoints may be used to achieve the linearity specification shown above, for example,calibration at 0.75 × V_{DDQ} and 0.20 × V_{DDQ}.
3. DQ-to-DQ mismatch within byte variation for a given component, including DQS (characterized).

$$\text{DQ-to-DQ mismatch} = \frac{R_{ODT}(MAX) - R_{ODT}(MIN)}{R_{ODT}(AVG)}$$

Output Driver and Termination Register Temperature and Voltage Sensitivity

When temperature and/or voltage change after calibration, the tolerance limits are widenaccording to the tables below.

Table 4-135: Output Driver and Termination Register Sensitivity Definition

Resistor	Definition Point	Min	Max	Unit	Notes
R_{ONPD}	0.50 × V_{DDQ}	90 - (dR_{ONdT} × |ΔT|) - (dR_{ONdV} × |ΔV|)	110 + (dR_{ONdT} × |ΔT|) - (dR_{ONdV} × |ΔV|)	%	1, 2
V_{OHPU}	0.50 × V_{DDQ}	90 - (dV_{OHdT} × |ΔT|) - (dV_{OHdV} × |ΔV|)	110 + (dV_{OHdT} × |ΔT|) - (dV_{OHdV} × |ΔV|)		1, 2
$R_{TT(I/O)}$	0.50 × V_{DDQ}	90 - (dR^{ONdT} × |ΔT|) - (dR_{ONdV} × |ΔV|)	110 + (dR_{ONdT} × |ΔT|) - (dR_{ONdV} × |ΔV|)		1, 2, 3
$R_{TT(IN)}$	0.50 × V_{DD2}	90 - (dR_{ONdT} × |ΔT|) - (dR_{ONdV}× |ΔV|)	110 + (dR_{ONdT} × |ΔT|) - (dR_{ONdV} × |ΔV|)		1, 2, 4

Notes:

1. ΔT = T - T(@calibration), ΔV = V - V(@calibration)
2. dR_{ONdT}, dR_{ONdV}, dV_{OHdT}, dV_{OHdV}, dR_{TTdV}, and dR_{TTdT} are not subject to production testbut are verified by design and characterization.
3. This parameter applies to input/output pin such as DQS, DQ, and DMI.
4. This parameter applies to input pin such as CK, CA, and CS.
5. Refer to Pull-up/Pull-down Driver Characteristics for V_{OHPU}.

Table 4-136: Output Driver and Termination Register Temperature and Voltage Sensitivity

Symbol	Parameter	Min	Max	Unit
dR_{ONdT}	R_{ON} temperature sensitivity	0	0.75	%/°C
dR_{ONdV}	R_{ON} voltage sensitivity	0	0.20	%/mV
dV_{OHdT}	V_{OH} temperature sensitivity	0	0.75	%/°C
dV_{OHdV}	V_{OH} voltage sensitivity	0	0.35	%/mV
dR_{TTdT}	R_{TT} temperature sensitivity	0	0.75	%/°C
dR_{TTdV}	R_{TT} voltage sensitivity	0	0.20	%/mV

ODT Mode Register

The ODT mode is enabled if MR11 OP[2:0] are non-zero. In this case, the value of R_{TT} isdetermined by the settings of those bits. The ODT mode is disabled if MR11 OP[2:0] = 0.

Asynchronous ODT

When ODT mode is enabled in MR11 OP[2:0], DRAM ODT is always High-Z. The DRAMODT feature is automatically turned ON asynchronously after a WRITE-1, MASKWRITE-1, or MPC[WRITE-FIFO] command. After the burst write is complete, the DRAMODT turns OFF asynchronously. The DQ bus ODT control is automatic and will turn theODT resistance on/off if DQ ODT is enabled in the mode register.
The following timing parameters apply when the DQ bus ODT is enabled:
• ODTLon, ^{t}ODTon (MIN), ^{t}ODTon (MAX)
• ODTLoff, ^{t}ODToff (MIN), ^{t}ODToff (MAX)
$ODTL_{ON}$ is a synchronous parameter and is the latency from a CAS-2 command to the^{t}ODTon reference. $ODTL_{ON}$ latency is a fixed latency value for each speed bin. Eachspeed bin has a different $ODTL_{ON}$ latency.

Minimum R_{TT} turn-on time (^{t}ODTon (MIN)) is the point in time when the device terminationcircuit leaves High-Z and ODT resistance begins to turn on.

Maximum R_{TT} turn on time (^{t}ODTon (MAX)) is the point in time when the ODT resistanceis fully on.

^{t}ODTon (MIN) and ^{t}ODTon (MAX) are measured once $ODTL_{on}$ latency is satisfied fromCAS-2 command.

$ODTL_{OFF}$ is a synchronous parameter and it is the latency from CAS-2 command to^{t}ODToff reference. $ODTL_{OFF}$ latency is a fixed latency value for each speed bin. Eachspeed bin has a different $ODTL_{OFF}$ latency.

Minimum R_{TT} turn-off time (^{t}ODToff (MIN)) is the point in time when the device terminationcircuit starts to turn off the ODT resistance.

Maximum ODT turn off time (^{t}ODToff (MAX)) is the point in time when the on-die terminationhas reached High-Z.

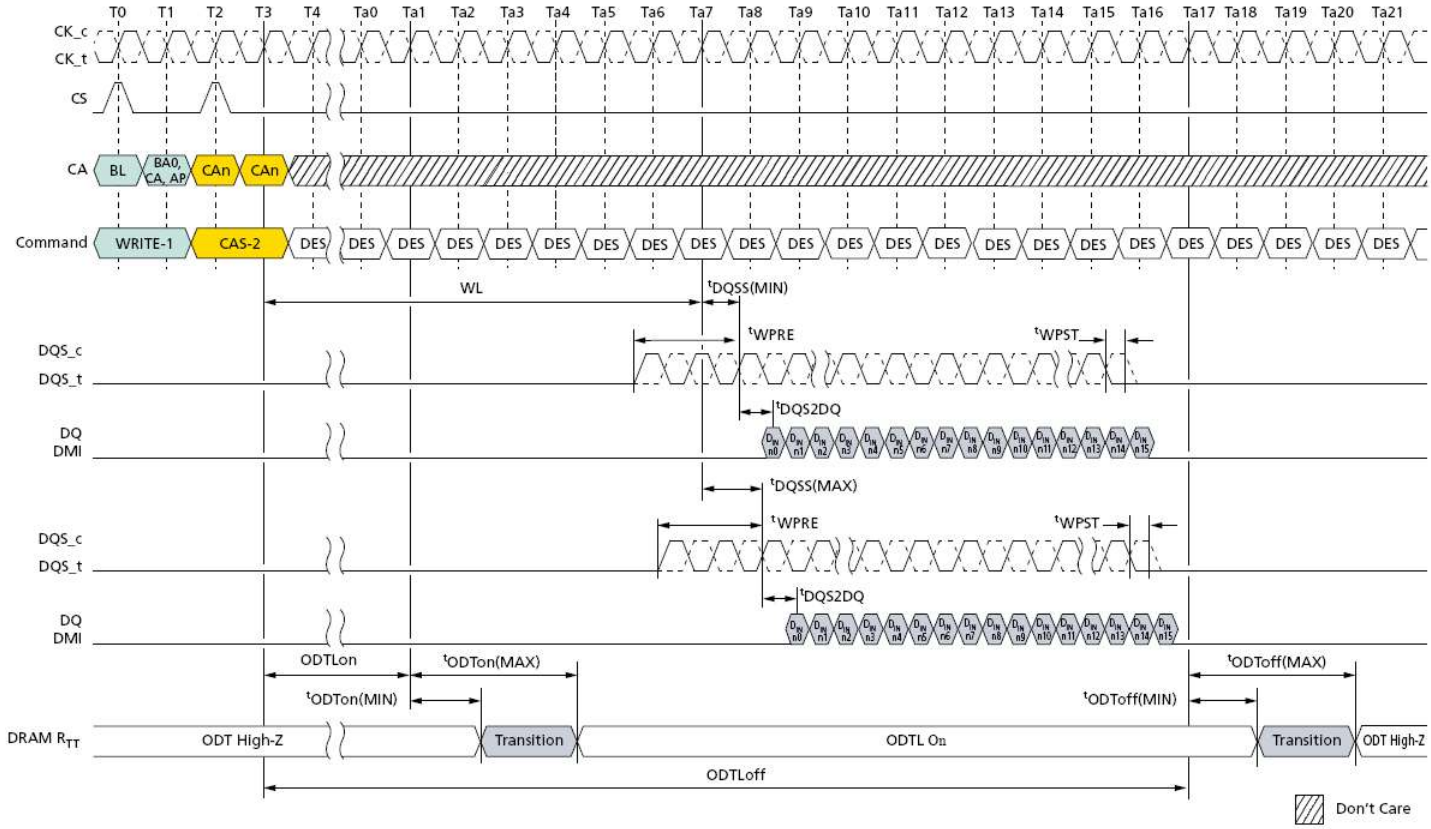
^{t}ODToff (MIN) and ^{t}ODToff (MAX) are measured once $ODTL_{off}$ latency is satisfied fromCAS-2 command.

Table 4-137: ODTLON and ODTLOFF Latency Values

$ODTL_{ON}$ Latency[1]		$ODTL_{OFF}$ Latency[2]		Lower Frequency Limit (>) (MHz)	Upper Frequency Limit (≤) (MHz)
^{t}WPRE = 2 ^{t}CK					
WL Set A (nCK)	WL Set B (nCK)	WL Set A (nCK)	WL Set B (nCK)		
N/A	N/A	N/A	N/A	10	266
N/A	N/A	N/A	N/A	266	533
N/A	6	N/A	22	533	800
4	12	20	28	800	1066
4	14	22	32	1066	1333
6	18	24s	36	1333	1600
6	20	26	40	1600	1866
8	24	28	44	1866	2133

Notes:
1. $ODTL_{ON}$ is referenced from CAS-2 command.
2. $ODTL_{OFF}$ as shown in table assumes BL = 16. For BL32, 8 ^{t}CK should be added.

Figure 4-127: Asynchronous ODTon/ODToff Timing



Notes:

1. BL = 16, Write postamble = 0.5nCK, DQ/DQS: V_{SSQ} termination
2. Din n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid atthese times.

DQ ODT During Power-Down and Self Refresh Modes

DQ bus ODT will be disabled in power-down mode. In self refresh mode, the ODT willbe turned off when CKE is LOW but will be enabled if CKE is HIGH and DQ ODT is enabledin the mode register.

ODT During Write Leveling Mode

If ODT is enabled in MR11 OP[2:0] in write leveling mode, the device always providesthe termination on DQS signals. DQ termination is always off in write leveling mode.

Table 4-138: Termination State in Write Leveling Mode

ODT State in MR11 OP[2:0]	DQS Termination	DQ[15:0]/DMI[1:0] Termination
Disabled	Off	Off
Enabled	On	Off

4.41 Target Row Refresh Mode

The device limits the number of times that a given row can be accessed within a refreshperiod (^{t}REFW × 2) prior to requiring adjacent rows to be refreshed. The maximum activatecount (MAC) is the maximum number of activates that a single row can sustainwithin a refresh period before the adjacent rows need to be refreshed. The row receivingthe excessive actives is the target row (TRn), the adjacent rows to be refreshed are thevictim rows. When the MAC limit is reached on TRn, either the device receives all (R × 2)REFRESH commands before another row activate is issued, or the device should beplaced into targeted row refresh (TRR) mode. The TRR mode will refresh the rows adjacentto the TRn that encountered ^{t}MAC limit.

If the device supports unlimited MAC value: MR24 OP[2:0] = 000 and MR24 OP[3] = 1,TARGET ROW REFRESH operation is not required. Even though the device allows to setMR24 OP[7] = 1: TRR mode enable, in this case the device behavior is vendor specific.For example, a certain device may ignore MRW command for entering/exiting TRRmode or a certain device may support commands related TRR mode. See vendor devicedatasheets for details about TRR mode definition at supporting unlimited MAC valuecase.

There could be a maximum of two target rows to a victim row in a bank. The cumulativevalue of the activates from the two target rows on a victim row in a bank should not exceedMAC value.

MR24 fields are required to support the new TRR settings. Setting MR24 OP[7] = 1 enablesTRR mode and setting MR24 OP[7] = 0 disables TRR mode. MR24 OP[6:4] defineswhich bank (BAn) the target row is located in (refer to MR24 table for details).

The TRR mode must be disabled during initialization as well as any other device calibrationmodes. The TRR mode is entered from a DRAM idle state, once TRR mode hasbeen entered, no other mode register commands are allowed until TRR mode is completed;however, setting MR24 OP[7] = 0 to interrupt and reissue the TRR mode is allowed.

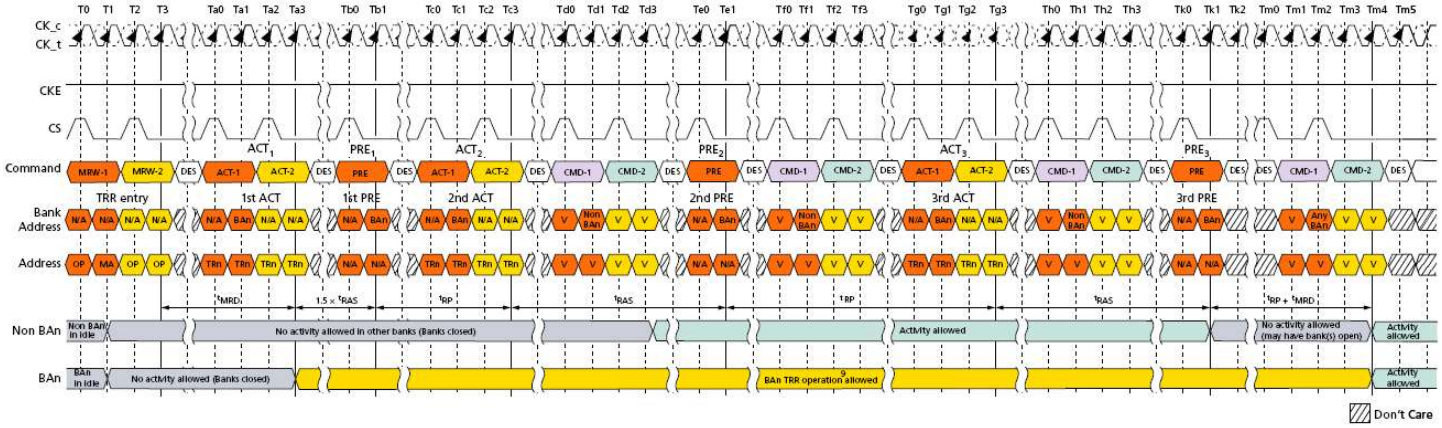
When enabled, TRR mode is self-clearing. the mode will be disabled automatically afterthe completion of defined TRR flow (after the third BAn precharge has completed plus^{t}MRD). Optionally, the TRR mode can also be exited via another MRS command at thecompletion of TRR by setting MR24 OP[7] = 0. If the TRR is exited via another MRS command,the value written to MR24 OP[6:4] are "Don't Care."

TRR Mode Operation

1. The timing diagram depicts TRR mode. The following steps must be performedwhen TRR mode is enabled. Thismode requires all three ACT (ACT1, ACT2, andACT3) and three corresponding PRE commands (PRE1, PRE2,and PRE3) to completeTRR mode. PRECHARGE All (PREA) commands issued while the device is inTRR modewill also perform precharge to BAn and counts towards PREn command.
2. Prior to issuing the MRW command to enter TRR mode, the device should be inthe idle state. MRW commandmust be issued with MR24 OP[7] = 1 and MR24OP[6:4] defining the bank in which the targeted row is located. Allother MR24 bitsshould remain unchanged.
3. No activity is to occur with the device until tMRD has been satisfied. When tMRDhas been satisfied, the onlycommands allowed BAn, until TRR mode has completed,are ACT and PRE.
4. The first ACT to the BAn with the TRn address can now be applied; no other commandis allowed at this point. Allother banks must remain inactive from when thefirst BAn ACT command is issued until [(1.5 x tRAS) + tRP] issatisfied.
5. After the first ACT to the BAn with the TRn address is issued, PRE to BAn is to beissued (1.5 × tRAS) later; andthen followed tRP later by the second ACT to the Banwith the TRn address.
6. After the second ACT to the BAn with the TRn address is issued, PRE to BAn is tobe issued tRAS later and thenfollowed tRP later by the third ACT to the BAn withthe TRn address.
7. After the third ACT to the BAn with the TRn address is issued, PRE to BAn wouldbe issued tRAS later. TRRmode is completed once tRP plus tMRD is satisfied.
8. TRR mode must be completed as specified to guarantee that adjacent rows are refreshed.Anytime the TRRmode is interrupted and not completed, the interruptedTRR mode must be cleared and then subsequentlyperformed again. To clear aninterrupted TRR mode, MR24 change is required with setting MR24 OP[7] = 0,MR24 OP[6:4] are "Don't care," followed by three PRE to BAn, with tRP time in betweeneach PRE command. Thecomplete TRR sequence (steps 2–7) must be thenreissued and completed to guarantee that the adjacent rowsare refreshed.

9. A REFRESH command to the device, or entering self refresh mode, is not allowedwhile the device is in TRRmode.

Figure 4-128: Target Row Refresh Mode



Notes:

1. TRn is the targeted row.
2. Bank BAn represents the bank in which the targeted row is located.
3. TRR mode self-clears after ^{t}MRD + ^{t}RP measured from the third BAn precharge PRE3 atclock edge Th4.
4. TRR mode or any other activity can be re-engaged after ^{t}RP + tMRD from the third Banprecharge PRE3.PRE_ALL also counts if it is issued instead of PREn. TRR mode is clearedby the device after PRE3 to the BAn bank.
5. ACTIVATE commands to BAn during TRR mode do not provide refresh support (the refreshcounter isunaffected).
6. The device must restore the degraded row(s) caused by excessive activation of the targetedrow (TRn) necessary to meetrefresh requirements.
7. A new TRR mode must wait ^{t}MRD + tRP time after the third precharge.
8. BAn may not be used with any other command.
9. ACT and PRE are the only allowed commands to BAn during TRR mode.
10. REFRESH commands are not allowed during TRR mode.
11. All timings are to be met by DRAM during TRR mode, such as ^{t}FAW. Issuing ACT1, ACT2,and ACT3 counts towards ^{t}FAW budget.

4.42 Post-Package Repair

The device has fail row address repair as an optional post-package repair (PPR) featureand it is readable through MR25 OP[7:0].

PPR provides simple and easy repair method in the system and fail row address can berepaired by the electrical programming of Electrical-fuse scheme. The device can correctone row per bank with PPR.

Electrical-fuse cannot be switched back to un-fused states once it is programmed. Thecontroller should prevent unintended PPR mode entry and repair.

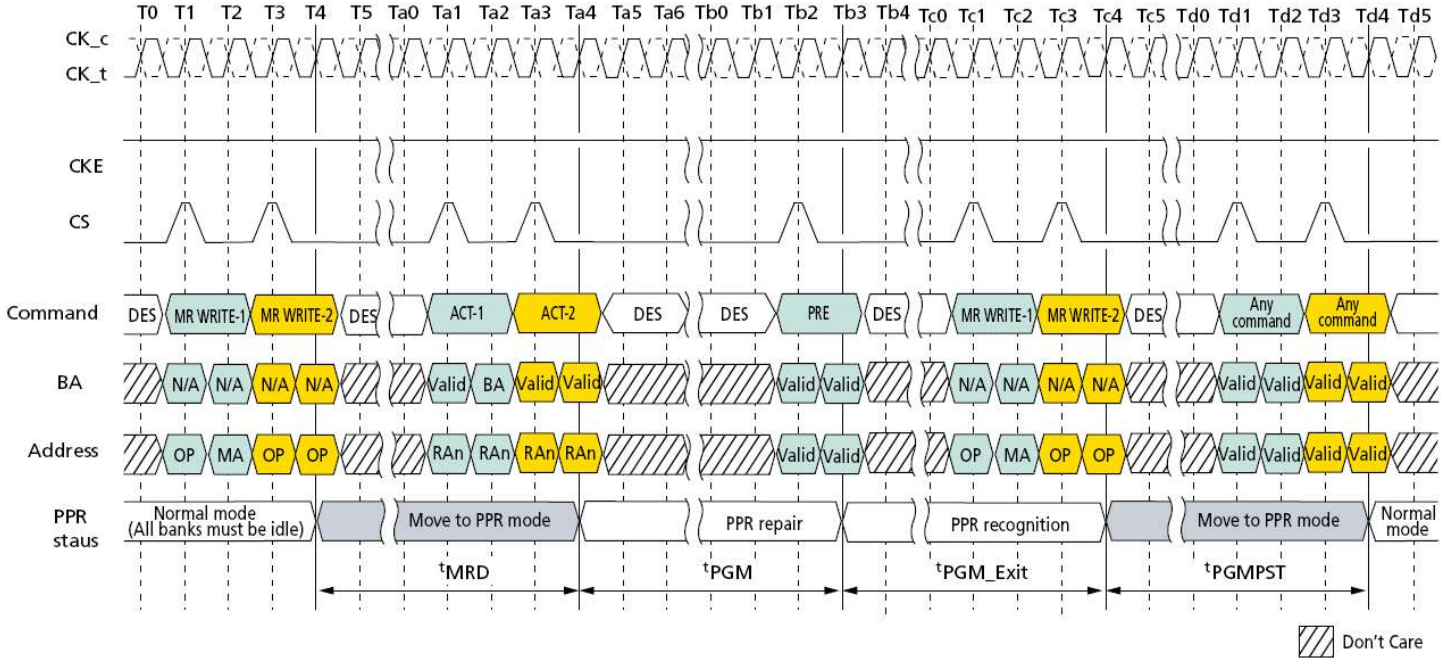
Failed Row Address Repair

1. Before entering PPR mode, all banks must be precharged.
2. Enable PPR using MR4 OP[4] = 1 and wait ^{t}MRD.
3. Issue ACT command with fail row address.
4. Wait ^{t}PGM to allow the device repair target row address internally then issue PRECHARGE
5. Wait ^{t}PGM_EXIT after PRECHARGE, which allows the device to recognize repairedrow address RAn.
6. Exit PPR mode with setting MR4 OP[4] = 0.
7. The device is ready for any valid command after ^{t}PGMPST.
8. In more than one fail address repair case, repeat step 2 to 7.

Once PPR mode is exited, to confirm whether the target row has correctly repaired, thehost can verify the repair by writing data into the target row and reading it back afterPPR exit with MR4 OP[4] = 0 and ^{t}PGMPST.

The following timing diagram shows PPR operation.

Figure 4-129: Post-Package Repair Timing



Notes:

1. During ^{t}PGM, any other commands (including refresh) are not allowed on each die.
2. With one PPR command, only one row can be repaired at one time per die.
3. When PPR procedure completes, reset procedure is required before normal operation.
4. During PPR, memory contents are not refreshed and may be lost.

Table 4-139: Post-Package Repair Timing Parameters

Parameter	Symbol	Min	Max	Units
PPR programming time	tPGM	1000	–	ms
PPR exit time	tPGM_EXIT	15	–	ns
New address setting time	tPGMPST	50	–	µs

4.43 Read Preamble Training

Read preamble training is supported through the MPC function.

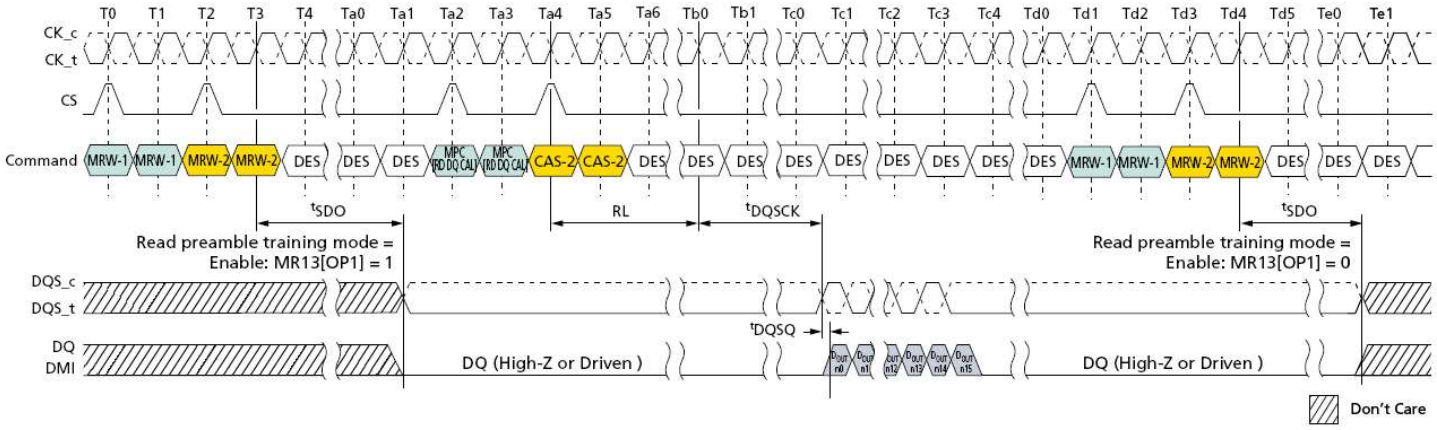
This mode can be used to train or read level the DQS receivers. After read preambletraining is enabled by MR13 OP[1] = 1, the device will drive DQS_t LOW and DQS_cHIGH within tSDO and remain at these levels until an MPC[READ DQ CALIBRATION]command is issued.

During read preamble training, the DQS preamble provided during normal operationwill not be driven by the device. After the MPC[READ DQ CALIBRATION] command isissued, the device will drive DQS_t/DQS_c and DQ like a normal READ burst after RLand tDQSCK. Prior to the MPC[READ DQ CALIBRATION] command, the device may ormay not drive DQ[15:0] in this mode.

While in read preamble training mode, only READ DQ CALIBRATION commands maybe issued.
- Issue an MPC[READ DQ CALIBRATION] command followed immediately by a CAS-2command.
- Each time an MPC[READ DQ CALIBRATION] command followed by a CAS-2 is receivedby the device, a 16-bitdata burst will, after the currently set RL, drive the eightbits programmed in MR32 followed by the eight bitsprogrammed in MR40 on all I/Opins.
- The data pattern will be inverted for I/O pins with a 1 programmed in the correspondinginvert mask mode registerbit.
- Note that the pattern is driven on the DMI pins, but no DATA BUS INVERSION functionis enabled, even if readDBI is enabled in the DRAM mode register.
- This command can be issued every tCCD seamlessly.
- The operands received with the CAS-2 command must be driven LOW.

Read preamble training is exited within tSDO after setting MR13 OP[1] = 0.

Figure 4-130: Read Preamble Training



Note:
1. Read DQ calibration supports only BL16 operation.

4.44 Electrical Specifications

Absolute Maximum Ratings

Stresses greater than those listed in the table below may cause permanent damage tothe device. This is a stress rating only, and functional operation of the device at theseconditions, or any other conditions outside those indicated in the operational sectionsof this document, is not implied. Exposure to absolute maximum rating conditions forextended periods may adversely affect reliability.

Table 4-140: Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Unit	Notes
V_{DD1} supply voltage relative to V_{SS}	V_{DD1}	–0.4	2.1	V	1
V_{DD2} supply voltage relative to V_{SS}	V_{DD2}	–0.4	1.5	V	1
V_{DDQ} supply voltage relative to V_{SS}	V_{DDQ}	–0.4	1.5	V	1
Voltage on any ball relative to V_{SS}	V_{IN}, V_{OUT}	–0.4	1.5	V	
Storage temperature	T_{STG}	–55	125	˚C	2

Notes:

1. For information about relationships between power supplies, see the Voltage Ramp andDevice Initialization section.
2. Storage temperature is the case surface temperature on the center/top side of the device.For measurement conditions, referto the JESD51-2 standard.

4.45 AC and DC Operating Conditions

Operation or timing that is not specified is illegal. To ensure proper operation, the devicemust be initialized properly.

Table 4-141: Recommended DC Operating Conditions

Symbol	Min	Typ	Max	DRAM	Unit	Notes
V_{DD1}	1.7	1.8	1.95	Core 1 power	V	1, 2
V_{DD2}	1.06	1.1	1.17	Core 2 power/Input buffer power	V	1, 2, 3
V_{DDQ}	1.06	1.1	1.17	I/O buffer power	V	2, 3

Notes:

1. V_{DD1} uses significantly less power than V_{DD2}.
2. The voltage range is for DC voltage only. DC voltage is the voltage supplied at theDRAM and is inclusive of all noise up to20 MHz at the DRAM package ball.
3. The voltage noise tolerance from DC to 20 MHz exceeding a peak-to-peak tolerance of45mV at the DRAM ball is not included in the TdIVW.

Table 4-142: Input Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input leakage current	IL	–4	4	µA	1, 2

Notes:

1. For CK_t, CK_c, CKE, CS, CA, ODT_CA, and RESET_n. Any input 0V ≤ V_{IN} ≤ V_{DD2}. (All otherpins not under test = 0V.
2. CA ODT is disabled for CK_t, CK_c, CS, and CA.

Table 4-143: Input/Output Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/Output leakage current	IOZ	–5	5	µA	1, 2

Notes:
1. For DQ, DQS_t, DQS_c, and DMI. Any I/O 0V ≤ V_{OUT} ≤ V_{DDQ}.
2. I/Os status are disabled: High Impedance and ODT off.

Table 4-144: Operating Temperature Range

Parameter/Condition	Symbol	Min	Max	Unit
Standard	T_{OPER}	Note 4	85	˚C

Note:
1. Refer to operating temperature range on top page.
2. When using the device in the elevated temperature range, some derating may be required.
   See Mode Registers for vendor-specific derating.
3. Either the device case temperature rating or the temperature sensor can be used to setan appropriate refresh rate, determine the need for AC timing derating, and/or monitorthe operating temperature (see Temperature Sensor). When using the temperature sensor,the actual device case temperature may be higher than the T_{OPER} rating that appliesfor the standard or elevated temperature range. For example, T_{CASE} could be above+85˚C when the temperature sensor indicates a temperature of less than +85˚C.
4. Refer to operating temperature range on top page.

4.46 AC and DC Input Measurement Levels

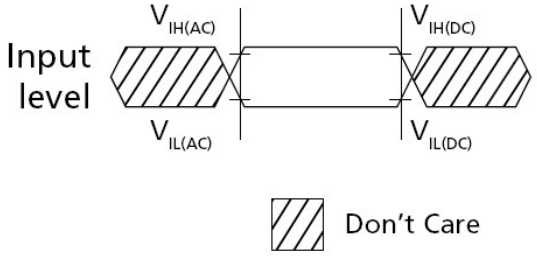
Input Levels for CKE

Table 4-145: Input Levels

Parameter	Symbol	Min	Max	Unit	Notes
Input HIGH level (AC)	$V_{IH(AC)}$	0.75 × V_{DD2}	V_{DD2} + 0.2	V	1
Input LOW level (AC)	$V_{IL(AC)}$	–0.2	0.25 × V_{DD2}	V	1
Input HIGH level (DC)	$V_{IH(DC)}$	0.65 × V_{DD2}	V_{DD2} + 0.2	V	
Input LOW level (DC)	$V_{IL(DC)}$	–0.2	0.35 × V_{DD2}	V	

Note:
1. See the AC Overshoot and Undershoot section.

Figure 4-131: Input Timing Definition for CKE



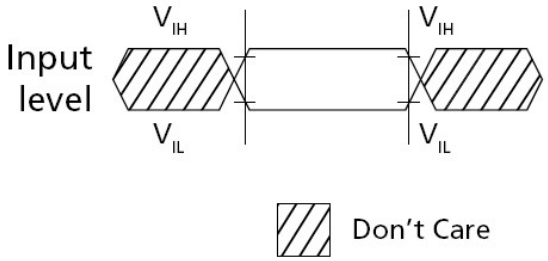
Input Levels for RESET_n

Table 4-146: Input Levels

Parameter	Symbol	Min	Max	Unit	Notes
Input HIGH level	V_{IH}	0.80 × V_{DD2}	V_{DD2} + 0.2	V	1
Input LOW level	V_{IL}	–0.2	0.20 × V_{DD2}	V	1

Note:
1. See the AC Overshoot and Undershoot section.

Figure 4-132: Input Timing Definition for RESET_n



Differential Input Voltage for CK

The minimum input voltage needs to satisfy both V_{indiff_CK} and $V_{indiff\_CK/2}$ specificationat input receiver and their measurement period is 1^{t}CK. V_{indiff_CK} is the peak-to-peakvoltage centered on 0 volts differential and V_{indiff_CK}/2 is maximum and minimum peakvoltage from 0 volts.

Figure 4-133: CK Differential Input Voltage

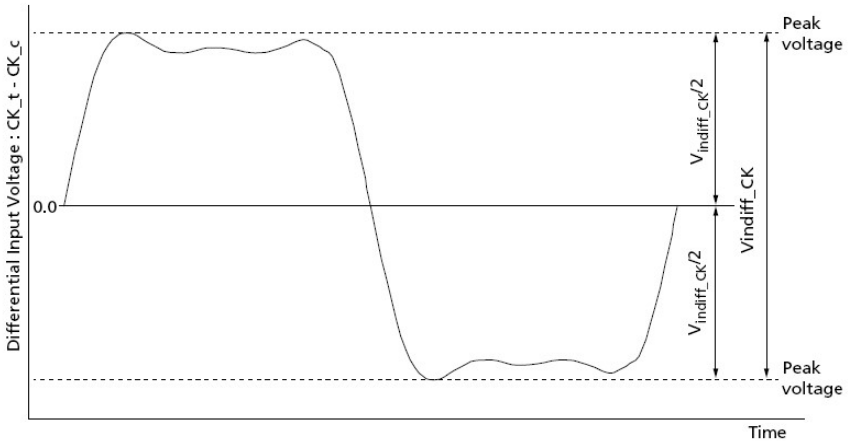


Table4-147: CK Differential Input Voltage

Parameter	Symbol	1600/1867		2133/2400/3200		Unit	Note
		Min	Max	Min	Max		
CK differential input voltage	V_{indiff_CK}	420	–	380	–	mV	1

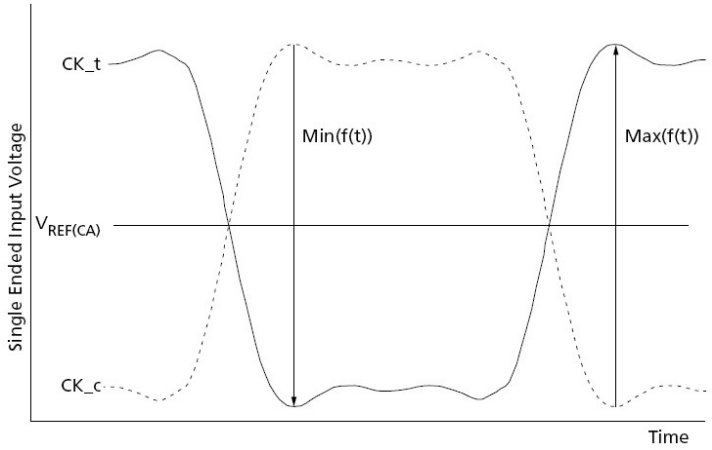
Note:
1. The peak voltage of differential CK signals is calculated in a following equation.
- V_{indiff_CK} = (Maximum peak voltage) - (Minimum peak voltage)
- Maximum peak voltage = MAX(f(t))
- Minimum peak voltage = MIN(f(t))
- f(t) = V_{CK_t} - V_{CK_c}

Peak Voltage Calculation Method

The peak voltage of differential clock signals are calculated in a following equation.

- $V_{IH.DIFF.peak}$ voltage = MAX(f(t))
- $V_{IL.DIFF.peak}$ voltage = MIN(f(t))
- f(t) = V_{CK_t} - V_{CK_c}

Figure 4-134: Definition of Differential Clock Peak Voltage



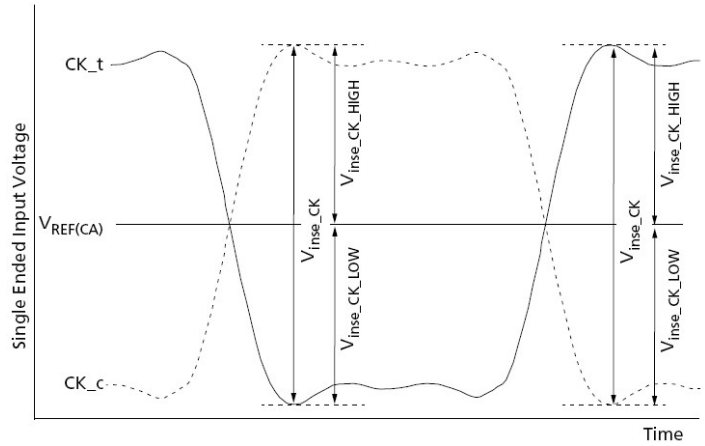
Note:

1. $V_{REF(CA)}$ is device internal setting value by V_{REF} training.

Single-Ended Input Voltage for Clock

The minimum input voltage need to satisfy V_{inse_CK}, $V_{inse\_CK\_HIGH}$, and $V_{inse_CK_LOW}$specification at input receiver.

Figure 4-135: Clock Single-Ended Input Voltage



Note:

1. $V_{REF(CA)}$ is device internal setting value by V_{REF} training.

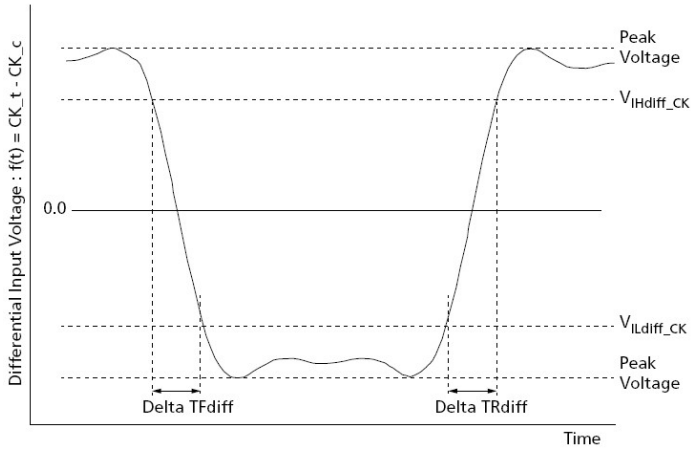
Table 4-148: Clock Single-Ended Input Voltage

Parameter	Symbol	1600/1867		2133/2400/3200		Unit
		Min	Max	Min	Max	
Clock single-ended input voltage	V_{inse_CK}	210	–	190	–	mV
Clock single-ended input voltage HIGH from $V_{REF(CA)}$	$V_{inse\_CK\_HIGH}$	105	–	95	–	mV
Clock single-ended input voltage LOW from $V_{REF(CA)}$	$V_{inse\_CK\_LOW}$	105	–	95	–	mV

Differential Input Slew Rate Definition for Clock

Input slew rate for differential signals (CK_t, CK_c) are defined and measured as shownbelow in figure and the tables.

Figure 4-136: Differential Input Slew Rate Definition for CK_t, CK_c



Notes:

1. Differential signal rising edge from V_{ILdiff_CK} to V_{IHdiff_CK} must be monotonic slope.
2. Differential signal falling edge from V_{IHdiff_CK} to V_{ILdiff_CK} must be monotonic slope.

Table 4-149: Differential Input Slew Rate Definition for CK_t, CK_c

Description	From	To	Defined by
Differential input slew rate for rising edge (CK_t - CK_c)	V_{ILdiff_CK}	V_{IHdiff_CK}	$\lvert V_{ILdiff\_CK} - V_{IHdiff\_CK}\rvert/\Delta TRdiff$
Differential input slew rate for falling edge (CK_t - CK_c)	V_{IHdiff_CK}	V_{ILdiff_CK}	$\lvert V_{ILdiff\_CK} - V_{IHdiff\_CK}\rvert/\Delta TFdiff$

Table 4-150: Differential Input Level for CK_t, CK_c

Parameter	Symbol	1600/1867		2133/2400/3200		Unit
		Min	Max	Min	Max	
Differential Input HIGH	V_{IHdiff_CK}	175	–	155	–	mV
Differential Input LOW	V_{ILdiff_CK}	–	–175	–	–155	mV

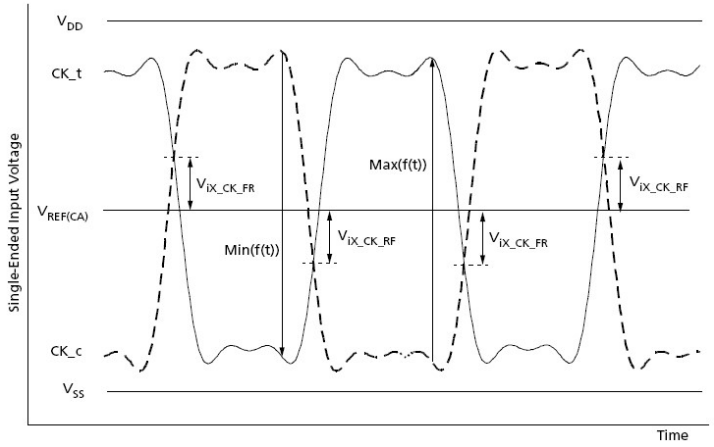
Table 4-151: Differential Input Slew Rate for CK_t, CK_c

Parameter	Symbol	1600/1867		2133/2400/3200		Unit
		Min	Max	Min	Max	
Differential input slew rate for clock	SRIdiff_CK	2	14	2	14	V/ns

Differential Input Cross-Point Voltage

The cross-point voltage of differential input signals (CK_t, CK_c) must meet the requirementsin table below. The differential input cross-point voltage VIX is measured fromthe actual cross-point of true and complement signals to the mid level that is $V_{REF(CA)}$.

Figure 4-137: V_{ix} Definition (Clock)



Note:

1.The base levels of $V_{ix\_CK\_FR}$ and $V_{ix\_CK\_RF}$ are $V_{REF(CA)}$ that is device internal setting valueby V_{REF} training.

Table 4-152: Cross-Point Voltage for Differential Input Signals (Clock)

Parameter	Symbol	1600/1867		2133/2400/3200		Unit
		Min	Max	Min	Max	
Clock single-ended cross-point voltage ratio	$V_{ix\_CK\_ratio}$	–	25	–	25	%

Notes:

1. $V_{ix\_CK\_ratio}$ is defined by this equation: $V_{ix\_CK\_ratio} = V_{ix\_CK\_FR}/|MIN(f(t))|$
2. $V_{ix\_CK\_ratio}$ is defined by this equation: $V_{ix\_CK\_ratio} = V_{ix\_CK\_RF}/MAX(f(t))$

Differential Input Voltage for DQS

The minimum input voltage needs to satisfy both V_{indiff_DQS} and $V_{indiff\_DQS}/2$ specificationat input receiver and their measurement period is 1UI (^{t}CK/2). V_{indiff_DQS} is thepeak to peak voltage centered on 0 volts differential and $V_{indiff\_DQS}/2$ is maximum andminimum peak voltage from 0 volts.

Figure 4-138: DQS Differential Input Voltage

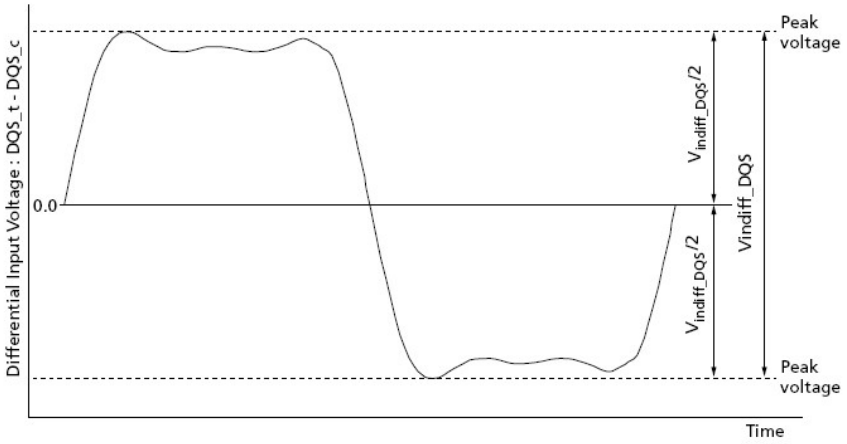


Table 4-153: DQS Differential Input Voltage

Parameter	Symbol	1600/1867		2133/2400/3200		Unit	Note
		Min	Max	Min	Max		
DQS differential input voltage	V_{indiff_DQS}	360	–	360	–	mV	1

Note:

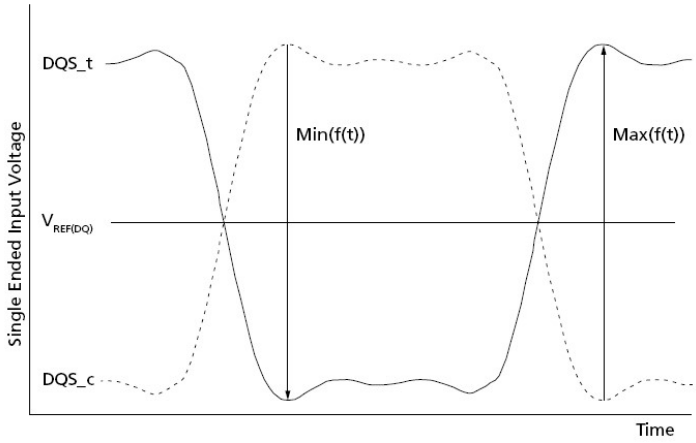
1. The peak voltage of differential DQS signals is calculated in a following equation.
   - V_{indiff_DQS} = (Maximum peak voltage) - (Minimum peak voltage)
   - Maximum peak voltage = MAX(f(t))
   - Minimum peak voltage = MIN(f(t))
   - f(t) = V_{DQS_t} - V_{DQS_c}

Peak Voltage Calculation Method

The peak voltage of differential DQS signals are calculated in a following equation.

- $V_{IH.DIFF.peak}$ voltage = MAX(f(t))
- $V_{IL.DIFF.peak}$ voltage = MIN(f(t))
- f(t) = V_{DQS_t} - V_{DQS_c}

Figure 4-139: Definition of Differential DQS Peak Voltage



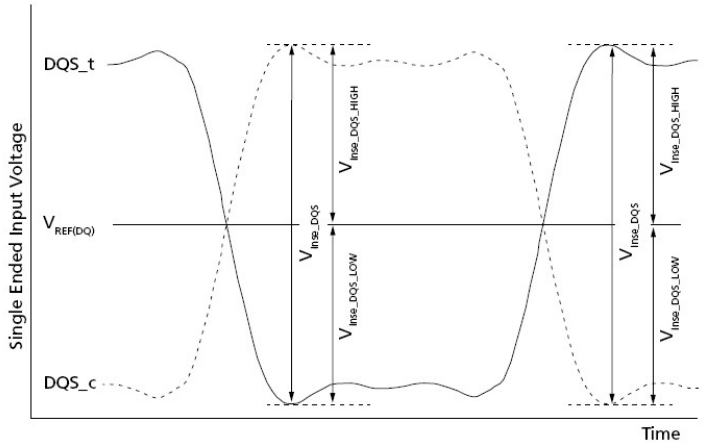
Note:

1. $V_{REF(DQ)}$ is device internal setting value by V_{REF} training.

Single-Ended Input Voltage for DQS

The minimum input voltage need to satisfy V_{inse_DQS}, $V_{inse\_DQS\_HIGH}$, and $V_{inse_DQS_LOW}$specification at input receiver.

Figure 4-140: DQS Single-Ended Input Voltage



Note:

1. $V_{REF(DQ)}$ is device internal setting value by V_{REF} training.

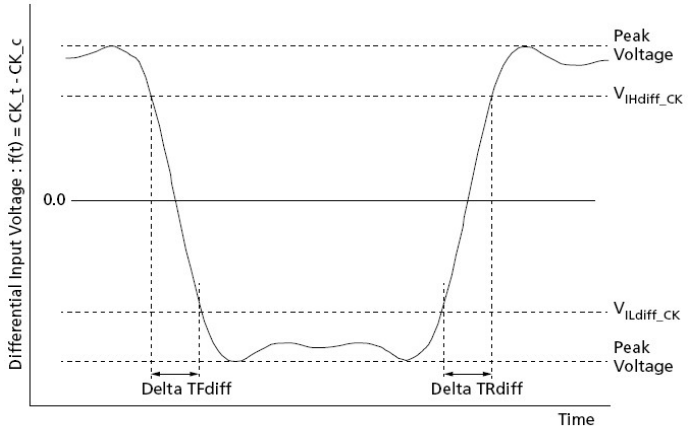
Table 4-154: DQS Single-Ended Input Voltage

Parameter	Symbol	1600/1867		2133/2400/3200		Unit
		Min	Max	Min	Max	
DQS single-ended input voltage	V_{inse_DQS}	180	–	180	–	mV
DQS single-ended input voltage HIGH from $V_{REF(DQ)}$	$V_{inse\_DQS\_HIGH}$	90	–	90	–	mV
DQS single-ended input voltage LOW from $V_{REF(DQ)}$	$V_{inse\_DQS\_LOW}$	90	–	90	–	mV

Differential Input Slew Rate Definition for DQS

Input slew rate for differential signals (DQS_t, DQS_c) are defined and measured asshown below in figure and the tables.

Figure 4-141: Differential Input Slew Rate Definition for DQS_t, DQS_c



Notes:

1. Differential signal rising edge from V_{ILdiff_DQS} to V_{IHdiff_DQS} must be monotonic slope.
2. Differential signal falling edge from V_{IHdiff_DQS} to V_{ILdiff_DQS} must be monotonic slope.

Table 4-155: Differential Input Slew Rate Definition for DQS_t, DQS_c

Description	From	To	Defined by
Differential input slew rate for rising edge (DQS_t - DQS_c)	V_{ILdiff_DQS}	V_{IHdiff_DQS}	$\lvert V_{ILdiff\_DQS} - V_{IHdiff\_DQS}\rvert/\Delta TRdiff$
Differential input slew rate for falling edge (DQS_t - DQS_c)	V_{IHdiff_DQS}	V_{ILdiff_DQS}	$\lvert V_{ILdiff\_DQS} - V_{IHdiff\_DQS}\rvert/\Delta TFdiff$

Table 4-156: Differential Input Level for DQS_t, DQS_c

Parameter	Symbol	1600/1867		2133/2400/3200		Unit
		Min	Max	Min	Max	
Differential Input HIGH	V_{IHdiff_DQS}	140	–	140	–	mV
Differential Input LOW	V_{ILdiff_DQS}	–	–140	–	–140	mV

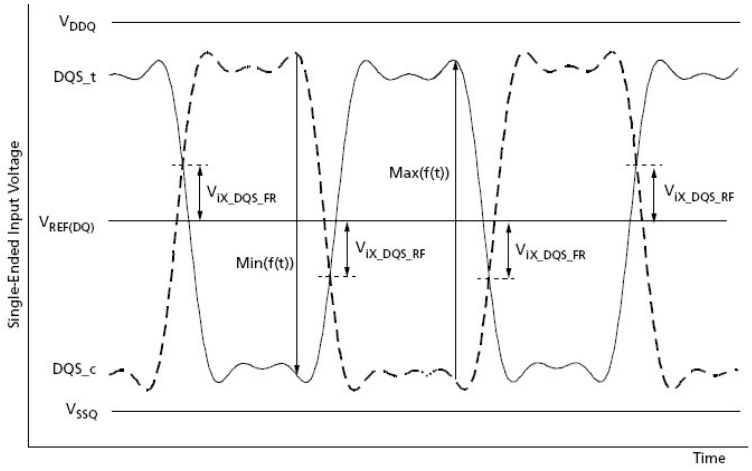
Table 4-157: Differential Input Slew Rate for DQS_t, DQS_c

Parameter	Symbol	1600/1867		2133/2400/3200		Unit
		Min	Max	Min	Max	
Differential input slew rate	SRIdiff	2	14	2	14	V/ns

Differential Input Cross-Point Voltage

The cross-point voltage of differential input signals (DQS_t, DQS_c) must meet the requirementsin table below. The differential input cross-point voltage V_{IX} is measuredfrom the actual cross-point of true and complement signals to the mid level that is$V_{REF(DQ)}$.

Figure 4-142: Vix Definition (DQS)



Note:

1. The base levels of $V_{ix\_DQS\_FR}$ and $V_{ix\_DQS\_RF}$ are $V_{REF(DQ)}$ that is device internal setting valueby V_{REF} training.

Table 4-158: Cross-Point Voltage for Differential Input Signals (DQS)

Notes 1 and 2 apply to entire table

Parameter	Symbol	1600/1867		2133/2400/3200		Unit
		Min	Max	Min	Max	
Clock single-ended cross-point voltage ratio	$V_{ix\_DQS\_ratio}$	–	20	–	20	%

Notes:

1. $V_{ix\_DQS\_ratio}$ is defined by this equation: $V_{ix\_DQS\_ratio} = V_{ix\_DQS\_FR}/\lvert MIN(f(t))\rvert$
2. $V_{ix\_DQS\_ratio}$ is defined by this equation: $V_{ix\_DQS\_ratio} = V_{ix\_DQS\_RF}/MAX(f(t))$

Input Levels for ODT_CA

Table 4-159: Input Levels for ODT_CA

Parameter	Symbol	Min	Max	Unit
ODT input HIGH level	V_{IHODT}	0.75 × V_{DD2}	V_{DD2} + 0.2	V
ODT input LOW level	V_{ILODT}	–0.2	0.25 × V_{DD2}	V

Note:

1. See the Overshoot and Undershoot section.

4.47 Output Slew Rate and Overshoot/Undershoot specifications

Single-Ended Output Slew Rate

Table 4-160: Single-Ended Output Slew Rate

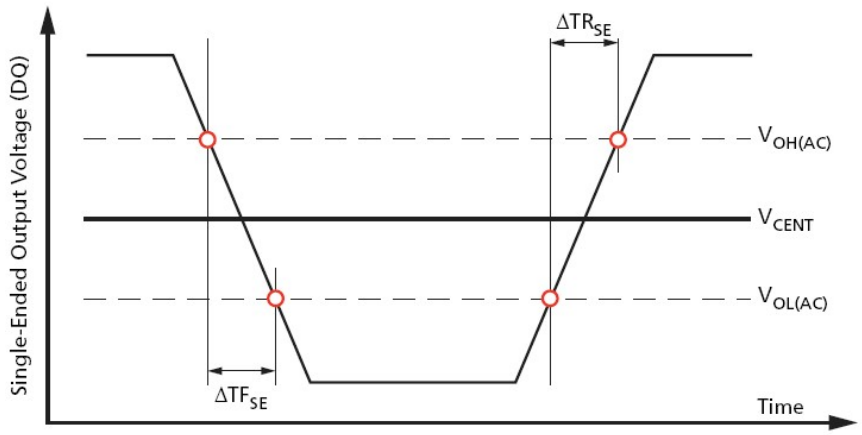
Notes 1-5 applies to entire table

Parameter	Symbol	Value		Units
		Min	Max	
Single-ended output slew rate (V_{OH} = V_{DDQ}x 0.5)	SRQse	3.0	9.0	V/ns
Output slew rate matching ratio (rise to fall)	–	0.8	1.2	–

Notes:

1. SR = Slew rate; Q = Query output; se = Single-ended signal
2. Measured with output reference load.
3. The ratio of pull-up to pull-down slew rate is specified for the same temperature andvoltage, over the entire temperature andvoltage range. For a given output, it representsthe maximum difference between pull-up and pull-down drivers due toprocessvariation.
4. The output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ = 0.2 × $V_{OH(DC)}$ and $V_{OH(AC)}$ = 0.8 × $V_{OH(DC)}$.
5. Slew rates are measured under average SSO conditions with 50% of the DQ signals perdata byte switching.

Figure 4-143: Single-Ended Output Slew Rate Definition



Differential Output Slew Rate

Table 4-161: Differential Output Slew Rate

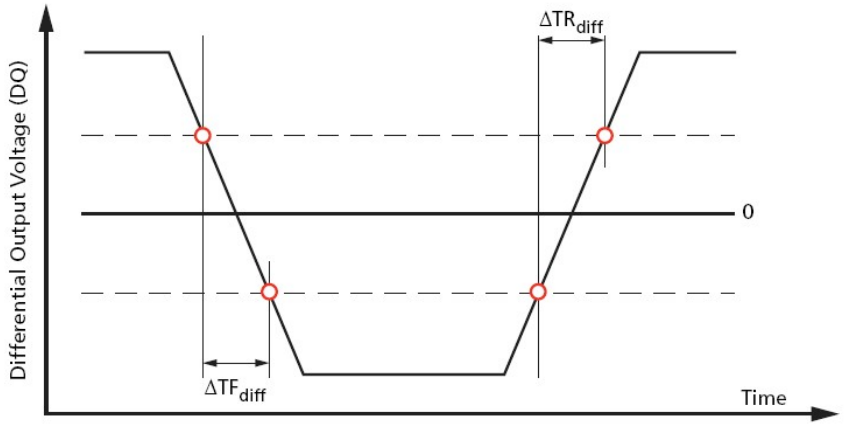
Notes 1-4 applies to entire table

Parameter	Symbol	Value		
		Min	Max	Units
Differential output slew rate (V_{OH} = V_{DDQ} x 0.5)	SRQdiff	6	18	V/ns

Notes:

1. SR = Slew rate; Q = Query output; se = Differential signal
2. Measured with output reference load.
3. The output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ = 0.2 × $V_{OH(DC)}$ and $V_{OH(AC)}$ = 0.8 × $V_{OH(DC)}$.
4. Slew rates are measured under average SSO conditions with 50% of the DQ signals perdata byte switching.

Figure 4-144: Differential Output Slew Rate Definition



Overshoot and Undershoot Specifications

Table 4-162: AC Overshoot/Undershoot Specifications

Parameter		1600	1866	3200	Unit
Maximum peak amplitude provided for overshootarea	MAX	0.3	0.3	0.3	V
Maximum peak amplitude provided for undershootarea	MAX	0.3	0.3	0.3	V
Maximum area above V_{DD}/ V_{DDQ}	MAX	0.1	0.1	0.1	V-ns
Maximum area below V_{SS}/ V_{SSQ}	MAX	0.1	0.1	0.1	V-ns

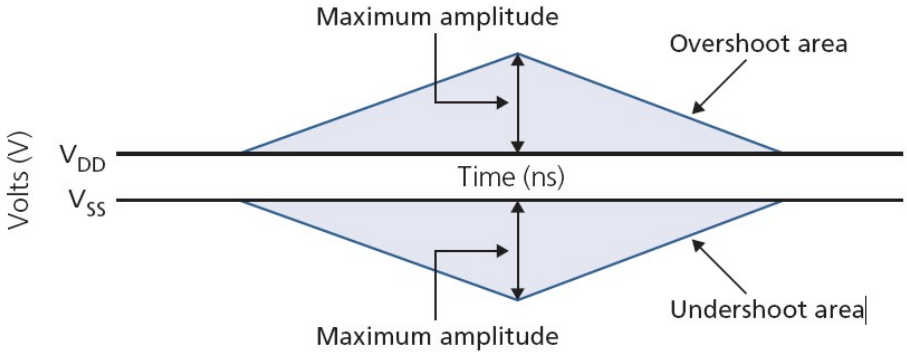
Notes:

1. V_{DD} stands for V_{DD2} for CA[5:0], CK_t, CS_n, CKE, and ODT. V_{DD} stands for V_{DDQ} for DQ,DMI, DQS_t, and DQS_c.
2. V_{SS} stands for V_{SS} for CA[5:0], CK_t, CK_c, CS_n, CKE, and ODT. V_{SS} stands for V_{SSQ} forDQ, DMI, DQS_t, and DQS_c.
3. Maximum peak amplitude values are referenced from actual V_{DD} and V_{SS} values.
4. Maximum area values are referenced from maximum V_{DD} and V_{SS} values.

Table 4-163: Overshoot/Undershoot Specification for CKE and RESET

Parameter	Specification
Maximum peak amplitude provided for overshoot area	0.35V
Maximum peak amplitude provided for undershoot area	0.35V
Maximum area above V_{DD}	0.8 V-ns
Maximum area below V_{SS}	0.8 V-ns

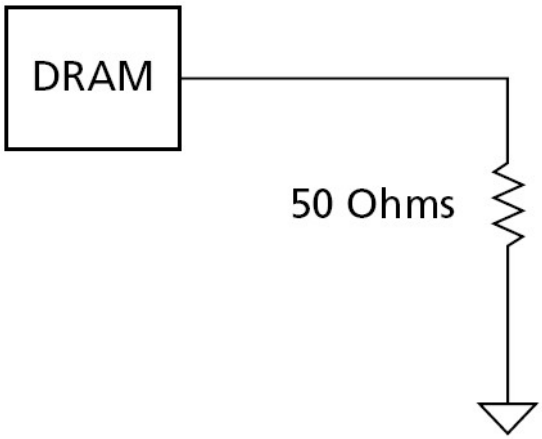
Figure 4-145: Overshoot and Undershoot Definition



4.48 Driver Output Timing Reference Load

Timing reference loads are not intended as a precise representation of any particularsystem environment or depiction of an actual load presented by a production tester.System designers should use IBIS or other simulation tools to correlate the timing referenceload to a system environment. Manufacturers correlate to their production testconditions, generally one or more coaxial transmission lines terminated at the testerelectronics.

Figure 4-146: Driver Output Timing Reference Load



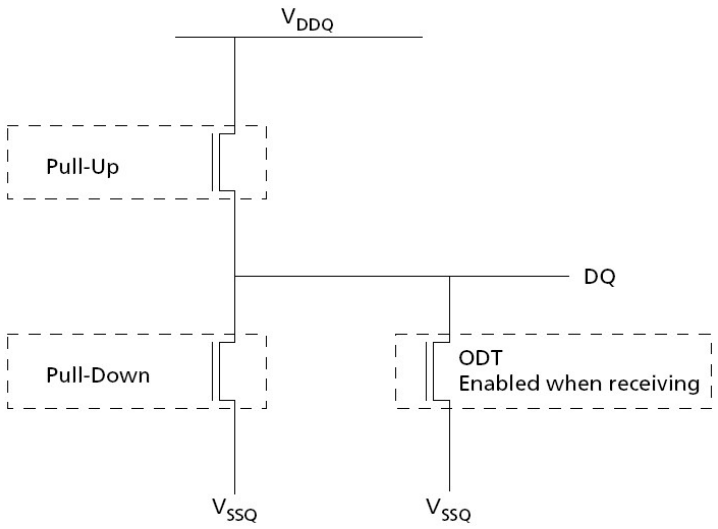
Note:

1. All output timing parameter values are reported with respect to this reference load; thisreference load is also used to report slew rate.

4.49 LVSTL I/O System

LVSTL I/O cells are comprised of a driver pull-up and pull-down and a terminator.

Figure 4-147: LVSTL I/O Cell

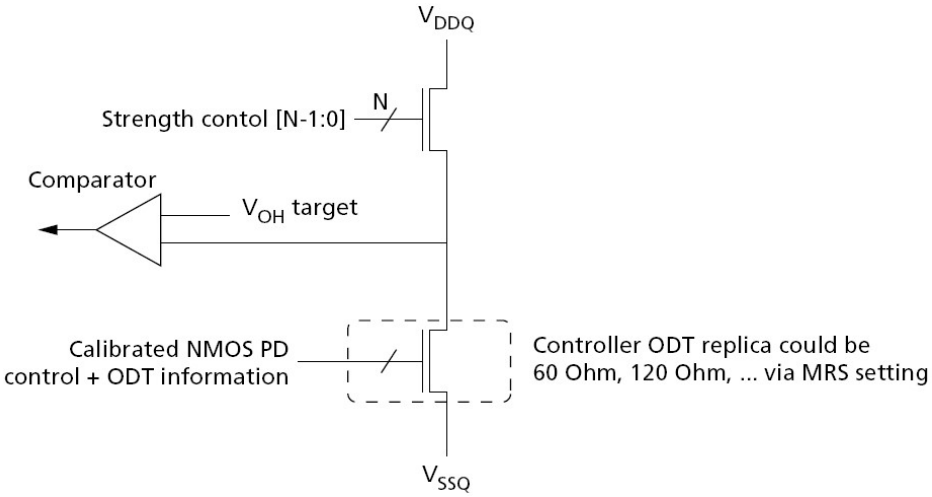


To ensure that the target impedance is achieved, calibrate the LVSTL I/O cell as followingexample:

1. Calibrate the pull-down device against a 240 ohm resistor to V_{DDQ} via the ZQ pin.
• Set strength control to minimum setting
• Increase drive strength until comparator detects data bit is less than $V_{DDQ}/2$
• NMOS pull-down device is calibrated to 240 ohms

2. Calibrate the pull-up device against the calibrated pull-down device.
• Set V_{OH} target and NMOS controller ODT replica via MRS (V_{OH} can be automaticallycontrolled by ODT MRS)
• Set strength control to minimum setting
• Increase drive strength until comparator detects data bit is greater than V_{OH} target
• NMOS pull-up device is calibrated to V_{OH} target

Figure 4-148: Pull-Up Calibration



4.50 Input/Output Capacitance

Table 4-164 Input/Output Capacitance

Notes 1 and 2 apply to entire table

Parameter	Symbol	Min	Max	Unit	Notes
Input capacitance, CK_t and CK_c	C_{CK}	0.5	0.9	pF	
Input capacitance delta, CK_t and CK_c	C_{DCK}	0	0.09		3
Input capacitance, all other input-only pins	C_I	0.5	0.9		4
Input capacitance delta, all other input-only pins	C_{DI}	-0.1	0.1		5
Input/output capacitance, DQ, DMI, DQS_t, DQS_c	C_{IO}	0.7	1.3		6
Input/output capacitance delta, DQS_t, DQS_c	C_{DDQS}	0	0.1		7
Input/output capacitance delta, DQ, DMI	C_{DIO}	-0.1	0.1		8
Input/output capacitance, ZQ pin	C_{ZQ}	0	5.0		

Notes:

1. This parameter applies to LPDDR4 die only (does not include package capacitance).
2. This parameter is not subject to production testing; it is verified by design and characterization.The capacitance is measuredaccording to JEP147 (procedure for measuring inputcapacitance using a vector network analyzer), with V_{DD1}, V_{DD2},V_{DDQ}, and V_{SS} applied;all other pins are left floating.
3. Absolute value of $C_{CK\_t} – CC_{K\_c}$.
4. C_I applies to CS, CKE, and CA[5:0].
5. $C_{DI} = C_I – 0.5 × (C_{CK\_t} + {}_{CCK\_c})$; it does not apply to CKE.
6. DMI loading matches DQ and DQS.
7. Absolute value of C_{DQS}_t and C_{DQS_c}.
8. $C_{DIO} = C_{IO} – 0.5 × (C_{DQS\_t}$ + CDQS_c) in byte-lane.

4.51 I_{DD} Specification Parameters and Test Conditions

Table 4-165: I_{DD} Measurement Conditions

Switching for CA								
CK_t edge	**R1**	**R2**	**R3**	**R4**	**R5**	**R6**	**R7**	**R8**
CKE	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
CS	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
CA0	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA1	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA2	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA3	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA4	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA5	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH

Notes:

1. LOW = $V_{IN} \le V_{IL(DC)}$ MAX
   HIGH = $V_{IN} \ge V_{IH(DC)}$ MIN
   STABLE = Inputs are stable at a HIGH or LOW level
2. CS must always be driven LOW.
3. 50% of CA bus is changing between HIGH and LOW once per clock for the CA bus.
4. The pattern is used continuously during IDD measurement for IDD values that requireswitching on the CA bus.

Table 4-166: CA Pattern for L_{DDR4R} for BL = 16

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	HIGH	HIGH	Read-1	L	H	L	L	L	L
N+1	HIGH	LOW		L	H	L	L	L	L
N+2	HIGH	HIGH	CAS-2	L	H	L	L	H	L
N+3	HIGH	LOW		L	L	L	L	L	L
N+4	HIGH	LOW	DES	L	L	L	L	L	L
N+5	HIGH	LOW	DES	L	L	L	L	L	L
N+6	HIGH	LOW	DES	L	L	L	L	L	L
N+7	HIGH	LOW	DES	L	L	L	L	L	L
N+8	HIGH	HIGH	Read-1	L	H	L	L	L	L
N+9	HIGH	LOW		L	H	L	L	H	L
N+10	HIGH	HIGH	CAS-2	L	H	L	L	H	H
N+11	HIGH	LOW		H	H	H	H	H	H
N+12	HIGH	LOW	DES	L	L	L	L	L	L
N+13	HIGH	LOW	DES	L	L	L	L	L	L
N+14	HIGH	LOW	DES	L	L	L	L	L	L
N+15	HIGH	LOW	DES	L	L	L	L	L	L

Notes:
1. BA[2:0] = 010; CA[9:4] = 000000 OR 111111; Burst order CA[3:2] = 00 or 11 (same asLPDDR3 I_{DD4R} specification).
2. CA pins are kept LOW with DES command to reduce ODT current (different from LPDDR3I_{DD4R} specification).

Table 4-167: CA Pattern for $I_{DD4W}$for BL = 16

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	HIGH	HIGH	Write-1	L	L	H	L	L	L
N+1	HIGH	LOW		L	H	L	L	L	L
N+2	HIGH	HIGH	CAS-2	L	H	L	L	H	L
N+3	HIGH	LOW		L	L	L	L	L	L
N+4	HIGH	LOW	DES	L	L	L	L	L	L
N+5	HIGH	LOW	DES	L	L	L	L	L	L
N+6	HIGH	LOW	DES	L	L	L	L	L	L
N+7	HIGH	LOW	DES	L	L	L	L	L	L
N+8	HIGH	HIGH	Write-1	L	L	H	L	L	L
N+9	HIGH	LOW		L	H	L	L	H	L
N+10	HIGH	HIGH	CAS-2	L	H	L	L	H	H
N+11	HIGH	LOW		L	L	H	H	H	H
N+12	HIGH	LOW	DES	L	L	L	L	L	L
N+13	HIGH	LOW	DES	L	L	L	L	L	L
N+14	HIGH	LOW	DES	L	L	L	L	L	L
N+15	HIGH	LOW	DES	L	L	L	L	L	L

Notes:
1. BA[2:0] = 010; CA[9:4] = 000000 or 111111 (same as LPDDR3 I_{DD4W}specification).
2. No burst ordering (different from LPDDR3I_{DD4W}specification).
3. CA pins are kept LOW with DES CMD to reduce ODT current (different from LPDDR3I_{DD4W}specification).

Table 4-168: Data Pattern for I_{DD4W} (DBI Off)for BL = 16

DBI Off Case										
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	# of 1s
BL0	1	1	1	1	1	1	1	1	0	8
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	1	1	1	1	1	1	0	0	0	6
BL7	1	1	1	1	0	0	0	0	0	4
BL8	1	1	1	1	1	1	1	1	0	8
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	1	1	1	1	1	1	0	0	0	6
BL15	1	1	1	1	0	0	0	0	0	4
BL16	1	1	1	1	1	1	0	0	0	6
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	1	1	1	1	1	1	1	1	0	8
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	1	1	1	1	1	1	0	0	0	6
BL27	1	1	1	1	0	0	0	0	0	4
BL28	1	1	1	1	1	1	1	1	0	8
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
# of 1s	16	16	16	16	16	16	16	16		

Note:

1. Simplified pattern; same data pattern was applied to DQ[4], DQ[5], DQ[6], and DQ[7] toreduce complexity for I_{DD4W} pattern programming.

Table 4-169: Data Pattern for I_{DD4R} (DBI Off)for BL = 16

DBI Off Case										
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	# of 1s
BL0	1	1	1	1	1	1	1	1	0	8
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	1	1	1	1	1	1	0	0	0	6
BL7	1	1	1	1	0	0	0	0	0	4
BL8	1	1	1	1	1	1	1	1	0	8
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	1	1	1	1	1	1	0	0	0	6
BL15	1	1	1	1	0	0	0	0	0	4
BL16	1	1	1	1	1	1	1	1	0	8
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	0	0	0	0
BL19	0	0	0	0	1	1	1	1	0	4
BL20	1	1	1	1	1	1	0	0	0	6
BL21	1	1	1	1	0	0	0	0	0	4
BL22	0	0	0	0	0	0	1	1	0	2
BL23	0	0	0	0	1	1	1	1	0	4
BL24	0	0	0	0	0	0	0	0	0	0
BL25	0	0	0	0	1	1	1	1	0	4
BL26	1	1	1	1	1	1	1	1	0	8
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	1	1	0	2
BL29	0	0	0	0	1	1	1	1	0	4
BL30	1	1	1	1	1	1	0	0	0	6
BL31	1	1	1	1	0	0	0	0	0	4
# of 1s	16	16	16	16	16	16	16	16		

Note:

1. Simplified pattern; same data pattern was applied to DQ[4], DQ[5], DQ[6], and DQ[7] toreduce complexity for I_{DD4R} pattern programming.

Table 4-170: Data Pattern for I_{DD4W} (DBI On)for BL = 16

DBI On Case										
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	# of 1s
BL0	0	0	0	0	0	0	0	0	1	1
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	0	0	0	0	0	0	1	1	1	3
BL7	1	1	1	1	0	0	0	0	0	4
BL8	0	0	0	0	0	0	0	0	1	1
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	0	0	0	0	0	0	1	1	1	3
BL15	1	1	1	1	0	0	0	0	0	4
BL16	0	0	0	0	0	0	1	1	1	3
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	0	0	0	0	0	0	0	0	1	1
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	0	0	0	0	0	0	1	1	1	3
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	0	0	1	1
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
# of 1s	8	8	8	8	8	8	16	16	8	

Note:

1. DBI enabled burst: BL0, BL6, BL8, BL14, BL16, BL22, BL26, and BL28.

Table 4-171: Data Pattern for I_{DD4R} (DBI On)for BL = 16

DBI On Case										
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	# of 1s
BL0	0	0	0	0	0	0	0	0	1	1
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	0	0	0	0	0	0	1	1	1	3
BL7	1	1	1	1	0	0	0	0	0	4
BL8	0	0	0	0	0	0	0	0	1	1
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	0	0	0	0	0	0	1	1	1	3
BL15	1	1	1	1	0	0	0	0	0	4
BL16	0	0	0	0	0	0	0	0	1	1
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	0	0	0	0
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	1	1	1	3
BL21	1	1	1	1	0	0	0	0	0	4
BL22	0	0	0	0	0	0	1	1	0	2
BL23	0	0	0	0	1	1	1	1	0	4
BL24	0	0	0	0	0	0	0	0	0	0
BL25	0	0	0	0	1	1	1	1	0	4
BL26	0	0	0	0	0	0	0	0	1	1
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	1	1	0	2
BL29	0	0	0	0	1	1	1	1	0	4
BL30	0	0	0	0	0	0	1	1	1	3
BL31	1	1	1	1	0	0	0	0	0	4
# of 1s	8	8	8	8	8	8	16	16	8	

Note:

1. DBI enabled burst: BL0, BL6, BL8, BL14, BL20, BL26, and BL30.

Table 4-172: CA Pattern for L_{DDR4R} for BL = 32

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	HIGH	HIGH	Read-1	L	H	L	L	L	L
N+1	HIGH	LOW		L	H	L	L	L	L
N+2	HIGH	HIGH	CAS-2	L	H	L	L	H	L
N+3	HIGH	LOW		L	L	L	L	L	L
N+4	HIGH	LOW	DES	L	L	L	L	L	L
N+5	HIGH	LOW	DES	L	L	L	L	L	L
N+6	HIGH	LOW	DES	L	L	L	L	L	L
N+7	HIGH	LOW	DES	L	L	L	L	L	L
N+8	HIGH	LOW	DES	L	L	L	L	L	L
N+9	HIGH	LOW	DES	L	L	L	L	L	L
N+10	HIGH	LOW	DES	L	L	L	L	L	L
N+11	HIGH	LOW	DES	L	L	L	L	L	L
N+12	HIGH	LOW	DES	L	L	L	L	L	L
N+13	HIGH	LOW	DES	L	L	L	L	L	L
N+14	HIGH	LOW	DES	L	L	L	L	L	L
N+15	HIGH	LOW	DES	L	L	L	L	L	L
N+16	HIGH	HIGH	READ-1	L	H	L	L	L	L
N+17	HIGH	LOW		L	H	L	L	H	L
N+18	HIGH	HIGH	CAS-2	L	H	L	L	H	H
N+19	HIGH	LOW		H	H	L	H	H	H
N+20	HIGH	LOW	DES	L	L	L	L	L	L
N+21	HIGH	LOW	DES	L	L	L	L	L	L
N+22	HIGH	LOW	DES	L	L	L	L	L	L
N+23	HIGH	LOW	DES	L	L	L	L	L	L
N+24	HIGH	LOW	DES	L	L	L	L	L	L
N+25	HIGH	LOW	DES	L	L	L	L	L	L
N+26	HIGH	LOW	DES	L	L	L	L	L	L
N+27	HIGH	LOW	DES	L	L	L	L	L	L
N+28	HIGH	LOW	DES	L	L	L	L	L	L
N+29	HIGH	LOW	DES	L	L	L	L	L	L
N+30	HIGH	LOW	DES	L	L	L	L	L	L
N+31	HIGH	LOW	DES	L	L	L	L	L	L

Notes:

1. BA[2:0] = 010, C[9:5] = 00000 or 11111, Burst order C[4:2] = 000 or 111.

Table 4-173: CA Pattern for I_{DD4W}BL = 32

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	HIGH	HIGH	WRITE-1	L	L	H	L	L	L
N+1	HIGH	LOW		L	H	L	L	L	L
N+2	HIGH	HIGH	CAS-2	L	H	L	L	H	L
N+3	HIGH	LOW		L	L	L	L	L	L
N+4	HIGH	LOW	DES	L	L	L	L	L	L
N+5	HIGH	LOW	DES	L	L	L	L	L	L
N+6	HIGH	LOW	DES	L	L	L	L	L	L
N+7	HIGH	LOW	DES	L	L	L	L	L	L
N+8	HIGH	LOW	DES	L	L	L	L	L	L
N+9	HIGH	LOW	DES	L	L	L	L	L	L
N+10	HIGH	LOW	DES	L	L	L	L	L	L
N+11	HIGH	LOW	DES	L	L	L	L	L	L
N+12	HIGH	LOW	DES	L	L	L	L	L	L
N+13	HIGH	LOW	DES	L	L	L	L	L	L
N+14	HIGH	LOW	DES	L	L	L	L	L	L
N+15	HIGH	LOW	DES	L	L	L	L	L	L
N+16	HIGH	HIGH	WRITE-1	L	L	H	L	L	L
N+17	HIGH	LOW		L	H	L	L	H	L
N+18	HIGH	HIGH	CAS-2	L	H	L	L	H	H
N+19	HIGH	LOW		L	L	L	H	H	H
N+20	HIGH	LOW	DES	L	L	L	L	L	L
N+21	HIGH	LOW	DES	L	L	L	L	L	L
N+22	HIGH	LOW	DES	L	L	L	L	L	L
N+23	HIGH	LOW	DES	L	L	L	L	L	L
N+24	HIGH	LOW	DES	L	L	L	L	L	L
N+25	HIGH	LOW	DES	L	L	L	L	L	L
N+26	HIGH	LOW	DES	L	L	L	L	L	L
N+27	HIGH	LOW	DES	L	L	L	L	L	L
N+28	HIGH	LOW	DES	L	L	L	L	L	L
N+29	HIGH	LOW	DES	L	L	L	L	L	L
N+30	HIGH	LOW	DES	L	L	L	L	L	L
N+31	HIGH	LOW	DES	L	L	L	L	L	L

Notes:
1. BA[2:0] = 010, C[9:5] = 00000 or 11111.

Table 4-174: Data Pattern for I_{DD4W} (DBI Off) BL = 32

DBI Off Case										
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	# of 1s
BL0	1	1	1	1	1	1	1	1	0	8
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	1	1	1	1	1	1	0	0	0	6
BL7	1	1	1	1	0	0	0	0	0	4
BL8	1	1	1	1	1	1	1	1	0	8
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	1	1	1	1	1	1	0	0	0	6
BL15	1	1	1	1	0	0	0	0	0	4
BL16	1	1	1	1	1	1	0	0	0	6
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	1	1	1	1	1	1	1	1	0	8
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	1	1	1	1	1	1	0	0	0	6
BL27	1	1	1	1	0	0	0	0	0	4
BL28	1	1	1	1	1	1	1	1	0	8
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
BL32	1	1	1	1	1	1	1	1	0	8
BL33	1	1	1	1	0	0	0	0	0	4
BL34	0	0	0	0	0	0	0	0	0	0
BL35	0	0	0	0	1	1	1	1	0	4
BL36	0	0	0	0	0	0	1	1	0	2
BL37	0	0	0	0	1	1	1	1	0	4
BL38	1	1	1	1	1	1	0	0	0	6

Table 4-174: Data Pattern for I_{DD4W} (DBI Off) BL = 32 (Continued)

DBI Off Case										
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	# of 1s
BL39	1	1	1	1	0	0	0	0	0	4
BL40	1	1	1	1	1	1	1	1	0	8
BL41	1	1	1	1	0	0	0	0	0	4
BL42	0	0	0	0	0	0	0	0	0	0
BL43	0	0	0	0	1	1	1	1	0	4
BL44	0	0	0	0	0	0	1	1	0	2
BL45	0	0	0	0	1	1	1	1	0	4
BL46	1	1	1	1	1	1	0	0	0	6
BL47	1	1	1	1	0	0	0	0	0	4
BL48	1	1	1	1	1	1	0	0	0	6
BL49	1	1	1	1	0	0	0	0	0	4
BL50	0	0	0	0	0	0	1	1	0	2
BL51	0	0	0	0	1	1	1	1	0	4
BL52	0	0	0	0	0	0	0	0	0	0
BL53	0	0	0	0	1	1	1	1	0	4
BL54	1	1	1	1	1	1	1	1	0	8
BL55	1	1	1	1	0	0	0	0	0	4
BL56	0	0	0	0	0	0	1	1	0	2
BL57	0	0	0	0	1	1	1	1	0	4
BL58	1	1	1	1	1	1	0	0	0	6
BL59	1	1	1	1	0	0	0	0	0	4
BL60	1	1	1	1	1	1	1	1	0	8
BL61	1	1	1	1	0	0	0	0	0	4
BL62	0	0	0	0	0	0	0	0	0	0
BL63	0	0	0	0	1	1	1	1	0	4
# of 1s	32	32	32	32	32	32	32	32		

Notes:

1. Simplified pattern; same data pattern was applied to DQ[4], DQ[5], DQ[6], and DQ[7] toreduce complexity for I_{DD4W} pattern programming.

Table 4-175: Data Pattern for I_{DD4R} (DBI Off) BL = 32

DBI Off Case										
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	# of 1s
BL0	1	1	1	1	1	1	1	1	0	8
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	1	1	1	1	1	1	0	0	0	6
BL7	1	1	1	1	0	0	0	0	0	4
BL8	1	1	1	1	1	1	1	1	0	8
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	1	1	1	1	1	1	0	0	0	6
BL15	1	1	1	1	0	0	0	0	0	4
BL16	1	1	1	1	1	1	0	0	0	6
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	1	1	1	1	1	1	1	1	0	8
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	1	1	1	1	1	1	0	0	0	6
BL27	1	1	1	1	0	0	0	0	0	4
BL28	1	1	1	1	1	1	1	1	0	8
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
BL32	0	0	0	0	0	0	1	1	0	2
BL33	0	0	0	0	1	1	1	1	0	4
BL34	1	1	1	1	1	1	0	0	0	6
BL35	1	1	1	1	0	0	0	0	0	4
BL36	1	1	1	1	1	1	1	1	0	8
BL37	1	1	1	1	0	0	0	0	0	4
BL38	0	0	0	0	0	0	0	0	0	0

Table 4-175: Data Pattern for I_{DD4R} (DBI Off) BL = 32 (Continued)

DBI Off Case										
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	# of 1s
BL39	0	0	0	0	1	1	1	1	0	4
BL40	0	0	0	0	0	0	1	1	0	2
BL41	0	0	0	0	1	1	1	1	0	4
BL42	1	1	1	1	1	1	0	0	0	6
BL43	1	1	1	1	0	0	0	0	0	4
BL44	1	1	1	1	1	1	1	1	0	8
BL45	1	1	1	1	0	0	0	0	0	4
BL46	0	0	0	0	0	0	0	0	0	0
BL47	0	0	0	0	1	1	1	1	0	4
BL48	1	1	1	1	1	1	1	1	0	8
BL49	1	1	1	1	0	0	0	0	0	4
BL50	0	0	0	0	0	0	0	0	0	0
BL51	0	0	0	0	1	1	1	1	0	4
BL52	1	1	1	1	1	1	0	0	0	6
BL53	1	1	1	1	0	0	0	0	0	4
BL54	0	0	0	0	0	0	1	1	0	2
BL55	0	0	0	0	1	1	1	1	0	4
BL56	0	0	0	0	0	0	0	0	0	0
BL57	0	0	0	0	1	1	1	1	0	4
BL58	1	1	1	1	1	1	1	1	0	8
BL59	1	1	1	1	0	0	0	0	0	4
BL60	0	0	0	0	0	0	1	1	0	2
BL61	0	0	0	0	1	1	1	1	0	4
BL62	1	1	1	1	1	1	0	0	0	6
BL63	1	1	1	1	0	0	0	0	0	4
# of 1s	32	32	32	32	32	32	32	32		

Note:

1. Simplified pattern; same data pattern was applied to DQ[4], DQ[5], DQ[6], and DQ[7] toreduce complexity for I_{DD4R} pattern programming.

Table 4-176: Data Pattern for I_{DD4W} (DBI On) BL = 32

DBI On Case										
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	# of 1s
BL0	0	0	0	0	0	0	0	0	1	1
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	0	0	0	0	0	0	1	1	1	3
BL7	1	1	1	1	0	0	0	0	0	4
BL8	0	0	0	0	0	0	0	0	1	1
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	0	0	0	0	0	0	1	1	1	3
BL15	1	1	1	1	0	0	0	0	0	4
BL16	0	0	0	0	0	0	1	1	1	3
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	0	0	0	0	0	0	0	0	1	1
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	0	0	0	0	0	0	1	1	1	3
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	0	0	1	1
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
BL32	0	0	0	0	0	0	0	0	1	1
BL33	1	1	1	1	0	0	0	0	0	4
BL34	0	0	0	0	0	0	0	0	0	0
BL35	0	0	0	0	1	1	1	1	0	4
BL36	0	0	0	0	0	0	1	1	0	2
BL37	0	0	0	0	1	1	1	1	0	4
BL38	0	0	0	0	0	0	1	1	1	3

Table 4-176: Data Pattern for I_{DD4W} (DBI On) BL = 32 (Continued)

DBI On Case										
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	# of 1s
BL39	1	1	1	1	0	0	0	0	0	4
BL40	0	0	0	0	0	0	0	0	1	1
BL41	1	1	1	1	0	0	0	0	0	4
BL42	0	0	0	0	0	0	0	0	0	0
BL43	0	0	0	0	1	1	1	1	0	4
BL44	0	0	0	0	0	0	1	1	0	2
BL45	0	0	0	0	1	1	1	1	0	4
BL46	0	0	0	0	0	0	1	1	1	3
BL47	1	1	1	1	0	0	0	0	0	4
BL48	0	0	0	0	0	0	1	1	1	3
BL49	1	1	1	1	0	0	0	0	0	4
BL50	0	0	0	0	0	0	1	1	0	2
BL51	0	0	0	0	1	1	1	1	0	4
BL52	0	0	0	0	0	0	0	0	0	0
BL53	0	0	0	0	1	1	1	1	0	4
BL54	0	0	0	0	0	0	0	0	1	1
BL55	1	1	1	1	0	0	0	0	0	4
BL56	0	0	0	0	0	0	1	1	0	2
BL57	0	0	0	0	1	1	1	1	0	4
BL58	0	0	0	0	0	0	1	1	1	3
BL59	1	1	1	1	0	0	0	0	0	4
BL60	0	0	0	0	0	0	0	0	1	1
BL61	1	1	1	1	0	0	0	0	0	4
BL62	0	0	0	0	0	0	0	0	0	0
BL63	0	0	0	0	1	1	1	1	0	4
# of 1s	16	16	16	16	16	16	32	32	16	

Note:

1. DBI enabled burst: BL0, BL6, BL8, BL14, BL16, BL22, BL26, BL28, BL32, BL38, BL40, BL46,BL48, BL54, BL58, and BL60.

Table 4-177: Data Pattern for I_{DD4R} (DBI On) BL = 32

DBI On Case										
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	# of 1s
BL0	0	0	0	0	0	0	0	0	1	1
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	0	0	0	0	0	0	1	1	1	3
BL7	1	1	1	1	0	0	0	0	0	4
BL8	0	0	0	0	0	0	0	0	1	1
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	0	0	0	0	0	0	1	1	1	3
BL15	1	1	1	1	0	0	0	0	0	4
BL16	0	0	0	0	0	0	1	1	1	3
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	0	0	0	0	0	0	0	0	1	1
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	0	0	0	0	0	0	1	1	1	3
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	0	0	1	1
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
BL32	0	0	0	0	0	0	1	1	0	2
BL33	0	0	0	0	1	1	1	1	0	4
BL34	0	0	0	0	0	0	1	1	1	3
BL35	1	1	1	1	0	0	0	0	0	4
BL36	0	0	0	0	0	0	0	0	1	1
BL37	1	1	1	1	0	0	0	0	0	4
BL38	0	0	0	0	0	0	0	0	0	0

Table 4-177: Data Pattern for I_{DD4R} (DBI On) BL = 32 (Continued)

DBI On Case										
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	# of 1s
BL39	0	0	0	0	1	1	1	1	0	4
BL40	0	0	0	0	0	0	1	1	0	2
BL41	0	0	0	0	1	1	1	1	0	4
BL42	0	0	0	0	0	0	1	1	1	3
BL43	1	1	1	1	0	0	0	0	0	4
BL44	0	0	0	0	0	0	0	0	1	1
BL45	1	1	1	1	0	0	0	0	0	4
BL46	0	0	0	0	0	0	0	0	0	0
BL47	0	0	0	0	1	1	1	1	0	4
BL48	0	0	0	0	0	0	0	0	1	1
BL49	1	1	1	1	0	0	0	0	0	4
BL50	0	0	0	0	0	0	0	0	1	1
BL51	0	0	0	0	1	1	1	1	0	4
BL52	0	0	0	0	0	0	1	1	1	3
BL53	1	1	1	1	0	0	0	0	0	4
BL54	0	0	0	0	0	0	1	1	0	2
BL55	0	0	0	0	1	1	1	1	0	4
BL56	0	0	0	0	0	0	0	0	0	0
BL57	1	1	1	1	0	0	0	0	0	4
BL58	0	0	0	0	0	0	0	0	1	1
BL59	1	1	1	1	0	0	0	0	0	4
BL60	0	0	0	0	0	0	1	1	0	2
BL61	0	0	0	0	1	1	1	1	0	4
BL62	0	0	0	0	0	0	1	1	1	3
BL63	1	1	1	1	0	0	0	0	0	4
# of 1s	16	16	16	16	16	16	32	32	16	

Note:

1. DBI enabled burst: BL0, BL6, BL8, BL14, BL16, BL22, BL26, BL28, BL34, BL36, BL42, BL44,BL48, BL52, BL58, and BL62.

I_{DD} Specifications

I_{DD} values are for the entire operating voltage range, and all of them are for the entirestandard temperature range.

Table 4-178: I_{DD} Specification Parameters and Operating Conditions

LPDDR4: V_{DD2}, V_{DDQ} = 1.06–1.17V; V_{DD1} = 1.70–1.95V

Parameter/Condition	Symbol	Power Supply	Notes
Operating one bank active-precharge current: ^{t}CK = ^{t}CK (MIN); ^{t}RC = ^{t}RC (MIN); CKE is HIGH; CS is LOW between valid commands; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD01}	V_{DD1}	
	I_{DD02}	V_{DD2}	
	I_{DD0Q}	V_{DDQ}	2
Idle power-down standby current: ^{t}CK = ^{t}CK (MIN); CKE is LOW; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD2P1}	V_{DD1}	
	I_{DD2P2}	V_{DD2}	
	I_{DD2PQ}	V_{DDQ}	2
Idle power-down standby current with clock stop: CK_t = LOW, CK_c = HIGH; CKE is LOW; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	I_{DD2PS1}	V_{DD1}	
	I_{DD2PS2}	V_{DD2}	
	I_{DD2PSQ}	V_{DDQ}	2
Idle non-power-down standby current: ^{t}CK = ^{t}CK (MIN); CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD2N1}	V_{DD1}	
	I_{DD2N2}	V_{DD2}	
	I_{DD2NQ}	V_{DDQ}	2
Idle non-power-down standby current with clock stopped: CK_t = LOW; CK_c = HIGH; CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	I_{DD2NS1}	V_{DD1}	
	I_{DD2NS2}	V_{DD2}	
	I_{DD2NSQ}	V_{DDQ}	2
Active power-down standby current: ^{t}CK = ^{t}CK (MIN); CKE is LOW; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD3P1}	V_{DD1}	
	I_{DD3P2}	V_{DD2}	
	I_{DD3PQ}	V_{DDQ}	2
Active power-down standby current with clock stop: CK_t = LOW, CK_c = HIGH; CKE is LOW; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	I_{DD3PS1}	V_{DD1}	
	I_{DD3PS2}	V_{DD2}	
	I_{DD3PSQ}	V_{DDQ}	3
Active non-power-down standby current: ^{t}CK = ^{t}CK (MIN); CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD3N1}	V_{DD1}	
	I_{DD3N2}	V_{DD2}	
	I_{DD3NQ}	V_{DDQ}	3
Active non-power-down standby current with clock stopped: CK_t = LOW, CK_c = HIGH; CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	I_{DD3NS1}	V_{DD1}	
	I_{DD3NS2}	V_{DD2}	
	I_{DD3NSQ}	V_{DDQ}	3
Operating burst READ current: ^{t}CK = ^{t}CK (MIN); CS is LOW between valid commands; One bank is active; BL = 16 or 32; RL = RL (MIN); CA bus inputs are switching; 50% data change each burst transfer; ODT is disabled	I_{DD4R1}	V_{DD1}	
	I_{DD4R2}	V_{DD2}	
	I_{DD4RQ}	V_{DDQ}	4

Table 178: I_{DD} Specification Parameters and Operating Conditions (Continued)

LPDDR4: V_{DD2}, V_{DDQ} = 1.06–1.17V; V_{DD1} = 1.70–1.95V

Parameter/Condition	Symbol	Power Supply	Notes
Operating burst WRITE current: ^{t}CK = ^{t}CK (MIN); CS is LOW between valid commands; One bank is active; BL = 16 or 32; WL =WL (MIN); CA bus inputs are switching; 50% data change eachburst transfer; ODT is disabled	I_{DD4W1}	V_{DD1}	
	I_{DD4W2}	V_{DD2}	
	I_{DD4WQ}	V_{DDQ}	3
All-bank REFRESH burst current: ^{t}CK = ^{t}CK (MIN); CKE is HIGH between valid commands; ^{t}RC = ^{t}RFCab (MIN); Burst refresh; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD51}	V_{DD1}	
	I_{DD52}	V_{DD2}	
	I_{DD5Q}	V_{DDQ}	3
All-bank REFRESH average current: ^{t}CK = ^{t}CK (MIN); CKE is HIGH between valid commands; ^{t}RC = ^{t}REFI; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD5AB1}	V_{DD1}	
	I_{DD5AB2}	V_{DD2}	
	I_{DD5ABQ}	V_{DDQ}	3
Per-bank REFRESH average current: ^{t}CK = ^{t}CK (MIN); CKE is HIGH between valid commands; ^{t}RC = ^{t}REFI/8; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD5PB1}	V_{DD1}	
	I_{DD5PB2}	V_{DD2}	
	I_{DD5PBQ}	V_{DDQ}	3
Power-down self refresh current: CK_t = LOW, CK_c = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable; Maximum 1x self refresh rate; ODT is disabled	I_{DD61}	V_{DD1}	5, 6
	I_{DD62}	V_{DD2}	5, 6
	I_{DD6Q}	V_{DDQ}	3, 5, 6

Notes:

1. ODT disabled: MR11[2:0] = 000b.
2. I_{DD} current specifications are tested after the device is properly initialized.
3. Measured currents are the summation of V_{DDQ} and V_{DD2}.
4. Guaranteed by design with output load = 5pF and R_{ON} = 40 ohm.
5. The 1x self refresh rate is the rate at which the device is refreshed internally during selfrefresh before going into the elevatedtemperature range.
6. This is the general definition that applies to full-array self refresh.
7. For all I_{DD} measurements, V_{IHCKE} = 0.8 × V_{DD2}; V_{ILCKE} = 0.2 × V_{DD2}.

4.52 AC Timing

Table 4-179: Clock Timing

Parameter	Symbol	Min/ Max	Data Rate		Unit
			1600	3200	
Average clock period	^{t}CK(avg)	Min	1250	625	ps
		Max	100	100	ns
Average HIGH pulse width	^{t}CH(avg)	Min	0.46		^{t}CK(avg)
		Max	0.54		
Average LOW pulse width	^{t}CL(avg)	Min	0.46		^{t}CK(avg)
		Max	0.54		
Absolute clock period	^{t}CK(abs)	Min	^{t}CK(avg)min + ^{t}JIT(per)min		ps
Absolute clock HIGH pulse width	^{t}CH(abs)	Min	0.43		^{t}CK(avg)
		Max	0.57		
Absolute clock LOW pulse width	^{t}CL(abs)	Min	0.43		^{t}CK(avg)
		Max	0.57		
Clock period jitter	^{t}JIT(per)allowed	Min	–70	–40	ps
		Max	70	40	
Maximum clock jitter between two consecutive clock cycles (includes clock period jitter)	^{t}JIT(cc)allowed	Max	140	80	ps

Table 4-180: Read Output Timing

Parameter	Symbol	Min/ Max	Data Rate						Unit	Notes
			533	1066	1600	2133	2667	3200		
DQS output access time from CK_t/CK_c	tDQSCK	Min	1500						ps	1
		Max	3500							
DQS output access time from CK_t/CK_c - voltage variation	tDQSCK_VOLT	Max	7						ps/mV	2
DQS output access time from CK_t/CK_c - temperature variation	tDQSCK_TEMP	Max	4						ps°/C	3
CK to DQS rank to rank variation	tDQSCK_rank2rank	Max	1.0						ns	4.5
DQS_t, DQS_c to DQ skew total, per group, per access (DBI Disabled)	tDQSQ	Max	0.18						UI	6
DQ output hold time total from DQS_t, DQS_c (DBI Disabled)	tQH	Min	MIN(tQSH, tQSL)						ps	6
Data output valid window time total, per pin (DBI-Disabled)	tQW_total	Min	0.75			0.73		0.70	UI	6, 11
DQS_t, DQS_c to DQ skew total, per group, per access (DBI-Enabled)	tDQSQ_DBI	Max	0.18						UI	6
DQ output hold time total from DQS_t, DQS_c (DBI-Enabled)	tQH_DBI	Min	MIN(tQSH_DBI, tQSL_DBI)						ps	6
Data output valid window time total, per pin (DBI-Enabled)	tQW_total_DBI	Min	0.75			0.73		0.70	UI	6, 11
DQS_t, DQS_c differential output LOW time (DBIDisabled)	tQSL	Min	tCL(abs) - 0.05						tCK(avg)	9, 11
DQS_t, DQS_c differential output HIGH time (DBIDisabled)	tQSH	Min	tCH(abs) - 0.05						tCK(avg)	10, 11
DQS_t, DQS_c differential output LOW time (DBIEnabled)	tQSL-DBI	Min	tCL(abs) - 0.045						tCK(avg)	9, 11
DQS_t, DQS_c differential output HIGH time (DBIEnabled)	tQSL-DBI	Min	tCH(abs) - 0.045						tCK(avg)	10, 11
Read preamble	tRPRE	Min	1.8						tCK(avg)	
Read postamble	tRPST	Min	0.4 (or 1.4 if extra postamble is programmed in MR)						tCK(avg)	

Table 4-180: Read Output Timing (Continued)

Parameter	Symbol	Min/ Max	Data Rate						Unit	Notes
			533	1066	1600	2133	2667	3200		
DQS Low-Z from clock	^{t}LZ(DQS)	Min	(RL x ^{t}CK) + ^{t}DQSCK(Min) - (^{t}RPRE(Max) x ^{t}CK) - 200ps						ps	
DQ Low-Z from clock	^{t}LZ(DQ)	Min	(RL x ^{t}CK) + tDQSCK(Min) - 200ps						ps	
QS High-Z from clock	^{t}HZ(DQS)	Min	(RL x $_{t}$CK) + tDQSCK(Max)+(BL/2 x ^{t}CK) + (^{t}RPST(Max) x ^{t}CK) - 100ps						ps	
DQ High-Z from clock	^{t}HZ(DQ)	Min	(RL x ^{t}CK) + ^{t}DQSCK(Max) + ^{t}DQSQ(Max) + (BL/2 x ^{t}CK) - 100ps						ps	

Notes:

1. This parameter includes DRAM process, voltage, and temperature variation. It also includesthe AC noise impact forfrequencies >20 MHz and a MAX voltage of 45mV peakto-peak from DC-20 MHz at a fixed temperature on the package.The voltage supplynoise must comply with the component MIN/MAX DC operating conditions.
2. ^{t}DQSCK_volt max delay variation as a function of DC voltage variation for V_{DDQ} andV_{DD2}. The voltage supply noise must comply with the component MIN/MAX DC operatingconditions. The voltage variation is defined as theMAX[ABS(^{t}DQSCK(MIN)@V1 -^{t}DQSCK(MAX)@V2), ABS(^{t}DQSCK(MAX)@V1 - ^{t}DQSCK(MIN)@V2)]/ABS(V1 - V2).
3. ^{t}DQSCK_temp MAX delay variation as a function of temperature.
4. The same voltage and temperature are applied to ^{t}DQSCK_rank2rank.
5. ^{t}DQSCK_rank2rank parameter is applied to multi-ranks per byte lane within a packageconsisting of the same design dies.
6. DQ-to-DQS differential jitter where the total includes the sum of deterministic and randomtiming terms for a specified BER.
7. The deterministic component of the total timing.
8. This parameter will be characterized and guaranteed by design.
9. ^{t}QSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c,as measured from one falling edgeto the next consecutive rising edge.
10. ^{t}QSH describes the instantaneous differential output high pulse width on DQS_t -DQS_c, as measured from one fallingedge to the next consecutive rising edge.
11. This parameter is a function of input clock jitter. These values assume MIN ^{t}CH(abs) and^{t}CL(abs). When the input clockjitter MIN ^{t}CH(abs) and ^{t}CL(abs) is 0.44 or greater than^{t}CK(avg), the MIN value of ^{t}QSL will be ^{t}CL(abs) - 0.04 and ^{t}QSHwill be ^{t}CH(abs) - 0.04.

Table 4-181: Write Voltage and Timing

Note UI = ^{t}CK(AVG)(MIN)/2

Parameter	Symbol	Min/ Max	Data Rate						Unit	Notes
			533	1066	1600	2133	2667	3200		
Rx timing window total at V_{dIVW} voltage levels	TdIVW _total	Max	0.22					0.25	UI	1, 2, 3
DQ and DMI input pulse width (at V_{CENT_DQ})	TdIPW	Min	0.45						UI	7
DQ-to-DQS offset	^{t}DQS2DQ	Min	200						ps	6
		Max	800							
DQ-to-DQ offset	^{t}DQDQ	Max	30						ps	7
DQ-to-DQS offset temperature variation	^{t}DQS2DQ _temp	Max	0.6						ps/°C	8
DQ-to-DQS offset voltage variation	^{t}DQS2DQ _volt	Max	33						ps/50mV	9
DQ-to-DQS offset rank to rank variation	^{t}DQS2DQ _rank2rank	Max	200						ps	10, 11
WRITE command to first DQS transition	^{t}DQSS	Min	0.75						^{t}CK(avg)	
		Max	1.25							
DQS input HIGH-level width	^{t}DQSH	–	0.4						^{t}CK(avg)	
DQS input LOW-level width	^{t}DQSL	Min	0.4						^{t}CK(avg)	
DQS falling edge to CK setup time	^{t}DSS	Min	0.2						^{t}CK(avg)	
DQS falling edge from CK hold time	^{t}DSH	Min	0.2						^{t}CK(avg)	
Write postamble	^{t}WPST	Min	0.4 (or 1.4 if extra postamble is programmed in MR)						^{t}CK(avg)	
Write preamble	^{t}WPRE	Min	1.8						^{t}CK(avg)	

Notes:

1. Data Rx mask voltage and timing parameters are applied per pin and include the DRAMDQ-to-DQS voltage AC noise impact for frequencies >20 MHz with a maximum voltageof 45mV peak-to-peak at a fixed temperature on the package. Thevoltage supply noisemust comply to the component MIN/MAX DC operating conditions.
2. Rx differential DQ-to-DQS jitter total timing window at the V_{dIVW} voltage levels.
3. Defined over the DQ internal V_{REF} range. The Rx mask at the pin must be within the internalV_{REF} DQ range irrespective ofthe input signal common mode.
4. Rx mask defined for one pin toggling with other DQ signals in a steady state.
5. DQ-only minimum input pulse width defined at the $V_{CENT\_DQ(pin\_mid)}$.
6. DQ-to-DQS offset is within byte from DRAM pin to DRAM internal latch. Includes allDRAM process, voltage, and temperature variations.
7. DQ-to-DQ offset defined within byte from DRAM pin to DRAM internal latch for a givencomponent.
8. ^{t}DQS2DQ (MAX) delay variation as a function of temperature.
9. ^{t}DQS2DQ (MAX) delay variation as a function of the DC voltage variation for V_{DDQ} andV_{DD2}. It includes the V_{DDQ} andV_{DD2} AC noise impact for frequencies >20 MHz and MAXvoltage of 45mV peak-to-peak from DC-20 MHz at a fixed temperature onhe package.For tester measurement, V_{DDQ} = V_{DD}2 is assumed.
10. The same voltage and temperature are applied to ^{t}DQS2DQ_rank2rank.
11. ^{t}DQS2DQ_rank2rank parameter is applied to multi-ranks per byte lane within a packageconsisting of the same design die.

Table 4-182: CKE Input Timing

Parameter	Symbol	Min/ Max	Data Rate		Unit	Notes
			1600	3200		
CKE minimum pulse width (HIGH and LOW pulse width)	tCKE	Min	MAX(7.5ns, 4nCK)		ns	1
Delay from valid command to CKE input LOW	tCMDCKE	Min	MAX(1.75ns, 3nCK)		ns	1
Valid clock requirement after CKE input LOW	tCKELCK	Min	MAX(5ns, 5nCK)		ns	1
Valid CS requirement before CKE input LOW	tCSCKE	Min	1.75		ns	
Valid CS requirement after CKE input LOW	tCKELCS	Min	MAX(5ns, 5nCK)		ns	1
Valid Clock requirement before CKE Input HIGH	tCKCKEH	Min	MAX(1.75ns, 3nCK)		ns	1
Exit power-down to next valid command delay	tXP	Min	MAX(7.5ns, 5nCK)		ns	1
Valid CS requirement before CKE input HIGH	tCSCKEH	Min	1.75		ns	
Valid CS requirement after CKE input HIGH	tCKEHCS	Min	MAX(7.5ns, 5nCK)		ns	1
Valid clock and CS requirement after CKE input LOW after MRW command	tMRWCKEL	Min	MAX(14ns, 10nCK)		ns	1
Valid clock and CS requirement after CKE input LOW after ZQ calibration start command	tZQCKE	Min	MAX(1.75ns, 3nCK)		ns	1

Note:

1. Delay time has to satisfy both analog time(ns) and clock count(nCK). For example,tCMDCKE will not expire until CK hastoggled through at least 3 full cycles (3tCK) and3.75ns has transpired. The case which 3nCK is applied to is shown below.

Figure 4-149: tCMDCKE Timing

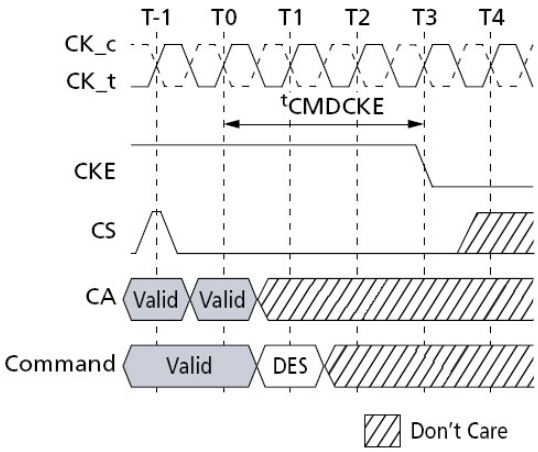


Table 4-183: Command Address Input Timing

Parameter	Symbol	Min/ Max	Data Rate						Unit	Notes
			533	1066	1600	2133	2667	3200		
Command/address valid window (referenced from CA V_{IL}/V_{IH} to CK V_{IX})	^{t}cIVW	Min	0.3						^{t}CK(avg)	1, 2, 3
Address and control input pulse width (referenced to V_{REF})	^{t}cIPW	Min	0.55	0.55	0.55	0.6	0.6	0.6	^{t}CK(avg)	4

Notes:
1. CA Rx mask timing parameters at the pin including voltage and temperature drift.
2. Rx differential CA to CK jitter total timing window at the V_{cIVW} voltage levels.
3. Defined over the CA internal V_{REF} range. The Rx mask at the pin must be within the internal$V_{REF(CA)}$ range irrespectiveof the input signal common mode.
4. CA only minimum input pulse width defined at the V_{CENT_CA}(pin mid).

Table 4-184: Boot Timing Parameters (10–55 MHz)

Parameter	Symbol	Min/ Max	Value	Unit
Clock cycle time	^{t}CKb	Min	18	ns
		Max	100	
DQS output data acess time from CK	^{t}DQSCKb	Min	1.0	ns
		Max	10.0	
DQS edge to output data edge	^{t}DQSQb	Max	1.2	ns

Table 4-185: Mode Register Timing Parameters

Parameter	Symbol	Min/ Max	Data Rate		Unit
			1600	3200	
MODE REGISTER WRITE (MRW) command period	^{t}MRW	Min	MAX(10ns, 10nCK)		ns
MODE REGISTER SET command delay	^{t}MRD	Min	MAX(14ns, 10nCK)		ns
MODE REGISTER READ (MRR) command period	^{t}MRR	Min	8		^{t}CK(AVG)
Additional time after ^{t}XP has expired until the MRR command may be issued	^{t}MRRI	Min	^{t}RCD(min) + 3nCK		ns
Delay from MRW command to DQS driven out	^{t}SDO	Max	MAX(12nCK, 20ns)		ns

Table 4-186: Core Timing Parameters

Refresh rate is determined by the value in MR4 OP[2:0]

Parameter	Symbol	Min/ Max	Data Rate						Unit	Notes
			533	1066	1600	2133	2667	3200		
READ latency (DBI disa-bled)	RL-A	Min	6	10	14	20	24	28	tCK(AVG)	
READ latency (DBI ena-bled)	RL-B	Min	6	12	16	22	28	32	tCK(AVG)	
WRITE latency (Set A)	WL-A	Min	4	6	8	10	12	14	tCK(AVG)	
WRITE latency (Set B)	WL-B	Min	4	8	12	18	22	26	tCK(AVG)	
ACTIVATE-to-ACTIVATE command period (same bank)	tRC	Min	tRAS + tRPab (with all-bank precharge) tRAS + tRPpb (with per-bank precharge)						ns	1
Minimum self refresh time (entry to exit)	tSR	Min	MAX(15ns, 3nCK)						ns	
Self refresh exit to next valid command delay	tXSR	Min	MAX(tRFCab + 7.5ns, 2nCK)						ns	
CAS-to-CAS delay	tCCD	Min	8						tCK(AVG)	
CAS-to-CAS delay masked write	tCCDMW	Min	32						tCK(AVG)	
Internal READ-to-PRECHARGE command delay	tRTP	Min	MAX(7.5ns, 8nCK)						ns	
RAS-to-CAS delay	tRCD	Min	MAX(18ns, 4nCK)						ns	
Row precharge time (single bank)	tRPpb	Min	MAX(18ns, 3nCK)						ns	
Row precharge time (all banks)	tRPab	Min	MAX(21ns, 3nCK)						ns	
Row active time	tRAS	Min	MAX(42ns, 3nCK)						ns	1
		Max	MIN(9 × tREFI × Refresh Rate1, 70.2)						µs	
Write recovery time	tWR	Min	MAX(18ns, 4nCK)						ns	
Write-to-read delay	tWTR	Min	MAX(10ns, 8nCK)						ns	
Active bank A to active bank B	tRRD	Min	MAX(10ns, 4nCK)						ns	
Precharge-to-precharge delay	tPPD	Min	4						tCK(AVG)	2
Four-bank activate window	tFAW	Min	40						ns	
Delay from SRE command to CKE input LOW	tESCKE	Min	MAX(1.75ns, 3nCK)						–	3

Notes:

1. DRAM devices should be evenly addressed when being accessed. Disproportionate accessesto a particular row addressmay result in reduction of the product lifetime.
2. Precharge to precharge timing restriction does not apply to AUTO PRECHARGE commands.
3. Delay time has to satisfy both analog time(ns) and clock count (nCK). It means thattESCKE will not expire until CK hastoggled through at least three full cycles (3 tCK) and1.75ns has transpired. The case which 3nCK is applied to is shownbelow.

Figure 4-150: ^{t}ESCKE Timing

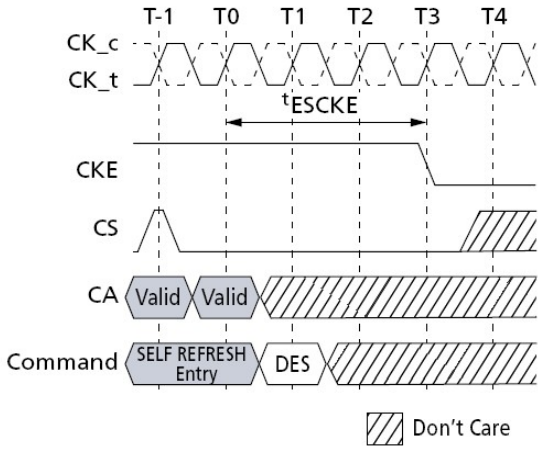


Table 4-187: CA Bus ODT Timing

Parameter	Symbol	Min/ Max	Data Rate
			533-3200
CA ODT value update time	^{t}ODTUP	Min	RU(20ns/^{t}CK,avg)

Table 4-188: CA Bus Training Parameters

Parameter	Symbol	Min/ Max	Data Rate		Unit	Notes
			1600	3200		
Valid clock requirement after CKE Input LOW	tCKELCK	Min	MAX(5ns, 5nCK)		tCK	
Data setup for VREF training mode	tDStrain	Min	2		ns	
Data hold for VREF training mode	tDHtrain	Min	2		ns	
Asynchronous data read	tADR	Max	20		ns	
CA BUS TRAINING command-to-command delay	tCACD	Min	RU(tADR/tCK)		tCK	1
Valid strobe requirement before CKE LOW	tDQSCKE	Min	10		ns	
First CA BUS TRAINING command following CKE LOW	tCAENT	Min	250		ns	
V_{REF} step time – multiple steps	tVREF-ca_LONG	Max	250		ns	
V_{REF} step time – one step	tVREF-ca_SHORT	Max	80		ns	
Valid clock requirement before CS HIGH	tCKPRECS	Min	2tCK + tXP		–	
Valid clock requirement after CS HIGH	tCKPSTCS	Min	MAX(7.5ns, 5nCK)		–	
Minimum delay from CS to DQS toggle in command bus training	tCS_VREF	Min	2		tCK	
Minimum delay from CKE HIGH to strobe High-Z	tCKEHDQS	Min	10		ns	
CA bus training CKE HIGH to DQ tri-state	tMRZ	Min	1.5		ns	
ODT turn-on latency from CKE	tCKELODTon	Min	20		ns	
ODT turn-off latency from CKE	tCKEHODT-	Min	20		ns	
Exit command bus training mode to next valid command delay	tXCBT_Short	Min	MAX(200ns, 5nCK)		–	2
	tXCBT_Middle	Min	MAX(200ns, 5nCK)		–	2
	tXCBT_Long	Min	MAX(250ns, 5nCK)		–	2

Note:

1. If tCACD is violated, the data for samples that violate tCACD will not be available, exceptfor the last sample (where tCACDafter this sample is met). Valid data for the last samplewill be available after tADR.
2. Exit command bus training mode to next valid command delay time depends on valueof $V_{REF(CA)}$ setting: MR12 OP[5:0] and $V_{REF(CA)}$ range: MR12 OP[6] of FSP-OP 0 and 1. Thedetails are shown in tFC value mapping table. Additionally exit command bus trainingmode to next valid command delay time may affect $V_{REF(DQ)}$ setting. Settling time of$V_{REF(DQ)}$ level is same as $V_{REF(CA)}$ level.

Table 4-189: Asynchronous ODT Turn On and Turn Off Timing

Symbol	800–1600 MHz	Unit
tODTon,min	1.5	ns
tODTon,max	3.5	ns
tODToff,min	1.5	ns
tODToff,max	3.5	ns

Table 4-190: Temperature Derating Parameters

Parameter	Symbol	Min/ Max	Data Rate		Unit
			1600	3200	
DQS output access time from CK_t/ CK_c (derated)	tDQSCKd	Max	3600		ps
RAS-to-CAS delay (derated)	tRCDd	Min	tRCD + 1.875		ns
ACTIVATE-to-ACTIVATE command period (same bank, derated)	tRCd	Min	tRC + 3.75		ns
Row active time (derated)	tRASd	Min	tRAS + 1.875		ns
Row precharge time (derated)	tRPd	Min	tRP + 1.875		ns
Active bank A to active bank B (derated)	tRRD	Min	tRRD + 1.875		ns

Note:

1. At higher temperatures (>85°C), AC timing derating may be required. If derating is requiredthe device will set MR4 OP[2:0] = 110b.

4.53 CA Rx Voltage and Timing

The command and address (CA), including CS input receiver compliance mask for voltageand timing, is shown in the CA Receiver (Rx) Mask figure below. All CA and CS signalsapply the same compliance mask and operate in single data rate mode.

The CA input Rx mask for voltage and timing is applied across all pins, as shown in thefigure below. The Rx mask defines the area that the input signal must not encroach ifthe DRAM input receiver is expected to successfully capture a valid input signal; it is notthe valid data eye.

Figure 4-151: CA Receiver (Rx) Mask

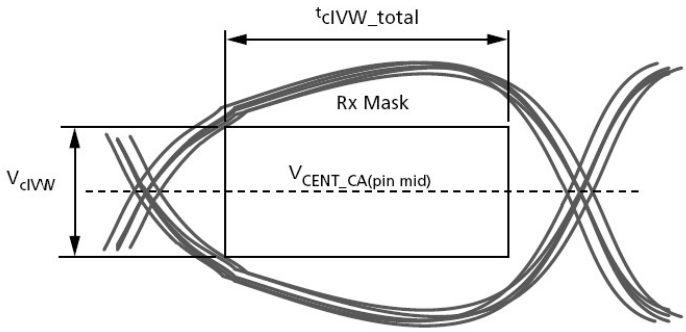
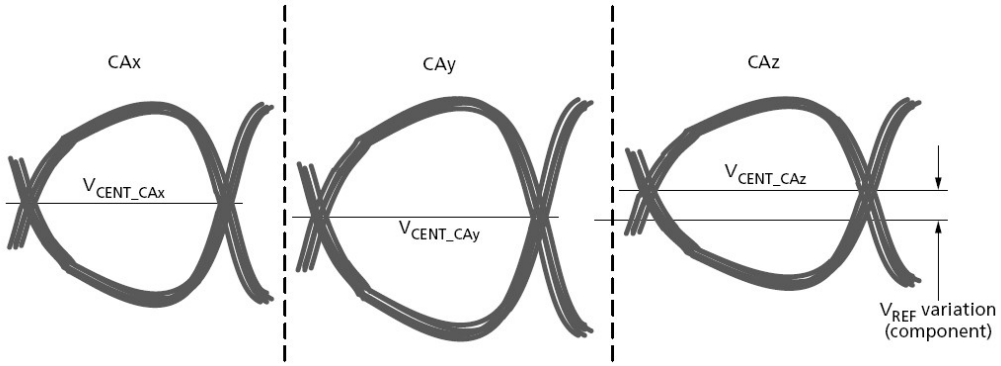
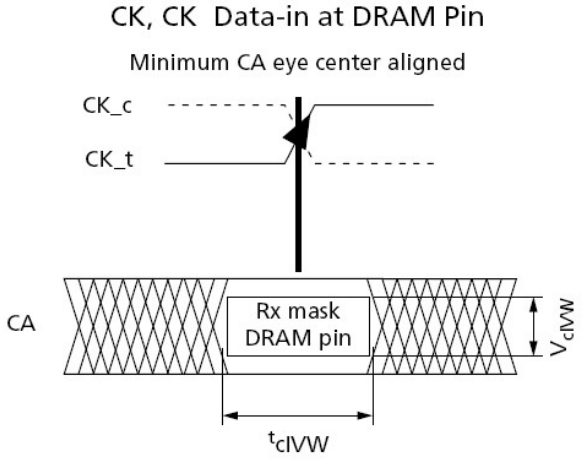


Figure 4-152: Across Pin VREF (CA) Voltage Variation



$V_{CENT\_CA(pin\ mid)}$ is defined as the midpoint between the largest V_{CENT_CA}voltage leveland the smallest V_{CENT_CA} voltage level across all CA and CS pins for a given DRAMcomponent. Each CA V_{CENT} level is defined by the center, which is, the widest openingof the cumulative data input eye, as depicted in the figure above. This clarifies that anyDRAM component level variation must be accounted for within the CA Rx mask. Thecomponent-level V_{REF} will be set by the system to account for R_{ON} and ODT settings.

Figure 4-153: CA Timings at the DRAM Pins

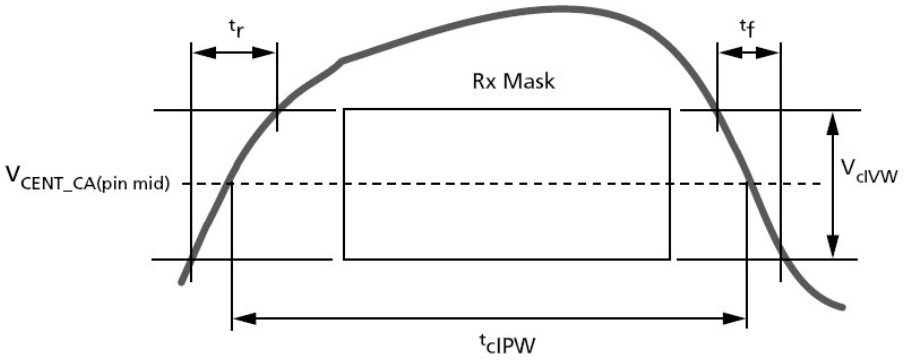


TcIVW for all CA signals is defined as centered on the CK_t/CK_c crossing at the DRAM pin.

Note:

1. All of the timing terms in above figure are measured from the CK_t/CK_c to the center(midpoint) of the TcIVW window takenat the VcIVW_total voltage levels centeredaround $V_{CENT\_CA(pin\ mid)}$.

Figure 4-154: CA tCIPW and SRIN_CIVW Definition (for Each Input Pulse)



Note:

1. SRIN_CIVW = V_{CIVW_total}/(tr or tf); signal must be monotonic within tr and tf range.

Figure 4-155: CA V_{IHL_AC} Definition (for Each Input Pulse)

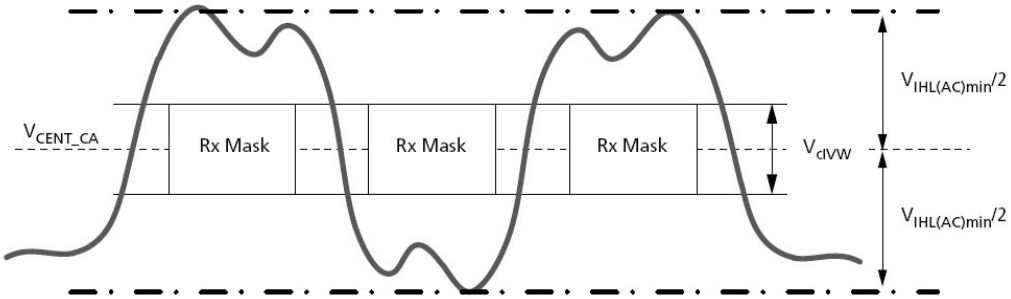


Table 4-191: DRAM CMD/ADR, CS

UI = tCK(AVG)MIN

Symbol	Parameter	DQ – 1333[7]		DQ –1600/1866		DQ – 3200		Unit	Notes
		Min	Max	Min	Max	Min	Max		
V_{CIVW}	Rx mask voltage peak-to-peak	–	175	–	175	–	155	mV	1, 2, 3
$V_{IHL(AC)}$	CA AC input pulse ampli-tude peak-to-peak	210	–	210	–	190	–	mV	4, 6
SRIN_CIVW	Input slew rate over V_{CIVW}	1	7	1	7	1	7	V/ns	5

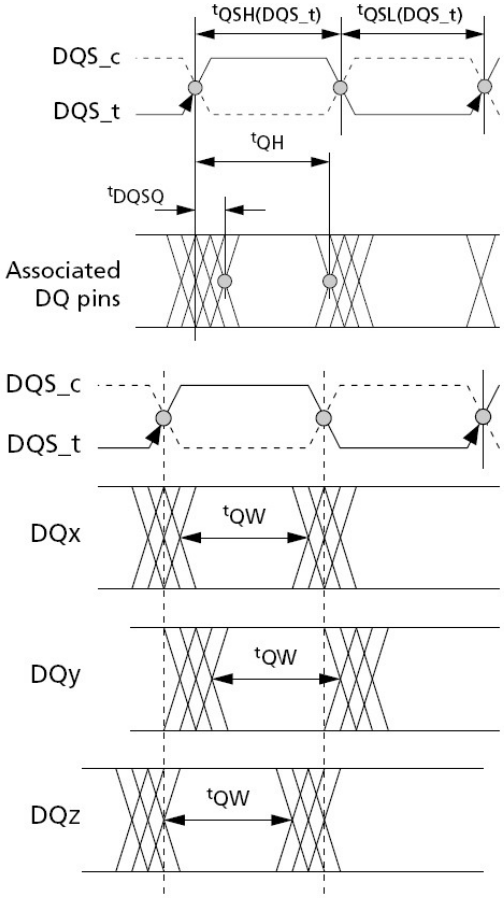
Notes:

1. CA Rx mask voltage and timing parameters at the pin, including voltage and temperaturedrift.
2. Rx mask voltage V_{CIVW} total (MAX) must be centered around $V_{CENT\_CA(pin\ mid)}$.
3. Defined over the CA internal V_{REF} range. The Rx mask at the pin must be within the internal$V_{REF(CA)}$range irrespective of theinput signal common mode.
4. CA-only input pulse signal amplitude into the receiver must meet or exceed $V_{IHL(AC)}$ atany point over the total UI. No timingrequirement above level. $V_{IHL(AC)}$ is the peak-topeakvoltage centered around $V_{CENT\_CA(pin\ mid)}$, such that $V_{IHL(AC)/2}$ (MIN) mustbe metboth above and below V_{CENT_CA}.
5. Input slew rate over V_{CIVW} mask is centered at $V_{CENT\_CA(pin\ mid)}$.
6. $V_{IHL(AC)}$ does not have to be met when no transitions are occurring.
7. The Rx voltage and absolute timing requirements apply for DQ operating frequencies ator below 1333 for all speed bins. Forexample the tCIVW(ps) = 450ps at or below 1333operating frequencies.

4.54 DQ Tx Voltage and Timing

DRAM Data Timing

Figure 4-156: Read Data Timing Definitions – ^{t}QH and ^{t}DQSQ Across DQ Signals per DQS Group



4.55 DQ Rx Voltage and Timing

The DQ input receiver mask for voltage and timing is applied per pin, as shown in theDQ Receiver (Rx) Mask figure below. The total mask (V_{dIVW_total}, TdIVW_total) definesthe area that the input signal must not encroach in order for the DQ input receiver tosuccessfully capture an input signal. The mask is a receiver property, and it is not thevalid data eye.

Figure 4-157: DQ Receiver (Rx) Mask

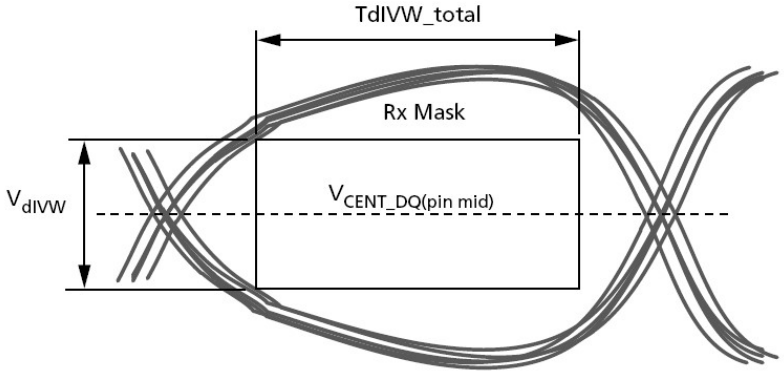
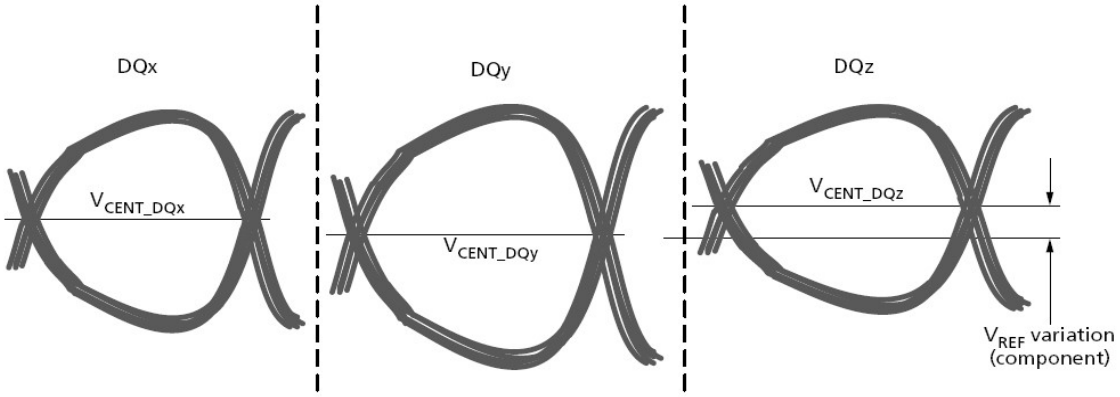
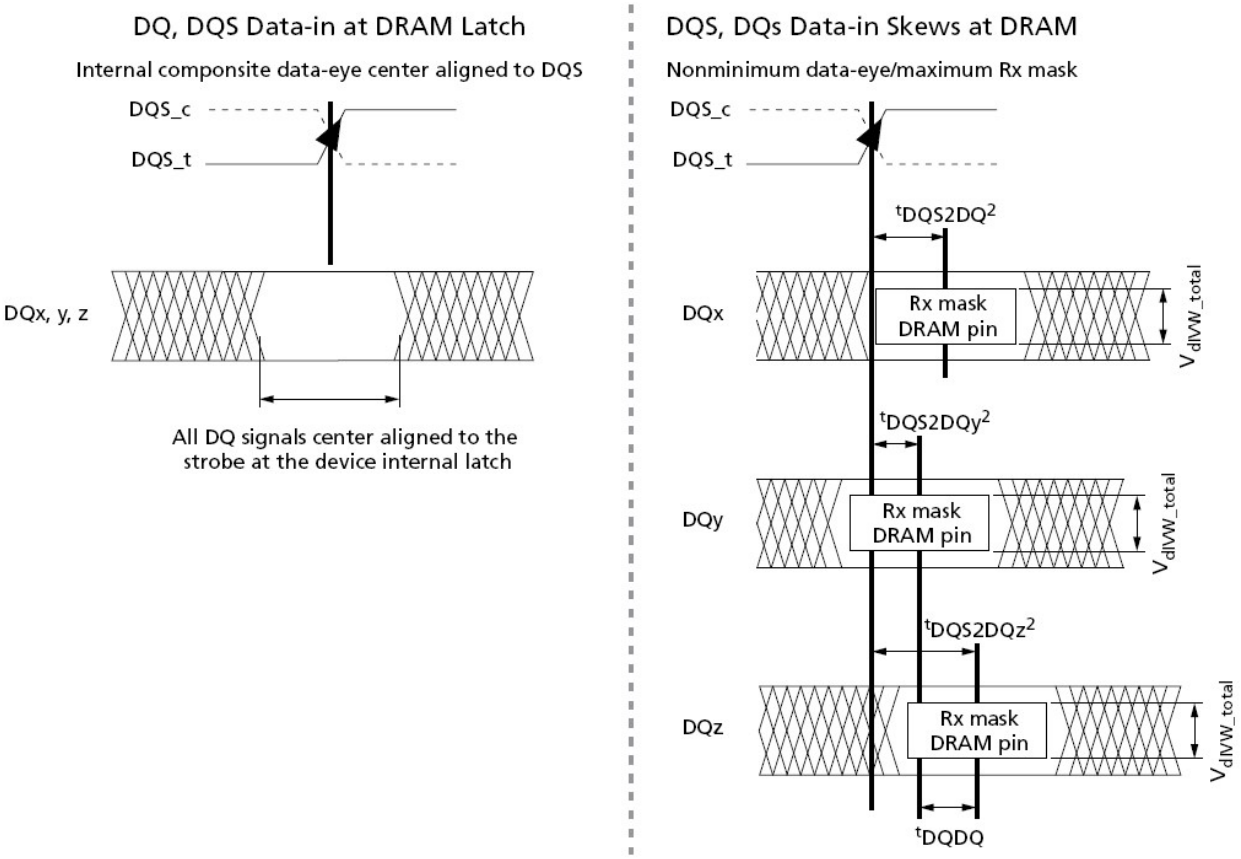


Figure 4-158: Across Pin V_{REF} DQ Voltage Variation



$V_{CENT\_DQ(pin\_mid)}$ is defined as the midpoint between the largest V_{CENT_DQ} voltage leveland the smallest V_{CENT_DQ} voltage level across all DQ pins for a given DRAM component.Each V_{CENT_DQ} is defined by the center, which is the widest opening of the cumulativedata input eye as shown in the figure above. This clarifies that any DRAM componentlevel variation must be accounted for within the DRAM Rx mask. The componentlevelV_{REF} will be set by the system to account for R_{ON} and ODT settings.

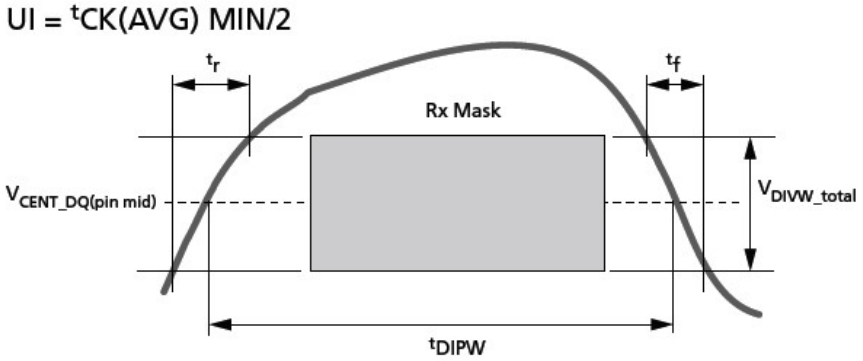
Figure 4-159: DQ-to-DQS ^{t}DQS2DQ and ^{t}DQDQ



Notes:
1. These timings at the DRAM pins are referenced from the internal latch.
2. ^{t}DQS2DQ is measured at the center (midpoint) of the TdIVW window.
3. DQz represents the MAX ^{t}DQS2DQ in this example.
4. DQy represents the MIN ^{t}DQS2DQ in this example.

All of the timing terms in DQ to DQS_t are measured from the DQS_t/DQS_c to the center(midpoint) of the TdIVW window taken at the V^{dIVW_total} voltage levels centeredaround $V_{CENT\_DQ(pin\_mid)}$. In figure above, the timings at the pins are referenced with respectto all DQ signals center-aligned to the DRAM internal latch. The data-to-data offsetis defined as the difference between the MIN and MAX ^{t}DQS2DQ for a given component.

Figure 4-160: DQ ^{t}DIPW and SRIN_dIVW Definition for Each Input Pulse



Note:

1. SRIN_dIVW = V_{dIVW_total}/(^{t}r or ^{t}f) signal must be monotonic within ^{t}r and ^{t}f range.

Figure 4-161: DQ $V_{IHL(AC)}$ Definition (for Each Input Pulse)

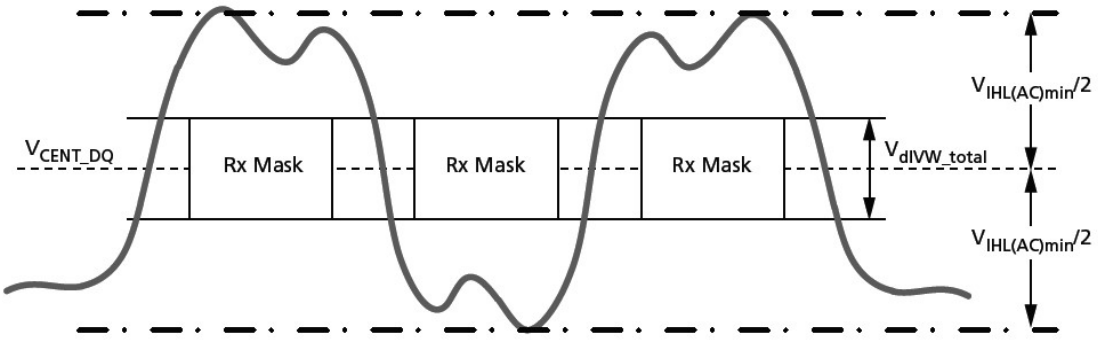


Table 4-192: DQs In Receive Mode

Note UI=^{t}CK(AVG)(MIN)/2

Symbol	Parameter	1600/1867		2133/2400		3200		Unit	Notes
		Min	Max	Min	Max	Min	Max		
V_{dIVW_total}	Rx mask voltage – peak-to-peak	–	140	–	140	–	140	mV	1, 2, 3
$V_{IHL(AC)}$	DQ AC input pulse ampli-tude peak-to-peak	180	–	180	–	180	–	mV	5, 7
SRIN_dIVW	Input slew rate over V_{dIVW_total}	1	7	1	7	1	7	V/ns	6

Notes:

1. Data Rx mask voltage and timing parameters are applied per pin and include the DRAMDQ-to-DQS voltage AC noiseimpact for frequencies >20 MHz with a maximum voltageof 45mV peak-to-peak at a fixed temperature on the package. Thevoltage supply noisemust comply to the component MIN/MAX DC operating conditions.
2. Rx mask voltage VdIVW_total (MAX) must be centered around $V_{CENT\_DQ(pin\_mid)}$.
3. Defined over the DQ internal V_{REF} range. The Rx mask at the pin must be within the internalV_{REF} DQ range irrespective ofthe input signal common mode.
4. Deterministic component of the total Rx mask voltage or timing. Parameter will be characterizedand guaranteed by design.
5. DQ-only input pulse amplitude into the receiver must meet or exceed $V_{IHL(AC)}$ at anypoint over the total UI. No timingrequirement above level. $V_{IHL(AC)}$ is the peak-to-peakvoltage centered around $V_{CENT\_DQ(pin\_mid)}$, such that$V_{IHL(AC)}$/2 (MIN)

must be met bothabove and below V_{CENT_DQ}.

6. Input slew rate over VdIVW mask centered at $V_{CENT\_DQ(pin\_mid)}$.
7. $V_{IHL(AC)}$ does not have to be met when no transitions are occurring.

4.56 Clock Specification

The specified clock jitter is a random jitter with Gaussian distribution. Input clocks violatingminimum or maximum values may result in device malfunction.

Table 4-193: Definitions and Calculations

Symbol	Description	Calculation	Notes
$^{t}CK(avg)$ and *n*CK	The average clock period across any consecutive 200-cycle window. Each clock period is calculated from rising clock edge to rising clock edge. Unit $^{t}CK(avg)$ represents the actual clock average $^{t}CK(avg)$ of the input clock under operation. Unit *n*CK represents one clock cycle of the input clock, counting from actual clock edge to actual clock edge. $^{t}CK(avg)$ can change no more than ±1% within a 100-clock-cycle window, provided that all jitter and timing specifications are met.	$^{t}CK(avg) = \left(\sum_{j=1}^{N} {}^{t}CK_j\right)/N$ Where N = 200	
$^{t}CK(abs)$	The absolute clock period, as measured from one rising clock edge to the next consecutive rising clock edge.		1
$^{t}CH(avg)$	The average HIGH pulse width, as calculated across any 200 consecutive HIGH pulses.	$^{t}CH(avg) = \left(\sum_{j=1}^{N} {}^{t}CH_j\right)/(N \times {}^{t}CK(avg))$ Where N = 200	
$^{t}CL(avg)$	The average LOW pulse width, as calculated across any 200 consecutive LOW pulses.	$^{t}CL(avg) = \left(\sum_{j=1}^{N} {}^{t}CL_j\right)/(N \times {}^{t}CK(avg))$ Where N = 200	
$^{t}JIT(per)$	The single-period jitter defined as the largest deviation of any signal ^{t}CK from $^{t}CK(avg)$.	$^{t}JIT(per) = \text{min/max of } \left({}^{t}CK_i - {}^{t}CK(avg)\right)$ Where i = 1 to 200	1
$^{t}JIT(per),act$	The actual clock jitter for a given system.		
$^{t}JIT(per),$ allowed	The specified clock period jitter allowance.		
$^{t}JIT(cc)$	The absolute difference in clock periods between two consecutive clock cycles. $^{t}JIT(cc)$ defines the cycle-to-cycle jitter.	$^{t}JIT(cc) = \text{max of } \left({}^{t}CK_{i+1} - {}^{t}CK_i\right)$	1
$^{t}ERR(nper)$	The cumulative error across *n* multiple consecutive cycles from $^{t}CK(avg)$.	$^{t}ERR(nper) = \left(\sum_{j=i}^{i+n-1} {}^{t}CK_j\right) - (n \times {}^{t}CK(avg))$	1
$^{t}ERR(nper),act$	The actual clock jitter over *n* cycles for a given system.		

Table 4-193: Definitions and Calculations (Continued)

Symbol	Description	Calculation	Notes
^{t}ERR(nper), allowed	The specified clock jitter allowance over *n* cycles.		
^{t}ERR(nper),min	The minimum ^{t}ERR(nper).	^{t}ERR(nper),min = (1 + 0.68LN(n)) × ^{t}JIT(per),min	2
^{t}ERR(nper),max	The maximum ^{t}ERR(nper).	^{t}ERR(nper),max = (1 + 0.68LN(n)) × ^{t}JIT(per),max	2
^{t}JIT(duty)	Defined with absolute and average specifications for ^{t}CH and ^{t}CL, respectively.	^{t}JIT(duty),min = MIN((^{t}CH(abs),min – ^{t}CH(avg),min), (^{t}CL(abs),min – ^{t}CL(avg),min)) × ^{t}CK(avg) ^{t}JIT(duty),max = MAX((^{t}CH(abs),max – ^{t}CH(avg),max), (^{t}CL(abs),max – ^{t}CL(avg),max)) × ^{t}CK(avg)	

Notes:
1. Not subject to production testing.
2. Using these equations, ^{t}ERR(nper) tables can be generated for each ^{t}JIT(per),act value.

^{t}CK(abs), ^{t}CH(abs), and ^{t}CL(abs)

These parameters are specified with their average values; however, the relationship betweenthe average timing and the absolute instantaneous timing (defined in the followingtable) is applicable at all times.

Table 4-194: ^{t}CK(abs), ^{t}CH(abs), and ^{t}CL(abs) Definitions

Parameter	Symbol	Minimum	Unit
Absolute clock period	^{t}CK(abs)	^{t}CK(avg),min + ^{t}JIT(per),min	ps1
Absolute clock HIGH pulse width	^{t}CH(abs)	^{t}CH(avg),min + ^{t}JIT(duty),min2/^{t}CK(avg)min	^{t}CK(avg)
Absolute clock LOW pulse width	^{t}CL(abs)	^{t}CL(avg),min + ^{t}JIT(duty),min2/^{t}CK(avg)min	^{t}CK(avg)

Notes:
1. ^{t}CK(avg),min is expressed in ps for this table.
2. ^{t}JIT(duty),min is a negative value.

4.57 Clock Period Jitter

LPDDR4 devices can tolerate some clock period jitter without core timing parameterderating. This section describes device timing requirements with clock period jitter(^{t}JIT(per)) in excess of the values found in the AC Timing table. Calculating cycle timederating and clock cycle derating are also described.

Clock Period Jitter Effects on Core Timing Parameters

Core timing parameters (^{t}RCD, ^{t}RP, ^{t}RTP, ^{t}WR, ^{t}WRA, ^{t}WTR, ^{t}RC, ^{t}RAS, ^{t}RRD, ^{t}FAW) extendacross multiple clock cycles. Clock period jitter impacts these parameters whenmeasured in numbers of clock cycles. Within the specification limits, the device is characterizedand verified to support ^{t}nPARAM = RU[^{t}PARAM/^{t}CK(avg)]. During device operationwhere clock jitter is outside specification limits, the number of clocks, or^{t}CK(avg), may need to be increased based on the values for each core timing parameter.

Cycle Time Derating for Core Timing Parameters

For a given number of clocks (^{t}nPARAM), when ^{t}CK(avg) and ^{t}ERR(tnPARAM),act exceed^{t}ERR(^{t}nPARAM),allowed, cycle time derating may be required for core timing parameters.

$$\text{CycleTimeDerating} = \max\left\{\left(\frac{{}^{t}\text{PARAM} + {}^{t}\text{ERR}({}^{t}\text{nPARAM}),\text{act} - {}^{t}\text{ERR}({}^{t}\text{nPARAM}),\text{allowed}}{{}^{t}\text{nPARAM}} - {}^{t}\text{CK(avg)}\right), 0\right\}$$

Cycle time derating analysis should be conducted for each core timing parameter. Theamount of cycle time derating required is the maximum of the cycle time deratings determinedfor each individual core timing parameter.

Clock Cycle Derating for Core Timing Parameters

For each core timing parameter and a given number of clocks (^{t}nPARAM), clock cyclederating should be specified with ^{t}JIT(per).

For a given number of clocks (^{t}nPARAM), when ^{t}CK(avg) plus (^{t}ERR(^{t}nPARAM),act) exceedthe supported cumulative ^{t}ERR(tnPARAM),allowed, derating is required. If theequation below results in a positive value for a core timing parameter (^{t}CORE), the requiredclock cycle derating will be that positive value (in clocks).

$$\text{ClockCycleDerating} = \text{RU}\left\{\frac{{}^{t}\text{PARAM} + {}^{t}\text{ERR}({}^{t}\text{nPARAM}),\text{act} - {}^{t}\text{ERR}({}^{t}\text{nPARAM}),\text{allowed}}{{}^{t}\text{CK(avg)}}\right\} - {}^{t}\text{nPARAM}$$

Cycle-time derating analysis should be conducted for each core timing parameter.

Clock Jitter Effects on Command/Address Timing Parameters

Command/address timing parameters (^{t}IS, ^{t}IH, ^{t}ISb, ^{t}IHb) are measured from a commandaddress signal (CS or CA[5:0]) transition edge to its respective clock signal (CK_t/CK_c) crossing. The specification values are not affected by the ^{t}JIT(per) applied, becausethe setup and hold times are relative to the clock signal crossing that latches thecommand/address. Regardless of clock jitter values, these values must be met.

Clock Jitter Effects on READ Timing Parameters

^{t}RPRE

When the device is operated with input clock jitter, ^{t}RPRE must be derated by the^{t}JIT(per),act,max of the input clock that exceeds ^{t}JIT(per),allowed,max. Output deratingsare relative to the input clock:

$${}^{t}\text{RPRE(min,derated)} = 0.9 - \left(\frac{{}^{t}\text{JIT(per)},\text{act},\text{max} - {}^{t}\text{JIT(per)},\text{allowed},\text{max}}{{}^{t}\text{CK(avg)}}\right)$$

For example, if the measured jitter into a LPDDR4 device has ^{t}CK(avg) = 625ps,^{t}JIT(per),act,min = –xx, and ^{t}JIT(per),act,max = +xx ps, then ^{t}RPRE,min,derated = 0.9 -(^{t}JIT(per),act,max - ^{t}JIT(per),allowed,max)/^{t}CK(avg) = 0.9 - (xx - xx)/xx = yy tCK(avg).

^{t}LZ(DQ), ^{t}HZ(DQ), ^{t}DQSCK, ^{t}LZ(DQS), ^{t}HZ(DQS)

These parameters are measured from a specific clock edge to a data signal transition(DMn or DQm, where: n = 0,1; and m = 0–15, and specified timings must be met withrespect to that clock edge. Therefore, they are not affected by ^{t}JIT(per).

^{t}QSH, ^{t}QSL

These parameters are affected by duty cycle jitter, represented by ^{t}CH(abs)min and^{t}CL(abs)min. These parameters determine the absolute data-valid window at the devicepin. The absolute minimum data-valid window at the device pin = MIN {(^{t}QSH(abs)min- ^{t}DQSQmax), (^{t}QSL(abs)min - ^{t}DQSQmax)}. This minimum data valid window must be met at the target frequency regardless of clock jitter.

^{t}RPST

^{t}RPST is affected by duty cycle jitter, represented by ^{t}CL(abs). Therefore, ^{t}RPST(abs)mincan be specified by ^{t}CL(abs)min. ^{t}RPST(abs)min = ^{t}CL(abs)min - 0.05 = ^{t}QSL(abs)min.

Clock Jitter Effects on WRITE Timing Parameters

^{t}DS, tDH

These parameters are measured from a data signal (DMIn or DQm, where n = 0, 1 and m= 0–15) transition edge to its respective data strobe signal (DQSn_t, DQSn_c: n = 0,1)crossing. The specification values are not affected by the amount of ^{t}JIT(per) applied,because the setup and hold times are relative to the data strobe signal crossing that latches the command/address. Regardless of clock jitter values, these values must bemet.

^{t}DSS, tDSH

These parameters are measured from a data signal (DQS_t, DQSn_c) crossing to its respectiveclock signal (CK_t, CK_c) crossing. When the device is operated with inputclock jitter, this parameter needs to be derated by the actual ^{t}JIT(per)act of the input clockin excess of the allowed period jitter ^{t}JIT(per)allowed.

^{t}DQSS

^{t}DQSS is measured from a data strobe signal (DQSn_t, DQSn_c) crossing to its respectiveclock signal (CK_t, CK_c) crossing. When the device is operated with input clock jitter,this parameter must be derated by the actual ^{t}JIT(per),act of the input clock in excessof ^{t}JIT(per)allowed.

$$t_{DQSS(min,derated)} = 0.75 - \left(\frac{t_{JIT(per),act,min} - t_{JIT(per),allowed,min}}{t_{CK(avg)}}\right)$$

$$t_{DQSS(max,derated)} = 1.25 - \left(\frac{t_{JIT(per),act,max} - t_{JIT(per),allowed,max}}{t_{CK(avg)}}\right)$$

For example, if the measured jitter into an LPDDR4 device has ^{t}CK(avg) = 625ps,
^{t}JIT(per),act,min = -xxps, and ^{t}JIT(per),act,max = +xx ps, then:
^{t}DQSS,(min,derated) = 0.75 - (-xx + yy)/625 = xxxx ^{t}CK(avg)
^{t}DQSS,(max,derated) = 1.25 - (xx – yy)/625 = xxxx ^{t}CK(avg)

4.58 LPDDR4 1.10V V_{DDQ}

This section defines LPDDR4 specifications to enable 1.10 V_{DDQ} operation of LPDDR4devices.

Power-Up and Initialization

To ensure proper functionality for power-up and reset initialization, default values forthe MR settings are provided in the table below.

Table 4-195: Mode Register Default Settings

Item	Mode Register Setting	Default Setting	Description
FSP-OP/WR	MR13 OP[7:6]	00b	FSP-OP/WR[0] are enabled
WLS	MR2 OP[6]	0b	WRITE latency set A is selected
WL	MR2 OP[5:3]	000b	WL = 4
RL	MR2 OP[2:0]	000b	RL = 6, *n*RTP = 8
nWR	MR1 OP[6:4]	000b	nWR = 6
DBI-WR/RD	MR3 OP[7:6]	00b	Write and read DBI are disabled
CA ODT	MR11 OP[6:4]	000b	CA ODT is disabled
DQ ODT	MR11 OP[2:0]	000b	DQ ODT is disabled
$V_{REF(CA)}$ setting	MR12 OP[6]	1b	$V_{REF(CA)}$ range[1] is enabled
$V_{REF(CA)}$ value	MR12 OP[5:0]	001101b	Range1: 27.2% of V_{DD2}
$V_{REF(DQ)}$ setting	MR14 OP[6]	1b	$V_{REF(DQ)}$ range[1] enabled
$V_{REF(DQ)}$ value	MR14 OP[5:0]	001101b	Range1: 27.2% of V_{DDQ}

Mode Register Definition

Mode register definitions are provided in the Mode Register Assignments table. In theaccess column of the table, R indicates read-only; W indicates write-only; R/W indicatesread- or write-capable or enabled. The MRR command is used to read from a register.
The MRW command is used to write to a register.

Table 4-196: Mode Register Assignments

Notes 1–5 apply to entire table

MR#	MA[5:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	00h	Device info	R	CATR	RFU	RFU	RZQI		RFU	Latency mode	REF
1	01h	Device feature 1	W	RD-PST	nWR (for AP)			RD-PRE	WR-PRE	BL	
2	02h	Device feature 2	W	WR Lev	WLS	WL			RL		
3	03h	I/O config-1	W	DBI-WR	DBI-RD	PDDS			PPRP	WR-PST	PU-CAL
4	04h	Refresh and training	R /W	TUF	Thermal offset		PPRE	SR abort	Refresh rate		
5	05h	Basic config-1	R	Manufacturer ID							
6	06h	Basic config-2	R	Revision ID1							
7	07h	Basic config-3	R	Revision ID2							
8	08h	Basic config-4	R	I/O width		Density				Type	
9	09h	Test mode	W	Vendor-specific test mode							
10	0Ah	I/O calibration	W	RFU							ZQ RST
11	0Bh	ODT	W	RFU	CA ODT			RFU	DQ ODT		
12	0Ch	VREF(CA)	R/W	RFU	VR_{CA}	$V_{REF(CA)}$					
13	0Dh	Register control	W	FSP-OP	FSP-WR	DMD	RRO	VRCG	VRO	RPT	CBT
14	0Eh	VREF(DQ)	R/W	RFU	VR_{DQ}	$V_{REF(DQ)}$					
15	0Fh	DQI-LB	W	Lower-byte invert register for DQ calibration							
16	10h	PASR_Bank	W	PASR bank mask							
17	11h	PASR_Seg	W	PASR segment mask							
18	12h	IT-LSB	R	DQS oscillator count – LSB							
19	13h	IT-MSB	R	DQS oscillator count – MSB							
20	14h	DQI-UB	W	Upper-byte invert register for DQ calibration							
21	15h	Vendor use	W	RFU							
22	16h	ODT feature 2	W	ODTD for x8_2ch	ODTD-CA	ODTE-CS	ODTE-CK	SoC ODT			
23	17h	DQS oscillator stop	W	DQS oscillator run-time setting							
24	18h	TRR control	R/W	TRR mode	TRR mode BAn			Unltd MAC	MAC value		
25	19h	PPR resources	R	B7	B6	B5	B4	B3	B2	B1	B0
26-29	1Ah~1Dh	–	–	Reserved for future use							

Table 4-196: Mode Register Assignments(Continued)

Notes 1–5 apply to entire table

MR#	MA[5:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
30	1Eh	Reserved for test	W	SDRAM will ignore							
31	1Fh	–	–	Reserved for future use							
32	20h	DQ calibration pattern A	W	See DQ calibration section							
33-38	21h≈26h	Do not use	–	Do not use							
39	27h	Reserved for test	W	SDRAM will ignore							
40	28h	DQ calibration pattern B	W	See DQ calibration section							
41-47	29h≈2Fh	Do not use	–	Do not use							
48-63	30h≈3Fh	Reserved	–	Reserved for future use							

Notes:

1. RFU bits must be set to 0 during MRW commands.
2. RFU bits are read as 0 during MRR commands.
3. All mode registers that are specified as RFU or write-only shall return undefined datawhen read via an MRR command.
4. RFU mode registers must not be written.
5. Writes to read-only registers will not affect the functionality of the device.

Table 4-197: MR0 Device Feature 0 (MA[5:0] = 00h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
CATR	RFU		RZQI		RFU	Latency mode	REF

Table 4-198: MR0 Device Feature 0 (MA[5:0] = 00h)

Register Information	Type	OP	Definition	Notes
Refresh mode	Read only	OP[0]	0b: Both legacy and modified refresh mode supported 1b: Only modified refresh mode supported	
Latency mode	Read only	OP[1]	0b: Device supports normal latency 1b: Device supports byte mode latency	5, 6
Built-in self-test for RZQ information	Read only	OP[4:3]	00b: RZQ self-test not supported 01b: ZQ may connect to V_{SSQ} or float 10b: ZQ may short to V_{DDQ} 11b: ZQ pin self-test completed, no error condition detected (ZQ may not connect to V_{SSQ}, float, or short to V_{DDQ})	1–4
CA terminating rank	Read only	OP[7]	0b: CA for this rank is not terminated 7 1b: CA for this rank is terminated	7

Notes:

1. RZQI MR value, if supported, will be valid after the following sequence:
   - Completion of MPC[ZQCAL START] command to either channel
   - Completion of MPC[ZQCAL LATCH] command to either channel then ^{t}ZQLAT is satisfied

   RZQI value will be lost after reset.
2. If ZQ is connected to V_{SSQ} to set default calibration, OP[4:3] must be set to 01b. If ZQ isnot connected to V_{SSQ}, eitherOP[4:3] = 01b or OP[4:3] = 10b might indicate a ZQ pin assemblyerror. It is recommended that the assembly error becorrected.
3. In the case of possible assembly error, the device will default to factory trim settings forRON, and will ignore ZQCALIBRATION commands. In either case, the device may notfunction as intended.
4. If the ZQ pin self-test returns OP[4:3] = 11b, the device has detected a resistor connectedto the ZQ pin. However, this resultcannot be used to validate the ZQ resistor value orthat the ZQ resistor meets the specified limits (that is, 240Ω±1%)
5. See byte mode addendum spec for byte mode latency details.
6. Byte mode latency for 2Ch. x16 device is only allowed when it is stacked in a same packagewith byte mode device.
7. CATR indicates whether CA for the rank will be terminated or not as a result of ODTCApad connection and MR22 OP[5]settings for x16 devices, MR22 OP[7:5] settings for bytemode devices.

Table 4-199: MR3 I/O Configuration 1 (MA[5:0] = 03h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DBI-WR	DBI-RD	PDDS			PPRP	WR-PST	PU-CAL

Table 4-200: MR3 Op-Code Bit Definitions

Feature	Type	OP	Definition	Notes
PU-CAL (Pull-up calibration point)	Write-only	OP[0]	0b: VDDQ/2.5 1b: VDDQ/3 (default)	1-4
WR-PST (WR postamble length)		OP[1]	0b: WR postamble = 0.5 × tCK (default) 1b: WR postamble = 1.5 × tCK	2, 3, 5
PPRP (Post-package repair protection)		OP[2]	0b: PPR protection disabled (default) 1b: PPR protection enabled	6
PDDS (Pull-down drive strength)		OP[5:3]	000b: RFU 001b: RZQ/1 010b: RZQ/2 011b: RZQ/3 100b: RZQ/4 101b: RZQ/5 110b:RZQ/6 (default) 111b: Reserved	1, 2, 3
DBI-RD (DBI-read enable)		OP[6]	0b: Disabled (default) 1b: Enabled	2, 3
DBI-WR (DBI-write enable)		OP[7]	0b: Disabled (default) 1b: Enabled	2, 3

Notes:

1. All values are typical. The actual value after calibration will be within the specified tolerancefor a given voltage andtemperature. Recalibration may be required as voltage andtemperature vary.
2. There are two physical registers assigned to each bit of this MR parameter, designatedset point 0 and set point 1. Only theregisters for the set point determined by the stateof the FSP-WR bit (MR13 OP[6]) will be written to with an MRW commandto this MRaddress, or read from with an MRR command to this address.
3. There are two physical registers assigned to each bit of this MR parameter, designatedset point 0 and set point 1.The devicewill operate only according to the values stored inthe registers for the active set point, for example, the set point determinedby the stateof the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point willbe determined by thestate of the FSP-OP bit (MR13 OP[7]). The values in the registersfor the inactive set point will be ignored by the device, andmay be changed withoutaffecting device operation.
4. For dual channel device, PU-CAL (MR3-OP[0]) must be set the same for both channels ona die. The SDRAM will read thevalue of only one register (Ch.A or Ch.B), vendor-specific,so both channels must be set the same.
5. 1.5 × tCK apply ≥ 1.6 GHz clock.
6. If MR3 OP[2] is set to 1b, PPR protection mode is enabled. The PPR protection bit is asticky bit and can only be set to 0b bya power on reset. MR4 OP[4] controls entry to PPRmode. If PPR protection is enabled then the DRAM will not allow writingof 1b to MR4OP[4].

Table 4-201: MR3 Op-Code Bit Definitions

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU	VR_{CA}	$V_{REF(CA)}$					

Table 4-202: MR12 Op-Code Bit Definitions

Feature	Type	OP	Data	Notes
$V_{REF(CA)}$ $V_{REF(CA)}$ settings	Read/ Write	OP[5:0]	000000b–110010b: See V_{REF} Settings Table All others: Reserved	1–3, 5, 6
VR_{CA} $V_{REF(CA)}$ range	Read/ Write	OP[6]	0b: $V_{REF(CA)}$ range[0] enabled 1b: $V_{REF(CA)}$ range[1] enabled (default)	1, 2, 4, 5, 6

Notes:

1. This register controls the $V_{REF(CA)}$ levels for frequency set point[1:0]. Values from eitherVR(ca)[0] or VR(ca)[1] may beselected by setting MR12 OP[6] appropriately.
2. A read to MR12 places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQwill be set to 0. See the MRROperation section.
3. A write to MR12 OP[5:0] sets the internal $V_{REF(CA)}$ level for FSP[0] when MR13 OP[6] = 0bor sets the internal $V_{REF(CA)}$level for FSP[1] when MR13 OP[6] = 1b. The time required for$V_{REF(CA)}$ to reach the set level depends on the step sizefrom the current level to the newlevel. See the $V_{REF(CA)}$ training section.
4. A write to MR12 OP[6] switches the device between two internal $V_{REF(CA)}$ ranges. Therange (range[0] or range[1]) mustbe selected when setting the $V_{REF(CA)}$ register. The value,once set, will be retained until overwritten or until the nextpower-on or resetevent.
5. There are two physical registers assigned to each bit of this MR parameter, designatedset point 0 and set point 1. Only theregisters for the set point determined by the stateof the FSP-WR bit (MR13 OP[6]) will be written to with an MRW commandto this MRaddress, or read from with an MRR command to this address.
6. There are two physical registers assigned to each bit of this MR parameter, designatedset point 0 and set point 1. Thedevice will operate only according to the values storedin the registers for the active set point, for example, the set pointdetermined by thestate of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive setpoint will be ignoredby the device, and may be changed without affecting device operation.

Table 4-203: Mode Register 14 (MA[5:0] = 0Eh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU	VR_{DQ}	$V_{REF(DQ)}$					

Table 4-204: MR14 Op-Code Bit Definition

Feature	Type	OP	Data	Notes
$V_{REF(DQ)}$ $V_{REF(DQ)}$ settings	Read/ Write	OP[5:0]	000000b–110010b: See V_{REF} Settings Table All others: Reserved	1–3, 5, 6
VR_{DQ} $V_{REF(DQ)}$ range		OP[6]	0b: $V_{REF(DQ)}$ range[0] enabled 1b: $V_{REF(DQ)}$ range[1] enabled (default)	1, 2, 4–6

Notes:

1. This register controls the $V_{REF(DQ)}$ levels for frequency set point[1:0]. Values from eitherVR_{DQ} [vendor defined] or VR_{DQ}[vendor defined] may be selected by setting OP[6] appropriately.
2. A read (MRR) to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits andunused DQ will be set to 0. Seethe MRR Operation section.
3. A write to OP[5:0] sets the internal $V_{REF(DQ)}$ level for FSP[0] when MR13 OP[6] = 0b, orsets FSP[1] when MR13 OP[6] =1b. The time required for $V_{REF(DQ)}$ to reach the set leveldepends on the step size from the current level to the new level.See the $V_{REF(DQ)}$ trainingsection.
4. A write to OP[6] switches the device between two internal $V_{REF(DQ)}$ ranges. The range(range[0] or range[1]) must beselected when setting the $V_{REF(DQ)}$ register. The value,once set, will be retained until overwritten, or until the nextpower-on or reset event.
5. There are two physical registers assigned to each bit of this MR parameter, designatedset point 0 and set point 1. Only theregisters for the set point determined by the stateof the FSP-WR bit (MR13 OP[6]) will be written to with an MRW commandto this MRaddress, or read from with an MRR command to this address.
6. There are two physical registers assigned to each bit of this MR parameter, designatedset point 0, and set point 1. Thedevice will operate only according to the values storedin the registers for the active set point, for example, the set pointdetermined by thestate of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive setpoint will be ignoredby the device, and may be changed without affecting device operation.

Table 4-205: V_{REF} Setting for Range[0] and Range[1]

Notes 1–3 apply to entire table

Function	OP	Range[0] Values		Range[1] Values	
		$V_{REF(CA)}$ (% of V_{DD2}) $V_{REF(DQ)}$ (% of V_{DDQ})		$V_{REF(CA)}$ (% of V_{DD2}) $V_{REF(DQ)}$ (% of V_{DDQ})	
V_{REF} setting for MR12 and MR14	OP[5:0]	000000b: 10.0%	011010b: 20.4%	000000b: 22.0%	011010b: 32.4%
		000001b: 10.4%	011011b: 20.8%	000001b: 22.4%	011011b: 32.8%
		000010b: 10.8%	011100b: 21.2%	000010b: 22.8%	011100b: 33.2%
		000011b: 11.2%	011101b: 21.6%	000011b: 23.2%	011101b: 33.6%
		000100b: 11.6%	011110b: 22.0%	000100b: 23.6%	011110b: 34.0%
		000101b: 12.0%	011111b: 22.4%	000101b: 24.0%	011111b: 34.4%
		000110b: 12.4%	100000b: 22.8%	000110b: 24.4%	100000b: 34.8%
		000111b: 12.8%	100001b: 23.2%	000111b: 24.8%	100001b: 35.2%
		001000b: 13.2%	100010b: 23.6%	001000b: 25.2%	100010b: 35.6%
		001001b: 13.6%	100011b: 24.0%	001001b: 25.6%	100011b: 36.0%
		001010b: 14.0%	100100b: 24.4%	001010b: 26.0%	100100b: 36.4%
		001011b: 14.4%	100101b: 24.8%	001011b: 26.4%	100101b: 36.8%
		001100b: 14.8%	100110b: 25.2%	001100b: 26.8%	100110b: 37.2%
		001101b: 15.2%	100111b: 25.6%	001101b: 27.2% de-fault	100111b: 37.6%
		001110b: 15.6%	101000b: 26.0%	001110b: 27.6%	101000b: 38.0%
		001111b: 16.0%	101001b: 26.4%	001111b: 28.0%	101001b: 38.4%
		010000b: 16.4%	101010b: 26.8%	010000b: 28.4%	101010b: 38.8%
		010001b: 16.8%	101011b: 27.2%	010001b: 28.8%	101011b: 39.2%
		010010b: 17.2%	101100b: 27.6%	010010b: 29.2%	101100b: 39.6%
		010011b: 17.6%	101101b: 28.0%	010011b: 29.6%	101101b: 40.0%
		010100b: 18.0%	101110b: 28.4%	010100b: 30.0%	101110b: 40.4%
		010101b: 18.4%	101111b: 28.8%	010101b: 30.4%	101111b: 40.8%
		010110b: 18.8%	110000b: 29.2%	010110b: 30.8%	110000b: 41.2%
		010111b: 19.2%	110001b: 29.6%	010111b: 31.2%	110001b: 41.6%
		011000b: 19.6%	110010b: 30.0%	011000b: 31.6%	110010b: 42.0%
		011001b: 20.0%	All others: Reserved	011001b: 32.0%	All others: Reserved

Notes:

1. These values may be used for MR14 OP[5:0] and MR12 OP[5:0] to set the $V_{REF(CA)}$ or$V_{REF(DQ)}$ levels in the device.
2. The range may be selected in each of the MR14 or MR12 registers by setting OP[6] appropriately.
3. Each of the MR14 or MR12 registers represents either FSP[0] or FSP[1]. Two frequency setpoints each for CA and DQ areprovided to allow for faster switching between terminatedand unterminated operation or between different high-frequencysettings, whichmay use different terminations values.

Table 4-206: Register Information (MA[5:0] = 16h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
ODTD for x8_2ch		ODTD-CA	ODTE-CS	ODTE-CK	SOC ODT		

Table 4-207: MR22 Register Information

Feature	Type	OP	Definition	Notes
SOC ODT (controller ODT value for V_{OH} calibration)	Write-only	OP[2:0]	000b: Disable (default) 001b: R_{ZQ}/1 010b: R_{ZQ} /2 011b: R_{ZQ} /3 100b: R_{ZQ} /4 101b: R_{ZQ} /5 110b: R_{ZQ} /6 111b: RFU	1, 2, 3
ODTE-CK (CK ODT enabled for non-terminating rank)	Write-only	OP[3]	0b: ODT-CK override disabled (default) 1b: ODT-CK override enabled	2, 3, 4, 6, 8
ODTE-CS (CS ODT enabled for non-terminating rank)	Write-only	OP[4]	0b: ODT-CS override disabled (default) 1b: ODT-CS override enabled	2, 3, 5, 6, 8
ODTD-CA (CA ODT termination disable)	Write-only	OP[5]	0b: CA ODT obeys ODT_CA bond pad (default) 1b: CA ODT disabled	2, 3, 6, 7, 8
ODTD for x8_2ch (Byte) mode	Write-only	OP[7:6]	See Byte Mode section	

Notes:

1. All values are typical.
2. There are two physical registers assigned to each bit of this MR parameter: designatedset point 0 and set point 1. Only theregisters for the set point determined by the stateof the FSP-WR bit (MR13 OP[6]) will be written to with an MRW commandor read fromwith an MRR command to this address.
3. There are two physical registers assigned to each bit of this MR parameter: designatedset point 0 and set point 1. Thedevice will operate only according to the values storedin the registers for the active set point determined by the state of theFSP-OP bit (MR13OP[7]). The values in the registers for the inactive set point will be ignored by the deviceand may bechanged without affecting device operation.
4. When OP[3] = 1 the CK signals will be terminated to the value set by MR11 OP[6:4] regardlessof the state of the ODT_CAbond pad. This overrides the ODT_CA bond pad forconfigurations where CA is shared by two or more devices but CK is not,enabling CK toterminate on all devices.
5. When OP[4] = 1 the CS signal will be terminated to the value set by MR11 OP[6:4] regardlessof the state of the ODT_CAbond pad. This overrides the ODT_CA bond pad forconfigurations where CA is shared by two or more devices but CS is not,enabling CS toterminate on all devices.
6. For system configurations where the CK, CS, and CA signals are shared between packages,the package design shouldprovide for the ODT_CA ball to be bonded on the systemboard outside of the memory package. This provides the necessarycontrol of theODT function for all die with shared command bus signals.
7. When OP[5] = 0, CA[5:0] will terminate when the ODT_CA bond pad is HIGH and MR11OP[6:4] is valid and disabletermination when ODT_CA is LOW or MR11 OP[6:4] is disabled.When OP[5] = 1, termination for CA[5:0] is disabledregardless of the state of theODT_CA bond pad or MR11 OP[6:4].
8. To ensure proper operation in a multi-rank configuration, when CA, CK or CS ODT is enabledvia MR11 OP[6:4] and also viaMR22 or ODT_CA pad setting, the rank providingODT will continue to terminate the command bus in all DRAM statesincluding Active,Self-refresh, Self-refresh Power-down, Active Power-down and Precharge Power-down.

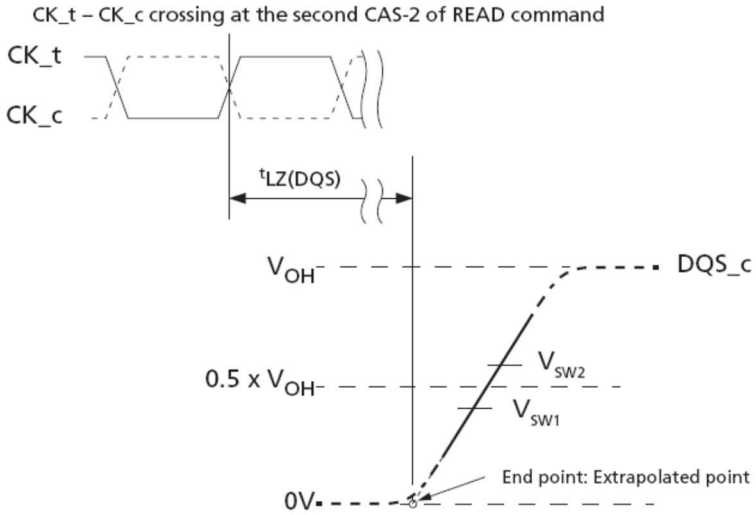
4.59 Burst READ Operation - LPDDR4 ATE Condition

tLZ(DQS), tLZ(DQ), tHZ(DQS), tHZ(DQ) Calculation

tHZ and tLZ transitions occur in the same time window as valid data transitions. Theseparameters are referenced to a specific voltage level that specifies when the device outputis no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS) andtLZ(DQ). This section shows a method to calculate the point when the device is no longerdriving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS) and tLZ(DQ), by measuringthe signal at two different voltages. The actual voltage measurement points arenot critical as long as the calculation is consistent. The parameters tLZ(DQS), tLZ(DQ),tHZ(DQS), and tHZ(DQ) are defined as single ended.

tLZ(DQS) and tHZ(DQS) Calculation for ATE (Automatic Test Equipment)

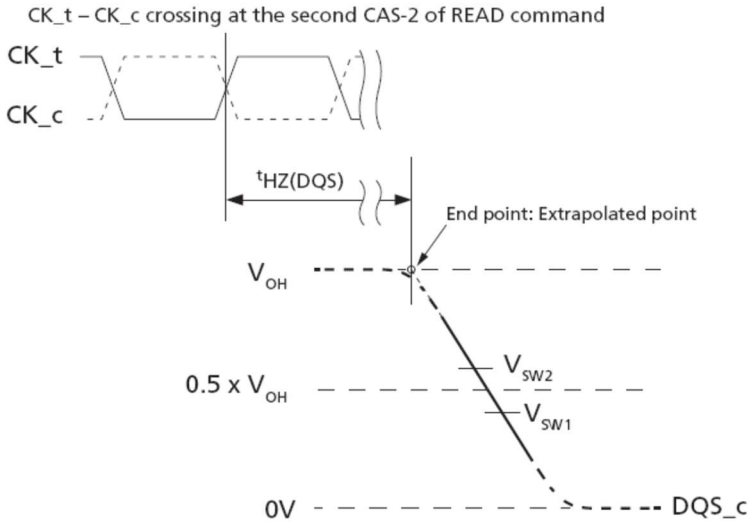
Figure 4-162: tLZ(DQS) Method for Calculating Transitions and Endpoint



Notes:

1. Conditions for calibration: Pull down driver R_{ON} = 40 ohms, $V_{OH} = V_{DDQ}/3$.
2. Termination condition for DQS_t and DQS_C = 50 ohms to V_{SSQ}.
3. The V_{OH} level depends on MR22 OP[2:0] and MR3 OP[0] settings as well as device tolerances.Use the actual V_{OH} valuefor tHZ and tLZ measurements.

Figure 4-163: tHZ(DQS) Method for Calculating Transitions and Endpoint



Notes:

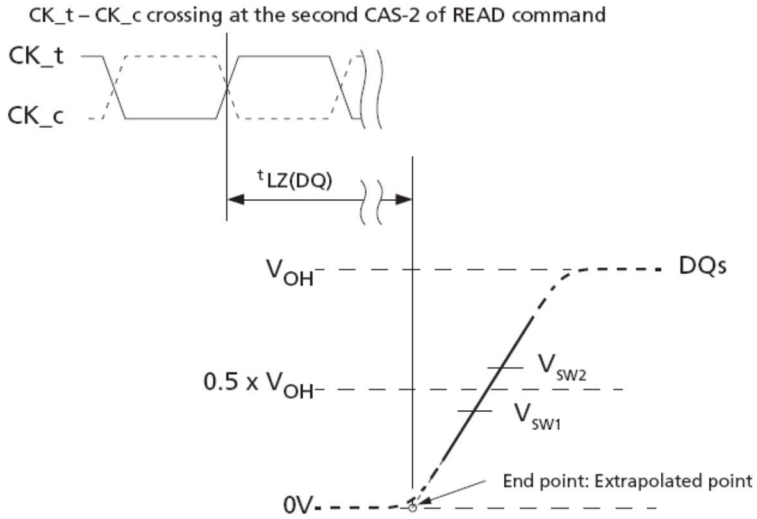
1. Conditions for calibration: Pull down driver R_{ON} = 40 ohms, $V_{OH} = V_{DDQ}/3$.
2. Termination condition for DQS_t and DQS_C = 50 ohms to V_{SSQ}.
3. The V_{OH} level depends on MR22 OP[2:0] and MR3 OP[0] settings as well as device tolerances.Use the actual V_{OH} valuefor tHZ and tLZ measurements.

Table 4-208: Reference Voltage for tLZ(DQS), tHZ(DQS) Timing Measurements

Measured Parameter	Measured Parameter Symbol	Vsw1	Vsw2	Unit
DQS_c Low-Z time from CK_t, CK_c	tLZ(DQS)	0.4 × V_{OH}	0.6 × V_{OH}	V
DQS_c High-Z time from CK_t, CK_c	tHZ(DQS)	0.4 × V_{OH}	0.6 × V_{OH}	

tLZ(DQ) and tHZ(DQ) Calculation for ATE (Automatic Test Equipment)

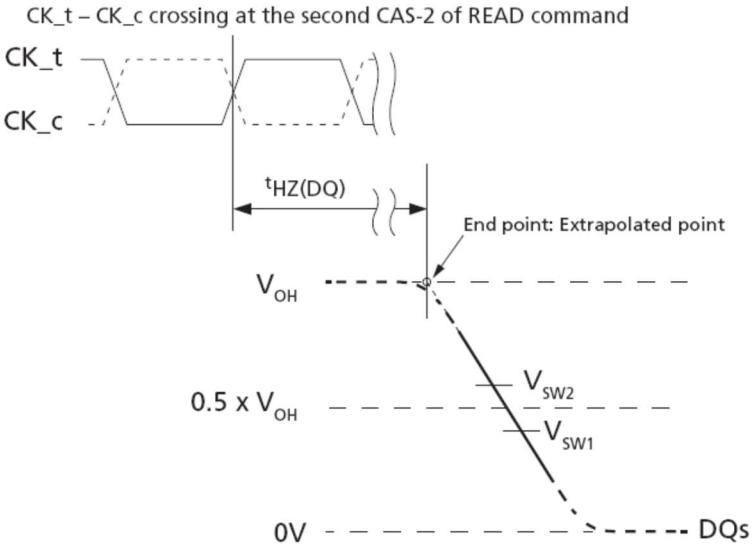
Figure 4-164: tLZ(DQ) Method for Calculating Transitions and Endpoint



Notes:

1. Conditions for calibration: Pull down driver R_{ON} = 40 ohms, $V_{OH} = V_{DDQ}/3$.
2. Termination condition for DQ and DMI = 50 ohms to V_{SSQ}.
3. The V_{OH} level depends on MR22 OP[2:0] and MR3 OP[0] settings as well as device tolerances.Use the actual V_{OH} valuefor tHZ and tLZ measurements.

Figure 4-165: tHZ(DQ) Method for Calculating Transitions and Endpoint



Notes:

1. Conditions for calibration: Pull down driver R_{ON} = 40 ohms, $V_{OH} = V_{DDQ}/3$.
2. Termination condition for DQ and DMI = 50 ohms to V_{SSQ}.
3. The V_{OH} level depends on MR22 OP[2:0] and MR3 OP[0] settings as well as device tolerances.Use the actual V_{OH} valuefor tHZ and tLZ measurements.

Table 4-209: Reference Voltage for ^{t}LZ(DQ), ^{t}HZ(DQ) Timing Measurements

Measured Parameter	Measured Parameter Symbol	Vsw1	Vsw2	Unit
DQ Low-Z time from CK_t, CK_c	^{t}LZ(DQ)	0.4 × V_{OH}	0.6 × V_{OH}	V
DQ High-Z time from CK_t, CK_c	^{t}HZ(DQ)	0.4 × V_{OH}	0.6 × V_{OH}	

4.60 VREF Specifications

Internal VREF(CA) Specifications

The device's internal $V_{REF(CA)}$ specification parameters are operating voltage range, stepsize, V_{REF} step time,V_{REF} full-range step time, and V_{REF} valid level.

The voltage operating range specifies the minimum required V_{REF} setting range forLPDDR4 devices. The minimum range is defined by $V_{REF,max}$ and $V_{REF,min}$.

Table 4-210: Internal $V_{REF(CA)}$ Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes
$V_{REF(CA),max\_r0}$	$V_{REF(CA)}$ range-0 MAX operat-ing point	–	–	30%	V_{DD2}	1, 11
$V_{REF(CA),min\_r0}$	$V_{REF(CA)}$ range-0 MIN operat-ing point	10%	–	–	V_{DD2}	1, 11
$VR_{EF(CA),max\_r1}$	$V_{REF(CA)}$ range-1 MAX operat-ing point	–	–	42%	V_{DD2}	1, 11
$V_{REF(CA),min\_r1}$	$V_{REF(CA)}$ range-1 MIN operat-ing point	22%	–	–	V_{DD2}	1, 11
$V_{REF(CA),step}$	$V_{REF(CA)}$ step size	0.30%	0.40%	0.50%	V_{DD2}	2
$V_{REF(CA),set\_tol}$	$V_{REF(CA)}$ set tolerance	–1.00%	0.00%	1%	V_{DD2}	3, 4, 6
	$V_{REF(CA)}$ set tolerance	-0.10%	0.00%	0.10%	V_{DD2}	3, 5, 7
^{t}VREF_TIME-SHORT	$V_{REF(CA)}$ step time	–	–	100	ns	8
^{t}VREF_TIME-MIDDLE		–	–	200	ns	12
^{t}VREF_TIME-LONG		–	–	250	ns	9
$^{t}V_{REF\_time\_weak}$		–	–	1	ms	13, 14
$V_{REF(CA)\_val\_tol}$	$V_{REF(CA)}$ valid tolerance	–0.10%	0.00%	0.10%	V_{DD2}	10

Notes:

1. $V_{REF(CA)}$ DC voltage referenced to $V_{DD2(DC)}$.
2. $V_{REF(CA)}$ step size increment/decrement range. $V_{REF(CA)}$ at DC level.
3. $V_{REF(CA),new} = V_{REF(CA),old} + n \times V_{REF(CA),step}$; n = number of steps; if increment, use "+"; ifdecrement, use "–".
4. The minimum value of $V_{REF(CA)}$ setting tolerance = $V_{REF(CA),new}$ - 1.0% × V_{DD2}. The maximumvalue of $V_{REF(CA)}$ setting tolerance = $V_{REF(CA),new}$ + 1.0% × V_{DD2}. For n > 4.
5. The minimum value of $V_{REF(CA)}$ setting tolerance = $V_{REF(CA),new}$ - 0.10% × V_{DD2}. The maximumvalue of $V_{REF(CA)}$ setting tolerance = $V_{REF(CA),new}$ + 0.10% × V_{DD2}. Forn < 4.
6. Measured by recording the minimum and maximum values of the $V_{REF(CA)}$ output overthe range, drawing a straight linebetween those points and comparing all other$V_{REF(CA)}$ output settings to that line.
7. Measured by recording the minimum and maximum values of the $V_{REF(CA)}$ output acrossfour consecutive steps (n = 4),drawing a straight line between those points and comparingall other $V_{REF(CA)}$ output settings to that line.

8.Time from MRW command to increment or decrement one step size for $V_{REF(CA)}$.
9.Time from MRW command to increment or decrement VREF,min to VREF,max or $V_{REF,max}$ to$V_{REF,min}$ change acrossthe $V_{REF(CA)}$ range in V_{REF} voltage.
10.Only applicable for DRAM component level test/characterization purposes. Not applicablefor normal mode of operation.V_{REF} valid is to qualify the step times which will becharacterized at the component level.
11.DRAM range-0 or range-1 set by MR12 OP[6].
12.Time from MRW command to increment or decrement more than one step size up to afull range of V_{REF} voltage within thesame $V_{REF(CA)}$ range.
13.Applies when VRCG high current mode is not enabled, specified by MR13 [OP3] = 0b.
14.$^{t}V_{REF}$_time_weak covers all $V_{REF(CA)}$ range and value change conditions are applied to$^{t}V_{REF}$_TIME-SHORT/MIDDLE/LONG.

Internal VREF(DQ) Specifications

The device's internal VREF(DQ) specification parameters are operating voltage range, stepsize, VREF step tolerance, VREF step time and VREF valid level.

The voltage operating range specifies the minimum required VREF setting range forLPDDR4 devices. The minimum range is defined by VREF,max and VREF,min.

Table 4-211: Internal $V_{REF(DQ)}$ Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes
$V_{REF(DQ),max\_r0}$	V_{REF} MAX operating point Range-0	–	–	30%	V_{DDQ}	1, 11
$V_{REF(DQ),min\_r0}$	V_{REF} MIN operating point Range-0	10%	–	–	V_{DDQ}	1, 11
$V_{REF(DQ),max\_r1}$	V_{REF} MAX operating point Range-1	–	–	42%	V_{DDQ}	1, 11
$V_{REF(DQ),min\_r1}$	V_{REF} MIN operating point Range-1	22%	–	–	V_{DDQ}	1, 11
$V_{REF(DQ),step}$	$V_{REF(DQ)}$ step size	0.30%	0.40%	0.50%	V_{DDQ}	2
$V_{REF(DQ),set\_tol}$	$V_{REF(DQ)}$ set tolerance	–1.00%	0.00%	1.00%	V_{DDQ}	3, 4, 6
		–0.10%	0.00%	0.10%	V_{DDQ}	3, 5, 7
$^{t}V_{REF}$_TIME-SHORT	$V_{REF(DQ)}$ step time	–	–	100	ns	8
$^{t}V_{REF}$_TIME-MIDDLE		–	–	200	ns	12
$^{t}V_{REF}$_TIME-LONG		–	–	250	ns	9
$^{t}V_{REF\_time\_weak}$		–	–	1	ms	13, 14
$V_{REF(DQ),val\_tol}$	$V_{REF(DQ)}$ valid tolerance	–0.10%	0.00%	0.10%	V_{DDQ}	10

Notes:
1. $V_{REF(DQ)}$ DC voltage referenced to $V_{DDQ(DC)}$.
2. $V_{REF(DQ)}$ step size increment/decrement range. $V_{REF(DQ)}$ at DC level.
3. $V_{REF(DQ),new} = V_{REF(DQ),old} + n \times V_{REF(DQ),step}$; n = number of steps; if increment, use "+"; ifdecrement, use "–".
4. The minimum value of $V_{REF(DQ)}$ setting tolerance = $V_{REF(DQ),new}$ - 1.0% × V_{DDQ}. The maximumvalue of $V_{REF(DQ)}$ setting tolerance = $V_{REF(DQ),new}$ + 1.0% × V_{DDQ}. For n > 4.
5. The minimum value of $V_{REF(DQ)}$setting tolerance = $V_{REF(DQ),new}$ - 0.10% × V_{DDQ}. The maximumvalue of $V_{REF(DQ)}$ setting tolerance = $V_{REF(DQ),new}$ + 0.10% × V_{DDQ}. For n < 4.
6. Measured by recording the minimum and maximum values of the $V_{REF(DQ)}$ output overthe range, drawing a straight linebetween those points and comparing all other$V_{REF(DQ)}$ output settings to that line.
7. Measured by recording the minimum and maximum values of the $V_{REF(DQ)}$ output acrossfour consecutive steps (n = 4),drawing a straight line between those points and comparingall other $V_{REF(DQ)}$ output settings to that line.
8. Time from MRW command to increment or decrement one step size for $V_{REF(DQ)}$.
9. Time from MRW command to increment or decrement $V_{REF,min}$ to $V_{REF,max}$ or $V_{REF,max}$ to$V_{REF,min}$ change across the $V_{REF(DQ)}$Range in $V_{REF(DQ)}$ Voltage.
10. Only applicable for DRAM component level test/characterization purposes. Not applicablefor normal mode of operation. V_{REF} valid is to qualify the step times which will becharacterized at the component level.
11. DRAM range-0 or range-1 set by MR14 OP[6].

12. Time from MRW command to increment or decrement more than one step size up to afull range of V_{REF} voltage within thesame $V_{REF(DQ)}$ range.
13. Applies when VRCG high current mode is not enabled, specified by MR13 [OP3] = 0.
14. $^{t}V_{REF\_time\_weak}$ covers all $V_{REF(DQ)}$ Range and Value change conditions are applied to$^{t}V_{REF}$_TIME-SHOR/MIDDLE/LONG.

4.61 Command Definitions and Timing Diagrams
Pull Up/Pull Down Driver Characteristics and Calibration

Table 4-212: Pull-Down Driver Characteristics – ZQ Calibration

R_{ONPD},nom	Register	Min	Nom	Max	Unit
40 ohms	R_{ON40PD}	0.9	1	1.1	R_{ZQ}/6
48 ohms	R_{ON48PD}	0.9	1	1.1	R_{ZQ}/5
60 ohms	R_{ON60PD}	0.9	1	1.1	R_{ZQ}/4
80 ohms	R_{ON80PD}	0.9	1	1.1	R_{ZQ}/3
120 ohms	$R_{ON120PD}$	0.9	1	1.1	R_{ZQ}/2
240 ohms	$R_{ON240PD}$	0.9	1	1.1	R_{ZQ}/1

Note:
1. All value are after ZQ calibration. Without ZQ calibration, R_{ONPD} values are ±30%.

Table 4-213: Pull-Up Characteristics – ZQ Calibration

V_{OHPU},nom	V_{OH},nom	Min	Nom	Max	Unit
V_{DDQ}/2.5	440	0.9	1	1.1	V_{OH},nom
V_{DDQ}/3	367	0.9	1	1.1	V_{OH},nom

Notes:
1. All value are after ZQ calibration. Without ZQ calibration, R_{ONPD} values are ±30%.
2. V_{OH},nom (mV) values are based on a nominal V_{DDQ} = 1.1V.

Table 4-214: Terminated Valid Calibration Points

V_{OHPU}	ODT Value					
	240	120	80	60	48	40
V_{DDQ}/2.5	Valid	Valid	Valid	DNU	DNU	DNU
V_{DDQ}/3	Valid	Valid	Valid	Valid	Valid	Valid

Notes:
1. Once the output is calibrated for a given $V_{OH(nom)}$ calibration point, the ODT value maybe changed without recalibration.
2. If the $V_{OH(nom)}$ calibration point is changed, then recalibration is required.
3. DNU = Do not use.

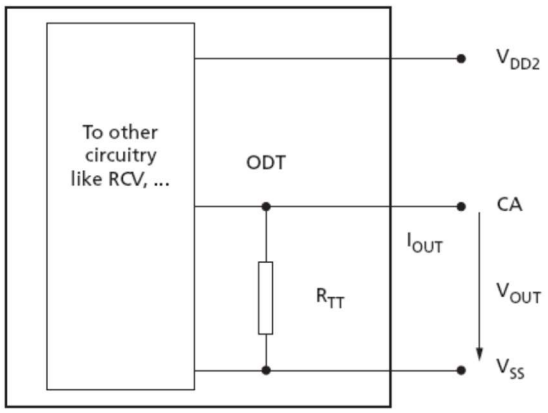
On-Die Termination for the Command/Address Bus

The on-die termination (ODT) feature allows the device to turn on/off termination resistancefor CK_t, CK_c, CS, and CA[5:0] signals without the ODT control pin. The ODTfeature is designed to improve signal integrity of the memory channel by allowing theDRAM controller to turn on and off termination resistance for any target DRAM devices via the mode register setting.

A simple functional representation of the DRAM ODT feature is shown below.

Figure 4-166: ODT for CA

$$R_{TT} = \frac{V_{OUT}}{|I_{OUT}|}$$



ODT Mode Register and ODT State Table

ODT termination values are set and enabled via MR11. The CA bus (CK_t, CK_c, CS,CA[5:0]) ODT resistance values are set by MR11 OP[6:4]. The default state for the CA isODT disabled.

ODT is applied on the CA bus to the CK_t, CK_c, CS, and CA signals. The CA ODT of thedevice is designed to enable one rank to terminate the entire command bus in a multiranksystem, so only one termination load will be present even if multiple devices aresharing the command signals. For this reason, CA ODT remains on, even when the deviceis in the power-down or self refresh power-down state.

The die has a bond pad (ODT_CA) for multirank operations. When the ODT_CA pad isLOW, the die will not terminate the CA bus regardless of the state of the mode registerCA ODT bits (MR11 OP[6:4]). If, however, the ODT_CA bond pad is HIGH and the moderegister CA ODT bits are enabled, the die will terminate the CA bus with the ODT valuesfound in MR11 OP[6:4]. In a multirank system, the terminating rank should be trainedfirst, followed by the non-terminating rank(s).

Table 4-215: Command Bus ODT State

CA ODTMR11[6:4	ODT_CA Bond Pad	ODTD-CAMR2 2 OP[5]	ODTE-CK MR22 OP[3]	ODTE-CS MR22 OP[4]	ODT State for CA	ODT State for CK	ODT State for CS
Disabled[1]	Valid[2]	Valid[3]	Valid[3]	Valid[3]	Off	Off	Off
Valid[3]	0	Valid[3]	0	0	Off	Off	Off
Valid[3]	0	Valid[3]	0	1	Off	Off	On
Valid[3]	0	Valid[3]	1	0	Off	On	Off
Valid[3]	0	Valid[3]	1	1	Off	On	On
Valid[3]	1	0	Valid[3]	Valid[3]	On	On	On
Valid[3]	1	1	Valid[3]	Valid[3]	Off	On	On

Notes:
1. Default value.
2. Valid = H or L (a defined logic level)
3. Valid = 0 or 1.
4. The state of ODT_CA is not changed when the device enters power-down mode. Thismaintains termination for alternateranks in multirank systems.

ODT Mode Register and ODT Characteristics

Table 4-216: ODT DC Electrical Characteristics for Command/Address Bus – up to 3200 Mbps

R_{ZQ} = 240Ω±1% over entire operating range after calibration

MR11 OP[6:4]	R_{TT}	V_{OUT}	Min	Nom	Max	Unit	Notes
001b	240Ω	$V_{OL(DC)}$ = 0.1 × V_{DD2}	0.8	1	1.1	R_{ZQ}/1	1, 2
		$V_{OM(DC)}$ = 0.33 × V_{DD2}	0.9	1	1.1		
		$V_{OH(DC)}$ = 0.5 × V_{DD2}	0.9	1	1.2		
010b	120Ω	$V_{OL(DC)}$ = 0.1 × V_{DD2}	0.8	1	1.1	R_{ZQ}/2	1, 2
		$V_{OM(DC)}$ = 0.33 × V_{DD2}	0.9	1	1.1		
		$V_{OH(DC)}$ = 0.5 × V_{DD2}	0.9	1	1.2		
011b	80Ω	$V_{OL(DC)}$ = 0.1 × V_{DD2}	0.8	1	1.1	R_{ZQ}/3	1, 2
		$V_{OM(DC)}$ = 0.33 × V_{DD2}	0.9	1	1.1		
		$V_{OH(DC)}$ = 0.5 × V_{DD2}	0.9	1	1.2		
100b	60Ω	$V_{OL(DC)}$ = 0.1 × V_{DD2}	0.8	1	1.1	R_{ZQ}/4	1, 2
		$V_{OM(DC)}$ = 0.33 × V_{DD2}	0.9	1	1.1		
		$V_{OH(DC)}$ = 0.5 × V_{DD2}	0.9	1	1.2		
101b	48Ω	$V_{OL(DC)}$ = 0.1 × V_{DD2}	0.8	1	1.1	R_{ZQ}/5	1, 2
		$V_{OM(DC)}$ = 0.33 × V_{DD2}	0.9	1	1.1		
		$V_{OH(DC)}$ = 0.5 × V_{DD2}	0.9	1	1.2		
110b	40Ω	$V_{OL(DC)}$ = 0.1 × V_{DD2}	0.8	1	1.1	R_{ZQ}/6	1, 2
		$V_{OM(DC)}$ = 0.33 × V_{DD2}	0.9	1	1.1		
		$V_{OH(DC)}$ = 0.5 × V_{DD2}	0.9	1	1.2		
Mismatch, CA -CA within clock group		0.33 × V_{DD2}	–	–	2	%	1, 2, 3

Notes:

1. The tolerance limits are specified after calibration with stable temperature and voltage.To understand the behavior of thetolerance limits when voltage or temperaturechanges after calibration, see the section on voltage and temperaturesensitivity.
2. Pull-down ODT resistors are recommended to be calibrated at 0.33 × V_{DD2}. Other calibrationpoints may be required toachieve the linearity specification shown above, forexample, calibration at 0.5 × V_{DD2} and 0.1 × V_{DD2}.
3. CA to CA mismatch within clock group variation for a given component including CK_t,CK_c ,and CS (characterized).

$$\text{CA-to-CA mismatch} = \frac{R_{ODT}(MAX) - R_{ODT}(MIN)}{R_{ODT}(AVG)}$$

Table 4-217: ODT DC Electrical Characteristics for Command/Address Bus – Beyond 3200 Mbps

R_{ZQ} = 240Ω±1% over entire operating range after calibration

MR11 OP[6:4]	R_{TT}	V_{OUT}	Min	Nom	Max	Unit	Notes
001b	240Ω	$V_{OL(DC)}$ = 0.1 × V_{DD2}	0.8	1	1.1	R_{ZQ}/1	1, 2
		$V_{OM(DC)}$ = 0.33 × V_{DD2}	0.9	1	1.1		
		$V_{OH(DC)}$ = 0.5 × V_{DD2}	0.9	1	1.3		
010b	120Ω	$V_{OL(DC)}$ = 0.1 × V_{DD2}	0.8	1	1.1	R_{ZQ}/2	1, 2
		$V_{OM(DC)}$ = 0.33 × V_{DD2}	0.9	1	1.1		
		$V_{OH(DC)}$ = 0.5 × V_{DD2}	0.9	1	1.3		
011b	80Ω	$V_{OL(DC)}$ = 0.1 × V_{DD2}	0.8	1	1.1	R_{ZQ}/3	1, 2
		$V_{OM(DC)}$ = 0.33 × V_{DD2}	0.9	1	1.1		
		$V_{OH(DC)}$ = 0.5 × V_{DD2}	0.9	1	1.3		
100b	60Ω	$V_{OL(DC)}$ = 0.1 × V_{DD2}	0.8	1	1.1	R_{ZQ}/4	1, 2
		$V_{OM(DC)}$ = 0.33 × V_{DD2}	0.9	1	1.1		
		$V_{OH(DC)}$ = 0.5 × V_{DD2}	0.9	1	1.3		
101b	48Ω	$V_{OL(DC)}$ = 0.1 × V_{DD2}	0.8	1	1.1	R_{ZQ}/5	1, 2
		$V_{OM(DC)}$ = 0.33 × V_{DD2}	0.9	1	1.1		
		$V_{OH(DC)}$ = 0.5 × V_{DD2}	0.9	1	1.3		
110b	40Ω	$V_{OL(DC)}$ = 0.1 × V_{DD2}	0.8	1	1.1	R_{ZQ}/6	1, 2
		$V_{OM(DC)}$ = 0.33 × V_{DD2}	0.9	1	1.1		
		$V_{OH(DC)}$ = 0.5 × V_{DD2}	0.9	1	1.3		
Mismatch, CA -CA within clock group		0.33 × V_{DD2}	–	–	2	%	1, 2, 3

Notes:

1. The tolerance limits are specified after calibration with stable temperature and voltage.To understand the behavior of thetolerance limits when voltage or temperaturechanges after calibration, see the section on voltage and temperaturesensitivity.
2. Pull-down ODT resistors are recommended to be calibrated at 0.33 × V_{DD2}. Other calibrationpoints may be required toachieve the linearity specification shown above, e.g.calibration at 0.5 × V_{DD2} and 0.1 × V_{DD2}.
3. CA to CA mismatch within clock group variation for a given component including CK_t,CK_c ,and CS (characterized).

$$\text{CA-to-CA mismatch} = \frac{R_{ODT}(MAX) - R_{ODT}(MIN)}{R_{ODT}(AVG)}$$

DQ On-Die Termination

On-die termination (ODT) is a feature that allows the device to turn on/off terminationresistance for each DQ, DQS, and DMI signal without the ODT control pin. The ODTfeature is designed to improve signal integrity of the memory channel by allowing theDRAM controller to turn on and off termination resistance for any target DRAM devices during WRITE or MASK WRITE operation.

The ODT feature is off and cannot be supported in power-down and self refresh modes.

The switch is enabled by the internal ODT control logic, which uses the WRITE-1 orMASK WRITE-1 command and other mode register control information. The value ofRTT is determined by the MR bits.

$$R_{TT} = \frac{V_{OUT}}{|I_{OUT}|}$$

Figure 167: Functional Representation of DQ ODT

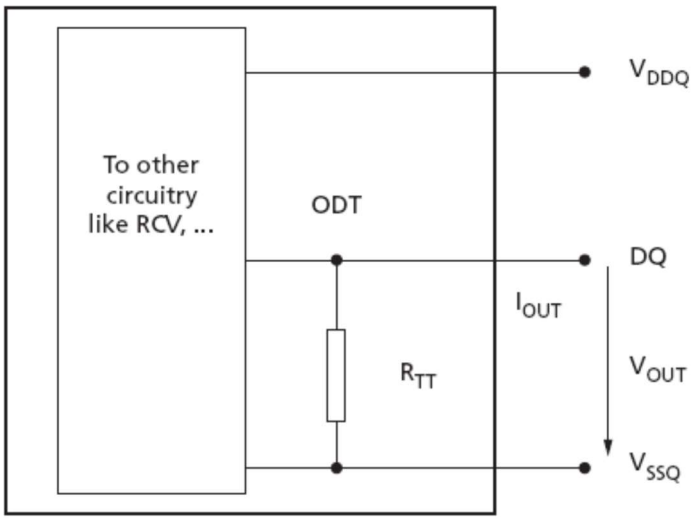


Table 4-218: ODT DC Electrical Characteristics for DQ Bus– up to 3200 Mbps

R_{ZQ} = 240Ω±1% over entire operating range after calibration

MR11 OP[2:0]	R_{TT}	V_{OUT}	Min	Nom	Max	Unit	Notes
001b	240Ω	$V_{OL(DC)}$ = 0.1 × V_{DDQ}	0.8	1	1.1	R_{ZQ}/1	1, 2
		$V_{OM(DC)}$ = 0.33 × V_{DDQ}	0.9	1	1.1		
		$V_{OH(DC)}$ = 0.5 × V_{DDQ}	0.9	1	1.2		
010b	120Ω	$V_{OL(DC)}$ = 0.1 × V_{DDQ}	0.8	1	1.1	R_{ZQ}/2	1, 2
		$V_{OM(DC)}$ = 0.33 × V_{DDQ}	0.9	1	1.1		
		$V_{OH(DC)}$ = 0.5 × V_{DDQ}	0.9	1	1.2		
011b	800Ω	$V_{OL(DC)}$ = 0.1 × V_{DDQ}	0.8	1	1.1	R_{ZQ}/3	1, 2
		$V_{OM(DC)}$ = 0.33 × V_{DDQ}	0.9	1	1.1		
		$V_{OH(DC)}$ = 0.5 × V_{DDQ}	0.9	1	1.2		
100b	600Ω	$V_{OL(DC)}$ = 0.1 × V_{DDQ}	0.8	1	1.1	R_{ZQ}/4	1, 2
		$V_{OM(DC)}$ = 0.33 × V_{DDQ}	0.9	1	1.1		
		$V_{OH(DC)}$ = 0.5 × V_{DDQ}	0.9	1	1.2		
101b	48Ω	$V_{OL(DC)}$ = 0.1 × V_{DDQ}	0.8	1	1.1	R_{ZQ}/5	1, 2
		$V_{OM(DC)}$ = 0.33 × V_{DDQ}	0.9	1	1.1		
		$V_{OH(DC)}$ = 0.5 × V_{DDQ}	0.9	1	1.2		
110b	40Ω	$V_{OL(DC)}$ = 0.1 × V_{DDQ}	0.8	1	1.1	R_{ZQ}/6	1, 2
		$V_{OM(DC)}$ = 0.33 × V_{DDQ}	0.9	1	1.1		
		$V_{OH(DC)}$ = 0.5 × V_{DDQ}	0.9	1	1.2		
Mismatch error, DQ-to-DQ with-in a channel		0.33 × V_{DDQ}	–	–	2	%	1, 2, 3

Notes:

1. The ODT tolerance limits are specified after calibration with stable temperature andvoltage. To understand the behavior ofthe tolerance limits when voltage or temperaturechanges after calibration, see the following section on voltage andtemperaturesensitivity.
2. Pull-down ODT resistors are recommended to be calibrated at 0.33 × V_{DDQ}. Other calibrationpoints may be required toachieve the linearity specification shown above, (forexample, calibration at 0.5 × V_{DDQ} and –0.1 × V_{DDQ}.
3. DQ-to-DQ mismatch within byte variation for a given component, including DQS (characterized).

$$\text{DQ-to-DQ mismatch} = \frac{R_{ODT}(MAX) - R_{ODT}(MIN)}{R_{ODT}(AVG)}$$

Table 4-219: ODT DC Electrical Characteristics for DQ Bus – Beyond 3200 Mbps

R_{ZQ} = 240Ω±1% over entire operating range after calibration

MR11	R_{TT}	V_{OUT}	Min	Nom	Max	Unit	Notes
001b	240Ω	$V_{OL(DC)}$ = 0.1 × V_{DDQ}	0.8	1	1.1	R_{ZQ}/1	1, 2
		$V_{OM(DC)}$ = 0.33 × V_{DDQ}	0.9	1	1.1		
		$V_{OH(DC)}$ = 0.5 × V_{DDQ}	0.9	1	1.3		
010b	120Ω	$V_{OL(DC)}$ = 0.1 × V_{DDQ}	0.8	1	1.1	R_{ZQ}/2	1, 2
		$V_{OM(DC)}$ = 0.33 × V_{DDQ}	0.9	1	1.1		
		$V_{OH(DC)}$ = 0.5 × V_{DDQ}	0.9	1	1.3		
011b	800Ω	$V_{OL(DC)}$ = 0.1 × V_{DDQ}	0.8	1	1.1	R_{ZQ}/3	1, 2
		$V_{OM(DC)}$ = 0.33 × V_{DDQ}	0.9	1	1.1		
		$V_{OH(DC)}$ = 0.5 × V_{DDQ}	0.9	1	1.3		
100b	600Ω	$V_{OL(DC)}$ = 0.1 × V_{DDQ}	0.8	1	1.1	R_{ZQ}/4	1, 2
		$V_{OM(DC)}$ = 0.33 × V_{DDQ}	0.9	1	1.1		
		$V_{OH(DC)}$ = 0.5 × V_{DDQ}	0.9	1	1.3		
101b	48Ω	$V_{OL(DC)}$ = 0.1 × V_{DDQ}	0.8	1	1.1	R_{ZQ}/5	1, 2
		$V_{OM(DC)}$ = 0.33 × V_{DDQ}	0.9	1	1.1		
		$V_{OH(DC)}$ = 0.5 × V_{DDQ}	0.9	1	1.3		
110b	40Ω	$V_{OL(DC)}$ = 0.1 × V_{DDQ}	0.8	1	1.1	R_{ZQ}/6	1, 2
		$V_{OM(DC)}$ = 0.33 × V_{DDQ}	0.9	1	1.1		
		$V_{OH(DC)}$ = 0.5 × V_{DDQ}	0.9	1	1.3		
Mismatch error, DQ-to-DQ with-in a channel		0.33 × V_{DDQ}	–	–	2	%	1, 2, 3

Notes:

1. The ODT tolerance limits are specified after calibration with stable temperature andvoltage. To understand the behavior ofthe tolerance limits when voltage or temperaturechanges after calibration, see the following section on voltage andtemperaturesensitivity.
2. Pull-down ODT resistors are recommended to be calibrated at 0.33 × V_{DDQ}. Other calibrationpoints may be required toachieve the linearity specification shown above, forexample, calibration at 0.5 × V_{DDQ} and –0.1 × V_{DDQ}.
3. DQ-to-DQ mismatch within byte variation for a given component, including DQS (characterized).

$$\text{DQ-to-DQ mismatch} = \frac{R_{ODT}(MAX) - R_{ODT}(MIN)}{R_{ODT}(AVG)}$$

Output Driver and Termination Register Temperature and Voltage Sensitivity

When temperature and/or voltage change after calibration, the tolerance limits are widenaccording to the tables below.

Table 4-220: Output Driver and Termination Register Sensitivity Definition

Resistor	Definition Point	Min	Max	Unit	Notes
R_{ONPD}	$0.33 \times V_{DDQ}$	$90 - (dR_{ONdT} \cdot \lvert\Delta T\rvert) - (dR_{ONdV} \cdot \lvert\Delta V\rvert)$	$110 + (dR_{ONdT} \cdot \lvert\Delta T\rvert) + (dR_{ONdV} \cdot \lvert\Delta V\rvert)$	%	1, 2
V_{OHPU}	$0.33 \times V_{DDQ}$	$90 - (dV_{OHdT} \cdot \lvert\Delta T\rvert) - (dV_{OHdV} \cdot \lvert\Delta V\rvert)$	$110 + (dV_{OHdT} \cdot \lvert\Delta T\rvert) + (dV_{OHdV} \cdot \lvert\Delta V\rvert)$		1, 2, 5
$R_{TT(I/O)}$	$0.33 \times V_{DDQ}$	$90 - (dR_{ONdT} \cdot \lvert\Delta T\rvert) - (dR_{ONdV} \cdot \lvert\Delta V\rvert)$	$110 + (dR_{ONdT} \cdot \lvert\Delta T\rvert) + (dR_{ONdV} \cdot \lvert\Delta V\rvert)$		1, 2, 3
$R_{TT(IN)}$	$0.33 \times V_{DD2}$	$90 - (dR_{ONdT} \cdot \lvert\Delta T\rvert) - (dR_{ONdV} \cdot \lvert\Delta V\rvert)$	$110 + (dR_{ONdT} \cdot \lvert\Delta T\rvert) + (dR_{ONdV} \cdot \lvert\Delta V\rvert)$		1, 2, 4

Notes:

1. △T = T - T(@calibration), △T = V - V(@calibration)
2. dR_{ONdT}, dR_{ONdV}, dV_{OHdT}, dV_{OHdV}, dR_{TTdV}, and dR_{TTdT} are not subject to production testbut are verified by designand characterization.
3. This parameter applies to input/output pin such as DQS, DQ, and DMI.
4. This parameter applies to input pin such as CK, CA, and CS.
5. Refer to Pull-up/Pull-down Driver Characteristics for V_{OHPU}.

Table 4-221: Output Driver and Termination Register Temperature and Voltage Sensitivity

Symbol	Parameter	Min	Max	Unit
dR_{ONdT}	R_{ON} temperature sensitivity	0	0.75	%/°C
dR_{ONdV}	R_{ON} voltage sensitivity	0	0.2	%/mV
dV_{OHdT}	V_{OH} temperature sensitivity	0	0.75	%/°C
dV_{OHdV}	V_{OH} voltage sensitivity	0	0.35	%/mV
dR_{TTdT}	R_{TT} temperature sensitivity	0	0.75	%/°C
dR_{TTdV}	R_{TT} voltage sensitivity	0	0.2	%/mV

4.62 AC and DC Operating Conditions

Recommended DC Operating Conditions

Operation or timing that is not specified is illegal. To ensure proper operation, the devicemust be initialized properly.

Table 4-222: Recommended DC Operating Conditions

Symbol	Min	Typ	Max	DRAM	Unit	Notes
V_{DD1}	1.7	1.8	1.95	Core 1 power	V	1, 2
V_{DD2}	1.06	1.1	1.17	Core 2 power/Input buffer power	V	1, 2, 3
V_{DDQ}	1.06	1.1	1.17	I/O buffer power	V	2, 3

Notes:

1. V_{DD1} uses significantly less power than V_{DD2}.
2. The voltage range is for DC voltage only. DC voltage is the voltage supplied at the DRAM and is inclusive of all noise up to 20 MHz at the DRAM package ball.
3. The voltage noise tolerance from DC to 20 MHz exceeding a peak-to-peak tolerance of 45mV at the DRAM ball is not included in the TdIVW.

4.63 Output Slew Rate and Overshoot/Undershoot specifications

Single-Ended Output Slew Rate

Table 4-223: Single-Ended Output Slew Rate

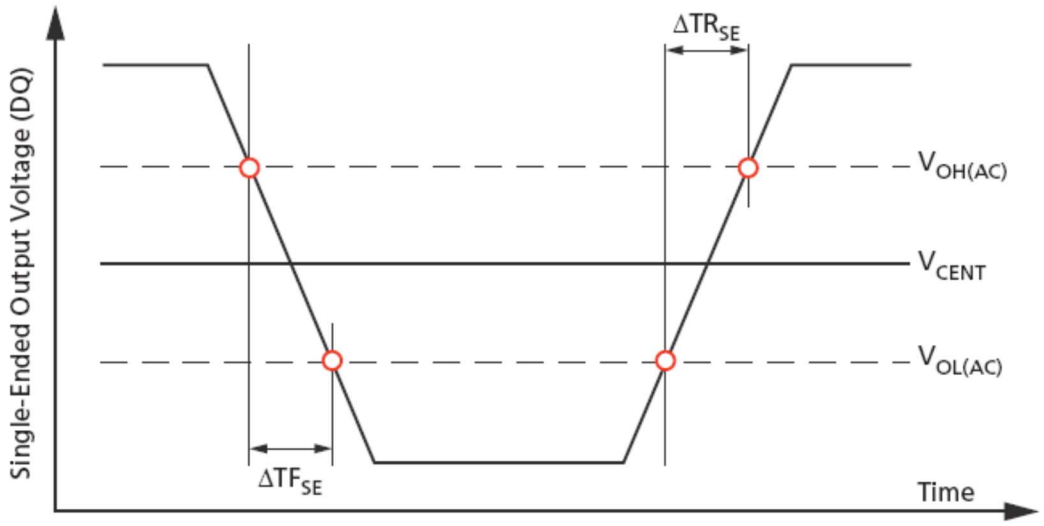
Note 1-5 applies to entire table

Parameter	Symbol	Value		
		Min	Max	Units
Single-ended output slew rate (V_{OH} = V_{DDQ}/3)	SRQse	3.5	9.0	V/ns
Output slew rate matching ratio (rise to fall)	–	0.8	1.2	–

Notes:

1. SR = Slew rate; Q = Query output; se = Single-ended signal
2. Measured with output reference load.
3. The ratio of pull-up to pull-down slew rate is specified for the same temperature andvoltage, over the entire temperature andvoltage range. For a given output, it representsthe maximum difference between pull-up and pull-down drivers due toprocessvariation.
4. The output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ = 0.2 × $V_{OH(DC)}$ and $V_{OH(AC)}$= 0.8 × $V_{OH(DC)}$.
5. Slew rates are measured under average SSO conditions with 50% of the DQ signals perdata byte switching.

Figure 168: Single-Ended Output Slew Rate Definition



Differential Output Slew Rate

Table 4-224: Differential Output Slew Rate

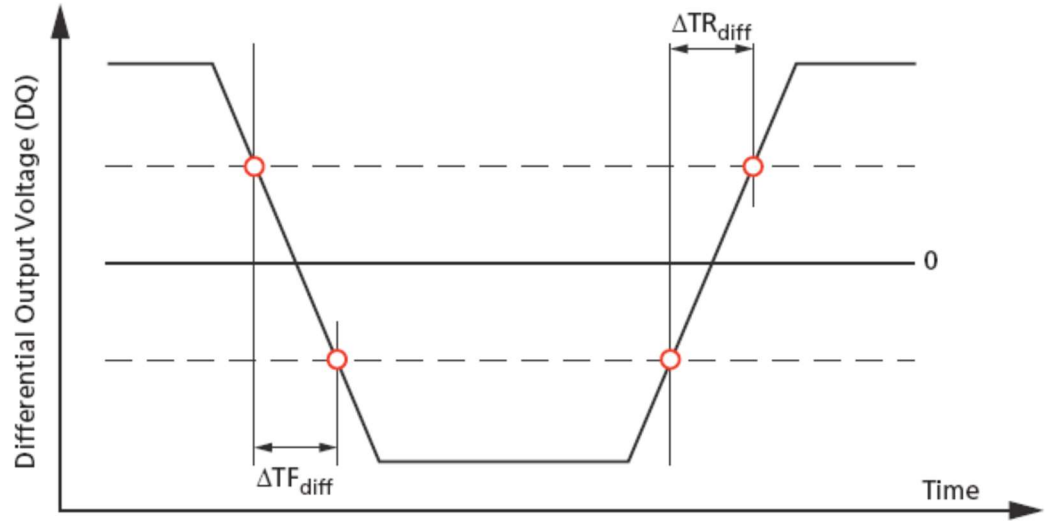
Note 1-4 applies to entire table

Parameter	Symbol	Value		
		Min	Max	Units
Differential output slew rate (V_{OH} = V_{DDQ}/3)	SRQdiff	7	18	V/ns

Notes:

1. SR = Slew rate; Q = Query output; se = Differential signal
2. Measured with output reference load.
3. The output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ = –0.8 × $V_{OH(DC)}$ and $V_{OH(AC)}$= 0.8 × $V_{OH(DC)}$.
4. Slew rates are measured under average SSO conditions with 50% of the DQ signals perdata byte switching.

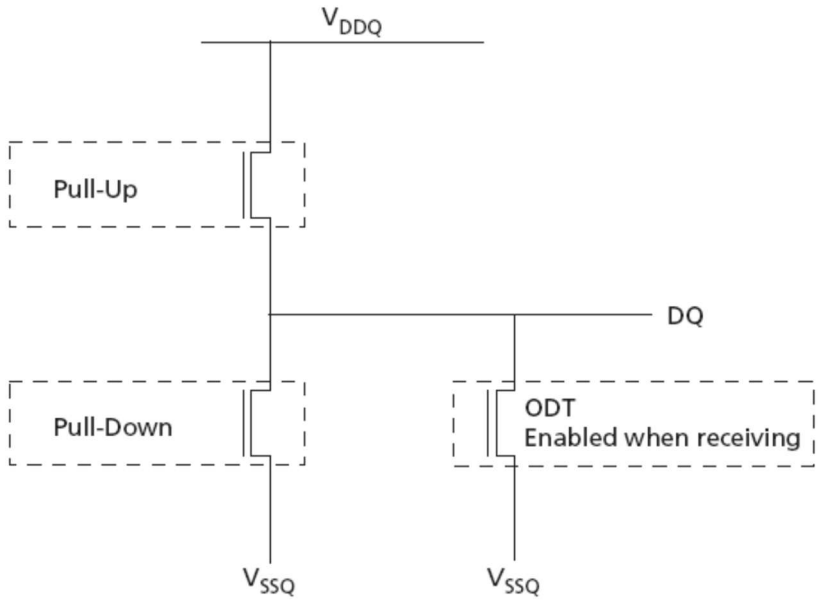
Figure 4-169: Differential Output Slew Rate Definition



4.64 LVSTL I/O System

LVSTL I/O cells are comprised of a driver pull-up and pull-down and a terminator.

Figure 170: Single-Ended Output Slew Rate Definition



To ensure that the target impedance is achieved, calibrate the LVSTL I/O cell as following example:

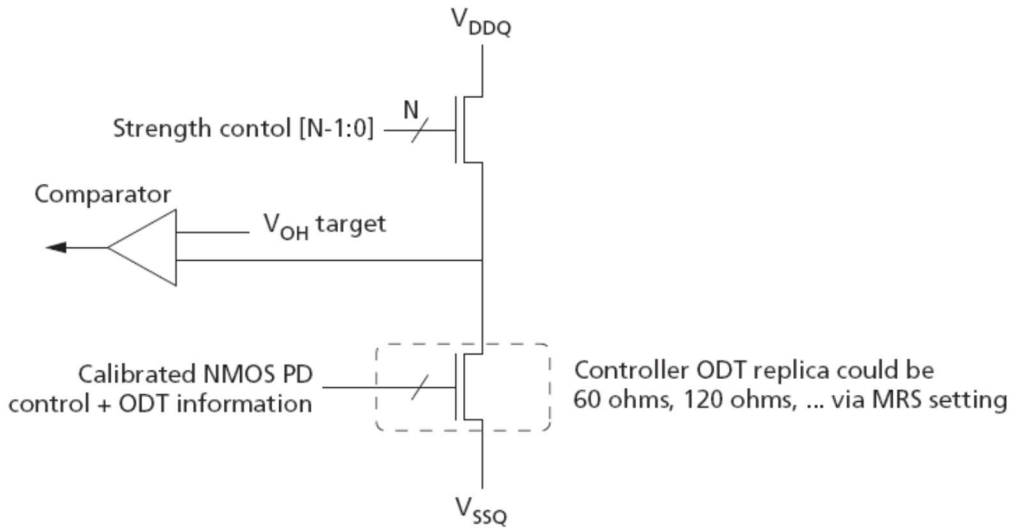
1. Calibrate the pull-down device against a 240 ohm resistor to V_{DDQ} via the ZQ pin.

- Set strength control to minimum setting
- Increase drive strength until comparator detects data bit is less than $V_{DDQ}/3$
- NMOS pull-down device is calibrated to 120 ohms

2. Calibrate the pull-up device against the calibrated pull-down device.

- Set V_{OH} target and NMOS controller ODT replica via MRS (V_{OH} can be automatically controlled by ODT MRS)
- Set strength control to minimum setting
- Increase drive strength until comparator detects data bit is greater than V_{OH} target
- NMOS pull-up device is calibrated to V_{OH} target

Figure 4-171: Pull-Up Calibration



4.65WRITE and MASKED WRITE Operation DQS Control (WDQS Control)

The device supports WRITE and MASKED WRITE operations with the following DQScontrols. Before and after WRITE and MASKED WRITE operations, DQS_t, and DQS_care required to have sufficient voltage gap to make sure the write buffers operating normallywithout any risk of meta-stability.

The device is supported by either of the two WDQS control modes below.
- Mode 1: Read based control
- Mode 2: WDQS_on / WDQS_off definition based control

Regardless of ODT enable/disable, WDQS related timing described here does not allowany change of existing command timing constraints for all READ/WRITE operations. Incase of any conflict or ambiguity on the command timing constraints caused by thespecification here, the specification defined in the Timing Constraints for TrainingCommands table should have higher priority than WDQS control requirements.

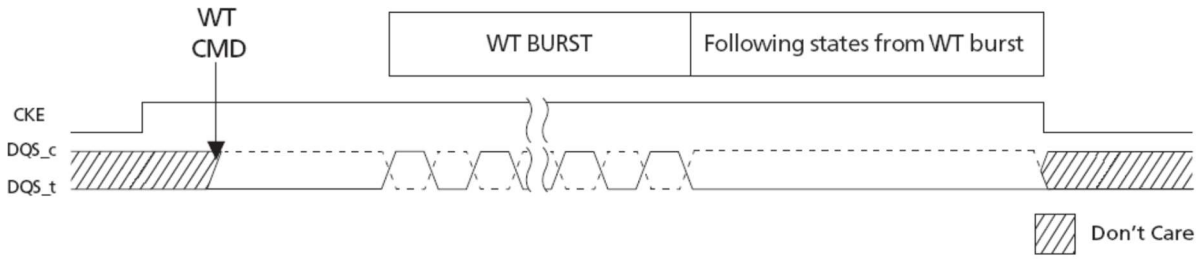
In order to prevent write preamble related failure, it is strongly recommended to supporteither of the two WDQS controls to the device.

WDQS Control Mode 1 – Read-Based Control

The device needs to be guaranteed the differential WDQS, but the differential WDQScan be controlled as described below. WDQS control requirements here can be ignoredwhile differential read DQS is operated or while DQS hands over from read to write orvice versa.

1. When WRITE/MASKED WRITE command is issued, SoC makes the transitionfrom driving DQS_c HIGH todriving differential DQS_t/DQS_c, followed by normaldifferential burst on DQS pins.
2. At the end of post amble of WRITE/MASKED WRITE burst, SoC resumes drivingDQS_c HIGH through thesubsequent states except for DQS toggling and DQSturn around time of WT-RD and RD-WT as long as CKE isHIGH.
3. When CKE is LOW, the state of DQS_t/DQS_c is allowed to be “Don’t Care.”

Figure 4-172: WDQS Control Mode 1



WDQS Control Mode 2 – WDQS_On/Off

After WRITE/MASKED WRITE command is issued, DQS_t and DQS_c required to bedifferential from WDQS_on, and DQS_t and DQS_c can be "Don't Care" status fromWDQS_off of WRITE/MASKED WRITE command. When ODT is enabled, WDQS_onand WDQS_off timing is located in the middle of the operations. When host disablesODT, WDQS_on and WDQS_off constraints conflict with tRTW. The timing does notconflict when ODT is enabled because WDQS_on and WDQS_off timing is covered inODTLon and ODTLoff. However, regardless of ODT on/off, WDQS_on/off timing belowdoes not change any command timing constraints for all read and write operations. Inorder to prevent the conflict, WDQS_on/off requirement can be ignored whereWDQS_on/off timing is overlapped with read operation period including READ burstperiod and tRPST or overlapped with turn-around time (RD-WT or WT-RD). In addition,the period during DQS toggling caused by read and write can be counted as WDQS_on/off.

Parameters

- WDQS_on: The maximum delay from WRITE/MASKED WRITE command to differentialDQS_t and DQS_c
- WDQS_off: The minimum delay for DQS_t and DQS_c differential input after the lastWRITE/MASKED WRITEcommand
- WDQS_Exception: The period where WDQS_on and WDQS_off timing is overlappedwith READ operation orwith DQS turn around (RD-WT, WT-RD)
  - WDQS_Exception @ ODT disable = MAX(WL-WDQS_on + ^{t}DQSTA - ^{t}WPRE - n ^{t}CK,0 ^{t}CK) where RD to WTcommand gap = ^{t}RTW(MIN)@ODT disable + n ^{t}CK
  - WDQS_Exception @ ODT enable = ^{t}DQSTA

Table 4-225: Differential Output Slew Rate

WRITE Latency		nWR	nRTP	WDQS_On (Max)		WDQS_Off (Min)		Lower Frequency	Upper Frequency
Set A	Set B			Set A	Set B	Set A	Set B	Limit (>)	Limit (≤)
4	4	6	8	0	0	15	15	10	266
6	8	10	8	0	0	18	20	266	533
8	12	16	8	0	6	21	25	533	800
10	18	20	8	4	12	24	32	800	1066
12	22	24	10	4	14	27	37	1066	1333
14	26	30	12	6	18	30	42	1333	1600
16	30	34	14	6	20	33	47	1600	1866
18	34	40	16	8	24	36	52	1866	2133

Notes:

1. WDQS_on/off requirement can be ignored when WDQS_on/off timing is overlapped with READ operation period including READ burst period and ^{t}RPST or overlapped with turn-around time (RD-WT or WT-RD).
2. DQS toggling period caused by read and write can be counted as WDQS_on/off.

Table 4-226: WDQS_On/WDQS_Off Allowable Variation Range

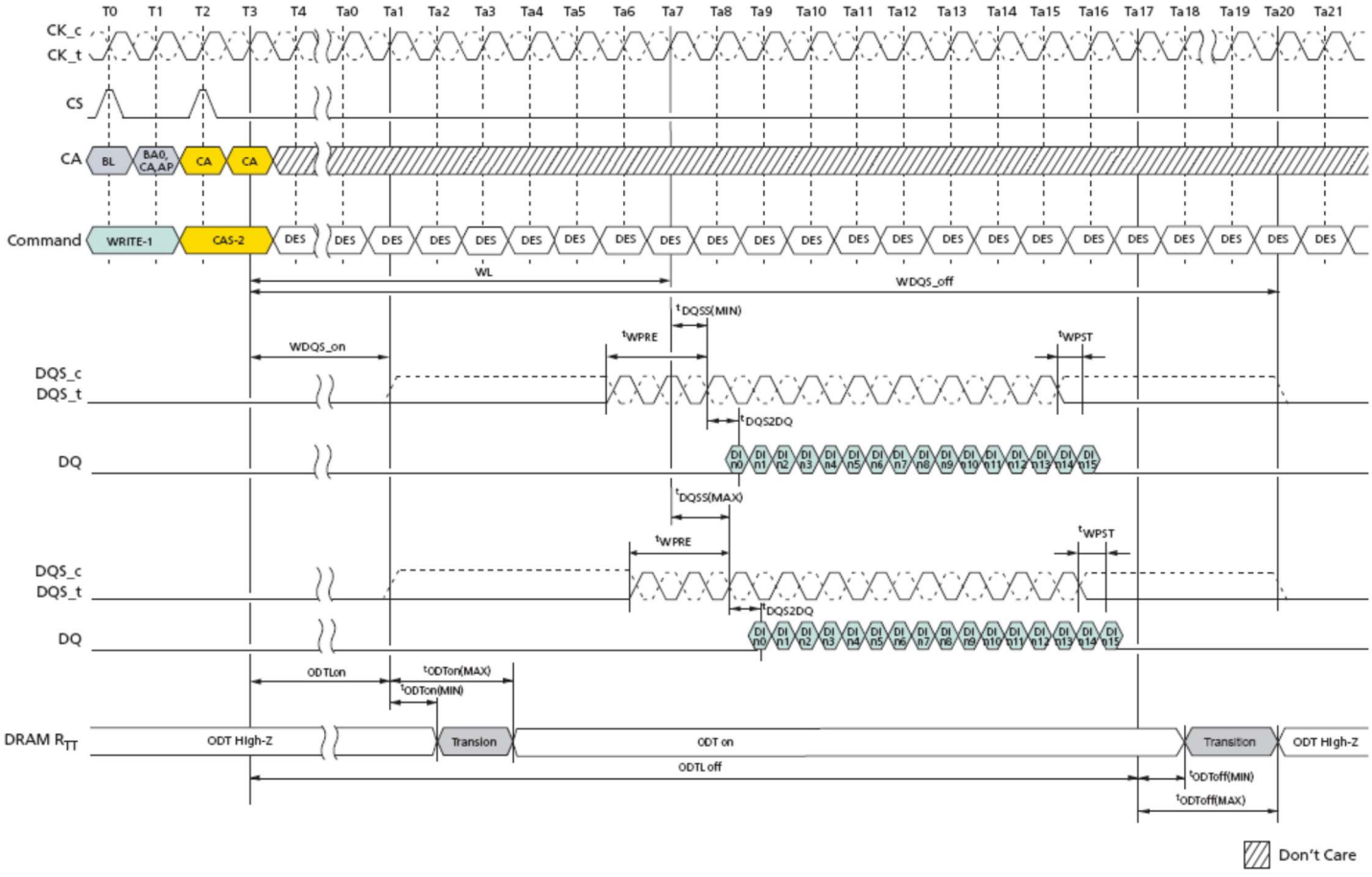
	Min	Max	Unit
WDQS_on	–0.25	0.25	tCK(avg)
WDQS_off	–0.25	0.25	tCK(avg)

Table 4-227: DQS Turn-Around Parameter

Parameter	Description	Value	Unit	Note
tDQSTA	Turn-around time RDQS to WDQS for WDQS control case	TBD	–	1

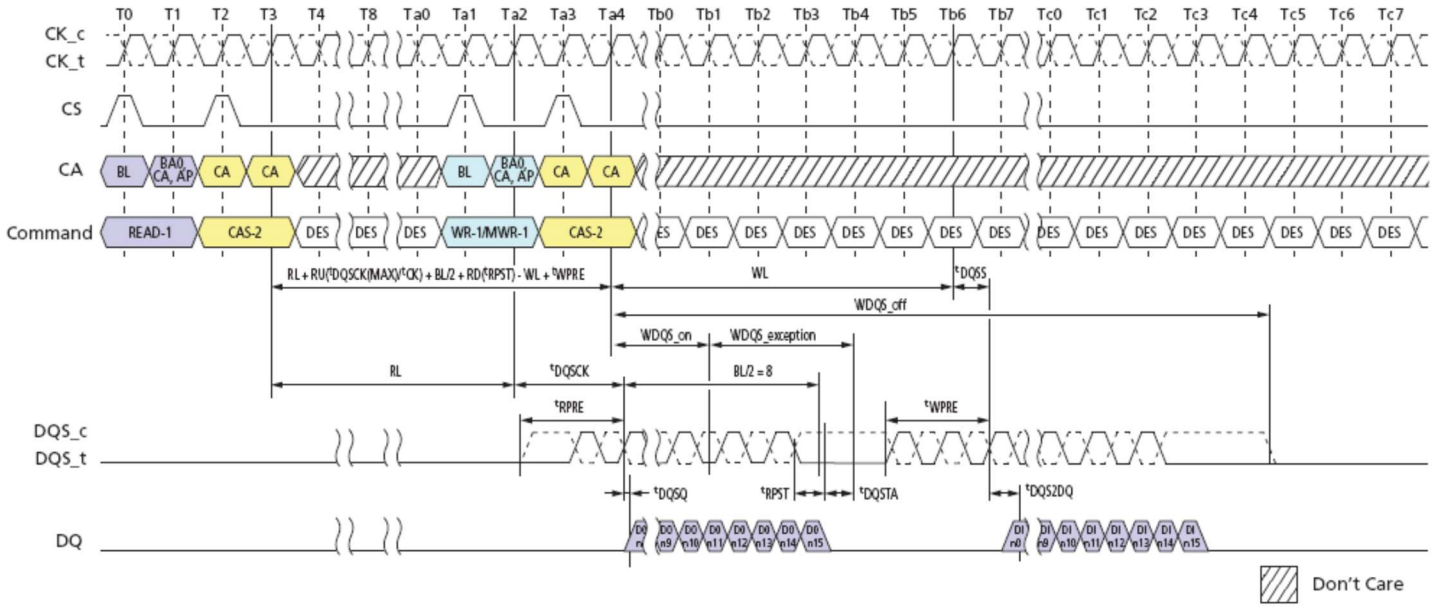
Note:
1. tDQSTA is only applied to WDQS_exception case when WDQS Control. Except for WDQSControl, tDQSTA can be ignored.

Figure 4-173: Burst WRITE Operation



Notes:
1. BL=16, Write postamble = 0.5nCK, DQ/DQS: V_{SSQ} termination.
2. DI n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid atthese times.
4. DRAM RTT is only applied when ODT is enabled (MR11 OP[2:0] is not 000b).

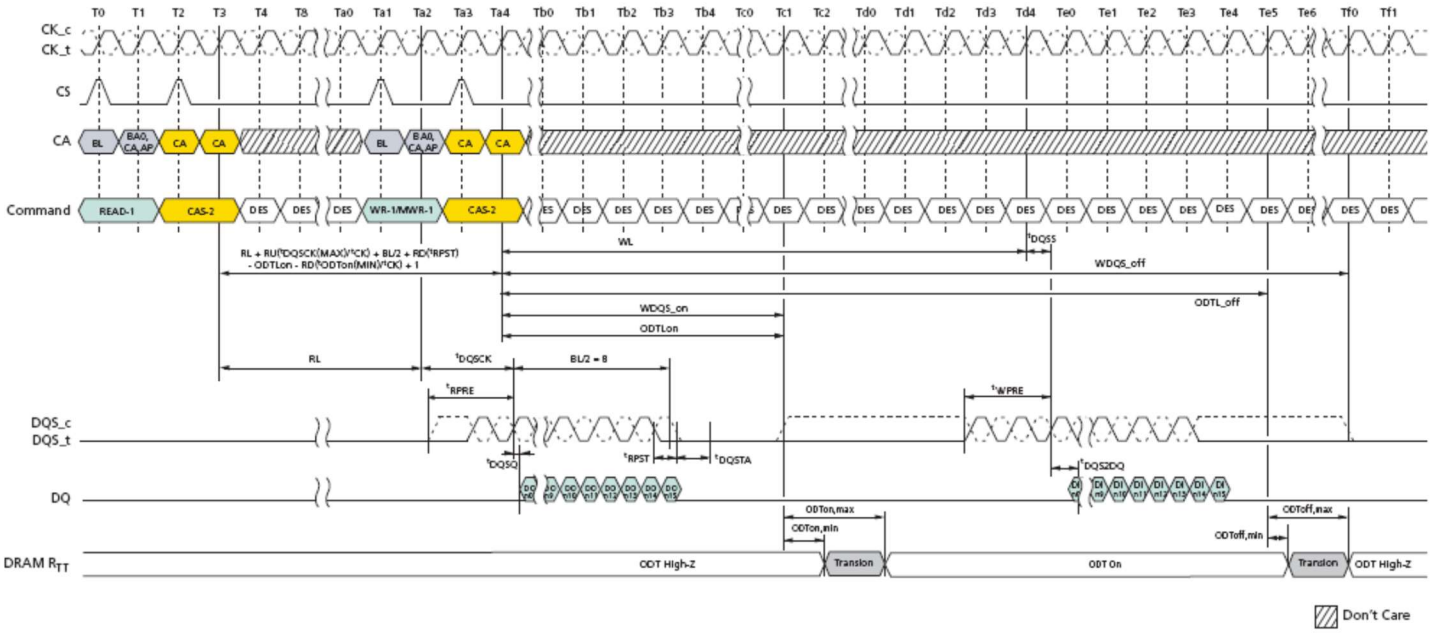
Figure 4-174: Burst READ Followed by Burst WRITE or Burst MASKED WRITE (ODT Disable)



Notes:

1. BL = 16, Read preamble = Toggle, Read postamble = 0.5nCK, Write preamble = 2nCK,Write postamble = 0.5nCK.
2. DO n = data-out from column n, DI n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid atthese times.
4. WDQS_on and WDQS_off requirement can be ignored where WDQS_on/off timing isoverlapped with READ operationperiod including READ burst period and tRPST or overlappedwith turn-around time (RD-WT or WT-RD).

Figure 4-175: Burst READ Followed by Burst WRITE or Burst MASKED WRITE (ODT Enable)



Notes:

1. BL = 16, Read preamble = Toggle, Read postamble = 0.5nCK, Write preamble = 2nCK,Write postamble = 0.5nCK,DQ/DQS:V_{SSQ} termination.
2. DO n = data-out from column n, DI n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid atthese times.
4. WDQS_on and WDQS_off requirement can be ignored where WDQS_on/off timing isoverlapped with READ operationperiod including READ burst period and tRPST or overlappedwith turn-around time (RD-WT or WT-RD).

5. eMMC

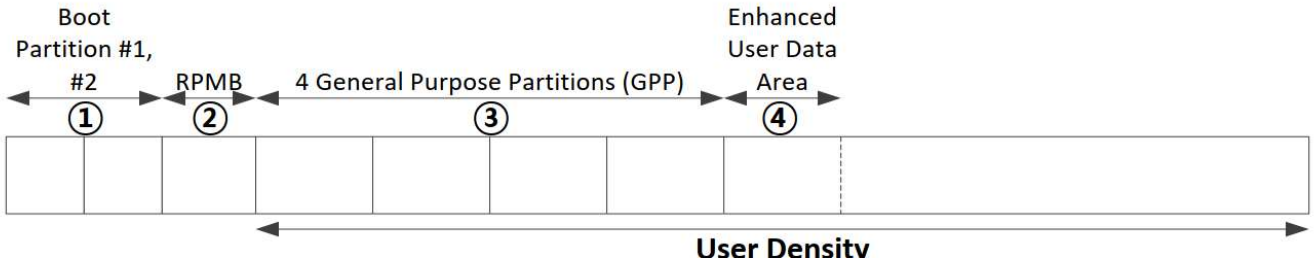
5.1 Technical Notes

HS400 Interface

Support HS400 DDR interface timing mode to achieve a bus speed of 400 MB/s at 200MHz clock frequency with 8bit bus width only. At this mode, the host may need to have an adjustable sampling point to reliably receive the incoming data, due to the speed. Please refer to JESD84-B50-1 standard for additional information.

Partition Management

The device initially consists of two Boot partitions, RPMB(Replay Protected Memory Block) partition and User Data Area. Both Boot and RPMB area have fixed size of area and can't be adjusted. Further information for re-partitioning these areas will be provided with additional application note and please contact to us.



Boot Area Partition and RPMB Area Partition

The device has fixed size of Boot and RPMB area.

Boot partition size is calculated as (128KB * BOOT_SIZE_MULT)
The size of Boot Area Partition 1 and 2 cannot be set independently. It is set as same value.

RPMB partition size is calculated as (128KB * RPMB_SIZE_MULT).
In RPMB partition, CMD 0, 6, 8, 12, 13, 15, 18, 23, 25 are admitted.

Access Size of RPMB partition is defined as the below:

Table 5-1 Setting sequence of Boot Area Partition size and RPMB Area Partition size

REL_WR_SEC_C	Description
REL_WR_SEC_C = 1	Access sizes 256B and 512B supported to RPMB partition
REL_WR_SEC_C > 1	Access sizes up to REL_WR_SEC_C * 512B supported to RPMB partition with 256B granularity

Any undefined set of parameters or sequence of commands results in failure access.
If the failure is in data programming case, the data is not programmed. And if the failure occurs in data read case, the read data is '0x00'.

Table 5-2 Capacity according to partition

Device	Boot partition 1 [KB]	Boot partition 2 [KB]	RPMB[KB]
8GB	4,096	4,096	4,096

Enhanced Partition (Area)

Xincun 8GB eMMC applies SLC Mode for Enhanced User Data Area and it leads to occupying double size of original set up size if master set some area of User Data Area as enhanced user area. For example, if master set 1MB as enhanced mode, then, total 2MB of user data area is used for it. Max Enhanced user Data Area follows below formula of JESD84-B50-1.

Max Enhanced User Data Area size is defined as (MAX_ENH_SIZE_MULT x HC_WP_GRP_SIZE x HC_ERASE_GRP_SIZE x 512Kbytes)

Table 5-3 Maximum Enhanced Partition Size

Device	LBA [Hex]	LBA [Dec.]	Max. Enhanced Partition Size
8GB	0x1D20	7,456	3,817,472 Bytes

User Density

As mentioned in Enhanced Partition (Area) section, total User Density depends on partition type to be set.Xincun 8GB applies SLC mode for enhanced user area and so, assigning any size for it occupies double of that value assigned. For example, assigning 64MB in the SLC mode takes 128MB of capacity in MLC.

Table 5-4 User Density Size

Device	LBA [Hex]	LBA [Dec.]	User Partition Size
8GB	0xE90000	15,269,888	7,818,182,656 Bytes

Boot operation

Device supports not only boot mode but also alternative boot mode. Device supports high speed timing and dual data rate during boot.

Figure 5-1 embedded MultiMediaCard state diagram (boot mode)

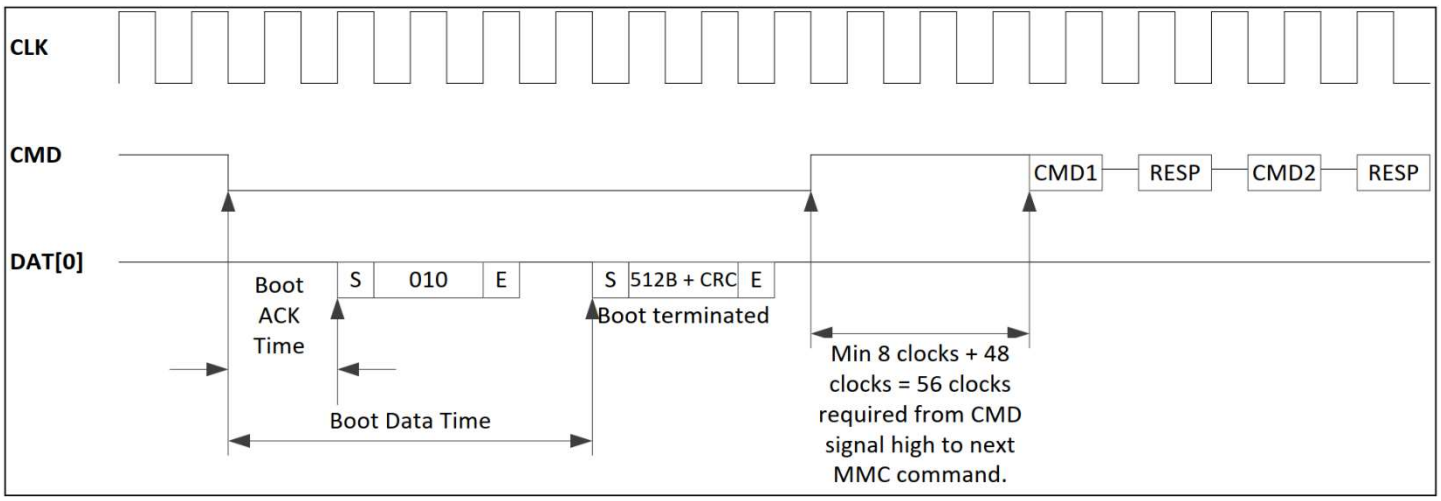


Figure 5-2 embedded MultiMediaCard state diagram (alternative boot mode)

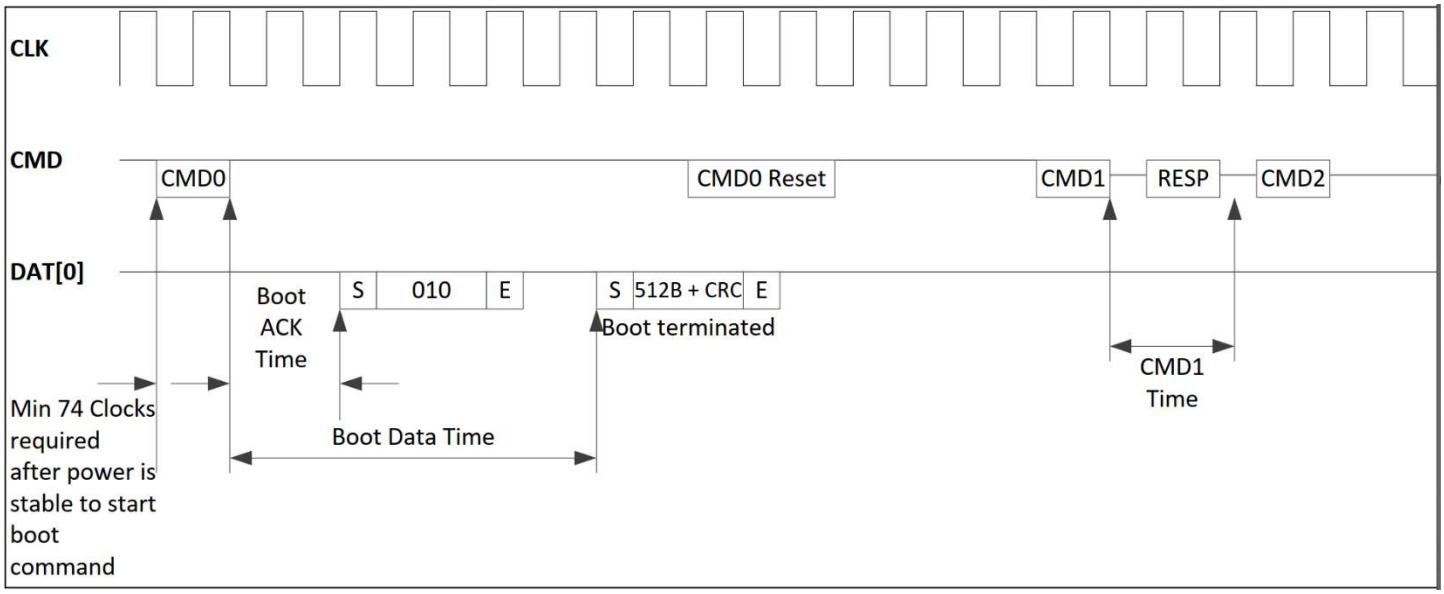


Table 5-5 Boot ack, boot data and initialization Time

Timing Factor	Value
Boot ACK Time	< 50 ms
Boot Data Time	< 1 sec
Initialization Time[1]	< 3 secs

Note:

1. The value for this initialization time is for such case which includes partition setting also. For details, please refer to INI_TIMEOUT_AP in Extended CSD Register of JESD84-B50-1.
   Normal initialization time (without partition setting) is completed within 1sec

Field Firmware Upgrade (FFU)

Field Firmware Updates (FFU) is for customer's FW updating in field for those cases of debugging, enhancing and adding new features of FW itself. The host can download a new version of the firmware into the eMMC device by this mechanism and whole FFU process can happen without affecting any user/OS data, even in parallel with Host's performing other operations.

For additional information refer to JEDEC Standards No. JESD84-B50-1.

Cache

This device supports 128KB of volatile memory as an eMMC cache for performance improvement of both sequentialand random access. For additional information please refer to JESD84-B50 standard.

Packed Commands

This device supports packed commands feature of eMMC standard version 5.0 and allows the host to pack Read or Write commands into groups (of single type of operation) and transfer these to the device in a single transfer on the bus, which leads reducing overall bus overheads and thus, enables optimal system performance.

Please refer to JESD84-B50 for information details.

Secure Delete

Sanitize

The device supports Sanitize operation for removing data from the unmapped user address space in the device, physically. Device keeps the sanitize operation until one of the following events occurs, with keeping busy asserted,

- Sanitize operation is complete
- HPI is used to abort the operation
- Power failure
- Hardware reset

No data should exist in the unmapped host address space after the sanitize operation is completed.

Secure Erase

This device supports the optional Secure Erase command, which is for backward compatibility reasons, as well as standard erase command. Host will erase provided range of LBAs and ensure no older copies of this data exist in the flash with this command.

Please refer to JEDEC Standards No. JESD84-B50 for more information.

Secure Trim

This device supports Secure Trim command which is similar to the Secure Erase command but different in thatperforms a secure purge operation on write blocks instead of erase groups. This is for backward compatibility reasons.

The secure trim command is performed in two steps:
1) Mark the LBA range as candidate for erase.
2) Do Erase the marked address range and then, ensure no old copies are left within that range. .
For additional information refer to JEDEC Standards No. JESD84-B50.

High Priority Interrupt (HPI)

This device supports High Priority Interrupt and prevent problem of Host being stalled due to too much delayed Write operation by new paging request of operating system, by user. It will delay the request for new paging until currently going write operation is completed.

Please refer to JEDEC Standards No. JESD84-B50 for more information.

Device Health

This device supports Device Health Report feature which is featured to others in that separately report SLC type area and other area by each bytes of DEVICE_LIFE_TIME_EST_TYP_A[268] and
DEVICE_LIFE_TIME_EST_TYP_A[269], respectively. It can be queried by standard MMC command for getting xtendedCSD structure. Please refer to below and JEDEC Standards No. JESD84-B50 for details.

DEVICE_LIFE_TIME_EST_TYP_A[268], The host may use it to query health information of SLC area.

DEVICE_LIFE_TIME_EST_TYP_B[269], The host may use it to query health information of other partition area.

Auto Power Saving Mode

This device supports Auto Power Saving Mode which can save power consumption definitely. Device will enter this mode if host does not issue any command during 1ms, after completion of previously issued command.

Any newly issued commands during this mode will be carried normally.

Table 5-6 Auto Power Saving Mode enter and exit

Mode	Enter Condition	Escape Condition
Auto Power Saving Mode	When previous operation which came from Host is completed and no com-mand is issued during a certain time.	If Host issues any command

Table 5-7 Auto Power Saving Mode and Sleep Mode

Mode	Enter Condition	Escape Condition
NAND Power	ON	ON/OFF
GotoSleep Time	< 100ms	< 1ms

Enhanced Strobe

Supports Enhanced Strobe which is new feature of eMMC version 5.1 standard to synchronize CMD response. Host shall support this feature and it enables faster and more reliable operation.

For more information, please refer to JEDEC Standards No. JESD84-B50.

Performance

Table 5-8 Sustained Sequential Performance

Capacity (GB)	Sequential Read (MB/s)	Sequential Write (MB/s)
8	250	25

Note:

1. Test Condition: Bus width x8, HS400, 512KB data transfer, Packed Off, Cache On, w/o file system overhead.

5.2 Register Value

Following sections are for describing all register value of eMMC device at its default. And these values here may be updated in later version without notice.

There are defined total six registers in this section: OCR, CID, CSD, EXT_CSD, RCA and DSR. All of them has its own commands corresponded and for details, please refer JEDEC Standards No. JESD84-B50 for details. The OCR, CID and CSD registers has information of device and content, while the RCA and DSR registers are for configuring parameters of device. For the EXT_CSD register, it contains both device specific information and actual configuration parameters.

OCR Register

The operation conditions register (OCR) contains: V_{CC} voltage profile of the device, access mode indication, status information bit. The status bit is set when the device finished its power up procedure. All eMMC devices shall have this register implemented.

Table 5-9 OCR Register

OCR bit	V_{CCQ} Voltage Window[2]	Register Value
[6:0]	Reserved	00 00000b
[7]	1.70 ~ 1.95	1b
[14:8]	2.0 ~ 2.6	000 0000b
[23:15]	2.7 ~ 3.6	1 1111 1111b
[28:24]	Reserved	0 0000b
[30:29]	Access Mode	00b (byte mode) -[2GB] 10b (sector mode) -[*Higher than 2GB only]
[31]	eMMC power up status bit (busy)[1]	

Notes:

1. This bit is set to LOW if the eMMC has not finished the power up routine.
2. The voltage for internal flash memory (V_{CC}) should be 2.7 ~ 3.6V regardless of OCR register value.

CID Register

The device Identification (CID) register is 128bits wide. It contains the device identification information used during the device identification phase (eMMC protocol). eMMC device shall have a unique identification number.

Users can define their own CID register and the CID contents will be programmed into the eMMC device when firmware fusing process. After the programming is complete, end users cannot change CID, unless the whole foundry production program is re-done. Users can install the new downloaded firmware into the device by using FFU (Field Firmware Update) mode.

Table 5-10 CID Register

Name	Field	Width	CID-slice	CID Value
Manufacturer ID	MID	8	[127:120]	0xAD
Reserved		6	[119:114]	–
Card/BGA	CBX	2	[113:112]	0x01
OEM/Application ID	OID	8	[111:104]	–
Product name	PNM	48	[103:56]	–
Product revision	PRV	8	[55:48]	–
Product serial number	PSN	32	[47:16]	–[3]
Manufacturing date	MDT	8	[15:8]	–[1]
CRC7 checksum	CRC	7	[7:1]	–[1]
not used, always '1'	–	1	[0:0]	–

Notes:

1.Tdescription are same as eMMC JEDEC standard.

2. PRV is composed of the revision count of controller and the revision count of F/W patch.

3. A 32 bits unsigned binary integer. (Random Number).

Product name table (In CID Register)

Table 5-11 Product name table

Part Number	Density (GB)	PKG Type
CTB78GB11K1	8	11.5x13.0x1.0

RCA Register

The writable 16-bit relative device address (RCA) register carries the device address assigned by the host during the device identification. This address is used for the addressed host-device communication after the device identification procedure. The default value of the RCA register is 0x0001. The value 0x0000 is reserved to set all devices into the Stand-by State with CMD7.

CSD Register

The device Specific Data (CSD) register provides information on how to access the device contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed, whether the DSR register can be used etc. The programmable part of the register (entries marked by W or E) can be changed by CMD27.

The CSD register defines the behavior or of eMMC devices. The eMMC behavior is related to the controller design. The following table shows a typical CSD definition of CTB78GB11K1 based eMMC. If users need to add on more features, firmware or hardware modifications may be necessary.

※Note that the register values are preliminary data and may be updated in a later version. And the updated value will be supported by specified application note later.

Table 5-12 Typical CSD Register

Name	Field	Bit	Type	Slice	Value	Note
CSD structure	CSD_STRUCTURE	2	R	[127:126]	0x03	
System specification version	SPEC_VERS	4	R	[125:122]	0x04	
Reserved	–	2	R	[121:120]	–	
Data read access-time	TAAC	8	R	[119:112]	0x27	
Data read access-time in CLK cycles (NSAC x 100)	NSAC	8	R	[111:104]	0x01	
Max. bus clock frequency	TRAN_SPEED	8	R	[103:96]	0x32	
Device command classes	CCC	12	R	[95:84]	0x8F5	
Max. read data block length	READ_BL_LEN	4	R	[83:80]	0x09	
Partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]	0x00	
Write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]	0x00	
Read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]	0x00	
DSR implemented	DSR_IMP	1	R	[76:76]	0x00	
Reserved	–	2	R	[75:74]	–	
Device size	C_SIZE	12	R	[73:62]	0xFFF	
Max read current@VCCQ min	VCCQ_R_CURR_MIN	3	R	[61:59]	0x07	
Max read current@VCCQ max	VCCQ_R_CURR_MAX	3	R	[58:56]	0x07	
Max write current@VCCQ min	VCCQ_W_CURR_MIN	3	R	[55:53]	0x07	
Max write current@VCCQ max	VCCQ_W_CURR_MAX	3	R	[52:50]	0x07	
Device size multiplier	C_SIZE_MULT	3	R	[49:47]	0x07	
Erase group size	ERASE_GRP_SIZE	5	R	[46:42]	0x1F	
Erase group size multiplier	ERASE_GRP_MULT	5	R	[41:37]	0x1F	
Write protect group size	WP_GRP_SIZE	5	R	[36:32]	0x0F	
Write protect group enable	WP_GRP_ENABLE	1	R	[31:31]	0x01	
Manufacturer default ECC	DEFAULT_ECC	2	R	[30:29]	0x00	
Write speed factor	R2W_FACTOR	3	R	[28:26]	0x02	

Table 5-12 Typical CSD Register (Continued)

Name	Field	Bit	Type	Slice	Value	Note
Max. write data block length	WRITE_BL_LEN	4	R	[25:22]	0x09	
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]	0x00	
Reserved	–	4	R	[20:17]	–	
Content protection application	CONTENT_PROT_APP	1	R	[16:16]	0x00	
File format group	FILE_FORMAT_GRP	1	R/W	[15:15]	0x00	
Copy flag (OTP)	COPY	1	R/W	[14:14]	0x01	
Permanent write protection	PERM_WRITE_PROTECT	1	R/W	[13:13]	0x00	
Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	[12:12]	0x00	
File format	FILE_FORMAT	2	R/W	[11:10]	0x00	
ECC code	ECC	2	R/W/E	[9:8]	0x00	
CRC	CRC	7	R/W/E	[7:1]	–	
Not used, always '1'	–	1		[0:0]	–	

Note:

1.The type of the CSD Registry entries in the Table 4-12 is coded as follows.

R: Read only

W: One time programmable and not readable

R/W: One time programmable and readable

W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.

R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.

R/W/C_P: Writable after value cleared by power failure and HW/rest assertion (the value not cleared by CMD0 reset) and readable.

R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.

W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable.

Extended CSD Register (EXT_CSD)

The Extended CSD register defines the additional behavior of eMMC devices due to limited CSD information. The following table shows a typical extended CSD definition of CTB78GB11K1 based eMMC. If users need to add on more features, firmware or hardware modifications may be necessary.

※Notethat the register values are preliminary data and may be updated in a later version. And the updated value will be supported by specified application note later.

Table 5-13 Typical EXT_CSD Register

Name	Field	Byte	Type	Slice	Value	Note
Properties Segment						
Reserved	–	6	–	[511:506]	–	
Extended security commands error	EXT_SECURITY_ERR	1	R	[505]	0x00	
Supported command sets	S_CMD_SET	1	R	[504]	0x01	
HPI features	HPI_FEATURES	1	R	[503]	0x01	
Background operations support	BKOPS_SUPPORT	1	R	[502]	0x01	
Max packed read commands	MAX_PACKED_READS	1	R	[501]	0x3F	
Max packed write commands	MAX_PACKED_WRITES	1	R	[500]	0x3F	
Data tag support	DATA_TAG_SUPPORT	1	R	[499]	0x01	
Tag unit size	TAG_UNIT_SIZE	1	R	[489]	0x08	
Tag resources size	TAG_RES_SIZE	1	R	[497]	0x00	
Context management capabilities	CONTEXT_CAPABILITIES	1	R	[496]	0x05	
Large unit size	LARGE_UNIT_SIZE_M1	1	R	[495]	0x07	
Extended partitions attribute support	EXT_SUPPORT	2	R	[494]	0x03	
Supported modes	SUPPORTED_MODES	1	R	[493]	0x01	
FFU features	FFU_FEATURES	1	R	[492]	0x00	
Operation codes timeout	OPERATION_CODE_TIMEOUT	1	R	[491]	0x10	
FFU Argument	FFU_ARG	4	R	[490:487]	0x00	
Barrier Support	BARRIER_SUPPORT	1	R	[486]	0x01	
Reserved	–	181	–	[485:309]	–	
CMD Queuing Support	CMDQ_SUPPORT	1	R	[308]	0x01	
CMD Queuing Depth	CMDQ_DEPTH	1	R	[307]	0x1F	
Reserved	–	1	–	[306]	–	
Number of FW sectors correctly programmed	NUMBER_OF_FW_ SECTOR S_CORRECTLY_ PROGRAM MED	4	R	[305:30]	0x00	
Vendor proprietary health report	VENDOR_PROPRIETARY_ HEALTH_REPORT	32	R	[301:270]	0x00	
Device life time estimation type B	DEVICE_LIFE_TIME_EST_TYP _B	1	R	[269]	0x01	Other area except EXT_CSD[268]
Device life time estimation type A	DEVICE_LIFE_TIME_EST_TYP _A	1	R	[268]	0x01	SLC type area

Table 5-13 Typical EXT_CSD Register (Continued)

Name	Field	Byte	Type	Slice	Value	Note
Properties Segment						
Pre EOL information	PRE_EOL_INFO	1	R	[267]	0x01	
Optimal read size	OPTIMAL_READ_SIZE	1	R	[266]	0x00	
Optimal write size	OPTIMAL_WRITE_SIZE	1	R	[265]	0x04	
Optimal trim unit size	OPTIMAL_TRIM_UNIT_SIZE	1	R	[264]	0x03	
Device version	DEVICE_VERSION	2	R	[263:262]	0x00	
Firmware version	FIRMWARE_VERSION	8	R	[261:254]	→	TBD
Power class for 200MHz, DDR at 3.6V	PWR_CL_DDR_200_360	1	R	[253]	0x77	
Cache size	CACHE_SIZE	4	R	[252:249]	→	0x00000400
Generic CMD6 timeout	GENERIC_CMD6_TIME	1	R	[248]	0x0A	
Power off notification(long) timeout	POWER_OFF_LONG_TIME	1	R	[247]	0x3C	
Background operations status	BKOPS_STATUS	1	R	[246]	0x00	
Number of correctlyprogrammed sectors	CORRECTLY_PRG_SECTORS_NUM	4	R	[245:242]	→	0x00000000
1st initialization time after partitioning	INI_TIMEOUT_AP	1	R	[241]	0x1E	
Cache Flushing Policy	CACHE_FLUSH_POLICY	1	R	[240]	0x01	
Power class for 52MHz, DDR at 3.6V	PWR_CL_DDR_52_360	1	R	[239]	0x77	
Power class for 52 MHz, DDR at1.95V	PWR_CL_DDR_52_195	1	R	[238]	0x77	
Power class for 200 MHz at 1.95V	PWR_CL_200_195	1	R	[237]	0x77	
Power class for 200 MHz, at 1.3V	PWR_CL_200_130	1	R	[236]	0x00	
Minimum write performance for 8 bit at 52 MHz in DDR mode	MIN_PERF_DDR_W_8_52	1	R	[235]	0x00	
Minimum read performance for 8 bit at 52 MHz in DDR mode	MIN_PERF_DDR_R_8_52	1	R	[234]	0x00	
Reserved	–	1	–	[233]	0x00	
TRIM multiplier	TRIM_MULT	1	R	[232]	0x02	
Secure feature support	SEC_FEATURE_SUPPORT	1	R	[231]	0x55	
Secure erase multiplier	SEC_ERASE_MULT	1	R	[230]	0x0A	
Secure trim multiplier	SEC_TRIM_MULT	1	R	[229]	0x0A	
Boot information	BOOT_INFO	1	R	[228]	0x07	
Reserved	–	1	–	[227]	–	
Boot partition size	BOOT_SIZE_MULTI	1	R	[226]	0x20	

Table 5-13 Typical EXT_CSD Register (Continued)

Name	Field	Byte	Type	Slice	Value	Note
Properties Segment						
Access size	ACC_SIZE	1	R	[225]	0x06	
High-capacity erase unit siz	HC_ERASE_GRP_SIZE	1	R	[224]	0x01	
High-capacity erase timeout	ERASE_TIMEOUT_MULT	1	R	[223]	0x02	
Reliable write sector count	REL_WR_SEC_C	1	R	[222]	0x01	
High-capacity write protect group size	HC_WP_GRP_SIZE	1	R	[221]	0x10	
Sleep current (V_{CC})	S_C_VCC	1	R	[220]	0x07	
Sleep current (V_{CCQ})	S_C_VCCQ	1	R	[219]	0x07	
Product state awareness timeout	PRODUCTION_STATE_ AWARENESS_TIMEOUT	1	R	[218]	0x0A	
Sleep/awake timeout	S_A_TIMEOUT	1	R	[217]	0x12	
Sleep notification timeout	SLEEP_NOTIFICATION_TIME	1	R	[216]	0x10	
Sector count	SEC_COUNT	4	R	[215:212]	→	8GB (0x00E90000)
Secure Write Protect Information	SECURE_WP_INFO	1	R	[211]	0x01	
Minimum write performance for 8bit at 52MHz	MIN_PERF_W_8_52	1	R	[210]	0x00	
Minimum read performance for 8bit at 52MHz	MIN_PERF_R_8_52	1	R	[209]	0x00	
Minimum write performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_W_8_26_4_52	1	R	[208]	0x00	
Minimum read performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_R_8_26_4_52	1	R	[207]	0x00	
Minimum write performance for 4bit at 26MHz	MIN_PERF_W_4_26	1	R	[206]	0x00	
Minimum read performance for 4bit at 26MHz	MIN_PERFR_4_26	1	R	[205]	0x00	
Reserved	–	1	–	[204]	–	
Power class or 26 MHz at 3.6V 1 R	PWR_CL_26_360	1	R	[203]	0x77	
Power class for 52 MHz at 3.6V 1 R	PWR_CL_52_360	1	R	[202]	0x77	
Power class for 26 MHz at 1.95V 1 R	PWR_CL_26_195	1	R	[201]	0x77	
Power class for 52 MHz at 1.95V 1 R	PWR_CL_52_195	1	R	[200]	0x77	
Partition switching timing	PARTITION_SWITCH_TIME	1	R	[199]	0x01	
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	R	[198]	0x64	

Table 5-13 Typical EXT_CSD Register (Continued)

Name	Field	Byte	Type	Slice	Value	Note
Properties Segment						
I/O Driver Strength CSD structure version	DRIVER_STRENGTH	1	R	[197]	0x1F	
Device type	DEVICE_TYPE	1	R	[196]	0x57	
Reserved	–	1	–	[195]	–	
CSD structure version	CSD_STRUCTURE	1	R	[194]	0x02	
Reserved	–	1	–	[193]	–	
Extended CSD revision	EXT_CSD_REV	1	R	[192]	0x08	
Modes Segment						
Command set	CMD_SET	1	R/W/E_P	[191]	0x00	
Reserved	–	1	–	[190]	–	
Command set revision	CMD_SET_REV	1	R	[189]	0x00	
Reserved	–	1	–	[188]	–	
Power class	POWER_CLASS	1	R/W/E_P	[187]	0x00	
Reserved	–	1	–	[186]	–	
High speed interface timing	HS_TIMING	1	R/W/E_P	[185]	0x01	
Strobe Support	STROBE_SUPPORT -	1	-R	[184]	0x01	
Bus width mode	BUS_WIDTH	1	W/E_P	[183]	0x00	
Reserved	–	1	–	[182]	–	
Erased memory content	ERASED_MEM_CONT	1	R	[181]	0x00	
Reserved	–	1	–	[180]	–	
Partition configuration	PARTITION_CONFI	1	R/W/E & R/W/E_P	[179]	0x00	
Boot config protection	BOOT_CONFIG_PROT	1	R/W &R/W/C_P	[178]	0x00	
Boot bus conditions	BOOT_BUS_CONDITIONS	1	R/W/E	[177]	0x00	
Reserved	–	1	–	[176]	–	
High-density erase group definition	ERASE_GROUP_DEF	1	R/W/E_P	[175]	0x00	
Boot write protection status registers	BOOT_WP_STATU	1	R	[174]	0x00	
Boot area write protection register	BOOT_WP	1	R/W & R/W/C_P	[173]	0x00	
Reserved	–	1	–	[172]	–	
User area write protection register	USER_WP	1	R/W, R/W/C_P & R/W/E_P	[171]	0x00	
Reserved	–	1	–	[170]	–	

Table 5-13 Typical EXT_CSD Register (Continued)

Name	Field	Byte	Type	Slice	Value	Note
Modes Segment						
FW configuration	FW_CONFIG	1	R/W	[169]	0x00	
RPMB size	RPMB_SIZE_MULT	1	R	[168]	0x20	
Write reliability setting register	WR_REL_SET	1	R/W	[167]	0x1F	
Write reliability parameter register	WR_REL_PARAM	1	R	[166]	0x14	
Start sanitize operation	SANITIZE_START	1	W/E_P	[165]	0x00	
Manually start background operations	BKOPS_START	1	W/E_P	[164]	0x00	
Enable background operations handshake	BKOPS_EN	1	R/W	[163]	0x00	
H/W reset function	RST_n_FUNCTION	1	R/W	[162]	0x00	
HPI management	HPI_MGMT	1	R/W/E_P	[161]	0x00	
Partitioning support	PARTITIONING_SUPPORT	1	R	[160]	0x07	
Max enhanced area size	MAX_ENH_SIZE_MULT	3	R	[159:157]	0xEC	8GB (0x0001D2)
Partitions attribute	PARTITIONS_ATTRIBUTE	1	R/W	[156]	0x00	
Partitioning setting	PARTITION_SETTING_ COMPLETED	1	R/W	[155]	0x00	
General purpose partition size	GP_SIZE_MULT	12	R/W	[154:143]	0x00	
Enhanced user data area size	ENH_SIZE_MULT	3	R/W	[142:140]	0x00	
Enhanced user data start address	ENH-START_ADDR	4	R/W	[139:136]	0x00	
Reserved	–	1	–	[135]	–	
Bad block management mode	SEC_BAD_BLK_MGMNT	1	R/W	[134]	0x00	
Production state awareness	PRODUCTION_ STATE_AWARENESS	1	R/W/E	[133]	0x00	
Package case temperature is controlled	TCASE_SUPPORT	1	W/E_P	[132]	0x00	
Periodic wake-up	PERIODIC_WAKEUP	1	R/W/E	[131]	0x00	
Program CID/CSD in DDR mode support	PROGRAM_CID_CSD_ DDR_SUPPORT	1	R	[130]	0x01	
Reserved	–	2	–	[129:128]	–	
Vendor Specific Fields	VENDOR_SPECIFIC_FIELD	64		[127:64]	0x00	
Native sector size	NATIVE_SECTOR_SIZE	1	R	[63]	0x00	
Sector size emulation	USE_NATIVE_SECTOR	1	R/W	[62]	0x00	
Sector size	DATA_SECTOR_SIZE	1	R	[61]	0x00	
1st initialization after disabling sector size emulation	INI_TIMEOUT_EMU	1	R	[60]	0x00	

Table 5-13 Typical EXT_CSD Register (Continued)

Name	Field	Byte	Type	Slice	Value	Note
Modes Segment						
Class 6 commands control	CLASS_6_CTRL	1	R/W/E_P	[59]	0x00	
Number of addressed group to be released	DYNCAP_NEEDED	1	R	[58]	0x00	
Exception events control	EXCEPTION_EVENTS_CTRL	2	R/W/E_P	[57:56]	0x00	
Exception events status	EXCEPTION_EVENTS_ STATUS	2	R	[55:54]	0x00	
Extended partitions attribute	EXT_PARTITIONS_ATTRIBUTE	2	R/W	[53:52]	0x00	
Context configuration	CONTEXT_CONF	15	R/W/E_P	[51:37]	0x00	
Packed command status	PACKED_COMMAND_STATUS	1	R	[36]	0x00	
Packed command failure index	PACKED_FAILURE_INDEX	1	R	[35]	0x00	
Power off notification	POWER_OFF_NOTIFICATION	1	R/W/E_P	[34]	0x00	
Control to turn the cache ON/OF	CACHE_CTRL	1	R/W/E_P	[33]	0x00	
Flushing of the cache	FLUSH_CACHE	1	W/E_P	[32]	0x00	
Reserved	–	1	–	[31]	–	
Mode config	MODE_CONFIG	1	R/W/E_P	[30]		
Mode operation codes	MODE_OPERATION_CODES	1	W/E_P	[29]	0x00	
Reserved	–	2	–	[28:27]	–	
FFU status	FFU_STATUS	1	R	[26]	0x00	
Pre loading data size	PRE_LOADING_ DATA_SIZE	4	R/W/E_P	[25:22]	→	8GB (003B0000)
Max pre loading data size	MAX_PRE_LOADING_ DATA_SIZE	4	R	[21:18]	→	8GB (003B0000)
Product state awareness enablement	PRODUCT_STATE_ AWARENESS_ ENABLEMENT	1	R/W/E & R	[17]	0x03	
Secure removal type	SECURE_REMOVAL_TYPE	1	R/W/E &R	[16]	0x09	
Command Queue Mode Enable	CMDQ_MODE_EN	1	R/W/E_P	[15]	0x00	
Reserved	–	15	–	[14:0]	–	

Note:

1.The following is for the type of the EXT_CSD Register entries in the Table 5-14.

R: Read only.

W: One time programmable and not readable.

R/W: One time programmable and readable.

W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.

R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.

R/W/C_P: Writable after value cleared by power failure and HW/reset assertion (the value not cleared by CMD0 reset) and readable.

R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.

W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable.

5.3 AC Parameter

Timing Parameter

Table 5-14 Timing Parameter

Timing Paramter		Max. Value
Initialization Time (tINIT)	Normal [1)]	1 sec
	After partition setting [2)]	3 sec
Read Timeout		100 ms
Write Timeout		350 ms
Erase Timeout		20 ms
Force Erase Timeout		3 min
Secure Erase Timeout		6 sec
Secure Trim step Timeout		6 sec
Trim Timeout		600 ms
Partition Switching Timeout (after Init)		10 ms
Power Off Notification (Short) Timeout		100 ms
Power Off Notification (Long) Timeout		600 ms

Notes:

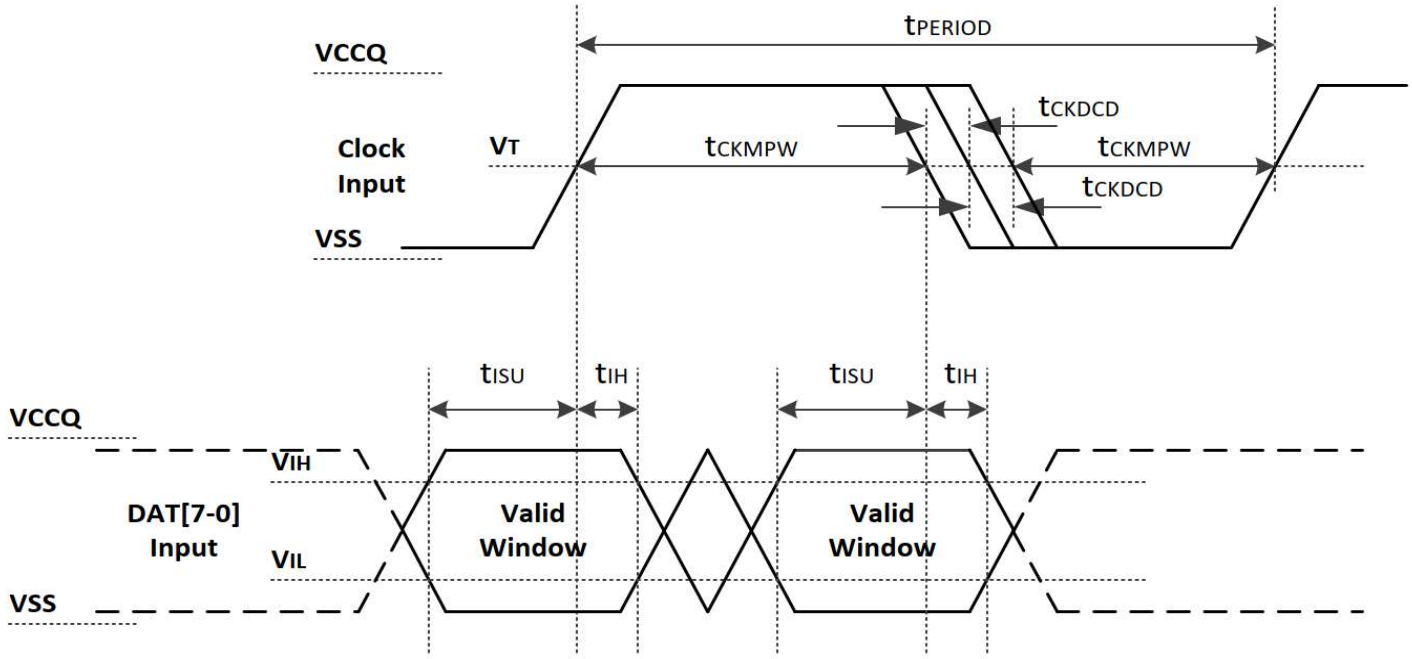
1.Normal Initialization Time without partition setting.

2.For the Initialization Time after partition setting, refer to INI_TIMEOUT_AP in EXT_CSD register.

3.All those Timeout Values specified in the above Table are only for testing purposes under specific test case only and it can vary in real cases. Also, it may be affected may vary due to user environment.

Bus Timing Specification in HS400 mode
HS400 Device Input Timing

Figure 5-3 HS400 Device Input Timing Diagram



Notes:

1.t_{ISU} and t_{IH} are measured at $V_{IL\ (max)}$ and $V_{IH\ (min)}$.

2.V_{IH} denotes $V_{IH\ (min)}$ and V_{IL} denotes $V_{IL\ (max)}$.

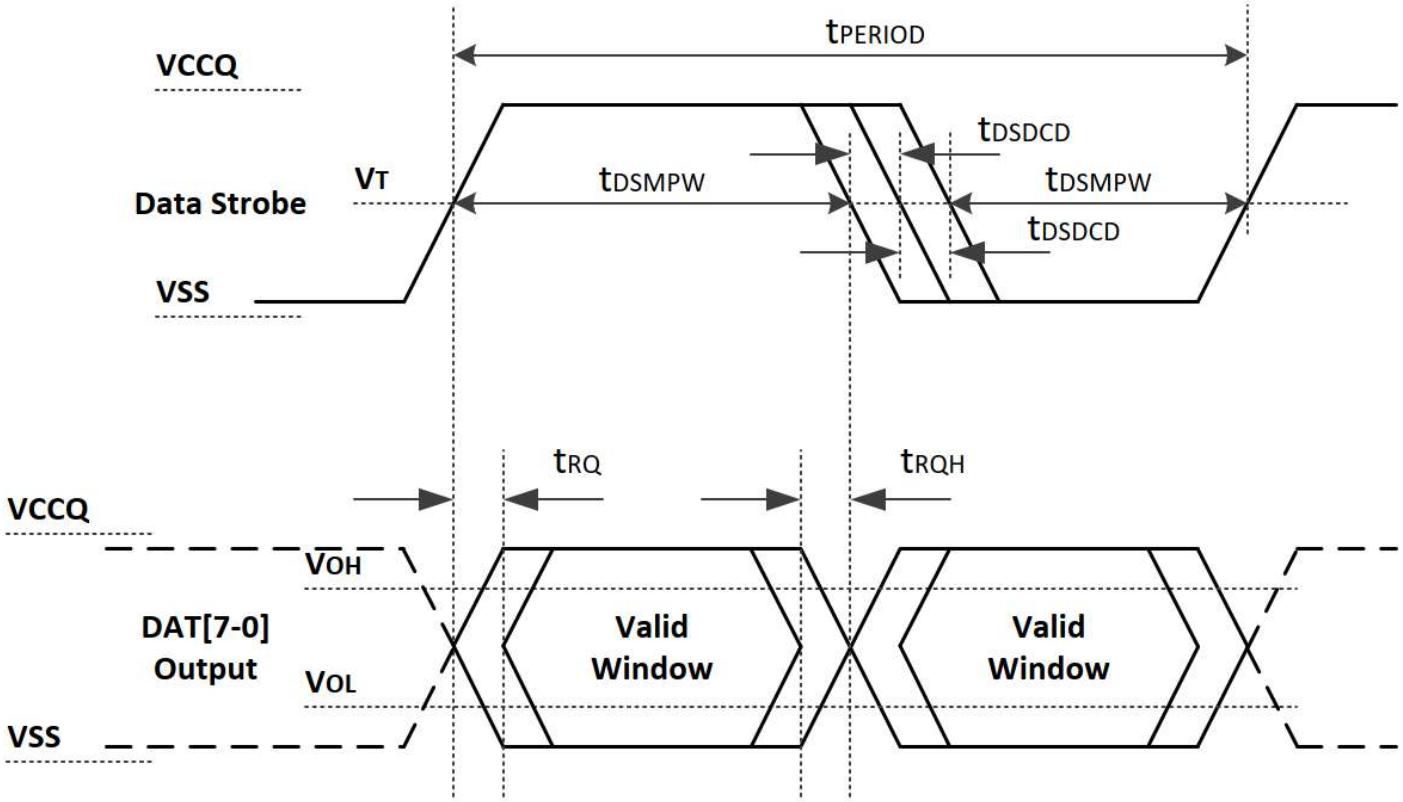
Table 5-15 HS400 Device Input Timing

Paramter	Symbol	Min	Max	Unit	Remark
Input CLK					
Cycle time datatransfer mode	t_{PERIOD}	5	–	ns	200MHz(Max), betweenwith respect to V_T.
Slew rate	SR	1.125	–	V/ns	
Duty cycle distortion	t_{CKDCD}	0.0	0.3	ns	
Minimum pulse width	t_{CKMPW}	2.2	–	ns	
Input DAT (referenced to CLK)					
Input set-up time	t_{ISUddr}	0.4	–	ns	
Input hold time	t_{IHddr}	0.4	–	ns	
Slew rate	SR	1.125	–	V/ns	

HS400 Device Onput Timing

Data Strobe is used to read data (data read and CRC status response read) in HS400 mode. The device output value of Data Strobe is “High-Z” when the device is not in outputting data(data read, CRC status response). Data Strobe is toggled only during data read period.

Figure 5-4 HS400 Device Output Timing Diagram



Note:

1.V_{OH} denotes $V_{OH\ (min)}$ and V_{OL} denotes $V_{OL\ (max)}$.

Table 5-16 HS400 DeviceOutput Timing

Paramter	Symbol	Min	Max	Unit	Remark
Data Strobe					
Cycle time datatransfer mode	t_{PERIOD}	5	–	ns	200MHz(Max), betweenwith respect to V_T.
Slew rate	SR	1.125	–	V/ns	
Duty cycle distortion	t_{CKDCD}	0.0	0.2	ns	
Minimum pulse width	t_{CKMPW}	2.0	–	ns	
Read pre-amble	t_{RPRE}	0.4	–	t_{PERIOD}	
Read post-amble	t_{RPST}	0.4	–	t_{PERIOD}	
Output DAT (referenced to Data Strobe)					
Output skew	t_{RQ}	–	0.4	ns	
Output hold skew	t_{RQH}	–	0.4	ns	
Slew rate	SR	1.125	–	V/ns	

Bus Signal Levels

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.

Figure 5-5 Bus Signal Levels

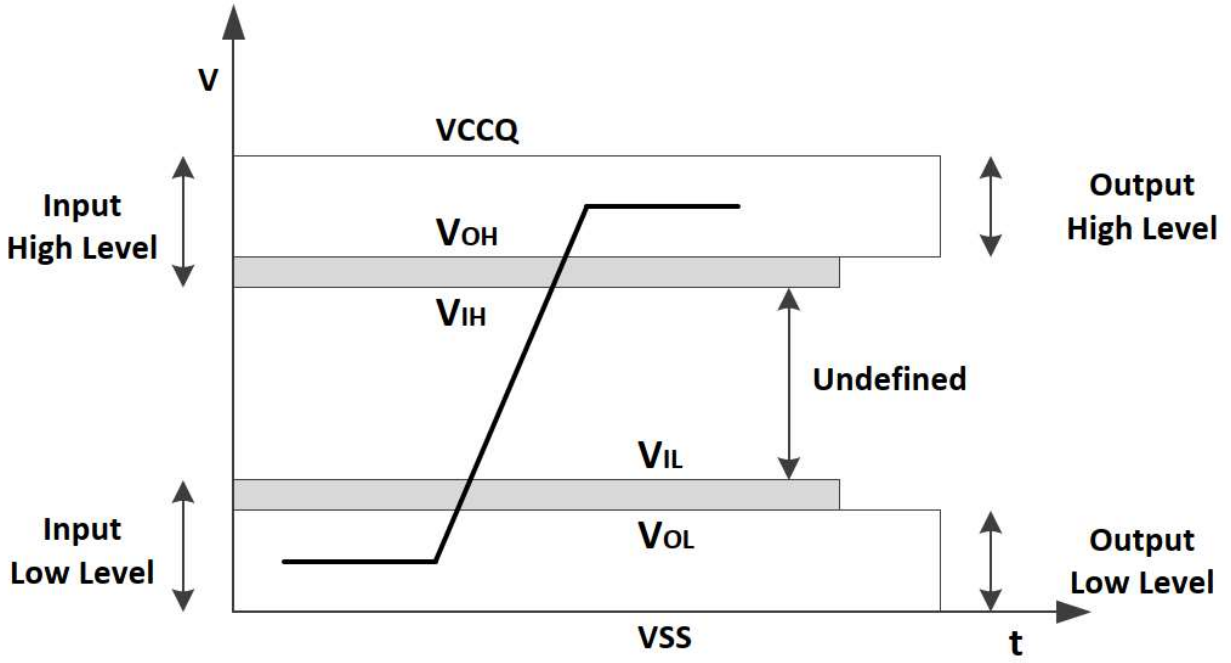


Table 5-17 Bus Signal Levels

Paramter	Symbol	Min	Max	Unit	Remark
Open-drain mode					
Output HIGH voltage	V_{OH}	V_{CCQ} – 0.2	–	V	
Output LOW voltage	V_{OL}	–	0.3	V	I_{OL} = TBD
Push-pull mode (High-voltage eMMC)					
Output HIGH voltage	V_{OH}	0.75 x V_{CCQ}	–	V	I_{OH} = –100uA @ V_{CCQ} min
Output LOW voltage	V_{OL}	–	0.125 x V_{CCQ}	V	I_{OL} = 100uA @ V_{CCQ} min
Input HIGH voltage	V_{IH}	0.625 x V_{CCQ}	V_{CCQ} + 0.3	V	
Input LOW voltage	V_{IL}	V_{SS} – 0.3	0.25 x V_{CCQ}	V	

Note:

1. Because VOH depends on external resistance value (including outside the package), this value does not apply as device specification. Host is responsible to choose the external pull-up and open drain resistance value to meet VOH Min value.

5.4 DC Parameter

Power Consumption

Table 5-18 Active Power Consumption during operation

Density (GB)	NAND Type (MLC)	CTRL (Max RMSmA)	NAND (Max RMS,mA)
8	64Gb x1	120	120

Notes:

1.Power Measurement conditions: Bus configuration =x8 @200MHz DDR.

2.Typical value is measured at V_{CC}/V_{CCQ}=3.3V, TA=25°C. Not 100% tested.

3.The measurement for max RMS current is the average RMS current consumption over a period of 100ms.

Table 5-19 Standby Power Consumption in auto power saving mode and standby state

Density (GB)	NAND Type (MLC)	CTRL (Ave. RMS, uA)		NAND (Max RMS,mA)	
		25°C (Typ)	85°C	25°C (Typ)	85°C
8	64Gb x1	130	800	40	50

Notes:

1.Power Measurement conditions: Bus configuration =x8, No CLK.

2.Typical value is measured at V_{CC}/V_{CCQ}=3.3V, TA=25°C. Not 100% tested.

Table 5-20 Sleep Power Consumption in Sleep State

Density (GB)	NAND Type (MLC)	CTRL (uA)		NAND (uA)
		25°C (Typ)	85°C	
8	64Gb x1	130	800	TBD [3]

Notes:

1.Power Measurement conditions: Bus configuration =x8, No CLK.

2.Typical value is measured at V_{CC}/V_{CCQ}=3.3V, TA=25°C. Not 100% tested.

3.In auto power saving mode, NAND power can not be turned off, However in sleep mode NAND power can be turned off. If NAND power is alive, NAND power is same with that of the Standby state.

Supply Voltage

Table 5-21 Supply Voltage

Symbol	Min (V)	Max (V)
V_{CCQ}	2.7	3.6
V_{CC}	2.7	3.6
V_{SS}	-0.5	0.5

Bus Signal Line Load

The total capacitance CL of each line of the eMMC bus is the sum of the bus master capacitance CHOST, the bus capacitance CBUS itself and the capacitance CDEVICE of the eMMC connected to this line:

$$C_L = C_{HOST} + C_{BUS} + C_{DEVICE}$$

The sum of the host and bus capacitances should be under 20pF.

Table 5-22 Bus SIgnal Line Load

Paramter	Symbol	Min	Typ	Max	Unit	Remark
Pull-up resistance for CMD	R_{CMD}	4.7		100	KOhm	to prevent bus floating
Pull-up resistance for DAT0-DAT7	R_{DAT}	10		100	KOhm	to prevent bus floating
Internal pull up resistance DAT1-DAT7	R_{int}	10		150	KOhm	to prevent unconnected lines floating
Single Device capacitance	C_{DEVICE}			6	pF	
Maximum signal line inductance				16	nHV	f_{PP}<= 52 MHz

Table 5-23 Capacitance and Resistance for HS400 mode

Paramter	Symbol	Min	Typ	Max	Unit	Remark
Bus signal line capacitance	C_L			13	pF	Single Device
Single Device capacitance	C_{DEVICE}			6	pF	
Pull-down resistance for Data Strobe	$R_{Data\ Strobe}$	10		100	KOhm	

5.5 Power Delivery And Capacitor Specifications

Power Domains

Xincun 8GB eMMC has three power domains assigned to V_{CCQ}, V_{CC} and V_{DDI_M}, as shown below.

Table 5-24 Power Domains

Symbol	Power Domain	Comments
V_{CCQ}	Host Interface	
V_{CC}	Memory	
V_{DDI_M}	Internal	V_{DDI_M} is the internal regulator connection to an external decoupling capacitor.

Capacitor Connection Guidelines

It is recommended to place the following capacitors on V_{CC}& V_{CCQ} domains:

- C_1/C_3= 4.7uF

◆E.g.:

Manufacturer	Manufacturer P/N
MURATA	GRM185R60J475ME15D
TAIYO YUDEN	JMK107BJ475MK-T

● C_2/C_4/C_6= 0.1uF
◆E.g.:

Manufacturer	Manufacturer P/N
MURATA	GRM155R71A104KA01D
KYOCERA	CM05X5R104K06AH

For VCC (3.3V), it is recommended to place:
● C_5(VCC) = 10uF
◆E.g.:

Manufacturer	Manufacturer P/N
TAIYO YUDEN	JMK107ABJ106MAHT
PANASONIC	ECJ-1VB0J106M
SAMSUNG	CL10A106MQ8NNNC

Capacitors Type:
- SMT-Ceramic
- X5R
- 6.3V
- Min height – 0.55mm
- Foot Print: 0402 or above

Suggested capacitors should be located as close to the supply ball as possible and they will eliminate as much trace inductance effects as possible and give cleaner voltage supply to device. Also, they reduce lead length and eliminate noise coupling onto through-hole components, which may have effects of antenna.

Make all of the power (high current) traces as short, direct, and thick as possible and put all capacitors as close to each other as possible, for reducing EMI radiated by the power traces due to the high switching currents through them. Again, it shall also reduce lead inductance and resistance as well and thus, noise spikes, ringings, and resistive losses which cause voltage errors.

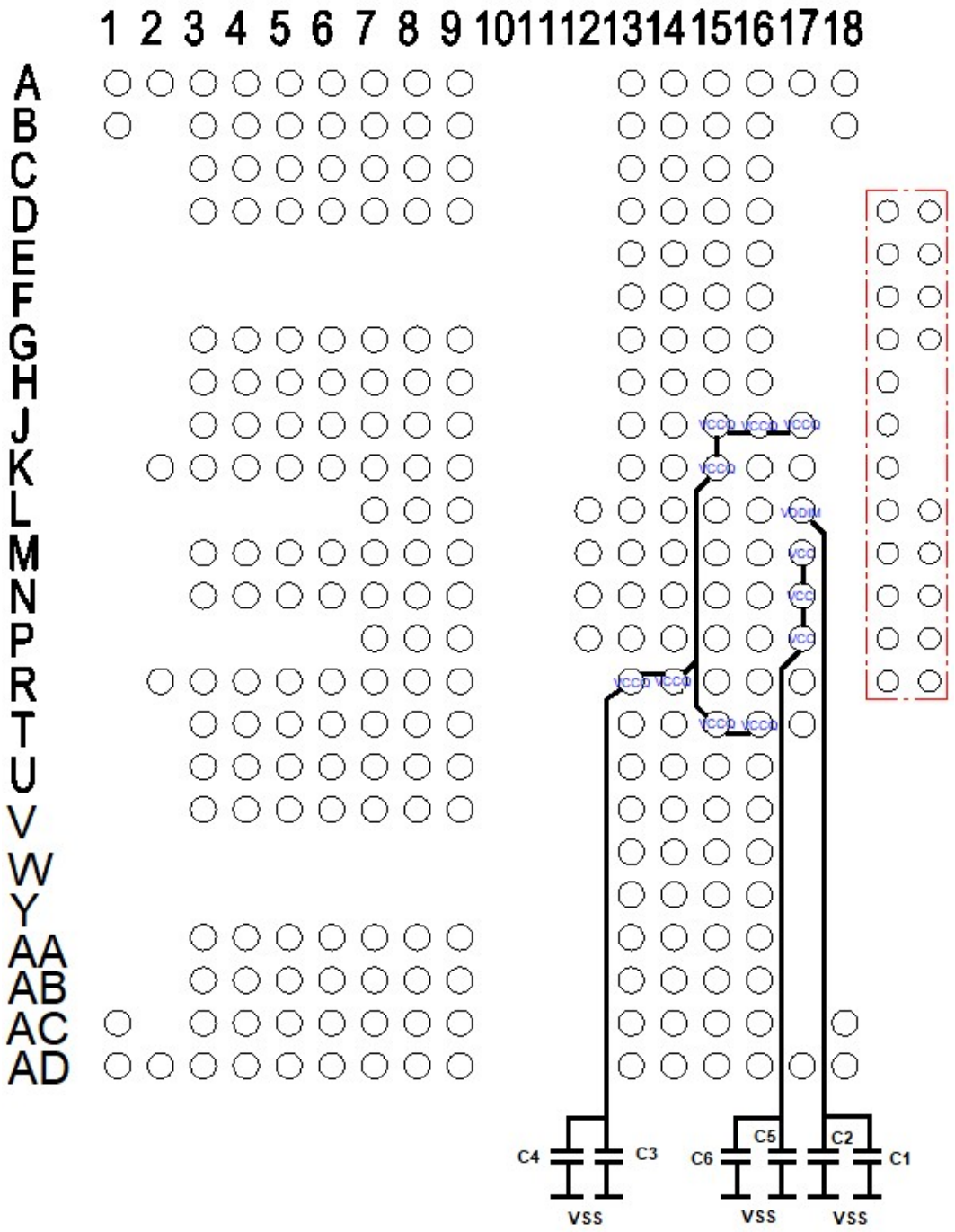
For the ground of these capacitors, they should be connected close together directly to a ground plane and it is also recommended to have a ground plane on both sides of the PCB, to reduce noise by eliminating ground loop errors as well.

The loop inductance per capacitor shall not exceed 3nH (both on V_{CC}/V_{CCQ}& V_{SS} loops).

Multiple via connections are recommended per each capacitor pad.

Signal Traces:
- Data, CMD, CLK & RCLK bus trace length mismatch should be minimal (up to +/-1mm).
- Traces should be 50ohm controlled impedance.

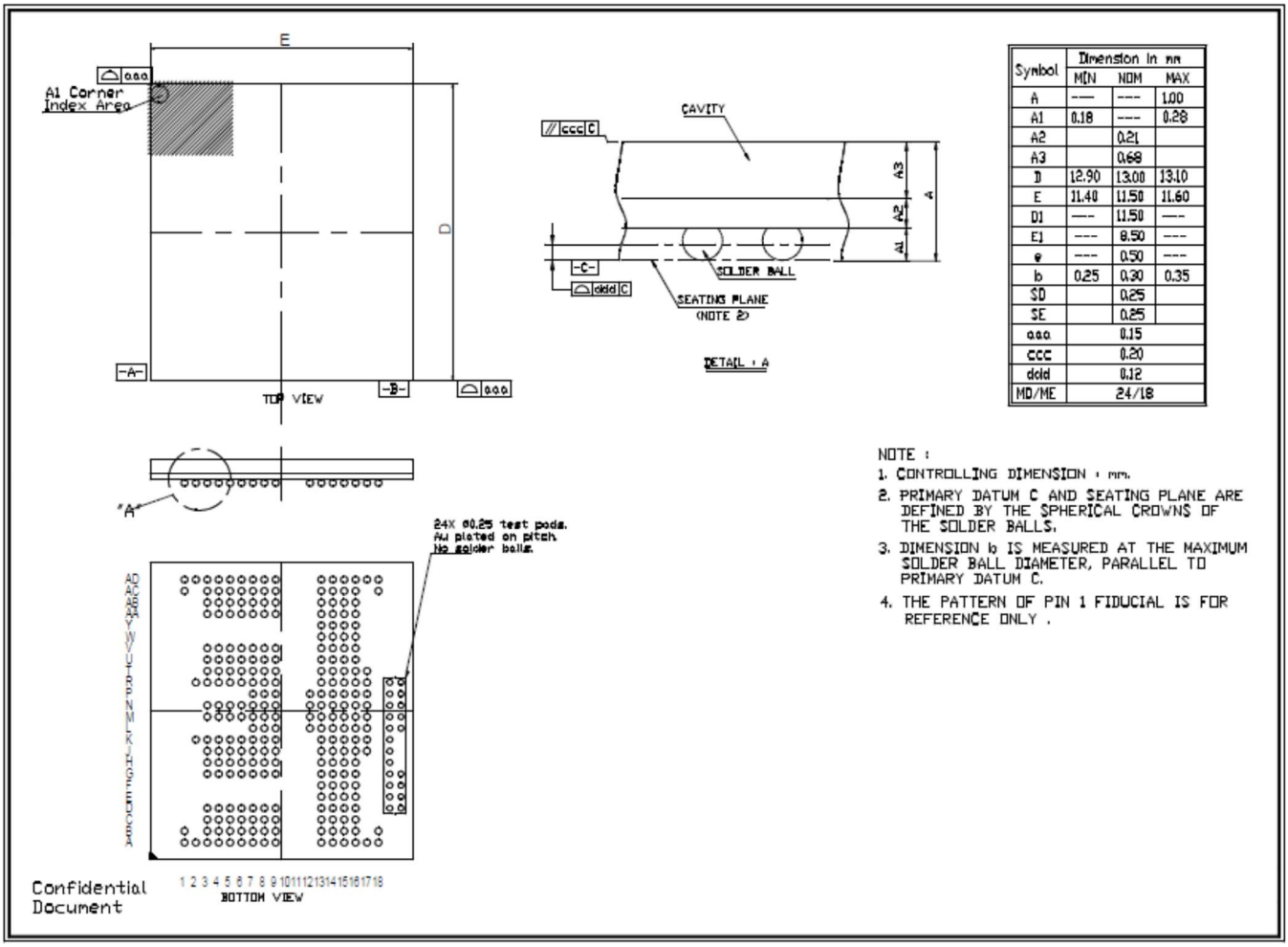
Figure 5-25 Recommended Power Domain Connections



Paramter	Symbol	Unit	Value
V_{DDI_M}	C1 + C2	uF	4.7 + 0.1
V_{CCQ}	C3 + C4	uF	4.7 + 0.1
V_{CC}	C5 + C6	uF	10 + 0.1

Note:
Coupling capacitor should be connected with V_{DD} and V_{SS} as closely as possible.

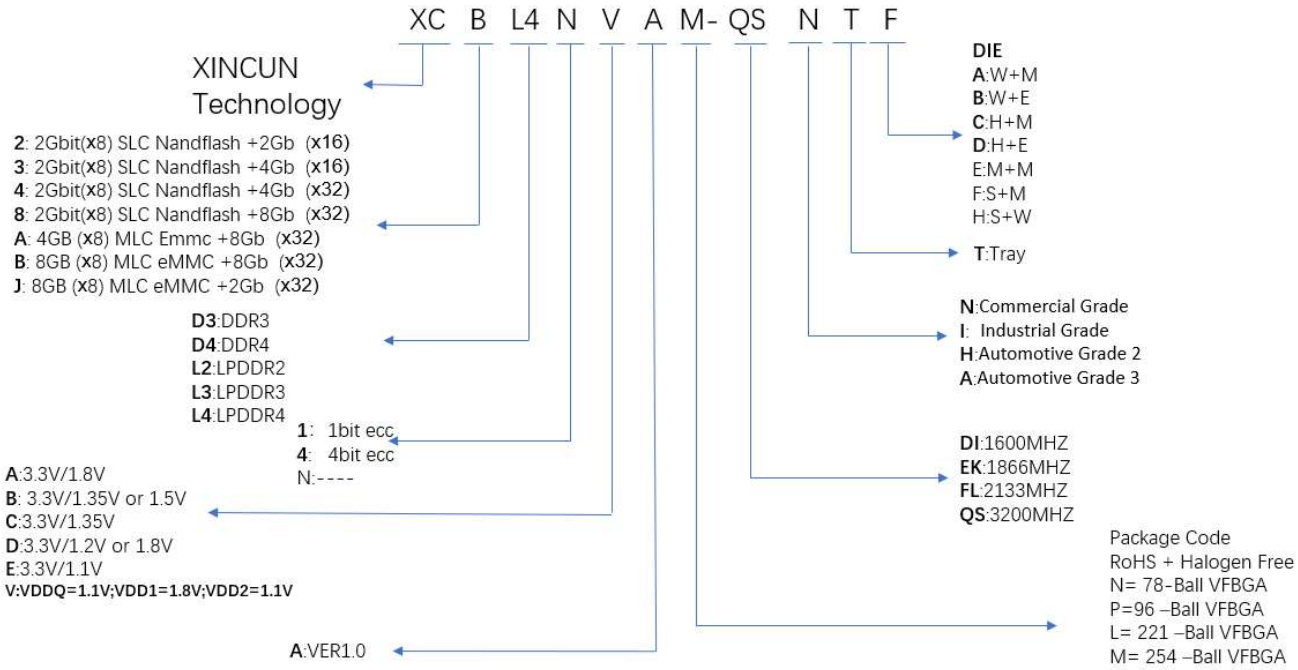
6. PACKAGE DIMENSION (254 Ball FBGA, 11.5x13x1.0mm)



Symbol	Dimension in mm		
	MIN	NOM	MAX
A	---	---	1.00
A1	0.18	---	0.28
A2		0.21	
A3		0.68	
D	12.90	13.00	13.10
E	11.40	11.50	11.60
D1	---	11.50	---
E1	---	8.50	---
e	---	0.50	---
b	0.25	0.30	0.35
SD		0.25	
SE		0.25	
aaa	0.15		
ccc	0.20		
ddd	0.12		
MD/ME	24/18		

NOTE :
1. CONTROLLING DIMENSION : mm.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY .

7. PART NUMBER LOGIC



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