NAND MCP 规格书

XC3D31BAH-DINA

NAND FLASH 2Gb (256x8) + DDR3 (L) SDRAM 4Gb (256x16)
1bit ECC,1600MHZ,FBGA 119 balls, 10 x13 mm x1.3mm

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Revision

Rev	Changes	Date	Note
Rev1.0	Initial release	2020.5.18	
Rev1.1	Update logo	2023.5.20	

1. 产品介绍：

XC3D31BAH-DINA 是一款多芯片封装内存(MCP),集成了 1 个 2Gb SLC NAND 和 1 个 4Gb DDR3(L) SDRAM. 擦写次数可达到 10 万次，DDR3 主频可支持 1600MHZ.具有节省空间的优势，让您的产品更加小型化。

1.1 产品特性：

- Nand Flash: 2G bits (256M x 8-bit).
- DDR3(L) SDRAM: 4G bits (32M x 8-Bank x16-bit).
- 擦写次数达 10 万次/程序循环.
- 支持 1bit ECC.
- 十年数据保存.
- 页面大小：2112 字节（2048+64 字节）.
- 块大小：64 页（128K+4K 字节）.
- DRAM 速率可达到 1600MHZ.

NAND 读取性能

- 随机读取速度：25us.
- 顺序读取周期：25ns.

NAND 写擦性能

- 页面程序时间：250us(typ.).
- 块擦除时间:2ms(typ.).

RAM 性能

- 8n-bit 预取架构 .
- 差分时钟输入（CK,CK#）.
- 可编程 CAS 读延迟 CL.
- 可实时选择 BC4 或 BL8(OTF).

电源输入

- NAND VCC: 3.3V (电压范围: 2.7-3.6V).
- DRAM VCC:1.35V(电压范围: 1.283-1.45V)/向后兼容 1.5V(电压范围: 1.425-1.575V).

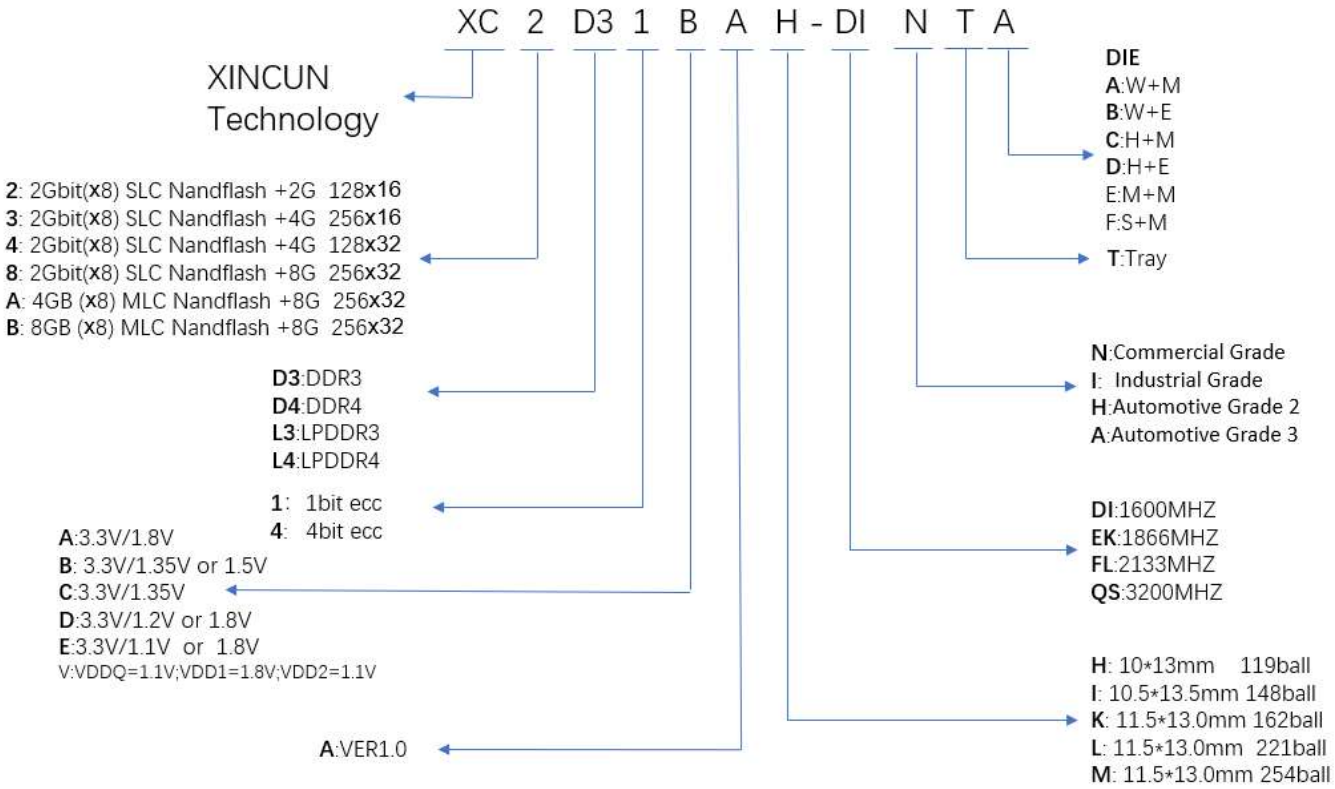
封装尺寸

- TFBGA 10 x13 x1.3mm.
- 119 Balls.
- Ball Pitch: 0.8mm.
- 重量: 283mg+/-5mg.

温度

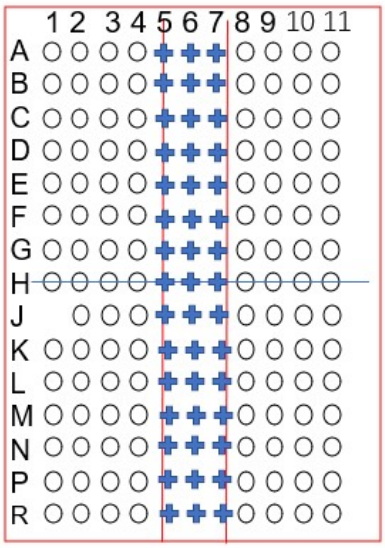
- 工作温度:-10 to +85 ℃.
- 储存温度:-55 to +125 ℃.

XINCUN 命 名 规 则 说 明



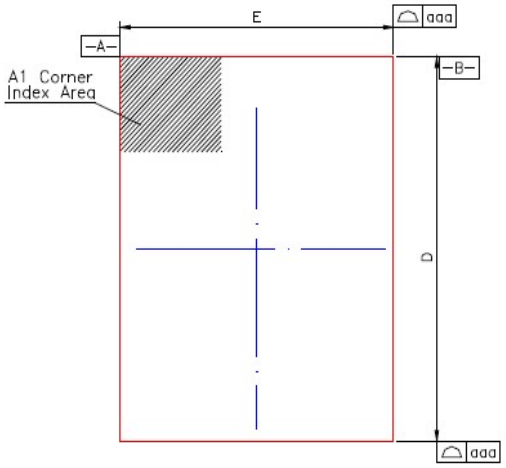
芯片引脚定义

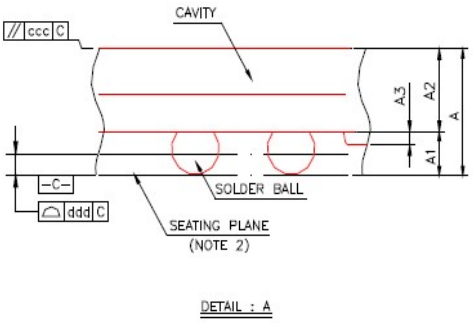
TOP VIEW



	1	2	3	4	5	6	7	8	9	10	11
A	NAF_WP-	DR3_VDD	NC	DR3_VSS				DR3_VSSQ	DR3_DQS01-	DR3_VDDQ	NAF_RYBY-
B	NAF_WE-	DR3_DQ14	DR3_VSSQ	DR3_DM01				DR3_DQS01	DR3_VSSQ	DR3_DQ15	NAF_RE-
C	NAF_ALE	DR3_VDDQ	DR3_DQ09	DR3_VDDQ				DR3_VDDQ	DR3_DQ08	DR3_VDDQ	NAF_CE-
D	NAF_CLE	DR3_DQ12	DR3_VSSQ	DR3_DQ11				DR3_DQ10	DR3_VSSQ	DR3_DQ13	NAF_VCC
E	NAF_VSS	DR3_VDD	DR3_VSSQ	DR3_VSS				DR3_VSSQ	DR3_DQS00-	DR3_VDDQ	NC
F	DDR3_VDD	DR3_DQ06	DR3_VSSQ	DR3_DM00				DR3_DQS00	DR3_VSSQ	DR3_DQ07	DR3_ZQ
G		DR3_VDDQ	DR3_DQ01	DR3_VDDQ				DR3_VDDQ	DR3_DQ00	DR3_VDDQ	DR3_VSS
H	NC	DR3_DQ04	DR3_VSSQ	DR3_DQ03				DR3_DQ02	DR3_VSSQ	DR3_DQ05	DR3_VSS
J	DDR3_VDD	DR3_VDD	DR3_VREFCA	DR3_VSS				DR3_VSS	DR3_CLK	DR3_VDD	NC
K	NAF_VSS	DR3_VDDQ	DR3_CKE	DR3_WE-				DR3_RAS-	DR3_CLK-	DR3_ODT	NAF_VCC
L	NC	DR3_BA02	DR3_BA00	DR3_BA01				DR3_CAS-	DR3_CS-	DR3_VDDQ	NC
M	NAF_DQ03	DR3_RESET-	DR3_ADR10/AP	DR3_ADR01				DR3_ADR02	DR3_ADR00	DR3_VDD	NAF_DQ04
N	NAF_DQ02	DR3_VSS	DR3_ADR03	DR3_ADR05				DR3_ADR06	DR3_ADR04	DR3_VSSQ	NAF_DQ05
P	NAF_DQ01	DR3_VREFDQ	DR3_ADR07	DR3_ADR09				DR3_ADR11	DR3_ADR08	DR3_VSS	NAF_DQ06
R	NAF_DQ00	DR3_VDD	DR3_ADR12/BC-	DR3_ADR14				NC	DR3_ADR13	NC	NAF_DQ07

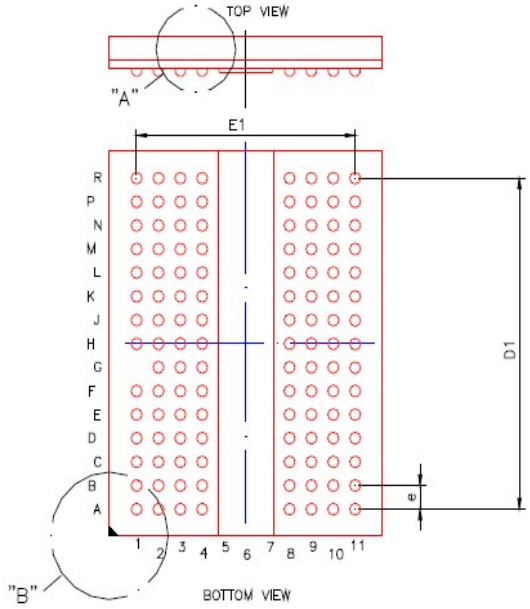
封装尺寸（119 balls TFBGA 10 x13 x1.3mm）

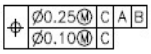


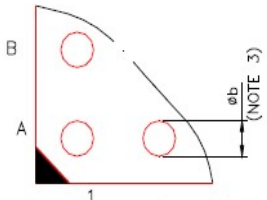


DETAIL : A

Symbol	Dimension in mm		
	MIN	NOM	MAX
A	---	1.20	1.30
A1	0.30	0.35	0.40
A2	---	---	0.96
A3	---	0.15	---
D	12.90	13.00	13.10
E	9.90	10.00	10.10
D1	---	11.20	---
E1	---	8.00	---
e	---	0.8	---
b	0.40	0.45	0.50
aaa	0.15		
ccc	0.20		
ddd	0.12		
MD/ME	15/11		







DETAIL : B

NOTE :
1. CONTROLLING DIMENSION : mm.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY .

Pin Descriptions：

Type Symbol	Description	Type Symbol	Description
I	Input	P	Power
O	Output	G	Ground
I/O	Bi-direction	X	No connect (No function, don't care)

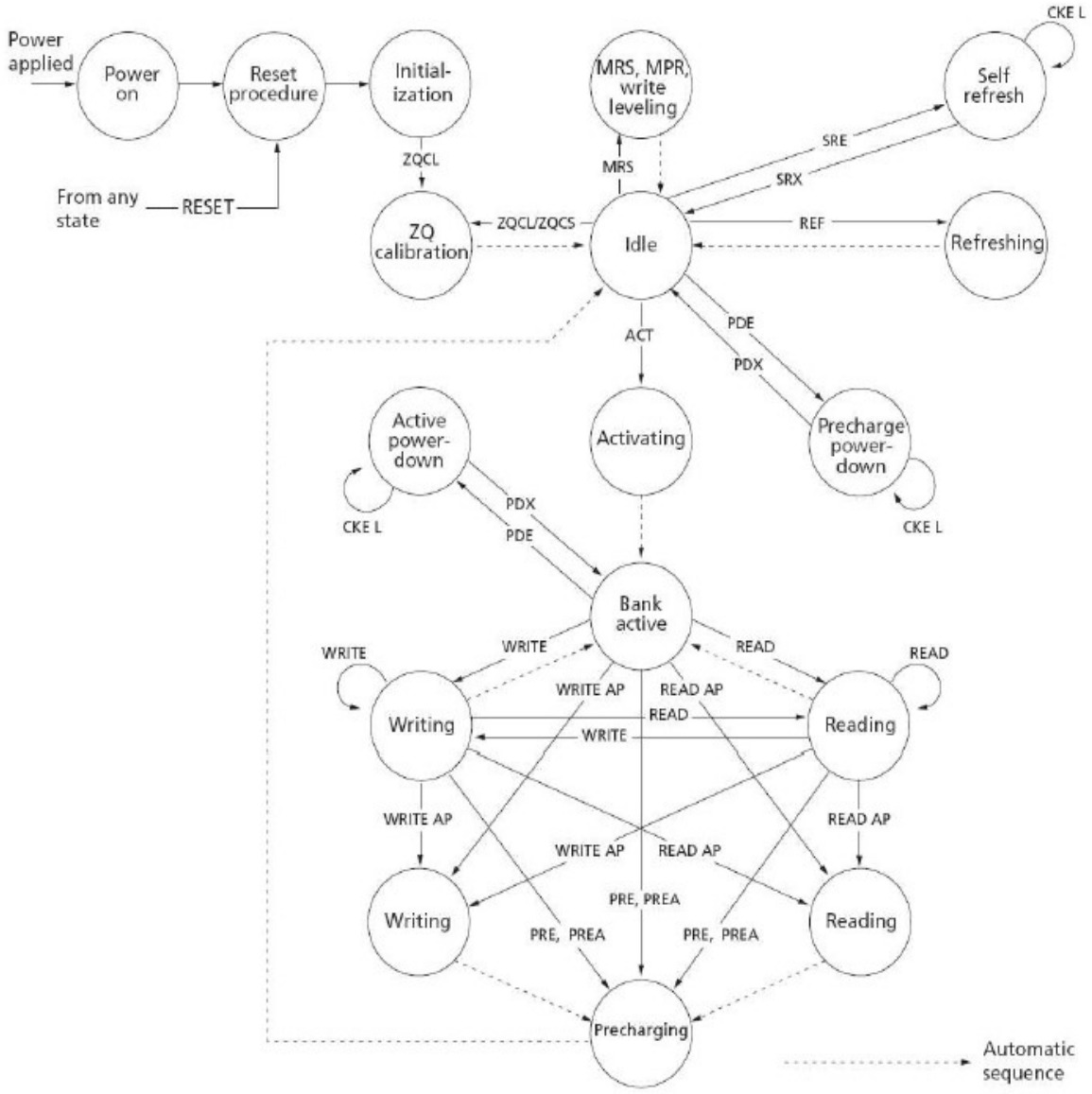
Net-Name	Type	Count	Description
DR3_ADR[00..14] (A0~A14)	I	15	**Address inputs:** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA [2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to V_{REFCA}. A12/BC#: When enabled in the mode register (MR), A12 is sampled during READ and WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH = BL8 or no burst chop, LOW = BC4). See Table 4-64.
DR3_BA[00..02] (BA0~BA2/ BA[2:0])	I	3	**Bank address inputs:** BA[2:0] define the bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. BA[2:0] are referenced to V_{REFCA}.
DR3_RESET- (RESET#)	I	1	**Reset:** RESET# is an active LOW CMOS input referenced to V_{SS}. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 × V_{DD} and DC LOW ≤ 0.2 × V_{DDQ}. RESET# assertion and de-assertion are asynchronous.
DR3_DQ[00..15] (DQ0~DQ15)	I/O	16	**Data Inputs/Output:** Bi-directional data bus, Referenced to V_{REFDQ}.
DR3_RAS-, DR3_CAS-, DR3_WE-	I	3	**Command inputs:** RAS#, CAS#, and WE# (along with CS#) define the command being entered and are referenced to V_{REFCA}.

DR3_CKE (CKE)	I	1	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. The specific circuitry that is enabled/disabled is dependent upon the DDR3(L) SDRAM configuration and operating mode. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle),or active power-down (row active in any bank). CKE is synchronous for power-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, RESET#, and ODT) are disabled during POWER-DOWN. Input buffers (excluding CKE and RESET#) are disabled during SELF REFRESH. CKE is referenced to V_{REFCA}.
DR3_CLK, DR3_CLK-(CK,CK#)	I	2	**Clock:** CK and CK# are differential clock inputs. All control and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data strobe (DQS, DQS#) is referenced to the crossings of CK and CK#.
DR3_CS- (CS#)	I	1	**Chip select:** CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external rank selection on systems with multiple ranks. CS# is considered part of the command
DR3_ODT (ODT)	I	1	**On-die termination:** ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3(L) SDRAM. When enabled in normal operation. The ODT input is ignored if disabled via the LOAD MODE command. ODT .
DR3_DQS00 (LDQS), DR3_DQS00-(/LDQS) DR3_DQS01 (UDQS), DR3_DQS01-(/UDQS) (DQS,DQS#)	I/O	4	**Data Strobe:** output with read data, input with write data. Edge aligned with read data, centered with write data. The data strobes DQS are paired with differential signals DQS#, respectively, to provide differential pair signaling to the system during both reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended.

DR3_DM00 (LDM) DR3_DM01 (UDM)	I	2	**Input data mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with the input data during a write access. Although the DM ball is input-only, the DM loading is designed to match that of the DQ and DQS balls. DM is
DR3_VREFCA (V_{REFCA})	P	1	**Reference voltage for control, command, and address:** V_{REFCA} must be maintained at all times (including self refresh) for proper device operation.
DR3_VREFDQ (V_{REFDQ})	P	1	**Reference voltage for data:** V_{REFDQ} must be maintained at all times (excluding self refresh) for proper device operation.
DR3_ZQ (ZQ)	P	1	**External reference ball for output drive calibration:** This ball is tied to external 240Ω resistor RZQ, which is tied to V_{SSQ}.
DR3_VDD (VDD)	P	8	Power Supply: 1.35V (1.283–1.45V) / Backward-compatible to 1.5V ±0.075V
DR3_VDDQ (VDDQ)	P	12	DQ Power Supply: 1.35V (1.283–1.45V) / Backward-compatible to 1.5V ±0.075V
DR3_VSS (VSS)	G	8	Ground
DR3_VSSQ (VSSQ)	G	12	DQ Ground
NC	X	8	Not Connect Pin (Don't Care)
NAF_ALE (ALE)	I	1	NAND FLASH Address Latch Enable. The Address Latch Enable activates the latching of the Address inputs in the Command Interface. When NAF_ALE is high, the inputs are latched on the rising edge of Write Enable.
NAF_CE- (CE#)	I	1	NAND FLASH Chip Enable. This signal controls selection of device. Active low.

NAF_CLE (CLE)	I	1	NAND FLASH Command Latch Enable. This signal controls the activation of sending operation mode command into the command register. When NAF_CLE is High, the command is latched into the command register from the I/O ports on the rising edge of the NAF_WE- signal.
NAF_DQ[00..07] (I/Ox)	I/O	8	NAND FLASH Address and Data I/O
NAF_RYBY- (R/B#)	O	1	NAND FLASH Ready/Busy. High: Ready, Low: Busy.
NAF_RE- (RE#)	I	1	NAND FLASH Read Enable, Active Low.
NAF_WE- (WE#)	I	1	NAND FLASH Write Enable, Active Low.
NAF_WP- (WP#)	I	1	NAND FLASH Write Protect, Active Low. This signal used to protect the device from inadvertent programming or erasing during power on/off transition. When Low, the internal high voltage generator is reset.
NAF_VCC (VCC)	P2	2	NAND FLASH Power Supply.
NAF_VSS (VSS)	G	2	NAND FLASH Ground.

State Diagram



ACT = ACTIVATE
MPR = Multipurpose register
MRS = Mode register set
PDE = Power-down entry
PDX = Power-down exit
PRE = PRECHARGE

PREA = PRECHARGE ALL
READ = RD, RDS4, RDS8
READ AP = RDAP, RDAPS4, RDAPS8
REF = REFRESH
RESET = START RESET PROCEDURE
SRE = Self refresh entry

SRX = Self refresh exit
WRITE = WR, WRS4, WRS8
WRITE AP = WRAP, WRAPS4, WRAPS8
ZQCL = ZQ LONG CALIBRATION
ZQCS = ZQ SHORT CALIBRATION

Functional Description

DDR3(L) SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is an 8n-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR3(L) SDRAM effectively consists of a single 8n-bit-wide, four-clock-cycle data transfer at the internal DRAM core and eight corresponding n-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

The differential data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the DDR3(L) SDRAM input receiver. DQS is center-aligned with data for WRITEs. The read data is transmitted by the DDR3(L) SDRAM and edge-aligned to the data strobes.

The DDR3(L) SDRAM operates from a differential clock (CK and CK#). The crossing of CK going HIGH and CK# going LOW is referred to as the positive edge of CK. Control, command, and address signals are registered at every positive edge of CK. Input data is registered on the first rising edge of DQS after the WRITE preamble, and output data is referenced on the first rising edge of DQS after the READ preamble.

Read and write accesses to the DDR3(L) SDRAM are burst-oriented. Accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE commands are used to select the bank and the starting column location for the burst access.

The device uses a READ and WRITE BL8 and BC4. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard DDR SDRAM, the pipelined, multibank architecture of DDR3(L) SDRAM allows for concurrent operation, thereby providing high bandwidth by hiding row precharge and activation time.

A self refresh mode is provided, along with a power-saving, power-down mode.

General Notes

- The functionality and the timing specifications discussed in this data sheet are for the DLL enable mode of operation (normal operation).
- Throughout this data sheet, various figures and text refer to DQs as “DQ.” DQ is to be interpreted as any and all DQ collectively, unless specifically stated otherwise.
- The terms “DQS” and “CK” found throughout this data sheet are to be interpreted as DQS, DQS# and CK, CK# respectively, unless specifically stated otherwise.
- Complete functionality may be described throughout the document; any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
- Any specific requirement takes precedence over a general statement.
- Any functionality not specifically stated is considered undefined, illegal, and not supported, and can result in unknown operation.
- Dynamic ODT has a special use case: when DDR3(L) devices are architected for use in a single rank memory array, the ODT ball can be wired HIGH rather than routed. Refer to the Dynamic ODT Special Use Case section.

Electrical Specifications

Absolute RatingS

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
V_{DD}	V_{DD} supply voltage relative to V_{SS}	–0.4	1.975	V	1
V_{DDQ}	V_{DD} supply voltage relative to V_{SSQ}	–0.4	1.975	V	
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	–0.4	1.975	V	
T_C	Operating case temperature	–10	95	℃	2, 3
T_{STG}	Storage temperature	–55	125	℃	

Notes:

1. V_{DD} and V_{DDQ} must be within 300mV of each other at all times, and V_{REF} must not be greater than 0.6 × V_{DDQ}. When V_{DD} and V_{DDQ} are <500mV, V_{REF} can be ≤300mV.

2. MAX operating case temperature. T_C is measured in the center of the package.

3. Device functionality is not guaranteed if the DRAM device exceeds the maximum T_C during operation.

Input/Output Capacitance

Input/Output Capacitance (DDR3L)

Capacitance Parameters	Symbol	DDR3-1066		DDR3-1333		DDR3-1600		Unit	Notes
		Min	Max	Min	Max	Min	Max		
CK and CK#	C_{CK}	0.8	1.6	0.8	1.4	0.8	1.4	pF	
ΔC: CK to CK#	C_{DCK}	0	0.15	0	0.15	0	0.15	pF	
Single-end I/O: DQ, DM	C_{IO}	1.4	2.5	1.4	2.3	1.4	2.2	pF	2
Differential I/O: DQS, DQS#,	C_{IO}	1.4	2.5	1.4	2.3	1.4	2.2	pF	
ΔC: DQS to DQS#	C_{DDQS}	0	0.2	0	0.15	0	0.15	pF	
ΔC: DQ to DQS	C_{DIO}	–0.5	0.3	–0.5	0.3	–0.5	0.3	pF	3
Inputs (CTRL, CMD, ADDR)	C_I	0.75	1.3	0.75	1.3	0.75	1.2	pF	4
ΔC: CTRL to CK	C_{DI_CTRL}	–0.5	0.3	–0.4	0.2	–0.4	0.2	pF	5
ΔC: CMD_ADDR to CK	$C_{DI\_CMD\_ADDR}$	–0.5	0.5	–0.4	0.4	–0.4	0.4	pF	6
ZQ pin capacitance	C_{ZQ}	–	3.0	–	3.0	–	3.0	pF	
Reset pin capacitance	C_{RE}	–	3.0	–	3.0	–	3.0	pF	

Notes:

1. $V_{DDQ} = V_{DD}$, $V_{REF} = V_{SS}$, f = 100 MHz, T_C = 25℃. $V_{OUT(DC)} = 0.5 \times V_{DDQ}$, V_{OUT} = 0.1V (peak-to-peak).

2. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.

3. $C_{DIO} = C_{IO(DQ)} - 0.5 \times (C_{IO(DQS)} + C_{IO(DQS\#)})$.

4. Excludes CK, CK#; CTRL = ODT, CS#, and CKE; CMD = RAS#, CAS#, and WE#; ADDR =A[*n*:0], BA[2:0].

5. $C_{DI\_CTRL} = C_{I(CTRL)} - 0.5 \times (C_{CK(CK)} + C_{CK(CK\#)})$.

6. $C_{DI\_CMD\_ADDR} = C_{I(CMD\_ADDR)} - 0.5 \times (C_{CK(CK)} + C_{CK(CK\#)})$.

Thermal Characteristics

Parameter/Condition	Value	Unit	Symbol	Notes
Operating case temperature	-10 to +85	℃	T_C	1, 2, 3
	-10 to +95	℃	T_C	1, 2, 3, 4

Notes:

1. MAX operating case temperature T_C is measured in the center of the package, as shown below.
2. A thermal solution must be designed to ensure that the device does not exceed the maximum T_C during operation.
3. Device functionality is not guaranteed if the device exceeds maximum T_C during operation.
4. If T_C exceeds 85°C, the DRAM must be refreshed externally at 2x refresh, which is a 3.9us interval refresh rate. The use of self refresh temperature (SRT) or automatic self refresh (ASR), must be enabled.

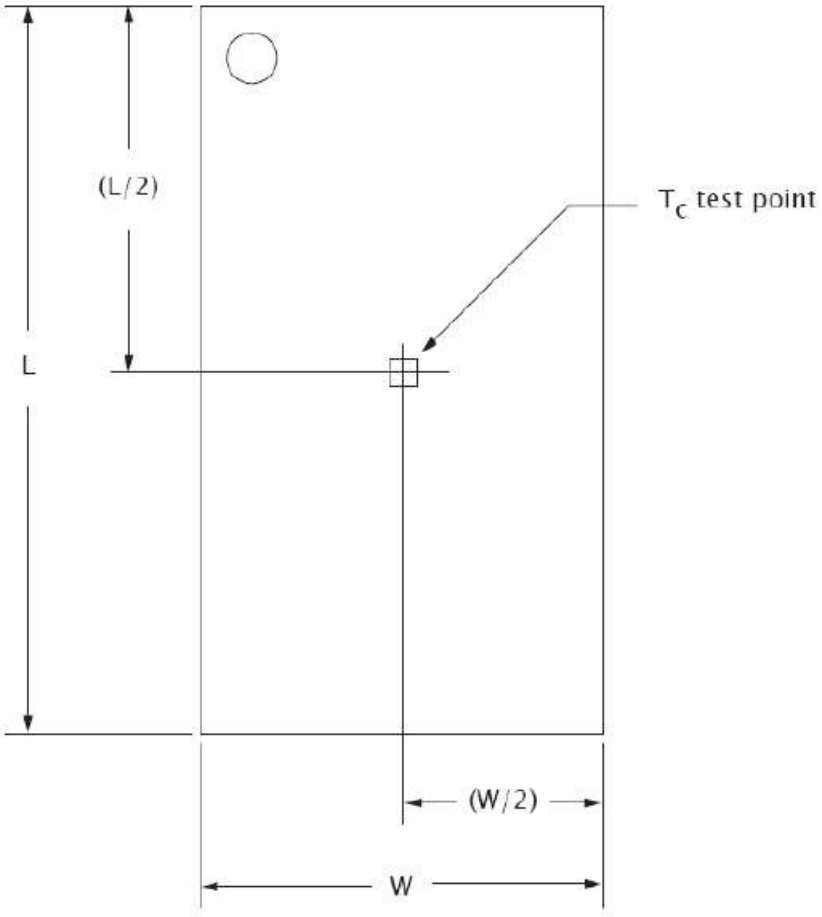


Figure 4-1: Thermal Measurement Point

Electrical Specifications – I_{DD} Specifications and Conditions

Within the following I_{DD} measurement tables, the following definitions and conditions are used, unless stated otherwise:

- LOW: $V_{IN} \leq V_{IL(AC)max}$; HIGH: $V_{IN} \geq V_{IH(AC)min}$.
- Midlevel: Inputs are $V_{REF} = V_{DD}/2$.
- R_{ON} set to RZQ/7 (34Ω)。
- $R_{TT,nom}$ set to RZQ/6 (40Ω).
- $R_{TT(WR)}$ set to RZQ/2 (120Ω).
- Q_{OFF} is enabled in MR1.
- ODT is enabled in MR1 ($R_{TT,nom}$) and MR2 ($R_{TT(WR)}$).
- External DQ/DQS/DM load resistor is 25Ω to $V_{DDQ}/2$.
- Burst lengths are BL8 fixed.
- AL equals 0 (except in I_{DD7}).
- I_{DD} specifications are tested after the device is properly initialized.
- Input slew rate is specified by AC parametric test conditions.
- Optional ASR is disabled.
- Read burst type uses nibble sequential (MR0[3] = 0).
- Loop patterns must be executed at least once before current measurements begin.

Timing Parameters Used for I_{DD} Measurements – Clock Units

I_{DD} Parameter	DDR3(L)-1066	DDR3(L)-1333	DDR3(L)-1600	Unit
	7-7-7	9-9-9	10-10-10	
tCK (MIN) I_{DD}	1.875	1.5	1.25	ns
CL I_{DD}	7	9	10	CK
tRCD (MIN) I_{DD}	7	9	10	CK
tRC (MIN) I_{DD}	27	33	38	CK
tRAS (MIN) I_{DD}	20	24	28	CK
tRP (MIN)	7	9	10	CK
tFAW	27	30	32	CK
tRRD I_{DD}	6	5	6	CK
tRFC	139	174	208	CK

I_{DD0} Measurement Loop

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data
Toggling	Static HIGH	0	0	ACT	0	0	1	1	0	0	0	0	0	0	0	–
			1	D	1	0	0	0	0	0	0	0	0	0	0	–
			2	D	1	0	0	0	0	0	0	0	0	0	0	–
			3	D#	1	1	1	1	0	0	0	0	0	0	0	–
			4	D#	1	1	1	1	0	0	0	0	0	0	0	–
				Repeat cycles 1 through 4 until *n*RAS - 1; truncate if needed												
			*n*RAS	PRE	0	0	1	0	0	0	0	0	0	0	0	–
				Repeat cycles 1 through 4 until *n*RC - 1; truncate if needed												
			*n*RC	ACT	0	0	1	1	0	0	0	0	0	F	0	–
			*n*RC + 1	D	1	0	0	0	0	0	0	0	0	F	0	–
			*n*RC + 2	D	1	0	0	0	0	0	0	0	0	F	0	–
			*n*RC + 3	D#	1	1	1	1	0	0	0	0	0	F	0	–
			*n*RC + 4	D#	1	1	1	1	0	0	0	0	0	F	0	–
				Repeat cycles *n*RC + 1 through *n*RC + 4 until *n*RC - 1 + *n*RAS -1; truncate if needed												
			*n*RC +*n*RAS	PRE	0	0	1	0	0	0	0	0	0	F	0	–
				Repeat cycles *n*RC + 1 through *n*RC + 4 until 2 × RC - 1; truncate if needed												
		1	2 × *n*RC	Repeat sub-loop 0, use BA[2:0] = 1												
		2	4 × *n*RC	Repeat sub-loop 0, use BA[2:0] = 2												
		3	6 × *n*RC	Repeat sub-loop 0, use BA[2:0] = 3												
		4	8 × *n*RC	Repeat sub-loop 0, use BA[2:0] = 4												
		5	10 × *n*RC	Repeat sub-loop 0, use BA[2:0] = 5												
		6	12 × *n*RC	Repeat sub-loop 0, use BA[2:0] = 6												
		7	14 × *n*RC	Repeat sub-loop 0, use BA[2:0] = 7												

Notes:

1. DQ, DQS, DQS# are midlevel.

2. DM is LOW.

3. Only selected bank (single) active.

I_{DD1} Measurement Loop

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[2]
Tog	Static	0	0	ACT	0	0	1	1	0	0	0	0	0	0	0	–
			1	D	1	0	0	0	0	0	0	0	0	0	0	–
			2	D	1	0	0	0	0	0	0	0	0	0	0	–
			3	D#	1	1	1	1	0	0	0	0	0	0	0	–
			4	D#	1	1	1	1	0	0	0	0	0	0	0	–
				Repeat cycles 1 through 4 until *n*RCD - 1; truncate if needed												
			*n*RCD	RD	0	1	0	1	0	0	0	0	0	0	0	00000000
				Repeat cycles 1 through 4 until *n*RAS - 1; truncate if needed												
			*n*RAS	PRE	0	0	1	0	0	0	0	0	0	0	0	–
				Repeat cycles 1 through 4 until *n*RC - 1; truncate if needed												
			*n*RC	ACT	0	0	1	1	0	0	0	0	0	F	0	–
			*n*RC + 1	D	1	0	0	0	0	0	0	0	0	F	0	–
			*n*RC + 2	D	1	0	0	0	0	0	0	0	0	F	0	–
			*n*RC + 3	D#	1	1	1	1	0	0	0	0	0	F	0	–
			*n*RC + 4	D#	1	1	1	1	0	0	0	0	0	F	0	–
				Repeat cycles *n*RC + 1 through *n*RC + 4 until *n*RC + *n*RCD - 1; truncate if needed												
			*n*RC +*n*RCD	RD	0	1	0	1	0	0	0	0	0	F	0	00110011
				Repeat cycles *n*RC + 1 through *n*RC + 4 until *n*RC + *n*RAS - 1; truncate if needed												
			*n*RC +*n*RAS	PRE	0	0	1	0	0	0	0	0	0	F	0	–
				Repeat cycle *n*RC + 1 through *n*RC + 4 until 2 × *n*RC - 1; truncate if needed												
		1	2 × *n*RC	Repeat sub-loop 0, use BA[2:0] = 1												
		2	4 × *n*RC	Repeat sub-loop 0, use BA[2:0] = 2												
		3	6 × *n*RC	Repeat sub-loop 0, use BA[2:0] = 3												
		4	8 × *n*RC	Repeat sub-loop 0, use BA[2:0] = 4												
		5	10 × *n*RC	Repeat sub-loop 0, use BA[2:0] = 5												
		6	12 × *n*RC	Repeat sub-loop 0, use BA[2:0] = 6												
		7	14 × *n*RC	Repeat sub-loop 0, use BA[2:0] = 7												

Notes:

1. DQ, DQS, DQS# are midlevel unless driven as required by the RD command.
2. DM is LOW.
3. Burst sequence is driven on each DQ signal by the RD command.
4. Only selected bank (single) active.

IDD Measurement Conditions for Power-Down Currents

Name	I_{DD2P0} Precharge Power-Down Current (Slow Exit)[1]	I_{DD2P1} Precharge Power-Down Current (Fast Exit)[1]	I_{DD2Q} Precharge Quiet Standby Current	I_{DD3P} Active Power-Down Current
Timing pattern	N/A	N/A	N/A	N/A
CKE	LOW	LOW	HIGH	LOW
External clock	Toggling	Toggling	Toggling	Toggling
tCK	tCK (MIN) I_{DD}	tCK (MIN) I_{DD}	tCK (MIN) I_{DD}	tCK (MIN) I_{DD}
tRC	N/A	N/A	N/A	N/A
tRAS	N/A	N/A	N/A	N/A
tRCD	N/A	N/A	N/A	N/A
tRRD	N/A	N/A	N/A	N/A
tRC	N/A	N/A	N/A	N/A
CL	N/A	N/A	N/A	N/A
AL	N/A	N/A	N/A	N/A
CS#	HIGH	HIGH	HIGH	HIGH
Command inputs	LOW	LOW	LOW	LOW
Row/column addr	LOW	LOW	LOW	LOW
Bank addresses	LOW	LOW	LOW	LOW
DM	LOW	LOW	LOW	LOW
Data I/O	Midlevel	Midlevel	Midlevel	Midlevel
Output buffer DQ, DQS	Enabled	Enabled	Enabled	Enabled
ODT[2]	Enabled, off	Enabled, off	Enabled, off	Enabled, off
Burst length	8	8	8	8
Active banks	None	None	None	All
Idle banks	All	All	All	None
Special notes	N/A	N/A	N/A	N/A

Notes:

1. MR0[12] defines DLL on/off behavior during precharge power-down only; DLL on (fast exit, MR0[12] = 1) and DLL off (slow exit, MR0[12] = 0).

2. “Enabled, off” means the MR bits are enabled, but the signal is LOW.

I_{DD2N} and I_{DD3N} Measurement Loop

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data
Toggling	Static HIGH	0	0	D	1	0	0	0	0	0	0	0	0	0	0	–
			1	D	1	0	0	0	0	0	0	0	0	0	0	–
			2	D#	1	1	1	1	0	0	0	0	0	F	0	–
			3	D#	1	1	1	1	0	0	0	0	0	F	0	–
		1	4–7	Repeat sub-loop 0, use BA[2:0] = 1												
		2	8–11	Repeat sub-loop 0, use BA[2:0] = 2												
		3	12–15	Repeat sub-loop 0, use BA[2:0] = 3												
		4	16–19	Repeat sub-loop 0, use BA[2:0] = 4												
		5	20–23	Repeat sub-loop 0, use BA[2:0] = 5												
		6	24–27	Repeat sub-loop 0, use BA[2:0] = 6												
		7	28–31	Repeat sub-loop 0, use BA[2:0] = 7												

Notes:

1. DQ, DQS, DQS# are midlevel.

2. DM is LOW.

3. All banks closed during I_{DD2N}; all banks open during I_{DD3N}.

IDD2NT Measurement Loop

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data
Toggling	Static HIGH	0	0	D	1	0	0	0	0	0	0	0	0	0	0	–
			1	D	1	0	0	0	0	0	0	0	0	0	0	–
			2	D#	1	1	1	1	0	0	0	0	0	F	0	–
			3	D#	1	1	1	1	0	0	0	0	0	F	0	–
		1	4–7	Repeat sub-loop 0, use BA[2:0] = 1; ODT = 0												
		2	8–11	Repeat sub-loop 0, use BA[2:0] = 2; ODT = 1												
		3	12–15	Repeat sub-loop 0, use BA[2:0] = 3; ODT = 1												
		4	16–19	Repeat sub-loop 0, use BA[2:0] = 4; ODT = 0												
		5	20–23	Repeat sub-loop 0, use BA[2:0] = 5; ODT = 0												
		6	24–27	Repeat sub-loop 0, use BA[2:0] = 6; ODT = 1												
		7	28–31	Repeat sub-loop 0, use BA[2:0] = 7; ODT = 1												

Notes:

1. DQ, DQS, DQS# are midlevel.

2. DM is LOW.

3. All banks closed.

IDD4R Measurement Loop

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[3]
Toggling	Static HIGH	0	0	RD	0	1	0	1	0	0	0	0	0	0	0	00000000
			1	D	1	0	0	0	0	0	0	0	0	0	0	–
			2	D#	1	1	1	1	0	0	0	0	0	0	0	–
			3	D#	1	1	1	1	0	0	0	0	0	0	0	–
			4	RD	0	1	0	1	0	0	0	0	0	F	0	00110011
			5	D	1	0	0	0	0	0	0	0	0	F	0	–
			6	D#	1	1	1	1	0	0	0	0	0	F	0	–
			7	D#	1	1	1	1	0	0	0	0	0	F	0	–
		1	8–15	Repeat sub-loop 0, use BA[2:0] = 1												
		2	16–23	Repeat sub-loop 0, use BA[2:0] = 2												
		3	24–31	Repeat sub-loop 0, use BA[2:0] = 3												
		4	32–39	Repeat sub-loop 0, use BA[2:0] = 4												
		5	40–47	Repeat sub-loop 0, use BA[2:0] = 5												
		6	48–55	Repeat sub-loop 0, use BA[2:0] = 6												
		7	56–63	Repeat sub-loop 0, use BA[2:0] = 7												

Notes:

1. DQ, DQS, DQS# are midlevel when not driving in burst sequence.

2. DM is LOW.

3. Burst sequence is driven on each DQ signal by the RD command.

4. All banks open.

IDD4W Measurement Loop

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[3]
Toggling	Static HIGH	0	0	WR	0	1	0	0	1	0	0	0	0	0	0	00000000
			1	D	1	0	0	0	1	0	0	0	0	0	0	–
			2	D#	1	1	1	1	1	0	0	0	0	0	0	–
			3	D#	1	1	1	1	1	0	0	0	0	0	0	–
			4	WR	0	1	0	0	1	0	0	0	0	F	0	00110011
			5	D	1	0	0	0	1	0	0	0	0	F	0	–
			6	D#	1	1	1	1	1	0	0	0	0	F	0	–
			7	D#	1	1	1	1	1	0	0	0	0	F	0	–
		1	8–15	Repeat sub-loop 0, use BA[2:0] = 1												
		2	16–23	Repeat sub-loop 0, use BA[2:0] = 2												
		3	24–31	Repeat sub-loop 0, use BA[2:0] = 3												
		4	32–39	Repeat sub-loop 0, use BA[2:0] = 4												
		5	40–47	Repeat sub-loop 0, use BA[2:0] = 5												
		6	48–55	Repeat sub-loop 0, use BA[2:0] = 6												
		7	56–63	Repeat sub-loop 0, use BA[2:0] = 7												

Notes:

1. DQ, DQS, DQS# are midlevel when not driving in burst sequence.

2. DM is LOW.

3. Burst sequence is driven on each DQ signal by the WR command.

4. All banks open.

IDD5B Measurement Loop

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data
Toggling	Static HIGH	0	0	REF	0	0	0	1	0	0	0	0	0	0	0	–
		1a	1	D	1	0	0	0	0	0	0	0	0	0	0	–
			2	D	1	0	0	0	0	0	0	0	0	0	0	–
			3	D#	1	1	1	1	0	0	0	0	0	F	0	–
			4	D#	1	1	1	1	0	0	0	0	0	F	0	–
		1b	5–8	Repeat sub-loop 1a, use BA[2:0] = 1												
		1c	9–12	Repeat sub-loop 1a, use BA[2:0] = 2												
		1d	13–16	Repeat sub-loop 1a, use BA[2:0] = 3												
		1e	17–20	Repeat sub-loop 1a, use BA[2:0] = 4												
		1f	21–24	Repeat sub-loop 1a, use BA[2:0] = 5												
		1g	25–28	Repeat sub-loop 1a, use BA[2:0] = 6												
		1h	29–32	Repeat sub-loop 1a, use BA[2:0] = 7												
		2	33–*n*RFC - 1	Repeat sub-loop 1a through 1h until *n*RFC - 1; truncate if needed												

Notes:

1. DQ, DQS, DQS# are midlevel.

2. DM is LOW.

IDD Measurement Conditions for IDD6, IDD6ET, and IDD8

I_{DD} Test	I_{DD6}: Self Refresh Current Normal Temperature Range Tc	I_{DD6ET}: Self Refresh Current Extended Temperature Range	I_{DD8}: Reset[2]
CKE	LOW	LOW	Midlevel
External clock	Off, CK and CK# = LOW	Off, CK and CK# = LOW	Midlevel
tCK	N/A	N/A	N/A
tRC	N/A	N/A	N/A
tRAS	N/A	N/A	N/A
tRCD	N/A	N/A	N/A
tRRD	N/A	N/A	N/A
tRC	N/A	N/A	N/A
CL	N/A	N/A	N/A
AL	N/A	N/A	N/A
CS#	Midlevel	Midlevel	Midlevel
Command inputs	Midlevel	Midlevel	Midlevel
Row/column addresses	Midlevel	Midlevel	Midlevel
Bank addresses	Midlevel	Midlevel	Midlevel
Data I/O	Midlevel	Midlevel	Midlevel
Output buffer DQ, DQS	Enabled	Enabled	Midlevel
ODT[1]	Enabled, midlevel	Enabled, midlevel	Midlevel
Burst length	N/A	N/A	N/A
Active banks	N/A	N/A	None
Idle banks	N/A	N/A	All
SRT	Disabled (normal)	Enabled (extended)	N/A
ASR	Disabled	Disabled	N/A

Notes:

1. “Enabled, midlevel” means the MR command is enabled, but the signal is midlevel.

2. During a cold boot RESET (initialization), current reading is valid after power is stable and RESET has been LOW for 1ms; During a warm boot RESET (while operating), current reading is valid after RESET has been LOW for 200ns + tRFC.

IDD7 Measurement Loop

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[3]
Toggling	Static HIGH	0	0	ACT	0	0	1	1	0	0	0	0	0	0	0	–
			1	RDA	0	1	0	1	0	0	0	1	0	0	0	00000000
			2	D	1	0	0	0	0	0	0	0	0	0	0	–
			3	Repeat cycle 2 until *n*RRD - 1												
		1	*n*RRD	ACT	0	0	1	1	0	1	0	0	0	F	0	–
			*n*RRD + 1	RDA	0	1	0	1	0	1	0	1	0	F	0	00110011
			*n*RRD + 2	D	1	0	0	0	0	1	0	0	0	F	0	–
			*n*RRD + 3	Repeat cycle *n*RRD + 2 until 2 × *n*RRD - 1												
		2	2 × *n*RRD	Repeat sub-loop 0, use BA[2:0] = 2												
		3	3 × *n*RRD	Repeat sub-loop 1, use BA[2:0] = 3												
		4	4 × *n*RRD	D	1	0	0	0	0	3	0	0	0	F	0	–
			4 × *n*RRD + 1	Repeat cycle 4 × *n*RRD until *n*FAW - 1, if needed												
		5	*n*FAW	Repeat sub-loop 0, use BA[2:0] = 4												
		6	*n*FAW + *n*RRD	Repeat sub-loop 1, use BA[2:0] = 5												
		7	*n*FAW + 2 × *n*RRD	Repeat sub-loop 0, use BA[2:0] = 6												
		8	*n*FAW + 3 × *n*RRD	Repeat sub-loop 1, use BA[2:0] = 7												
		9	*n*FAW + 4 × *n*RRD	D	1	0	0	0	0	7	0	0	0	F	0	–
			*n*FAW + 4 × *n*RRD + 1	Repeat cycle *n*FAW + 4 × *n*RRD until 2 × *n*FAW - 1, if needed												
		10	2 × *n*FAW	ACT	0	0	1	1	0	0	0	0	0	F	0	–
			2 × *n*FAW + 1	RDA	0	1	0	1	0	0	0	1	0	F	0	00110011
			2 × *n*FAW + 2	D	1	0	0	0	0	0	0	0	0	F	0	–
			2 × *n*FAW + 3	Repeat cycle 2 × *n*FAW + 2 until 2 × *n*FAW + *n*RRD - 1												
		11	2 × *n*FAW + *n*RRD	ACT	0	0	1	1	0	1	0	0	0	0	0	–
			2 × *n*FAW + *n*RRD + 1	RDA	0	1	0	1	0	1	0	1	0	0	0	00000000
			2 × *n*FAW + *n*RRD + 2	D	1	0	0	0	0	1	0	0	0	0	0	–
			2 × *n*FAW + *n*RRD + 3	Repeat cycle 2 × *n*FAW + *n*RRD + 2 until 2 × *n*FAW + 2 × *n*RRD - 1												
		12	2 × *n*FAW + 2 × *n*RRD	Repeat sub-loop 10, use BA[2:0] = 2												
		13	2 × *n*FAW + 3 × *n*RRD	Repeat sub-loop 11, use BA[2:0] = 3												
		14	2 × *n*FAW + 4 × *n*RRD	D	1	0	0	0	0	3	0	0	0	0	0	–
			2 × *n*FAW + 4 × *n*RRD + 1	Repeat cycle 2 × *n*FAW + 4 × *n*RRD until 3 × *n*FAW - 1, if needed												
		15	3 × *n*FAW	Repeat sub-loop 10, use BA[2:0] = 4												

IDD7 Measurement Loop (Continued)

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[3]
Toggling	Static HIGH	16	3 × *n*FAW + *n*RRD	Repeat sub-loop 11, use BA[2:0] = 5												
		17	3 × *n*FAW + 2 × *n*RRD	Repeat sub-loop 10, use BA[2:0] = 6												
		18	3 × *n*FAW + 3 × *n*RRD	Repeat sub-loop 11, use BA[2:0] = 7												
		19	3 × *n*FAW + 4 × *n*RRD	D	1	0	0	0	0	7	0	0	0	0	0	-
			3 × *n*FAW + 4 × *n*RRD + 1	Repeat cycle 3 × *n*FAW + 4 × *n*RRD until 4 × *n*FAW - 1, if needed												

Notes:

1. DQ, DQS, DQS# are midlevel unless driven as required by the RD command.

2. DM is LOW.

3. Burst sequence is driven on each DQ signal by the RD command.

4. AL = CL-1.

Electrical Characteristics – I_{DD} Specifications

I_{DD} Maximum Limits

Speed Bin		DDR3(L)-1066	DDR3(L)-1333	DDR3(L)-1600	Unit	Notes
Parameter	Symbol					
Operating current 0: One bank ACTIVATE-to-PRECHARGE	I_{DD0}	TBD	TBD	32	mA	1, 2
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	I_{DD1}	TBD	TBD	45	mA	1, 2
Precharge power-down current: Slow exit	I_{DD2P0}	TBD	TBD	12	mA	1, 2
Precharge power-down current: Fast exit	I_{DD2P1}	TBD	TBD	12	mA	1, 2
Precharge quiet standby current	I_{DD2Q}	TBD	TBD	15	mA	1, 2
Precharge standby current	I_{DD2N}	TBD	TBD	17	mA	1, 2
Precharge standby ODT current	I_{DD2NT}	TBD	TBD	22	mA	1, 2
Active power-down current	I_{DD3P}	TBD	TBD	17	mA	1, 2
Active standby current	I_{DD3N}	TBD	TBD	22	mA	1, 2
Burst read operating current	I_{DD4R}	TBD	TBD	92	mA	1, 2
Burst write operating current	I_{DD4W}	TBD	TBD	106	mA	1, 2
Burst refresh current	I_{DD5B}	TBD	TBD	156	mA	1, 2
Self refresh	I_{DD6}	TBD	TBD	15	mA	1, 2, 3
Extended temperature self refresh	I_{DD6ET}	TBD	TBD	23	mA	2, 4
All banks interleaved read current	I_{DD7}	TBD	TBD	132	mA	1, 2
Reset current	I_{DD8}	TBD	TBD	I_{DD2P0} + 2mA	mA	1, 2

Notes:

1. T_C = 85℃; SRT and ASR are disabled.
2. Enabling ASR could increase I_{DDx} by up to an additional 2mA.
3. Restricted to T_C (MAX) = 85℃.
4. T_C = 85℃; ASR and ODT are disabled; SRT is enabled.

Electrical Specifications – DC and AC

DC Operating Conditions

DC Electrical Characteristics and Operating Conditions

All voltages are referenced to V_{SS}

Parameter/Condition	Symbol	Min	Nom	Max	Unit	Notes
Supply voltage (DDR3)	V_{DD}	1.425	1.5	1.575	V	1, 2
I/O supply voltage (DDR3)	V_{DDQ}	1.425	1.5	1.575	V	1, 2
Supply voltage (DDR3L)	V_{DD}	1.283	1.35	1.45	V	1-7
I/O supply voltage (DDR3L)	V_{DDQ}	1.283	1.35	1.45	V	1-7
Input leakage current Any input 0V ≤ V_{IN} ≤ V_{DD}, V_{REF} pin 0V ≤ V_{IN} ≤ 1.1V	I_I	–2	–	2	uA	
V_{REF} supply leakage current V_{REFDQ} = V_{DD}/2 or V_{REFCA} = V_{DD}/2	I_{VREF}	–1	–	1	uA	8,9

Notes:

1. V_{DD} and V_{DDQ} must track one another. V_{DDQ} must be ≤ V_{DD}. V_{SS} = V_{SSQ}.
2. V_{DD} and V_{DDQ} may include AC noise of ±50mV (250 kHz to 20 MHz) in addition to the DC (0 Hz to 250 kHz) specifications. V_{DD} and V_{DDQ} must be at same level for valid AC timing parameters.
3. Maximum DC value may not be greater than 1.425V. The DC value is the linear average of V_{DD}/V_{DDQ}(t) over a very long period of time (for example, 1 second).
4. Under these supply voltages, the device operates to this DDR3L specification.
5. If the maximum limit is exceeded, input levels shall be governed by DDR3 specifications.
6. Under 1.5V operation, this DDR3L device operates in accordance with the DDR3 specifi-cations under the same speed timings as defined for this device.
7. Once initialized for DDR3L operation, DDR3 operation may only be used if the device is in reset while V_{DD} and V_{DDQ} are changed for DDR3 operation (see section: V_{DD} Voltage Switching).
8. The minimum limit requirement is for testing purposes. The leakage current on the V_{REF} pin should be minimal.
9. V_{REF} (see Table 4-17).

Input Operating Conditions

DC Electrical Characteristics and Input Conditions

All voltages are referenced to V_{SS}

Parameter/Condition	Symbol	Min	Nom	Max	Unit	Notes
V_{IN} low; DC/commands/address busses	V_{IL}	V_{SS}	N/A	See Table 4-18	V	
V_{IN} high; DC/commands/address busses	V_{IH}	See Table 4-18	N/A	V_{DD}	V	
Input reference voltage command/address bus	$V_{REFCA(DC)}$	0.49 × V_{DD}	0.5 × V_{DD}	0.51 × V_{DD}	V	1, 2
I/O reference voltage DQ bus	$V_{REFDQ(DC)}$	0.49 × V_{DD}	0.5 × V_{DD}	0.51 × V_{DD}	V	2, 3
I/O reference voltage DQ bus in SELF REFRESH	$V_{REFDQ(SR)}$	V_{SS}	0.5 × V_{DD}	V_{DD}	V	4
Command/address termination voltage (system level, not direct DRAM input)	V_{TT}	–	0.5 × V_{DDQ}	–	V	5

Notes:

1. $V_{REFCA(DC)}$ is expected to be approximately 0.5 × V_{DD} and to track variations in the DC level. Externally generated peak noise (non-common mode) on V_{REFCA} may not exceed ±1% × V_{DD} around the $V_{REFCA(DC)}$ value. Peak-to-peak AC noise on V_{REFCA} should not exceed ±2% of $V_{REFCA(DC)}$.
2. DC values are determined to be less than 20 MHz in frequency. DRAM must meet specifications if the DRAM induces additional AC noise greater than 20 MHz in frequency.
3. $V_{REFDQ(DC)}$ is expected to be approximately 0.5 × V_{DD} and to track variations in the DC level. Externally generated peak noise (non-common mode) on V_{REFDQ} may not exceed ±1% × V_{DD} around the $V_{REFDQ(DC)}$ value. Peak-to-peak AC noise on V_{REFDQ} should not exceed ±2% of $V_{REFDQ(DC)}$.
4. $V_{REFDQ(DC)}$ may transition to $V_{REFDQ(SR)}$ and back to $V_{REFDQ(DC)}$ when in SELF REFRESH, within restrictions outlined in the SELF REFRESH section.
5. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors. Minimum and maximum values are system-dependent.

Input Switching Conditions (DDR3L)

Parameter/Condition	Symbol	DDR3L-1066/1333/1600	Units
Command and Address			
Input high AC voltage: Logic 1	$V_{IH(AC160)min}$[5]	160	mV
	$V_{IH(AC135)min}$[5]	135	mV
	$V_{IH(AC125)min}$[5]	–	mV
Input high DC voltage: Logic 1	$V_{IH(DC90)min}$	90	mV
Input low DC voltage: Logic 0	$V_{IL(DC90)min}$	–90	mV
Input low AC voltage: Logic 0	$V_{IL(AC125)min}$[5]	–	mV
	$V_{IL(AC135)min}$[5]	–135	mV
	$V_{IL(AC160)min}$[5]	–160	mV
DQ and DM			
Input high AC voltage: Logic 1	$V_{IH(AC160)min}$[5]	160	mV
	$V_{IH(AC135)min}$[5]	135	mV
	$V_{IH(AC125)min}$[5]	–	mV
Input high DC voltage: Logic 1	$V_{IH(DC90)min}$	90	mV
Input low DC voltage: Logic 0	$V_{IL(DC90)min}$	–90	mV
Input low AC voltage: Logic 0	$V_{IL(AC125)min}$[5]	–	mV
	$V_{IL(AC135)min}$[5]	–135	mV
	$V_{IL(AC160)min}$[5]	–160	mV

Notes:

1. All voltages are referenced to V_{REF}. V_{REF} is V_{REFCA} for control, command, and address. All slew rates and setup/hold times are specified at the DRAM ball. V_{REF} is V_{REFDQ} for DQ and DM inputs.
2. Input setup timing parameters (tIS and tDS) are referenced at $V_{IL(AC)}/V_{IH(AC)}$, not $V_{REF(DC)}$.
3. Input hold timing parameters (tIH and tDH) are referenced at $V_{IL(DC)}/V_{IH(DC)}$, not $V_{REF(DC)}$.
4. Single-ended input slew rate = 1 V/ns; maximum input voltage swing under test is 900mV (peak-to-peak).
5. When two $V_{IH(AC)}$ values (and two corresponding $V_{IL(AC)}$ values) are listed for a specific speed bin, the user may choose either value for the input AC level. Whichever value is used, the associated setup time for that AC level must also be used. Additionally, one $V_{IH(AC)}$ value may be used for address/command inputs and the other $V_{IH(AC)}$ value may be used for data inputs.

Input Switching Conditions (DDR3)

Parameter/Condition	Symbol	DDR3-1066	Unit
Command and Address			
Input high AC voltage: Logic 1	$V_{IH(AC175)min}$	175	mV
	$V_{IH(AC150)min}$	150	mV
	$V_{IH(AC135)min}$	–	mV
	$V_{IH(AC125)min}$	–	mV
Input high DC voltage: Logic 1	$V_{IH(DC100)min}$	100	mV
Input low DC voltage: Logic 0	$V_{IL(DC100)max}$	–100	mV
Input low AC voltage: Logic 0	$V_{IL(AC125)max}$	–	mV
	$V_{IL(AC135)max}$	–	mV
	$V_{IL(AC150)max}$	–150	mV
	$V_{IL(AC175)max}$	–175	mV
DQ and DM			
Input high AC voltage: Logic 1	$V_{IH(AC175)min}$	175	mV
	$V_{IH(AC150)min}$	150	mV
	$V_{IH(AC135)min}$	–	mV
Input high DC voltage: Logic 1	$V_{IH(DC100)min}$	100	mV
Input low DC voltage: Logic 0	$V_{IL(DC100)max}$	–100	mV
Input low AC voltage: Logic 0	$V_{IL(AC135)max}$	–	mV
	$V_{IL(AC150)max}$	–150	mV
	$V_{IL(AC175)max}$	–175	mV

Notes:

1. All voltages are referenced to V_{REF}. V_{REF} is V_{REFCA} for control, command, and address. All slew rates and setup/hold times are specified at the DRAM ball. V_{REF} is V_{REFDQ} for DQ and DM inputs.
2. Input setup timing parameters (t_{IS} and t_{DS}) are referenced at $V_{IL(AC)}/V_{IH(AC)}$, not $V_{REF(DC)}$.
3. Input hold timing parameters (t_{IH} and t_{DH}) are referenced at $V_{IL(DC)}/V_{IH(DC)}$, not $V_{REF(DC)}$.
4. Single-ended input slew rate = 1 V/ns; maximum input voltage swing under test is 900mV (peak-to-peak).

Differential Input Operating Conditions (CK, CK# and DQS, DQS#) (DDR3L)

Parameter/Condition	Symbol	Min	Max	Units	Notes
Differential input logic high – slew	$V_{IH,diff(AC)slew}$	180	N/A	mV	4
Differential input logic low – slew	$V_{IL,diff(AC)slew}$	N/A	–180	mV	4
Differential input logic high	$V_{IH,diff(AC)}$	2 × ($V_{IH(AC)}$ - V_{REF})	V_{DD}/V_{DDQ}	mV	5
Differential input logic low	$V_{IL,diff(AC)}$	V_{SS}/V_{SSQ}	2 × ($V_{IL(AC)}$ - V_{REF})	mV	6
Differential input crossing voltage relative to V_{DD}/2 for DQS, DQS#; CK, CK#	V_{IX}	$V_{REF(DC)}$ - 150	$V_{REF(DC)}$ + 150	mV	5,7,9
Differential input crossing voltage relative to V_{DD}/2 for CK, CK#	$V_{IX}(175)$	$V_{REF(DC)}$ - 175	$V_{REF(DC)}$ + 175	mV	5,7-9
Single-ended low level for strobes	V_{SEH}	V_{DDQ}/2 + 160	V_{DDQ}	mV	5
Single-ended low level for CK, CK#		V_{DD}/2 + 160	V_{DD}	mV	5
Single-ended low level for strobes	V_{SEL}	V_{SSQ}	V_{DDQ}/2 - 160	mV	6
Single-ended low level for CK, CK#		V_{SS}	V_{DD}/2 - 160	mV	6

Differential Input Operating Conditions (CK, CK# and DQS, DQS#) (DDR3)

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Differential input voltage logic high - slew	$V_{IH,diff}$	200	N/A	mV	4
Differential input voltage logic low - slew	$V_{IL,diff}$	N/A	–200	mV	4
Differential input voltage logic high	$V_{IH,diff(AC)}$	2 × ($V_{IH(AC)}$ - V_{REF})	V_{DD}/V_{DDQ}	mV	5
Differential input voltage logic low	$V_{IL,diff(AC)}$	V_{SS}/V_{SSQ}	2 × ($V_{IL(AC)}$-V_{REF})	mV	6
Differential input crossing voltage relative to V_{DD}/2 for DQS, DQS#; CK, CK#	V_{IX}	$V_{REF(DC)}$ - 150	$V_{REF(DC)}$ + 150	mV	4, 7
Differential input crossing voltage relative to V_{DD}/2 for CK, CK#	V_{IX} (175)	$V_{REF(DC)}$ - 175	$V_{REF(DC)}$ + 175	mV	4, 7, 8
Single-ended high level for strobes	V_{SEH}	V_{DDQ}/2 + 175	V_{DDQ}	mV	5
Single-ended high level for CK, CK#		V_{DD}/2 + 175	V_{DD}	mV	5
Single-ended low level for strobes	V_{SEL}	V_{SSQ}	V_{DDQ}/2 - 175	mV	6
Single-ended low level for CK, CK#		V_{SS}	V_{DD}/2 – 175	mV	6

Notes:

1. Clock is referenced to V_{DD} and V_{SS}. Data strobe is referenced to V_{DDQ} and V_{SSQ}.

2. Reference is $V_{REFCA(DC)}$ for clock and $V_{REFDQ(DC)}$ for strobe.

3. Differential input slew rate = 2 V/ns.

4. Defines slew rate reference points, relative to input crossing voltages.

5. Minimum DC limit is relative to single-ended signals; overshoot specifications are applicable.

6. Maximum DC limit is relative to single-ended signals; undershoot specifications are applicable.

7. The typical value of $V_{IX(AC)}$ is expected to be about 0.5 × V_{DD} of the transmitting device, and $V_{IX(AC)}$ is expected to track variations in V_{DD}. $V_{IX(AC)}$ indicates the voltage at which differential input signals must cross.
8. The V_{IX} extended range (±175mV) is allowed only for the clock; this V_{IX} extended range is only allowed when the following conditions are met: The single-ended input signals are monotonic, have the single-ended swing V_{SEL}, V_{SEH} of at least $V_{DD}/2$

   ±250mV, and the differential slew rate of CK, CK# is greater than 3 V/ns.
9. V_{IX} must provide 25mV (single-ended) of the voltages separation.

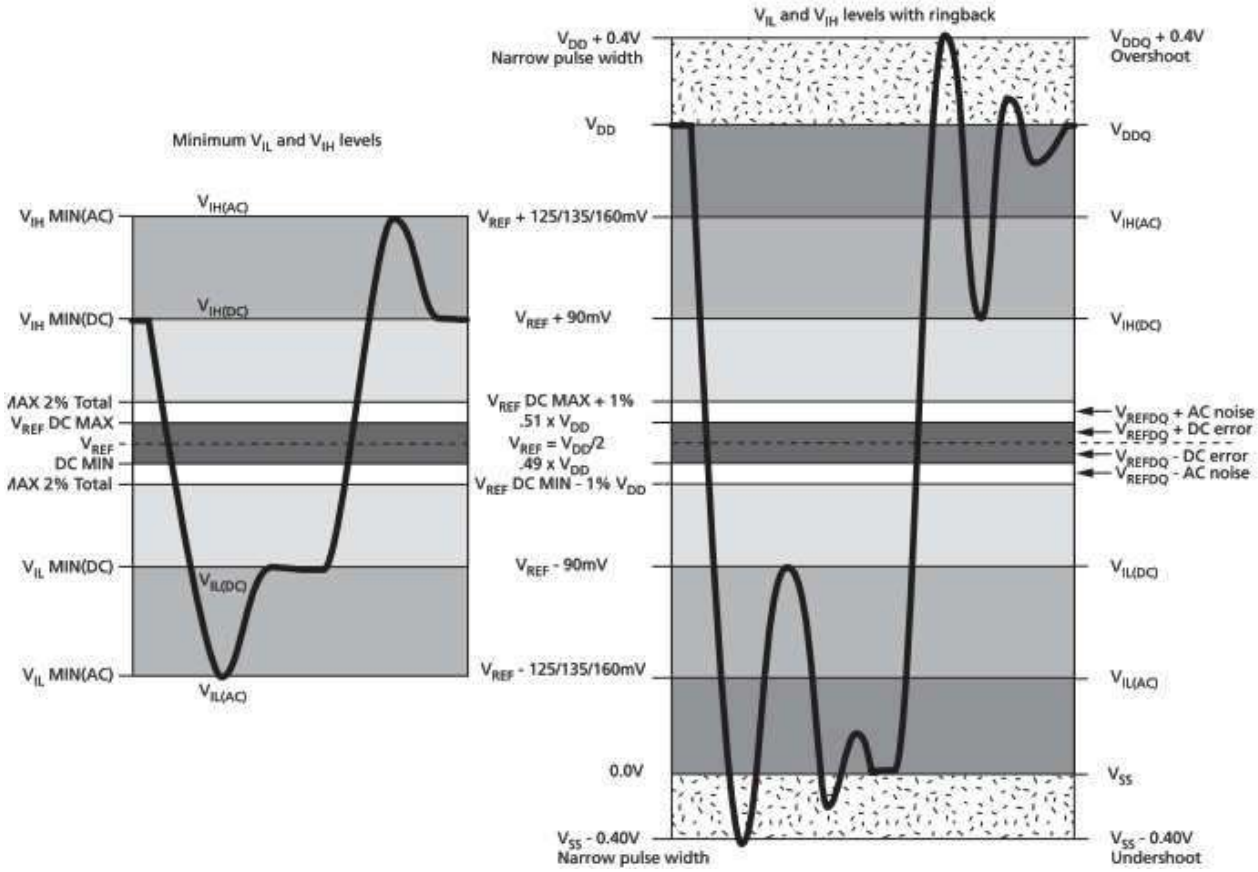


Figure 4-2: Input Signal

Note:

1. Numbers in diagrams reflect nominal values.

AC Overshoot/Undershoot Specification

Control and Address Pins

Parameter	DDR3(L)-1066	DDR3(L)-1333	DDR3(L)-1600
Maximum peak amplitude al-lowed for overshoot area (see Figure 4-3)	0.4V	0.4V	0.4V
Maximum peak amplitude al-lowed for undershoot area (see Figure 4-4)	0.4V	0.4V	0.4V
Maximum overshoot area above V_{DD} (see Figure 4-3)	0.5 V/ns	0.4 V/ns	0.33 V/ns
Maximum undershoot area be-low V_{SS} (see Figure 4-4)	0.5 V/ns	0.4 V/ns	0.33 V/ns

Clock, Data, Strobe, and Mask Pins

Parameter	DDR3(L)-1066	DDR3(L)-1333	DDR3(L)-1600
Maximum peak amplitude al-lowed for overshoot area (see Figure 4-3)	0.4V	0.4V	0.4V
Maximum peak amplitude al-lowed for undershoot area (see Figure 4-4)	0.4V	0.4V	0.4V
Maximum overshoot area above V_{DD}/V_{DDQ} (see Figure 4-3)	0.19 V/ns	0.15 V/ns	0.13 V/ns
Maximum undershoot area be-low V_{SS}/V_{SSQ} (see Figure 4-4)	0.19 V/ns	0.15 V/ns	0.13 V/ns

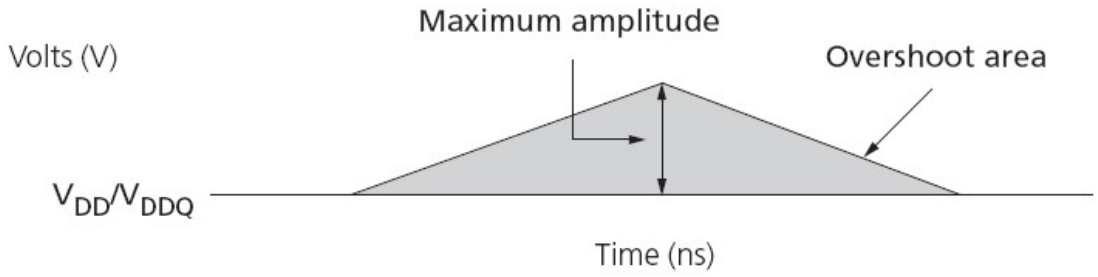


Figure 4-3: Overshoot

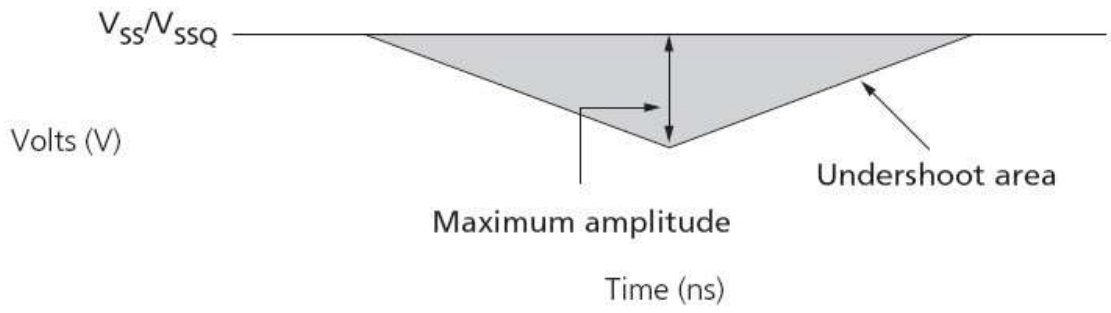


Figure 4-4: Undershoot

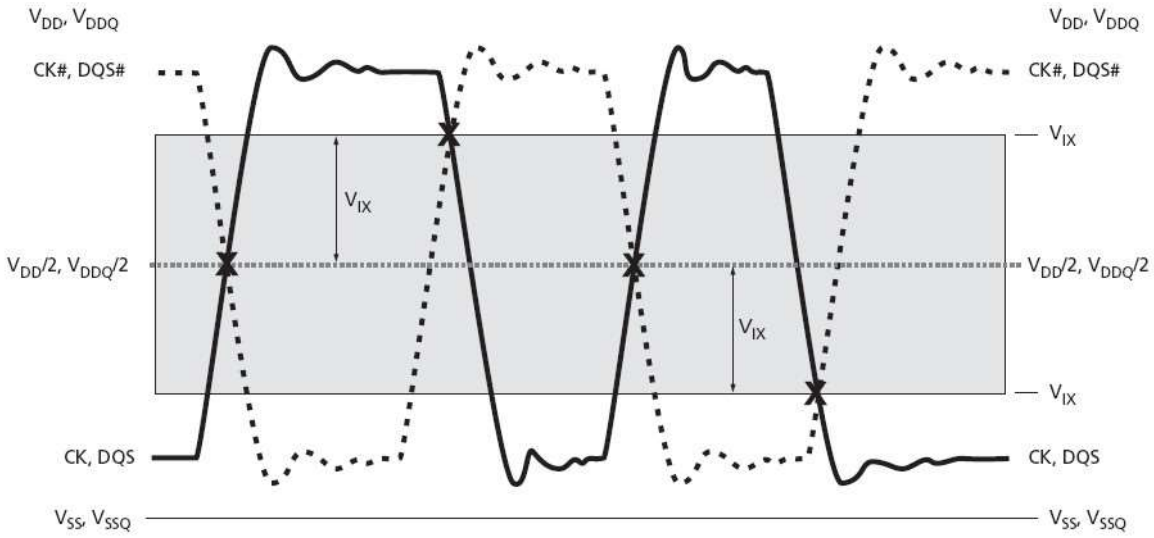


Figure 4-5: V_{IX} for Differential Signals

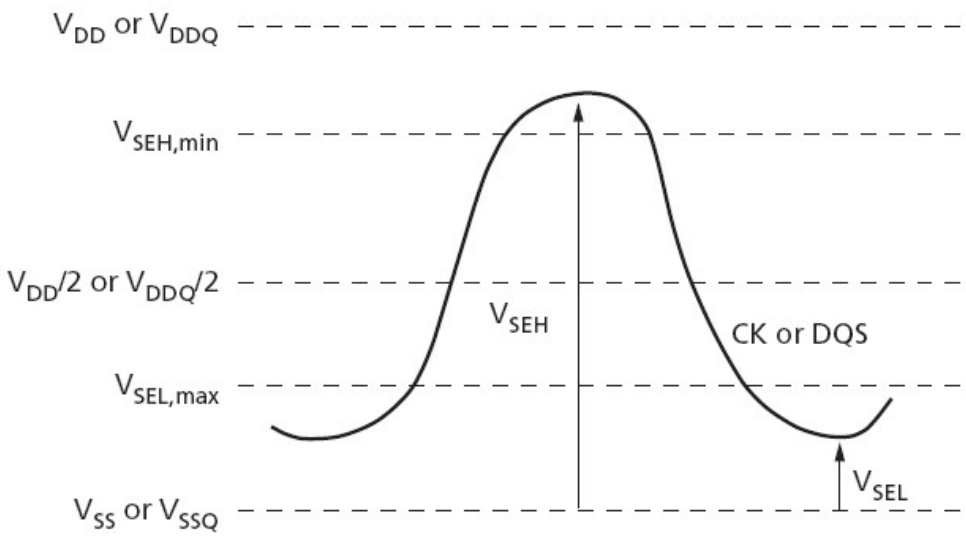


Figure 4-6: Single-Ended Requirements for Differential Signals

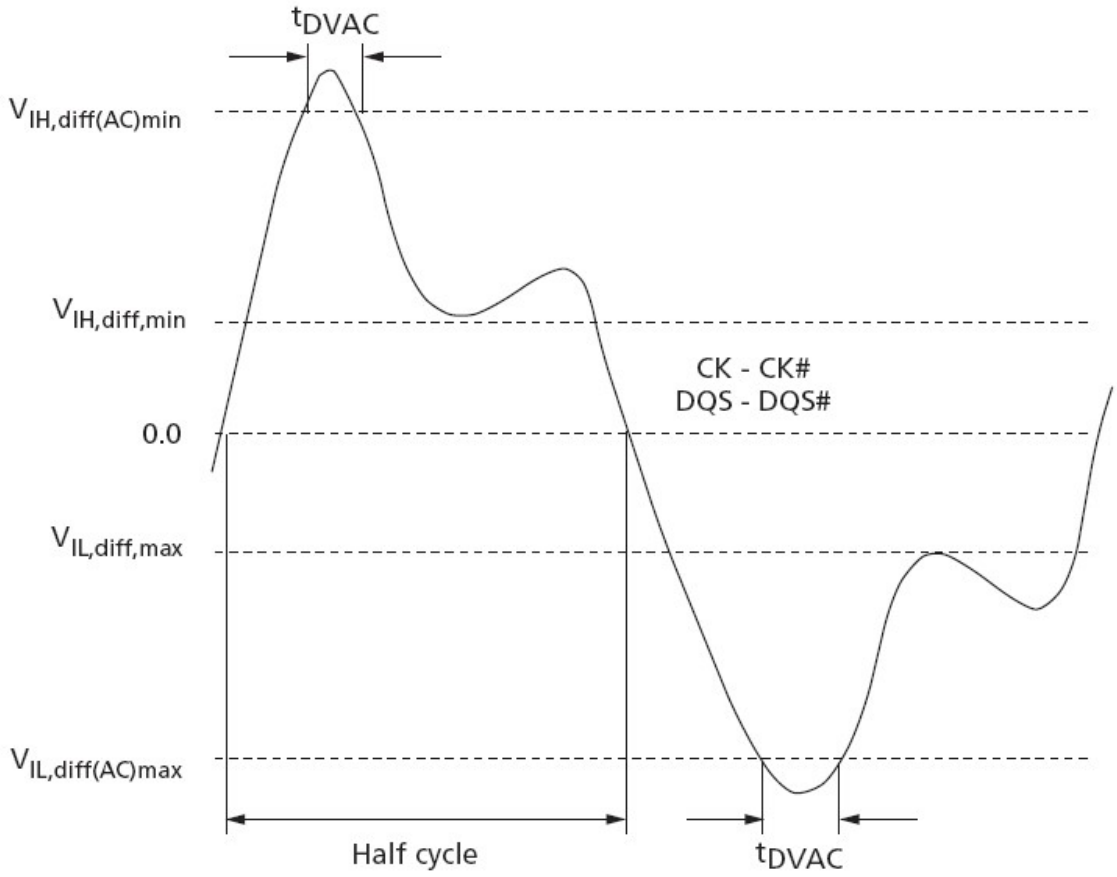


Figure 4-7: Definition of Differential AC-Swing and tDVAC

Minimum Required Time (tDVAC) for CK - CK# and DQS - DQS# Differential for AC Ringback (DDR3L)

Slew Rate (V/ns)	DDR3L-1066/1333/1600	
	tDVAC at 320mV (ps)	tDVAC at 270mV (ps)
>4.0	189	201
4.0	189	201
3.0	162	179
2.0	109	134
1.8	91	119
1.6	69	100
1.4	40	76
1.2	Note1	44
1.0	Note1	
<1.0		

Note:

1. Rising input signal shall become equal to or greater than $V_{IH(ac)}$ level and Falling input signal shall become equal to or less than $V_{IL(AC)}$ level.

Minimum Required Time (tDVAC) for CK - CK# and DQS - DQS# Differential for AC Ringback (DDR3)

Slew Rate (V/ns)	DDR3-1066	
	350mV (ps)	300mV (ps)
>4.0	75	175
4.0	57	170
3.0	50	167
2.0	38	163
1.9	34	162
1.6	29	161
1.4	22	159
1.2	13	155
1.0	0	150
<1.0	0	150

Note:

1. Below $V_{IL(AC)}$.

Slew Rate Definitions for Single-Ended Input Signals

Setup (tIS and tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of V_{REF} and the first crossing of $V_{IH(AC)min}$. Setup (tIS and tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of V_{REF} and the first crossing of $V_{IL(AC)max}$.

Hold (tIH and tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC)max}$ and the first crossing of V_{REF}. Hold (tIS and tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC)min}$ and the first crossing of V_{REF} (see Figure 4-8).

Single-Ended Input Slew Rate Definition

Input Slew Rates (Linear Signals)		Measured		Calculation
Input	Edge	From	To	
Setup	Rising	V_{REF}	$V_{IH(AC),min}$	$\frac{V_{IH(AC)min} - V_{REF}}{\Delta TRS_{se}}$
	Falling	V_{REF}	$V_{IL(AC),max}$	$\frac{V_{REF} - V_{IL(AC)max}}{\Delta TFS_{se}}$
Hold	Rising	$V_{IL(DC),max}$	V_{REF}	$\frac{V_{REF} - V_{IL(DC)max}}{\Delta TFH_{se}}$
	Falling	$V_{IL(DC),mix}$	V_{REF}	$\frac{V_{REF} - V_{IL(DC)max}}{\Delta TFH_{se}}$

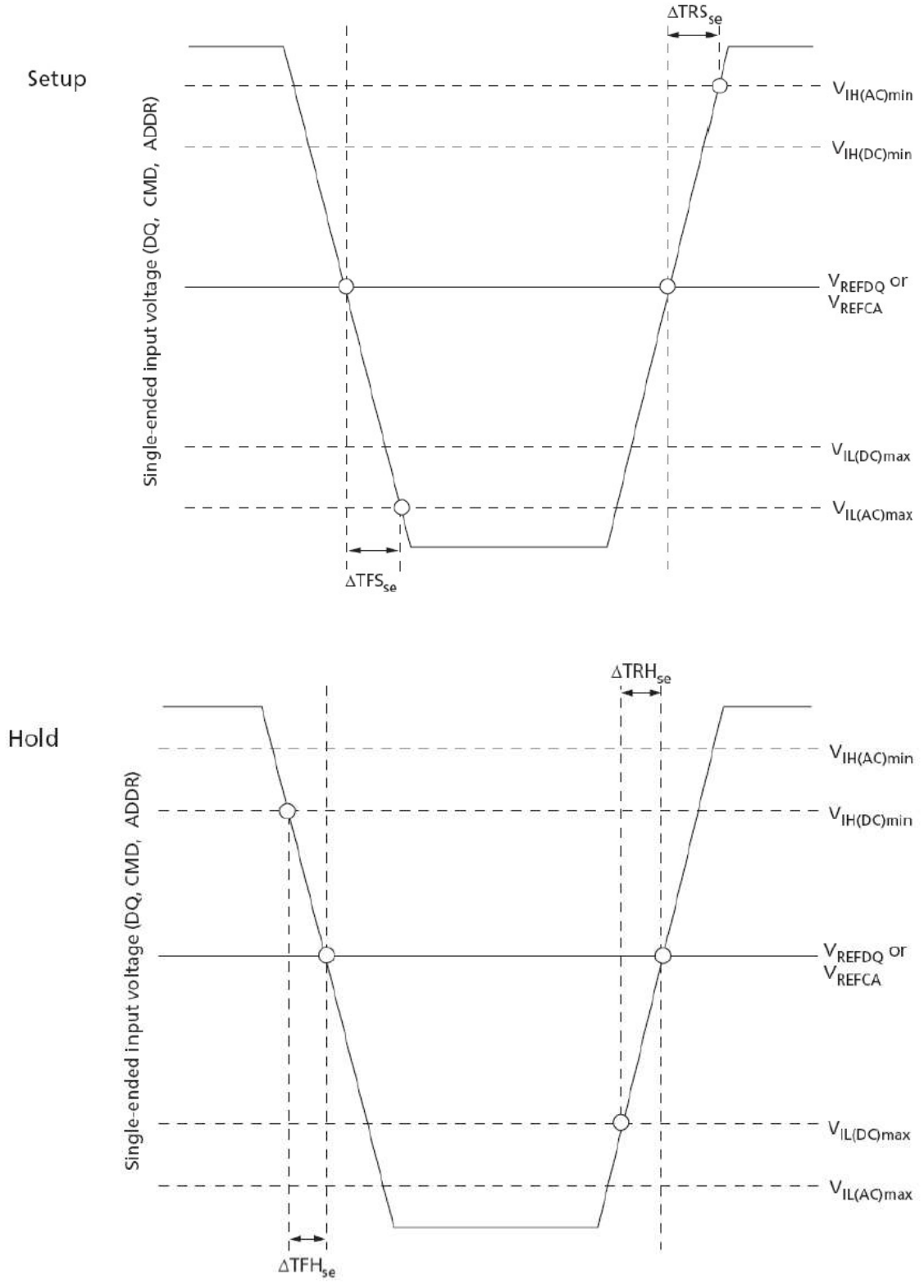


Figure 4-8: Nominal Slew Rate Definition for Single-Ended Input Signals

Slew Rate Definitions for Differential Input Signals

Input slew rate for differential signals (CK, CK# and DQS, DQS#) are defined and measured, as shown in Table 4-24 and Figure 4-9. The nominal slew rate for a rising signal is defined as the slew rate between $V_{IL,diff,max}$ and $V_{IH,diff,min}$. The nominal slew rate for a falling signal is defined as the slew rate between $V_{IH,diff,min}$ and $V_{IL,diff,max}$.

Table 4-24 Differential Input Slew Rate Definition

Differential Input Slew Rates (Linear Signals)		Measured		Calculation
Input	Edge	From	To	
CK and DQS refernce	Rising	$V_{IL,diff,max}$	$V_{IH,diff,min}$	$(V_{IH,diff,min}- V_{IL,diff,max})/ \triangle TR_{diff}$
	Falling	$V_{IH,diff,min}$	$V_{IL,diff,max}$	$(V_{IH,diff,min}- V_{IL,diff,max})/TF_{diff}$

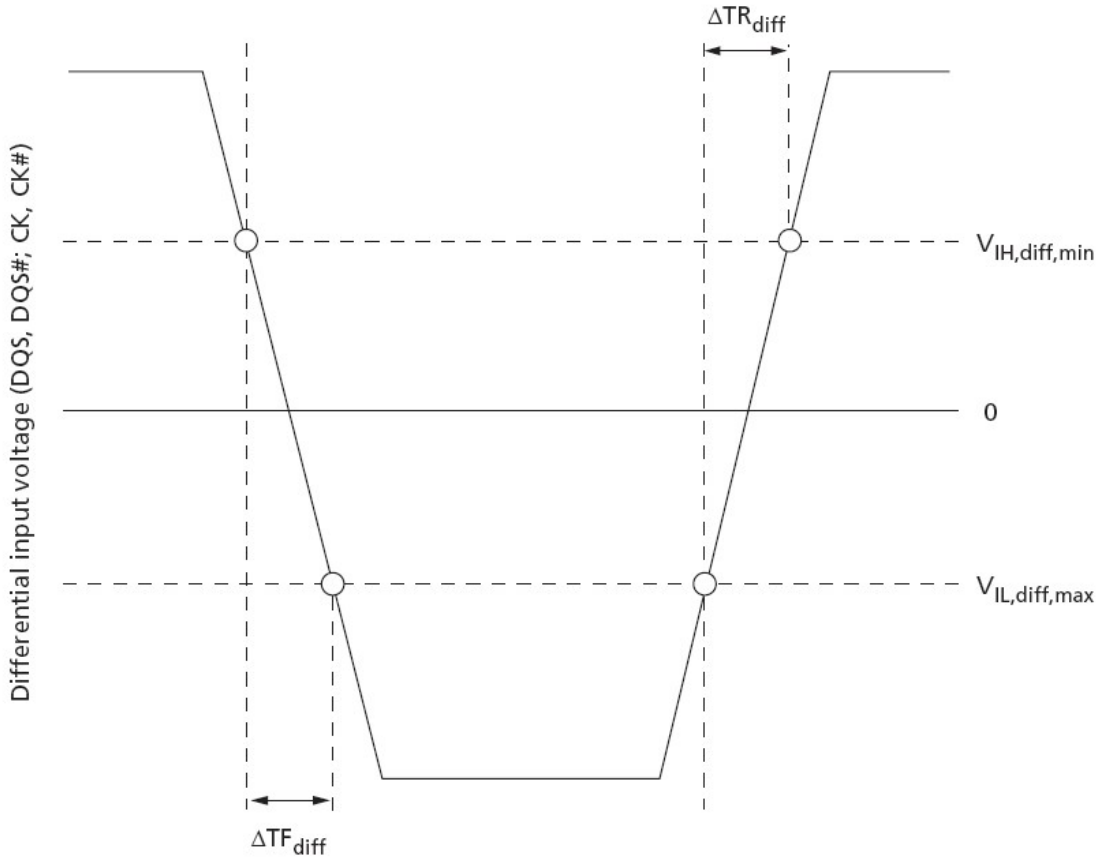


Figure 4-9: Nominal Differential Input Slew Rate Definition for DQS, DQS# and CK, CK#

ODT Characteristics

The ODT effective resistance R_{TT} is defined by MR1[9, 6, and 2]. ODT is applied to the DQ, DM, DQS and DQS#. The ODT target values and a functional representation are listed in Table 4-26 and Table 4-27. The individual pull-up and pull-down resistors ($R_{TT\ (PU)}$ and $R_{TT\ (PD)}$) are defined as follows:

- $R_{TT\ (PU)} = (V_{DDQ} - V_{OUT})/|I_{OUT}|$, under the condition that $R_{TT\ (PD)}$ is turned off.
- $R_{TT\ (PD)} = (V_{OUT})/|I_{OUT}|$, under the condition that $R_{TT\ (PU)}$ is turned off.

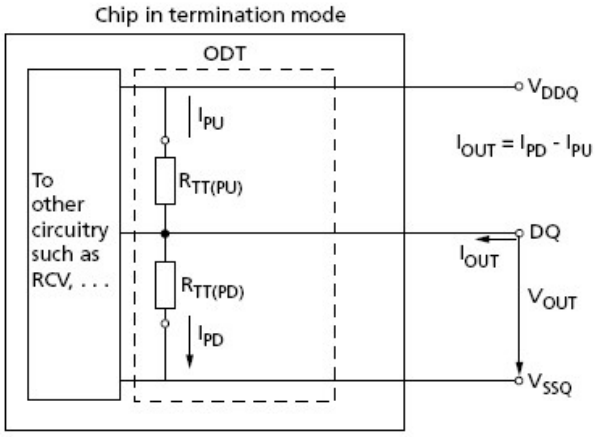


Figure 4-10: ODT Levels and I-V Characteristics

Table 4-25 On-Die Termination DC Electrical Characteristics

Parameter/Condition	Symbol	Min	Nom	Max	Unit	Notes
R_{TT} effective impedance	$R_{TT(EFF)}$	See Table 4-26				1, 2
Deviation of VM with respect to $V_{DDQ}/2$	ΔVM	–5		5	%	1, 2, 3

Notes:

1. Tolerance limits are applicable after proper ZQ calibration has been performed at a stable temperature and voltage (V_{DDQ} = V_{DD}, V_{SSQ} = V_{SS}). Refer to ODT Sensitivity if either the temperature or voltage changes after calibration.
2. Measurement definition for R_{TT}: Apply $V_{IH(AC)}$ to pin under test and measure current I[$V_{IH(AC)}$], then apply $V_{IL(AC)}$ to pin under test and measure current I[$V_{IL(AC)}$]:

$$R_{TT} = \frac{V_{IH(AC)} - V_{IL(AC)}}{I(V_{IH(AC)}) - I(V_{IL(AC)})}$$

3. Measure voltage (VM) at the tested pin with no load:

$$\Delta VM = \left[\frac{2 \times VM}{V_{DDQ}} - 1\right] \times 100$$

ODT Resistors

Table 4-26 provides an overview of the ODT DC electrical characteristics. The values provided are not specification requirements; however, they can be used as design guidelines to indicate what R_{TT} is targeted to provide:

- R_{TT} 120Ω is made up of $R_{TT120(PD240)}$ and $R_{TT120(PU240)}$.
- R_{TT} 60Ω is made up of $R_{TT60(PD120)}$ and $R_{TT60(PU120)}$.
- R_{TT} 40Ω is made up of $R_{TT40(PD80)}$ and $R_{TT40(PU80)}$.
- R_{TT} 30Ω is made up of $R_{TT30(PD60)}$ and $R_{TT30(PU60)}$.
- R_{TT} 20Ω is made up of $R_{TT20(PD40)}$ and $R_{TT20(PU40)}$.

Table 4-26-a: RTT Effective Impedances (DDR3L)

MR1 [9, 6, 2]	R_{TT}	Resistor	V_{OUT}	Min	Nom	Max	Units
0, 1, 0	120Ω	$R_{TT,120PD240}$	0.2 × V_{DDQ}	0.6	1.0	1.15	RZQ/1
			0.5 × V_{DDQ}	0.9	1.0	1.15	RZQ/1
			0.8 × V_{DDQ}	0.9	1.0	1.45	RZQ/1
		$R_{TT,120PU240}$	0.2 × V_{DDQ}	0.9	1.0	1.45	RZQ/1
			0.5 × V_{DDQ}	0.9	1.0	1.15	RZQ/1
			0.8 × V_{DDQ}	0.6	1.0	1.15	RZQ/1
	120Ω		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.65	RZQ/2
0, 0, 1	60Ω	$R_{TT,60PD120}$	0.2 × V_{DDQ}	0.6	1.0	1.15	RZQ/2
			0.5 × V_{DDQ}	0.9	1.0	1.15	RZQ/2
			0.8 × V_{DDQ}	0.9	1.0	1.45	RZQ/2
		$R_{TT,60PU120}$	0.2 × V_{DDQ}	0.9	1.0	1.45	RZQ/2
			0.5 × V_{DDQ}	0.9	1.0	1.15	RZQ/2
			0.8 × V_{DDQ}	0.6	1.0	1.15	RZQ/2
	60Ω		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.65	RZQ/4
0, 1, 1	40Ω	$R_{TT,40PD80}$	0.2 × V_{DDQ}	0.6	1.0	1.15	RZQ/3
			0.5 × V_{DDQ}	0.9	1.0	1.15	RZQ/3
			0.8 × V_{DDQ}	0.9	1.0	1.45	RZQ/3
		$R_{TT,40PU80}$	0.2 × V_{DDQ}	0.9	1.0	1.45	RZQ/3
			0.5 × V_{DDQ}	0.9	1.0	1.15	RZQ/3
			0.8 × V_{DDQ}	0.6	1.0	1.15	RZQ/3
	40Ω		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.65	RZQ/6
1, 0, 1	30Ω	$R_{TT,30PD60}$	0.2 × V_{DDQ}	0.6	1.0	1.15	RZQ/4
			0.5 × V_{DDQ}	0.9	1.0	1.15	RZQ/4
			0.8 × V_{DDQ}	0.9	1.0	1.45	RZQ/4
		$R_{TT,30PU60}$	0.2 × V_{DDQ}	0.9	1.0	1.45	RZQ/4
			0.5 × V_{DDQ}	0.9	1.0	1.15	RZQ/4
			0.8 × V_{DDQ}	0.6	1.0	1.15	RZQ/4
	30Ω		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.65	RZQ/8
1, 0, 0	20Ω	$R_{TT,20PD40}$	0.2 × V_{DDQ}	0.6	1.0	1.15	RZQ/6
			0.5 × V_{DDQ}	0.9	1.0	1.15	RZQ/6
			0.8 × V_{DDQ}	0.9	1.0	1.45	RZQ/6
		$R_{TT,20PU40}$	0.2 × V_{DDQ}	0.9	1.0	1.45	RZQ/6
			0.5 × V_{DDQ}	0.9	1.0	1.15	RZQ/6
			0.8 × V_{DDQ}	0.6	1.0	1.15	RZQ/6
	20Ω		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.65	RZQ/12

Table 4-26-b: RTT Effective Impedances (DDR3)

MR1 [9, 6, 2]	R_{TT}	Resistor	V_{OUT}	Min	Nom	Max	Unit
0, 1, 0	120Ω	$R_{TT120(PD240)}$	0.2 × V_{DDQ}	0.6	1.0	1.1	RZQ/1
			0.5 × V_{DDQ}	0.9	1.0	1.1	RZQ/1
			0.8 × V_{DDQ}	0.9	1.0	1.4	RZQ/1
		$R_{TT120(PU240)}$	0.2 × V_{DDQ}	0.9	1.0	1.4	RZQ/1
			0.5 × V_{DDQ}	0.9	1.0	1.1	RZQ/1
			0.8 × V_{DDQ}	0.6	1.0	1.1	RZQ/1
	120Ω		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.6	RZQ/2
0, 0, 1	60Ω	$R_{TT60(PD120)}$	0.2 × V_{DDQ}	0.6	1.0	1.1	RZQ/2
			0.5 × V_{DDQ}	0.9	1.0	1.1	RZQ/2
			0.8 × V_{DDQ}	0.9	1.0	1.4	RZQ/2
		$R_{TT60(PU120)}$	0.2 × V_{DDQ}	0.9	1.0	1.4	RZQ/2
			0.5 × V_{DDQ}	0.9	1.0	1.1	RZQ/2
			0.8 × V_{DDQ}	0.6	1.0	1.1	RZQ/2
	60Ω		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.6	RZQ/4
0, 1, 1	40Ω	$R_{TT40(PD80)}$	0.2 × V_{DDQ}	0.6	1.0	1.1	RZQ/3
			0.5 × V_{DDQ}	0.9	1.0	1.1	RZQ/3
			0.8 × V_{DDQ}	0.9	1.0	1.4	RZQ/3
		$R_{TT40(PU80)}$	0.2 × V_{DDQ}	0.9	1.0	1.4	RZQ/3
			0.5 × V_{DDQ}	0.9	1.0	1.1	RZQ/3
			0.8 × V_{DDQ}	0.6	1.0	1.1	RZQ/3
	40Ω		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.6	RZQ/6
1, 0, 1	30Ω	$R_{TT30(PD60)}$	0.2 × V_{DDQ}	0.6	1.0	1.1	RZQ/4
			0.5 × V_{DDQ}	0.9	1.0	1.1	RZQ/4
			0.8 × V_{DDQ}	0.9	1.0	1.4	RZQ/4
		$R_{TT30(PU60)}$	0.2 × V_{DDQ}	0.9	1.0	1.4	RZQ/4
			0.5 × V_{DDQ}	0.9	1.0	1.1	RZQ/4
			0.8 × V_{DDQ}	0.6	1.0	1.1	RZQ/4
	30Ω		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.6	RZQ/8
1, 0, 0	20Ω	$R_{TT20(PD40)}$	0.2 × V_{DDQ}	0.6	1.0	1.1	RZQ/6
			0.5 × V_{DDQ}	0.9	1.0	1.1	RZQ/6
			0.8 × V_{DDQ}	0.9	1.0	1.4	RZQ/6
		$R_{TT20(PU40)}$	0.2 × V_{DDQ}	0.9	1.0	1.4	RZQ/6
			0.5 × V_{DDQ}	0.9	1.0	1.1	RZQ/6
			0.8 × V_{DDQ}	0.6	1.0	1.1	RZQ/6
	20Ω		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.6	RZQ/12

Note:

1. Values assume an RZQ of 2400(±1%)

ODT Sensitivity

If either the temperature or voltage changes after I/O calibration, then the tolerance limits listed in Table 4-25 and Table 4-26 can be expected to widen according to Table 4-27 and Table 4-28.

Table 4-27: ODT Sensitivity Definition

Symbol	Min	Max	Unit
R_{TT}	0.9 - $dR_{TT}dT$ × |DT| - $dR_{TT}dV$ × |DV|	1.6 + $dR_{TT}dT$ × |DT| + $dR_{TT}dV$ × |DV|	RZQ/(2, 4, 6, 8, 12)

Note:

1. $\Delta T = T - T$(@ calibration), $\Delta V = V_{DDQ} - V_{DDQ}$(@ calibration) and $V_{DD} = V_{DDQ}$.

Table 4-28: ODT Sensitivity Definition

Change	Min	Max	Unit
$dR_{TT}dT$	0	1.5	%/℃
$dR_{TT}dV$	0	0.15	%/mV

Note:

1. $\Delta T = T - T$ (@ calibration), $\Delta V = V_{DDQ} - V_{DDQ}$ (@ calibration) and $V_{DD} = V_{DDQ}$.

ODT Timing Definitions

ODT loading differs from that used in AC timing measurements. The reference load for ODT timings is shown in Figure 4-11. Two parameters define when ODT turns on or off synchronously, two define when ODT turns on or off asynchronously, and another defines when ODT turns on or off dynamically. Table 4-30 outlines and provides definition and measurement references settings for each parameter.

ODT turn-on time begins when the output leaves High-Z and ODT resistance begins to turn on. ODT turn-off time begins when the output leaves Low-Z and ODT resistance begins to turn off.

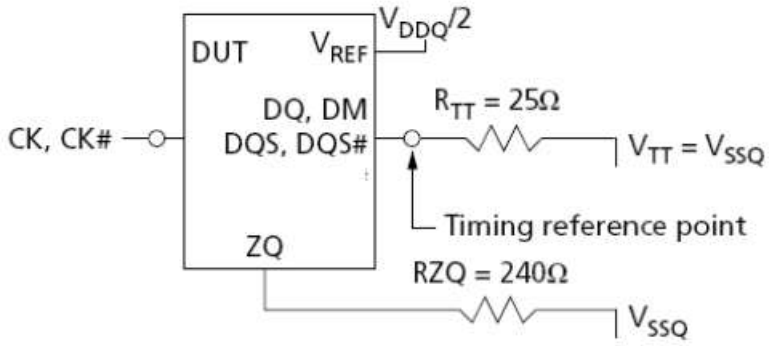


Figure 4-11: ODT Timing Reference Load

Table 4-29: ODT Timing Definitions

Symbol	Begin Point Definition	End Point Definition	Figure
tAON	Rising edge of CK - CK# defined by the end point of ODTLon	Extrapolated point at V_{SSQ}	Figure 4-12
tAOF	Rising edge of CK - CK# defined by the end point of ODTLoff	Extrapolated point at $VR_{TT,nom}$	Figure 4-12
tAONPD	Rising edge of CK - CK# with ODT first being registered HIGH	Extrapolated point at V_{SSQ}	Figure 4-13
tAOFPD	Rising edge of CK - CK# with ODT first being registered LOW	Extrapolated point at $VR_{TT,nom}$	Figure 4-13
tADC	Rising edge of CK - CK# defined by the end point of ODTLcnw, ODTLcwn4, or ODTLcwn8	Extrapolated points at $VR_{TT(WR)}$ and $VR_{TT,nom}$	Figure 4-14

Table 4-30-a: Reference Settings for ODT Timing Measurements

Measured Parameter	$R_{TT,nom}$ Setting	$R_{TT(WR)}$ Setting	V_{SW1}	V_{SW2}
tAON	RZQ/4 (60Ω)	N/A	50mV	100mV
	RZQ/12 (20Ω)	N/A	100mV	200mV
tAOF	RZQ/4 (60Ω)	N/A	50mV	100mV
	RZQ/12 (20Ω)	N/A	100mV	200mV
tAONPD	RZQ/4 (60Ω)	N/A	50mV	100mV
	RZQ/12 (20Ω)	N/A	100mV	200mV
tAOFPD	RZQ/4 (60Ω)	N/A	50mV	100mV
	RZQ/12 (20Ω)	N/A	100mV	200mV
tADC (DDR3L)	RZQ/12 (20Ω)	RZQ/2 (120Ω)	200mV	250mV
tADC (DDR3)	RZQ/12 (20Ω)	RZQ/2 (120Ω)	200mV	300mV

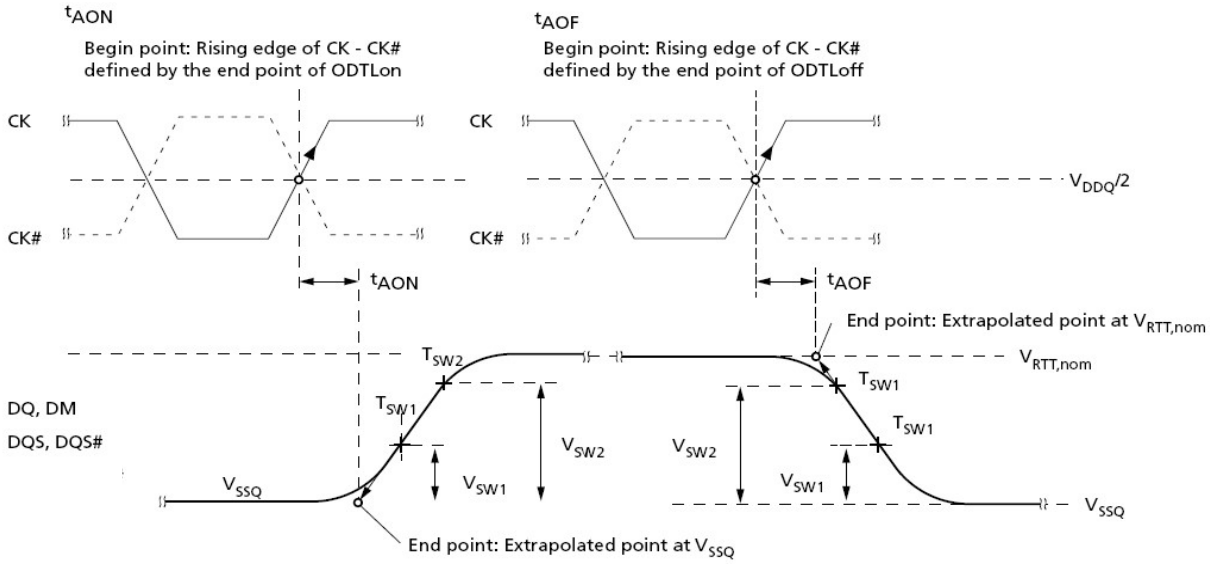


Figure 4-12: tAON and tAOF Definitions

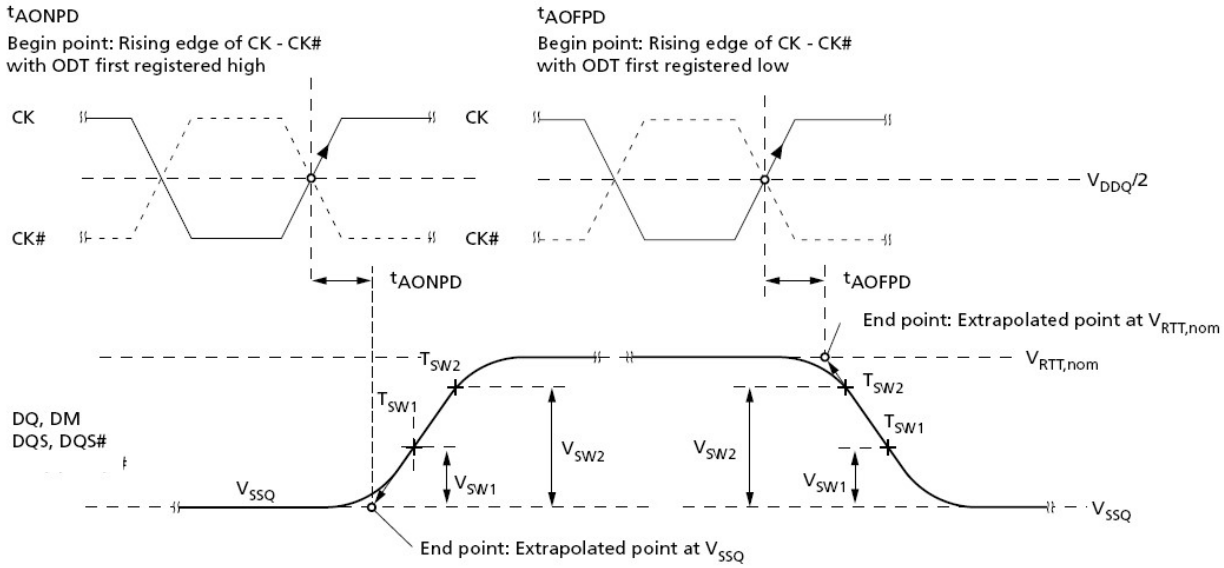


Figure 4-13: tAONPD and tAOFPD Definitions

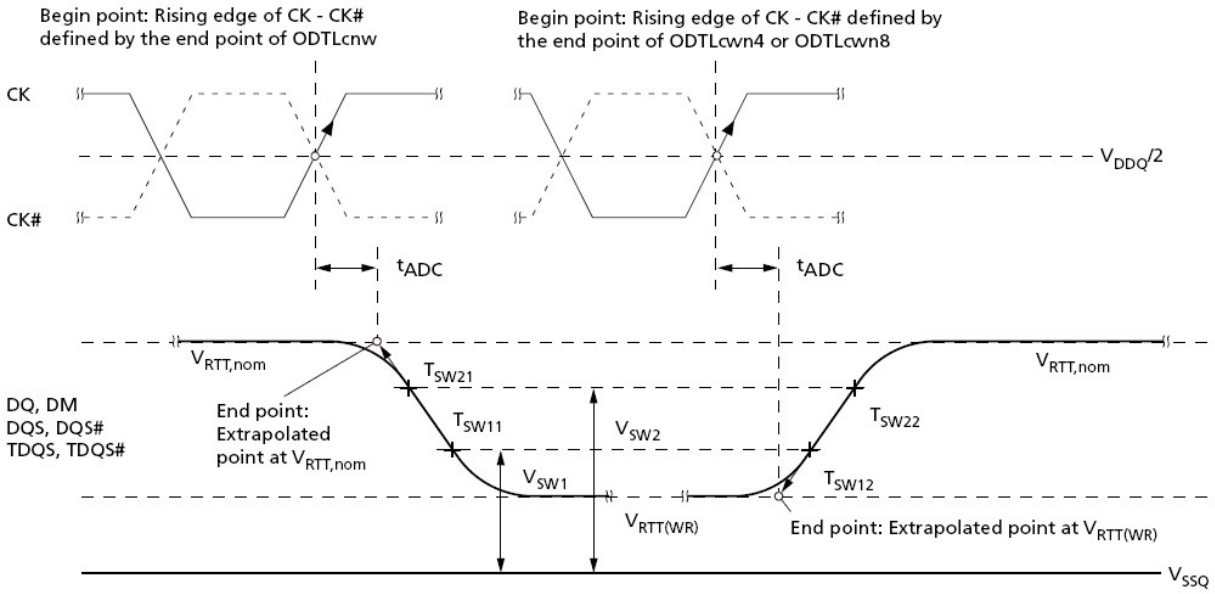


Figure 4-14: tADC Definition

Output Driver Impedance

The output driver impedance is selected by MR1[5,1] during initialization. The selected value is able to maintain the tight tolerances specified if proper ZQ calibration is performed. Output specifications refer to the default output driver unless specifically stated otherwise. A functional representation of the output buffer is shown below. The output driver impedance R_{ON} is defined by the value of the external reference resistor RZQ as follows:

- $R_{ON,x} = RZQ/y$ (with RZQ = 240Ω ±1%; χ=34Ω or 40Ω with y = 7 or 6, respectively).

The individual pull-up and pull-down resistors $R_{ON(PU)}$ and $R_{ON(PD)}$ are defined as follows:

- $R_{ON(PU)} = (V_{DDQ} - V_{OUT})/|I_{OUT}|$, when $R_{ON(PD)}$ is turned off.
- $R_{ON(PD)} = (V_{OUT})/|I_{OUT}|$, when $R_{ON(PU)}$ is turned off.

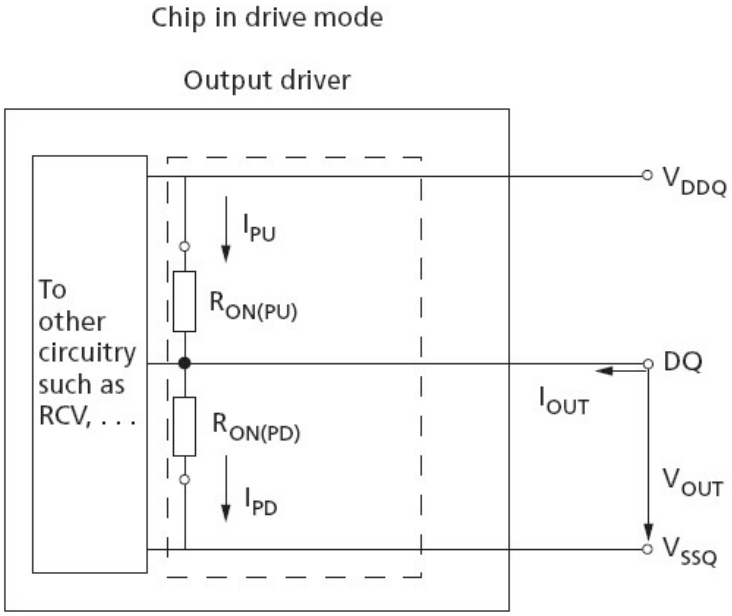


Figure 4-15: Output Driver

Ohm Output Driver Impedance

The 34Ω driver (MR1[5, 1] = 01) is the default driver. Unless otherwise stated, all timings and specifications listed herein apply to the 34Ω driver only. Its impedance R_{ON} is defined by the value of the external reference resistor RZQ as follows: R_{ON34} = RZQ/7 (with nominal RZQ = 240Ω ±1%) and is actually 34.3Ω ±1%.

Table 4-31-a: 34 Ohm Driver Impedance Characteristics (DDR3L)

MR1 [5, 1]	R_{ON}	Resistor	V_{OUT}	Min	Nom	Max	Units
0, 1	34.3Ω	$R_{ON,34PD}$	0.2 × V_{DDQ}	0.6	1.0	1.15	RZQ/7
			0.5 × V_{DDQ}	0.9	1.0	1.15	RZQ/7
			0.8 × V_{DDQ}	0.9	1.0	1.45	RZQ/7
		$R_{ON,34PU}$	0.2 × V_{DDQ}	0.9	1.0	1.45	RZQ/7
			0.5 × V_{DDQ}	0.9	1.0	1.15	RZQ/7
			0.8 × V_{DDQ}	0.6	1.0	1.15	RZQ/7
Pull-up/pull-down mismatch (MM_{PUPD})			$V_{IL(AC)}$ to $V_{IH(AC)}$	–10	N/A	10	%

Table 4-31-b: 34 Ohm Driver Impedance Characteristics (DDR3)

MR1 [5, 1]	R_{ON}	Resistor	V_{OUT}	Min	Nom	Max	Units
0, 1	34.3Ω	$R_{ON,34PD}$	0.2 × V_{DDQ}	0.6	1.0	1.1	RZQ/7
			0.5 × V_{DDQ}	0.9	1.0	1.1	RZQ/7
			0.8 × V_{DDQ}	0.9	1.0	1.4	RZQ/7
		$R_{ON,34PU}$	0.2 × V_{DDQ}	0.9	1.0	1.4	RZQ/7
			0.5 × V_{DDQ}	0.9	1.0	1.1	RZQ/7
			0.8 × V_{DDQ}	0.6	1.0	1.1	RZQ/7
Pull-up/pull-down mismatch (MM_{PUPD})			0.5 × V_{DDQ}	–10	N/A	10	%

Notes:

1. Tolerance limits assume RZQ of 240Ω ±1% and are applicable after proper ZQ calibration has been performed at a stable temperature and voltage: V_{DDQ} = V_{DD}; V_{SSQ} = V_{SS}). Refer to section: 34 Ohm Output Driver Sensitivity if either the temperature or the voltage changes after calibration.
2. Measurement definition for mismatch between pull-up and pull-down (MM_{PUPD}). Measure both $R_{ON(PU)}$ and $R_{ON(PD)}$ at 0.5 × V_{DDQ}:

$$MM_{PUPD} = \frac{R_{ON(PU)} - R_{ON(PD)}}{R_{ON,nom}} \times 100$$

Ohm Driver

Using Table 4-32, the 34Ω driver's current range has been calculated and summarized in Table 4-33 V_{DD} = 1.35V, Table 4-34 for V_{DD} = 1.45V, and Table 4-35 for V_{DD} = 1.283V. The individual pull-up and pull-down resistors $R_{ON34(PD)}$ and $R_{ON34(PU)}$ are defined as follows:

- $R_{ON34(PD)} = (V_{OUT})/|I_{OUT}|$; $R_{ON34(PU)}$ is turned off.
- $R_{ON34(PU)} = (V_{DDQ} - V_{OUT})/|I_{OUT}|$; $R_{ON34(PD)}$ is turned off.

Table 4-32: 34 Ohm Driver Pull-Up and Pull-Down Impedance Calculations

R_{ON}				Min	Nom	Max	Unit
RZQ = 240Ω±1%				237.6	240	242.4	Ω
RZQ/7 = (240Ω±1%)/7				33.9	34.3	34.6	Ω
MR1[5,1]	**R_{ON}**	**Resistor**	**V_{OUT}**	**Min**	**Nom**	**Max**	**Unit**
0, 1	34.3Ω	$R_{ON34(PD)}$	0.2 × V_{DDQ}	20.4	34.3	38.1	Ω
			0.5 × V_{DDQ}	30.5	34.3	38.1	Ω
			0.8 × V_{DDQ}	30.5	34.3	48.5	Ω
		$R_{ON34(PU)}$	0.2 × V_{DDQ}	30.5	34.3	48.5	Ω
			0.5 × V_{DDQ}	30.5	34.3	38.1	Ω
			0.8 × V_{DDQ}	20.4	34.3	38.1	Ω

Table 4-33: 34 Ohm Driver I_{OH}/I_{OL} Characteristics: V_{DD} = V_{DDQ} = 1.35V

MR1[5,1]	R_{ON}	Resistor	V_{OUT}	Max	Nom	Min	Unit
0, 1	34.3Ω	$R_{ON34(PD)}$	I_{OL} @ 0.2 × V_{DDQ}	13.3	7.9	7.1	mA
			I_{OL} @ 0.5 × V_{DDQ}	22.1	19.7	17.7	mA
			I_{OL} @ 0.8 × V_{DDQ}	35.4	31.5	22.3	mA
		$R_{ON34(PU)}$	I_{OH} @ 0.2 × V_{DDQ}	35.4	31.5	22.3	mA
			I_{OH} @ 0.5 × V_{DDQ}	22.1	19.7	17.7	mA
			I_{OH} @ 0.8 × V_{DDQ}	13.3	7.9	7.1	mA

Table 4-34: 34 Ohm Driver I_{OH}/I_{OL} Characteristics: V_{DD} = V_{DDQ} = 1.45V

MR1[5,1]	R_{ON}	Resistor	V_{OUT}	Max	Nom	Min	Unit
0, 1	34.3Ω	$R_{ON34(PD)}$	I_{OL} @ 0.2 × V_{DDQ}	14.2	8.5	7.6	mA
			I_{OL} @ 0.5 × V_{DDQ}	23.7	21.1	19.0	mA
			I_{OL} @ 0.8 × V_{DDQ}	38.0	33.8	23.9	mA
		$R_{ON34(PU)}$	I_{OH} @ 0.2 × V_{DDQ}	38.0	33.8	23.9	mA
			I_{OH} @ 0.5 × V_{DDQ}	23.7	21.1	19.0	mA
			I_{OH} @ 0.8 × V_{DDQ}	14.2	8.5	7.6	mA

Table 4-35: 34 Ohm Driver I_{OH}/I_{OL} Characteristics: $V_{DD} = V_{DDQ} = 1.283V$

MR1[5,1]	RON	Resistor	VOUT	Max	Nom	Min	Unit
0, 1	34.3Ω	$R_{ON34(PD)}$	I_{OL} @ 0.2 × V_{DDQ}	12.6	7.5	6.7	mA
			I_{OL} @ 0.5 × V_{DDQ}	21.0	18.7	16.8	mA
			I_{OL} @ 0.8 × V_{DDQ}	33.6	29.9	21.2	mA
		$R_{ON34(PU)}$	I_{OH} @ 0.2 × V_{DDQ}	33.6	29.9	21.2	mA
			I_{OH} @ 0.5 × V_{DDQ}	21.0	18.7	16.8	mA
			I_{OH} @ 0.8 × V_{DDQ}	12.6	7.5	6.7	mA

Ohm Output Driver Sensitivity

If either the temperature or the voltage changes after ZQ calibration, then the tolerance limits listed in

Table 4-31 can be expected to widen according to Table 4-36 and Table 4-37 .

Table 4-36: 34 Ohm Output Driver Sensitivity Definition

Symbol	Min	Max	Unit
$R_{ON(PD)}$ @ 0.2 × V_{DDQ}	0.6 - $dR_{ON}dTL$ × |ΔT| - $dR_{ON}dVL$ × |ΔV|	1.1 + $dR_{ON}dTL$ × |ΔT| + $dR_{ON}dVL$ × |ΔV|	RZQ/7
$R_{ON(PD)}$ @ 0.5 × V_{DDQ}	0.9 - $dR_{ON}dTM$ × |ΔT| - $dR_{ON}dVM$ × |ΔV|	1.1 + $dR_{ON}dTM$ × |ΔT| + $dR_{ON}dVM$ × |ΔV|	RZQ/7
$R_{ON(PD)}$ @ 0.8 × V_{DDQ}	0.9 - $dR_{ON}dTH$ × |ΔT| - $dR_{ON}dVH$ × |ΔV|	1.4 + $dR_{ON}dTH$ × |ΔT| + $dR_{ON}dVH$ × |ΔV|	RZQ/7
$R_{ON(PU)}$ @ 0.2 × V_{DDQ}	0.9 - $dR_{ON}dTL$ × |ΔT| - $dR_{ON}dVL$ × |ΔV|	1.4 + $dR_{ON}dTL$ × |ΔT| + $dR_{ON}dVL$ × |ΔV|	RZQ/7
$R_{ON(PU)}$ @ 0.5 × V_{DDQ}	0.9 - $dR_{ON}dTM$ × |ΔT| - $dR_{ON}dVM$ × |ΔV|	1.1 + $dR_{ON}dTM$ × |ΔT| + $dR_{ON}dVM$ × |ΔV|	RZQ/7
$R_{ON(PU)}$ @ 0.8 × V_{DDQ}	0.6 - $dR_{ON}dTH$ × |ΔT| - $dR_{ON}dVH$ × |ΔV|	1.1 + $dR_{ON}dTH$ × |ΔT| + $dR_{ON}dVH$ × |ΔV|	RZQ/7

Note:

1. $\Delta T = T - T_{(@CALIBRATION)}$;$\Delta V = V_{DDQ} - V_{DDQ(@CALIBRATION)}$; and $V_{DD} = V_{DDQ}$.

Table 4-37: 34 Ohm Output Driver Voltage and Temperature Sensitivity

Change	Min	Max	Unit
$dR_{ON}dTM$	0	1.5	%/℃
$dR_{ON}dVM$	0	0.13	%/mV
$dR_{ON}dTL$	0	1.5	%/℃
$dR_{ON}dVL$	0	0.13	%/mV
$dR_{ON}dTH$	0	1.5	%/℃
$dR_{ON}dVH$	0	0.13	%/mV

Alternative 40 Ohm Driver

Table 4-38-a: 40 Ohm Driver Impedance Characteristics (DDR3L)

MR1[5,1]	R_{ON}	Resistor	V_{OUT}	Max	Nom	Min	Unit
0, 0	40Ω	$R_{ON,40PD}$	0.2 × V_{DDQ}	0.6	1.0	1.15	RZQ/6
			0.5 × V_{DDQ}	0.9	1.0	1.15	RZQ/6
			0.8 × V_{DDQ}	0.9	1.0	1.45	RZQ/6
		$R_{ON,40PU}$	0.2 × V_{DDQ}	0.9	1.0	1.45	RZQ/6
			0.5 × V_{DDQ}	0.9	1.0	1.15	RZQ/6
			0.8 × V_{DDQ}	0.6	1.0	1.15	RZQ/6
Pull-up/pull-down mismatch (MM_{PUPD})			$V_{IL(AC)}$ to $V_{IH(AC)}$	-10	N/A	10	%

Table 4-38-b: 40 Ohm Driver Impedance Characteristics (DDR3)

MR1[5,1]	R_{ON}	Resistor	V_{OUT}	Max	Nom	Min	Unit
0, 0	40Ω	$R_{ON,40PD}$	0.2 × V_{DDQ}	0.6	1.0	1.1	RZQ/6
			0.5 × V_{DDQ}	0.9	1.0	1.1	RZQ/6
			0.8 × V_{DDQ}	0.9	1.0	1.4	RZQ/6
		$R_{ON,40PU}$	0.2 × V_{DDQ}	0.9	1.0	1.4	RZQ/6
			0.5 × V_{DDQ}	0.9	1.0	1.1	RZQ/6
			0.8 × V_{DDQ}	0.6	1.0	1.1	RZQ/6
Pull-up/pull-down mismatch (MM_{PUPD})			0.5 × V_{DDQ}	-10	N/A	10	%

Notes:

1. Tolerance limits assume RZQ of 240Ω ±1% and are applicable after proper ZQ calibration has been performed at a stable temperature and voltage (V_{DDQ} = V_{DD}; V_{SSQ} = V_{SS}). Refer to section: 40 Ohm Output Driver Sensitivity if either the temperature or the voltage changes after calibration.

2. Measurement definition for mismatch between pull-up and pull-down (MM_{PUPD}). Measure both $R_{ON(PU)}$ and $R_{ON(PD)}$ at 0.5 × V_{DDQ}:

$$MM_{PUPD} = \frac{R_{ON(PU)} - R_{ON(PD)}}{R_{ON,nom}} \times 100$$

Ohm Output Driver Sensitivity

If either the temperature or the voltage changes after I/O calibration, then the tolerance limits listed in Table 4-38 can be expected to widen according to Table 4-40 and Table 4-41.

Table 4-39: 40 Ohm Output Driver Sensitivity Definition

Symbol	Min	Max	Unit
$R_{ON(PD)}$ @ 0.2 × V_{DDQ}	0.6 - $dR_{ON}dTL$ × |ΔT| - $dR_{ON}dVL$ × |ΔV|	1.1 + $dR_{ON}dTL$ × |ΔT| + $dR_{ON}dVL$ × |ΔV|	RZQ/6
$R_{ON(PD)}$ @ 0.5 × V_{DDQ}	0.9 - $dR_{ON}dTM$ × |ΔT| - $dR_{ON}dVM$ × |ΔV|	1.1 + $dR_{ON}dTM$ × |ΔT| + $dR_{ON}dVM$ × |ΔV|	RZQ/6
$R_{ON(PD)}$ @ 0.8 × V_{DDQ}	0.9 - $dR_{ON}dTH$ × |ΔT| - $dR_{ON}dVH$ × |ΔV|	1.4 + $dR_{ON}dTH$ × |ΔT| + $dR_{ON}dVH$ × |ΔV|	RZQ/6
$R_{ON(PU)}$ @ 0.2 × V_{DDQ}	0.9 - $dR_{ON}dTL$ × |ΔT| - $dR_{ON}dVL$ × |ΔV|	1.4 + $dR_{ON}dTL$ × |ΔT| + $dR_{ON}dVL$ × |ΔV|	RZQ/6
$R_{ON(PU)}$ @ 0.5 × V_{DDQ}	0.9 - $dR_{ON}dTM$ × |ΔT| - $dR_{ON}dVM$ × |ΔV|	1.1 + $dR_{ON}dTM$ × |ΔT| + $dR_{ON}dVM$ × |ΔV|	RZQ/6
$R_{ON(PU)}$ @ 0.8 × V_{DDQ}	0.6 - $dR_{ON}dTH$ × |ΔT| - $dR_{ON}dVH$ × |ΔV|	1.1 + $dR_{ON}dTH$ × |ΔT| + $dR_{ON}dVH$ × |ΔV|	RZQ/6

Note:

1. $\Delta T = T - T_{(@CALIBRATION)}$, $\Delta V = V_{DDQ} - V_{DDQ(@CALIBRATION)}$; and $V_{DD} = V_{DDQ}$.

Table 4-40: 40 Ohm Output Driver Voltage and Temperature Sensitivity

Change	Min	Max	Unit
$dR_{ON}dTM$	0	1.5	%/℃
$dR_{ON}dVM$	0	0.15	%/mV
$dR_{ON}dTL$	0	1.5	%/℃
$dR_{ON}dVL$	0	0.15	%/mV
$dR_{ON}dTH$	0	1.5	%/℃
$dR_{ON}dVH$	0	0.15	%/mV

Output Characteristics and Operating Conditions

Table 4-41: Single-Ended Output Driver Characteristics

All voltages are referenced to V_{SS}

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Output leakage current: DQ are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ}; ODT is disabled; ODT is HIGH	I_{OZ}	–5	5	uA	1
DDR3L: Output slew rate: Single-ended; For rising and falling edges, measure between $V_{OL(AC)}$ = V_{REF} - 0.09 ×	SRQ_{se}	1.75	6	V/ns	1, 2, 3, 4
DDR3: Output slew rate: Single-ended; For rising and falling edges, measure between $V_{OL(AC)}$ = V_{REF} - 0.1	SRQ_{se}	2.5	6	V/ns	1, 2, 3, 4
Single-ended DC high-level output voltage	$V_{OH(DC)}$	0.8 × V_{DDQ}		V	1, 2, 5
Single-ended DC mid-point level output voltage	$V_{OM(DC)}$	0.5 × V_{DDQ}		V	1, 2, 5
Single-ended DC low-level output voltage	$V_{OL(DC)}$	0.2 × V_{DDQ}		V	1, 2, 5
Single-ended AC high-level output voltage	$V_{OH(AC)}$	V_{TT} + 0.1 × V_{DDQ}		V	1, 2, 3, 6
Single-ended AC low-level output voltage	$V_{OL(AC)}$	V_{TT} - 0.1 × V_{DDQ}		V	1, 2, 3, 6
Delta R_{ON} between pull-up and pull-down for DQ/DQS	MM_{PUPD}	–10	10	%	1, 7
Test load for AC timing and output slew rates	Output to V_{TT} (V_{DDQ}/2) via 25Ω resistor				3

Notes:

1. RZQ of 240Ω ±1% with RZQ/7 enabled (default 34Ω driver) and is applicable after proper ZQ calibration has been performed at a stable temperature and voltage (V_{DDQ} = V_{DD}; V_{SSQ} = V_{SS}).
2. V_{TT} = V_{DDQ}/2.
3. See Figure 4-18 for the test load configuration.
4. The 6 V/ns maximum is applicable for a single DQ signal when it is switching either from HIGH to LOW or LOW to HIGH while the remaining DQ signals in the same byte lane are either all static or all switching in the opposite direction. For all other DQ signal switching combinations, the maximum limit of 6 V/ns is reduced to 5 V/ns.
5. See Figure 4-15 for IV curve linearity. Do not use AC test load.
6. See Slew Rate Definitions for Single-Ended Output Signals for output slew rate.
7. See Figure 4-15 for additional information.
8. See Figure 4-16 for an example of a single-ended output signal.

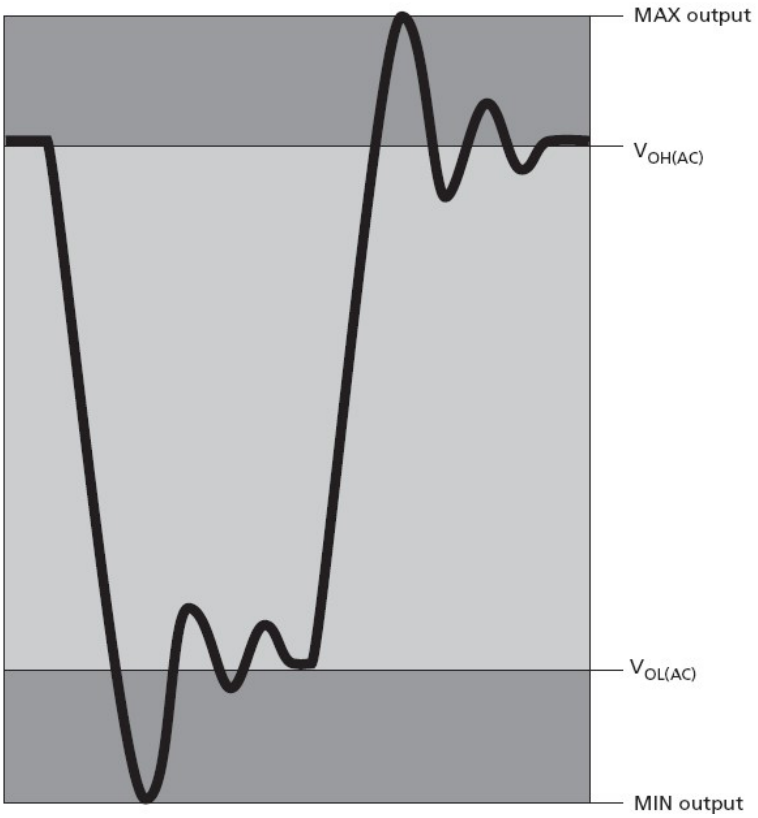


Figure 4-16: DQ Output Signal

Table 4-42: Differential Output Driver Characteristics

All voltages are referenced to V_{SS}

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Output leakage current: DQ are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ}; ODT is disabled; ODT is HIGH	Ioz	–5	5	uA	1
DDR3L: Output slew rate: Differential; For rising and falling edges, measure between $V_{OL,diff(AC)}$ = –0.18 ×	SRQ_{diff}	3.5	12	V/ns	1
DDR3: Output slew rate: Differential; For rising and falling edges, measure between $V_{OL,diff(AC)}$ = –0.2 ×	SRQ_{diff}	5	12	V/ns	1
Differential high-level output voltage	$V_{OH,diff(AC)}$	+0.2 × V_{DDQ}		V	1, 4
Differential low-level output voltage	$V_{OL,diff(AC)}$	–0.2 × V_{DDQ}		V	1, 4
Delta Ron between pull-up and pull-down for DQ/DQS	MM_{PUPD}	–10	10	%	1, 5
Test load for AC timing and output slew rates	Output to V_{TT} (V_{DDQ}/2) via 25Ω resistor				3

Notes:

1. RZQ of 240Ω ±1% with RZQ/7 enabled (default 34Ω driver) and is applicable after proper ZQ calibration has been performed at a stable temperature and voltage (V_{DDQ} = V_{DD}; V_{SSQ} = V_{SS}).
2. V_{REF} = V_{DDQ}/2; slew rate @ 5 V/ns, interpolate for faster slew rate.

3. See Figure 4-18 for the test load configuration.

4. See Table 4-46 for the output slew rate.

5. See Table 4-32 for additional information.

6. See Figure 4-17 for an example of a differential output signal.

Table 4-43 Differential Output Driver Characteristics $V_{OX(AC)}$

All voltages are referenced to V_{SS}

Parameter/ Condition	Symbol		DDR3(L)-1066 DQS/DQS# Differential Slew Rate									Unit
			3.5V/ns	4V/ns	5V/ns	6V/ns	7V/ns	8V/ns	9V/ns	10V/ns	12V/ns	
Output differential crosspoint voltage (DDR3)	$V_{OX(AC)}$	Max	–	–	150	–	–	–	–	–	–	mV
		Min	–	–	–150	–	–	–	–	–	–	mV
Parameter/ Condition	**Symbol**		**DDR3(L)-1066/1333 DQS/DQS# Differential Slew Rate**									**Unit**
			3.5V/ns	**4V/ns**	**5V/ns**	**6V/ns**	**7V/ns**	**8V/ns**	**9V/ns**	**10V/ns**	**12V/ns**	
Output differential crosspoint voltage (DDR3L)	$V_{OX(AC)}$	Max	115	130	135	195	205	205	205	205	205	mV
		Min	–115	–130	–135	–195	–205	–205	–205	–205	–205	mV
Parameter/ Condition	**Symbol**		**DDR3(L)-1600 DQS/DQS# Differential Slew Rate**									**Unit**
			3.5V/ns	**4V/ns**	**5V/ns**	**6V/ns**	**7V/ns**	**8V/ns**	**9V/ns**	**10V/ns**	**12V/ns**	
Output differential crosspoint voltage (DDR3L)	$V_{OX(AC)}$	Max	90	105	135	155	180	205	205	205	205	mV
		Min	–90	–105	–135	–155	–180	–205	–205	–205	–205	mV

1. RZQ of 240Ω ±1% with RZQ/7 enabled (default 34Ω driver) and is applicable after proper ZQ calibration has been performed at a stable temperature and voltage (V_{DDQ} = V_{DD}; V_{SSQ} = V_{SS}).

2. See Figure 4-18 for the test load configuration.

3. See Figure 4-17 for an example of a differential output signal.

4. For a differential slew rate between the list values, the $V_{OX(AC)}$ value may be obtained by linear interpolation.

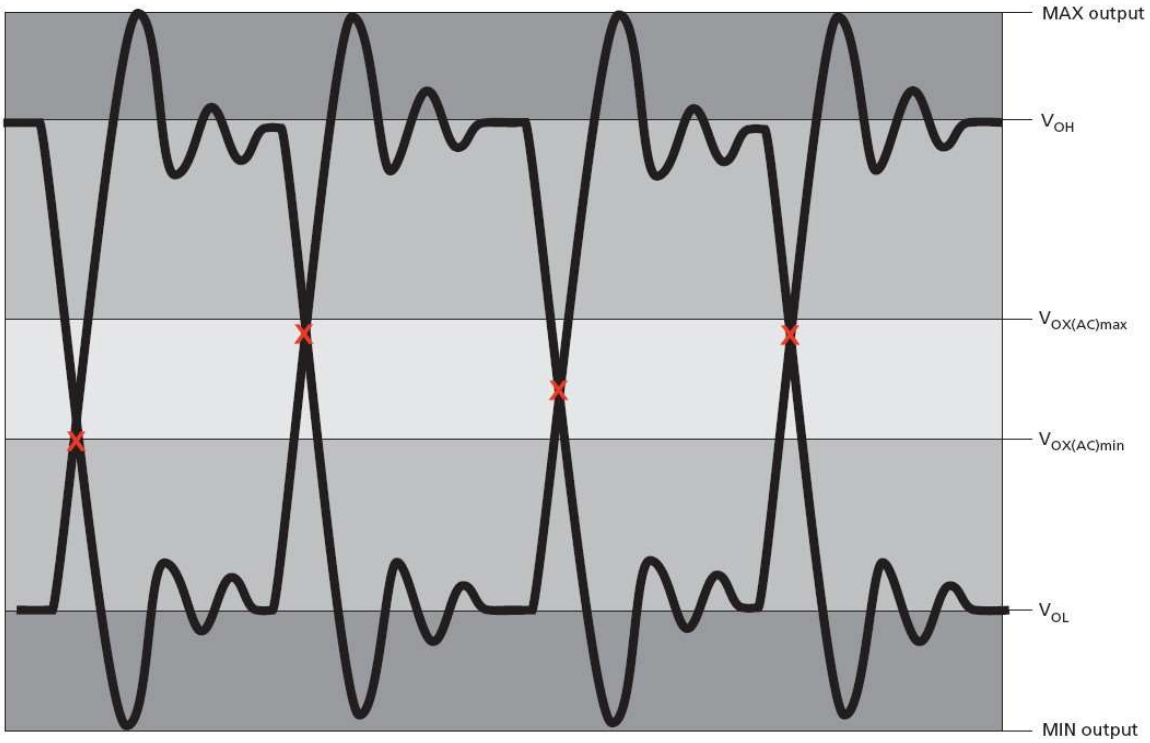


Figure 4-17: Differential Output Signal

Reference Output Load

Figure 4-18 represents the effective reference load of 25Ω used in defining the relevant device AC timing parameters (except ODT reference timing) as well as the output slew rate measurements. It is not intended to be a precise representation of a particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment.

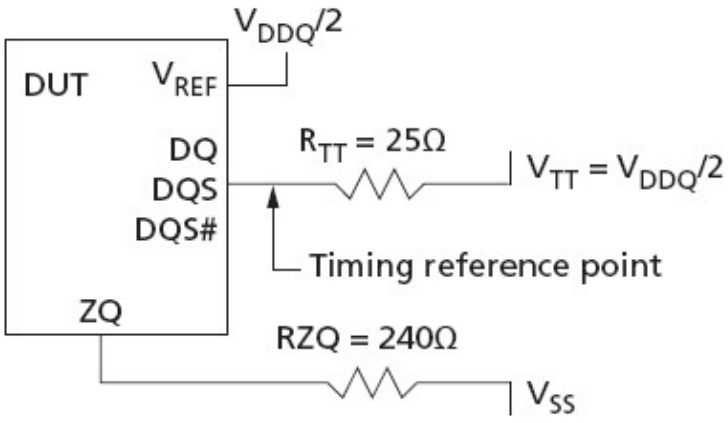


Figure 4-18: Reference Output Load for AC Timing and Output Slew Rate

Slew Rate Definitions for Single-Ended Output Signals

The single-ended output driver is summarized in Table 4-41. With the reference load for timing measurements, the output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single-ended signals.

Single-Ended Output Slew Rate Definition

Single-Ended Output Slew Rates (Linear Signals)		Measured		Calculation
Output	Edge	From	To	
DQ	Rising	$V_{OL(AC)}$	$V_{OH(AC)}$	$\frac{V_{OH(AC)} - V_{OL(AC)}}{\Delta TR_{se}}$
	Falling	$V_{OH(AC)}$	$V_{OL(AC)}$	$\frac{V_{OH(AC)} - V_{OL(AC)}}{\Delta TF_{se}}$

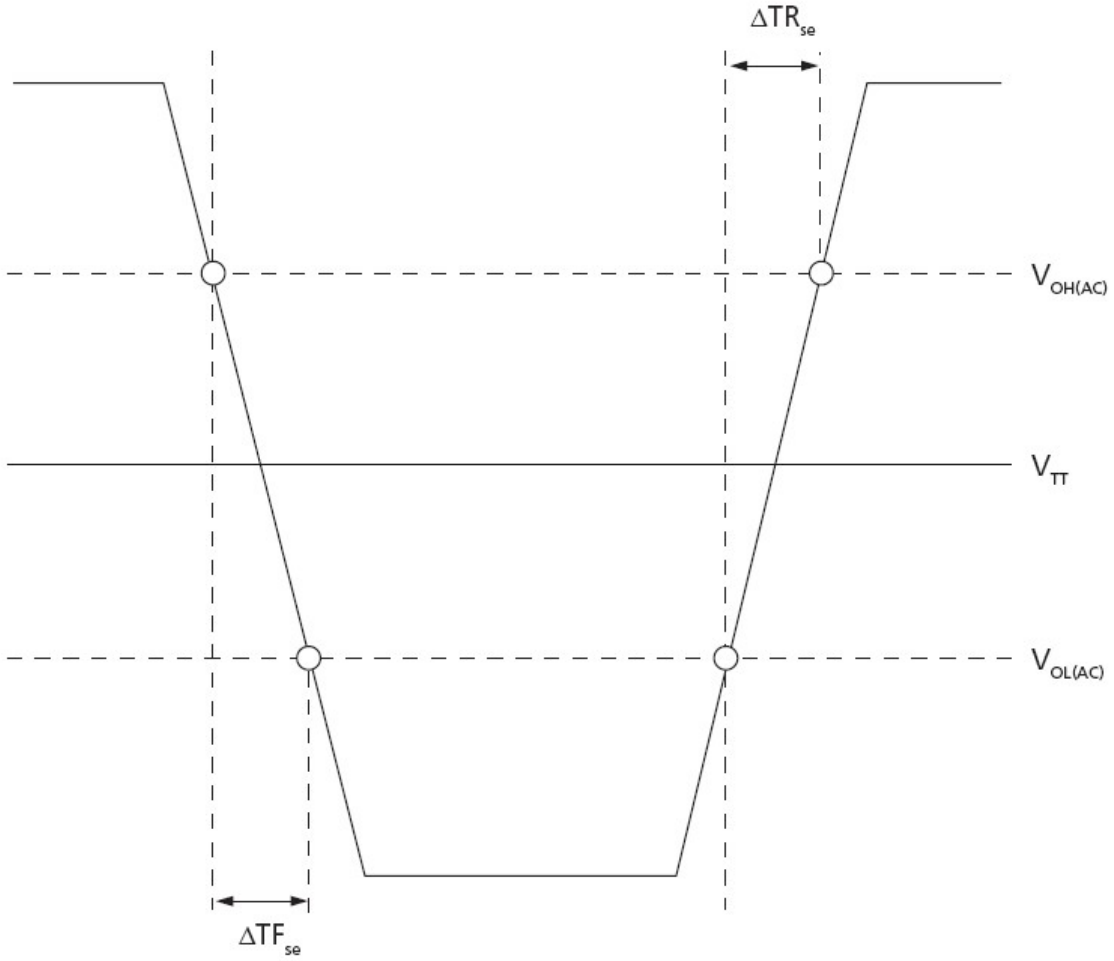


Figure 4-19: Nominal Slew Rate Definition for Single-Ended Output Signals

Slew Rate Definitions for Differential Output Signals

The differential output driver is summarized in Table 4-42. With the reference load for timing measurements, the output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for differential signals.

Table 4-45: Differential Output Slew Rate Definition

Differential Output Slew Rates (Linear Signals)		Measured		Calculation
Output	Edge	From	To	
DQS, DQS#	Rising	$V_{OL,diff(AC)}$	$V_{OH,diff(AC)}$	$\frac{V_{OH,diff(AC)} - V_{OL,diff(AC)}}{\Delta TR_{diff}}$
	Falling	$V_{OH,diff(AC)}$	$V_{OL,diff(AC)}$	$\frac{V_{OH,diff(AC)} - V_{OL,diff(AC)}}{\Delta TF_{diff}}$

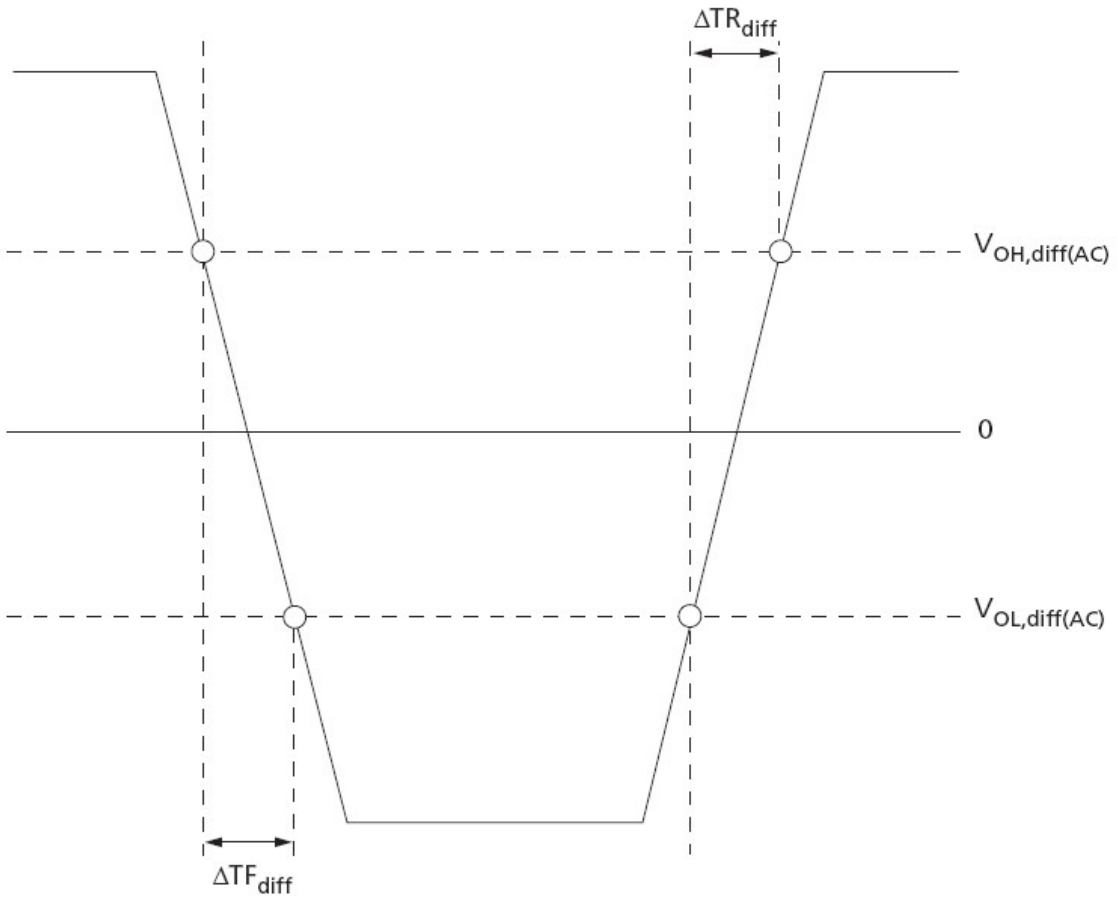


Figure 4-20: Nominal Differential Output Slew Rate Definition for DQS, DQS#

Speed Bin Table

Table 4-46-a: DDR3(L)-1066 Speed Bin

DDR3(L)-1066 Speed Bin					Unit	Notes
CL-tRCD-tRP			7-7-7			
Parameter		Symbol	Min	Max		
Internal READ command to first data		tAA	13.125	-	ns	
ACTIVATE to internal READ or WRITE delay time		tRCD	13.125	-	ns	
PRECHARGE command period		tRP	13.125	-	ns	
ACTIVATE-to-ACTIVATE or REFRESH command period		tRC	50.625	-	ns	
ACTIVATE-to-PRECHARGE command		tRAS	37.5	9 x tREFI	ns	1
CL=5	CWL=5	tCK (AVG)	3.0	3.3	ns	2
	CWL=6	tCK (AVG)	Reserved		ns	3
CL=6	CWL=5	tCK (AVG)	2.5	3.3	ns	2
	CWL=6	tCK (AVG)	Reserved		ns	3
CL=7	CWL=5	tCK (AVG)	Reserved		ns	3
	CWL=6	tCK (AVG)	1.875	<2.5	ns	2,3
CL=8	CWL=5	tCK (AVG)	Reserved		ns	3
	CWL=6	tCK (AVG)	1.875	<2.5	ns	2
Supported CL settings			5,6,7,8		CK	
Supported CWL settings			5,6		CK	

Notes:

1. tREFI depends on T_{OPER}.

2. The CL and CWL settings result in tCK requirements. When making a selection of tCK, both CL and CWL requirement settings need to be fulfilled.

3. Reserved settings are not allowed.

Table 4-46-b: DDR3(L)-1333 Speed Bin

DDR3(L)-1333 Speed Bin					Unit	Notes
CL-tRCD-tRP			9-9-9			
Parameter		Symbol	Min	Max		
Internal READ command to first data		tAA	13.5	-	ns	
ACTIVATE to internal READ or WRITE delay time		tRCD	13.5	-	ns	
PRECHARGE command period		tRP	13. 5	-	ns	
ACTIVATE-to-ACTIVATE or REFRESH command		tRC	49.5	-	ns	
ACTIVATE-to-PRECHARGE command period		tRAS	36	9 x tREFI	ns	1
CL=5	CWL=5	tCK (AVG)	3.0	3.3	ns	2
	CWL=6.7	tCK (AVG)	Reserved		ns	3
CL=6	CWL=5	tCK (AVG)	2.5	3.3	ns	2
	CWL=6	tCK (AVG)	Reserved		ns	3
	CWL=7	tCK (AVG)	Reserved		ns	3
CL=7	CWL=5	tCK (AVG)	Reserved		ns	3
	CWL=6	tCK (AVG)	1.875	<2.5	ns	2,3
	CWL=7	tCK (AVG)	Reserved		ns	3
CL=8	CWL=5	tCK (AVG)	Reserved		ns	3
	CWL=6	tCK (AVG)	1.875	<2.5	ns	2
	CWL=7	tCK (AVG)	Reserved		ns	3
CL=9	CWL=5,6	tCK (AVG)	Reserved		ns	3
	CWL=7	tCK (AVG)	1.5	<1.875	ns	2,3
CL=10	CWL=5,6	tCK (AVG)	Reserved		ns	3
	CWL=7	tCK (AVG)	1.5	<1.875	ns	2
Supported CL settings			5,6,7,8,9,10		CK	
Supported CWL settings			5,6,7		CK	

Notes:

1. tREFI depends on T_{OPER}.

2. The CL and CWL settings result in tCK requirements. When making a selection of tCK, both CL and CWL requirement settings need to be fulfilled.

3. Reserved settings are not allowed.

Table 4-46-c: DDR3(L)-1600 Speed Bin

DDR3(L)-1600 Speed Bin					Unit	Notes
CL-tRCD-tRP			11-11-11			
Parameter		Symbol	Min	Max		
Internal READ command to first data		tAA	13.75	-	ns	
ACTIVATE to internal READ or WRITE delay time		tRCD	13.75	-	ns	
PRECHARGE command period		tRP	13.75	-	ns	
ACTIVATE-to-ACTIVATE or REFRESH command		tRC	48.75	-	ns	
ACTIVATE-to-PRECHARGE command period		tRAS	35	9 x tREFI	ns	1
CL=5	CWL=5	tCK (AVG)	3.0	3.3	ns	2
	CWL=6,7,8	tCK (AVG)	Reserved		ns	3
CL=6	CWL=5	tCK (AVG)	2.5	3.3	ns	2
	CWL=6	tCK (AVG)	Reserved		ns	3
	CWL=7,8	tCK (AVG)	Reserved		ns	3
CL=7	CWL=5	tCK (AVG)	Reserved		ns	3
	CWL=6	tCK (AVG)	1.875	<2.5	ns	2
	CWL=7	tCK (AVG)	Reserved		ns	3
	CWL=8	tCK (AVG)	Reserved		ns	3
CL=8	CWL=5	tCK (AVG)	Reserved		ns	3
	CWL=6	tCK (AVG)	1.875	<2.5	ns	2
	CWL=7	tCK (AVG)	Reserved		ns	3
	CWL=8	tCK (AVG)	Reserved		ns	3
CL=9	CWL=5,6	tCK (AVG)	Reserved		ns	3
	CWL=7	tCK (AVG)	1.5	<1.875	ns	2
	CWL=8	tCK (AVG)	Reserved		ns	3
CL=10	CWL=5,6	tCK (AVG)	Reserved		ns	3
	CWL=7	tCK (AVG)	1.5	<1.875	ns	2
	CWL=8	tCK (AVG)	Reserved		ns	3
CL=11	CWL=5,6,7	tCK (AVG)	Reserved		ns	3
	CWL=8	tCK (AVG)	1.25	<1.5	ns	2
Supported CL settings			5,6,7,8,9,10,11		CK	
Supported CWL settings			5,6,7,8		CK	

Notes:

1. tREFI depends on T_{OPER}.

2. The CL and CWL settings result in tCK requirements. When making a selection of tCK, both CL and CWL requirement settings need to be fulfilled.

3. Reserved settings are not allowed.

Electrical Characteristics and AC Operating Conditions

Table 4-47: Electrical Characteristics and AC Operating Conditions DDR3(L)

Notes 1–8 apply to the entire table

Parameter		Symbol	DDR3(L)-1066		DDR3(L)-1333		DDR3(L)-1600		Units	Notes
			Min	Max	Min	Max	Min	Max		
Clock Timing										
Clock period average: DLL disable mode	T_C ≤ 85℃	$_tCK$ (DLL_DIS)	8	7800	8	7800	8	7800	ns	9, 42
	T_C = >85℃ to 95℃		8	3900	8	3900	8	3900	ns	42
Clock period average: DLL enable mode		$_tCK(AVG)$	See Speed Bin Tables 4-46 for tCK range allowed						ns	10, 11
High pulse width average		$_tCH(AVG)$	0.47	0.53	0.47	0.53	0.47	0.53	CK	12
Low pulse width average		$_tCL(AVG)$	0.47	0.53	0.47	0.53	0.47	0.53	CK	12
Clock period jitter	DLL locked	$_tJITper$	–90	90	–80	80	–70	70	ps	13
	DLL locking	$_tJITper,lck$	–80	80	–70	70	–60	60	ps	13
Clock absolute period		$_tCK (ABS)$	MIN = $_tCK (AVG)$ MIN + $_tJITper$ MIN; MAX = $_tCK (AVG)$ MAX + $_tJITper$ MAX						ps	
Clock absolute high pulse width		$_tCH (ABS)$	0.43	–	0.43	–	0.43	–	$_tCK$ (AVG)	14
Clock absolute low pulse width		$_tCL (ABS)$	0.43	–	0.43	–	0.43	–	$_tCK$ (AVG)	15
Cycle-to-cycle jitter	DLL locked	$_tJITcc$	180		160		140		ps	16
	DLL locking	$_tJITcc,lck$	160		140		120		ps	16
Cumulative error across	2 cycles	$_tERR2per$	–132	132	–118	118	–103	103	ps	17
	3 cycles	$_tERR3per$	–157	157	–140	140	–122	122	ps	17
	4 cycles	$_tERR4per$	–175	175	–155	155	–136	136	ps	17
	5 cycles	$_tERR5per$	–188	188	–168	168	–147	147	ps	17
	6 cycles	$_tERR6per$	–200	200	–177	177	–155	155	ps	17
	7 cycles	$_tERR7per$	–209	209	–186	186	–163	163	ps	17
	8 cycles	$_tERR8per$	–217	217	–193	193	–169	169	ps	17
	9 cycles	$_tERR9per$	–224	224	–200	200	–175	175	ps	17
	10 cycles	$_tERR10per$	–231	231	–205	205	–180	180	ps	17
	11 cycles	$_tERR11per$	–237	237	–210	210	–184	184	ps	17
	12 cycles	$_tERR12per$	–242	242	–215	215	–188	188	ps	17
	n = 13, 14 . . . 49, 50 cycles	$_tERRnper$	$_tERRnper$ MIN = (1 + 0.68ln[*n*]) ×$_tJITper$ MIN $_tERRnper$ MAX = (1 + 0.68ln[*n*]) ×$_tJITper$ MAX						ps	17

Table 4-47: Electrical Characteristics and AC Operating Conditions (Continued)

Notes 1–8 apply to the entire table

Parameter		Symbol	DDR3(L)-1066		DDR3(L)-1333		DDR3(L)-1600		Units	Notes
			Min	Max	Min	Max	Min	Max		
DQ Input Timing										
Data setup time to DQS, DQS#	Base (specification)	tDS (AC160)	40	–	–	–	–	–	ps	18, 19, 44
	V_{REF} @ 1V/ns		200	–	–	–	–	–	ps	19, 20
Data setup time to DQS, DQS#	Base (specification)	tDS (AC135)	90	–	45	–	25	–	ps	18, 19, 44
	V_{REF} @ 1 V/ns		250	–	180	–	160	–	ps	19, 20
Data hold time from DQS, DQS#	Base (specification)	tDH (DC90)	110	–	75	–	55	–	ps	18, 19
	V_{REF} @ 1 V/ns		200	–	165	–	145	–	ps	19, 20
Minimum data pulse width		tDIPW	490	–	400	–	360	–	ps	41
DQ Output Timing										
DQS, DQS# to DQ skew, per access		tDQSQ	–	150	–	125	–	100	ps	
DQ output hold time from DQS, DQS#		tQH	0.38	–	0.38	–	0.38	–	tCK (AVG)	21
DQ Low-Z time from CK, CK#		tLZDQ	–600	300	–500	250	–450	225	ps	22, 23
DQ High-Z time from CK, CK#		tHZDQ	–	300	–	250	–	225	ps	22, 23
DQ Strobe Input Timing										
DQS, DQS# rising to CK, CK# rising		tDQSS	–0.25	0.25	–0.25	0.25	–0.27	0.27	CK	25
DQS, DQS# differential input low pulse width		tDQSL	0.45	0.55	0.45	0.55	0.45	0.55	CK	
DQS, DQS# differential input high pulse width		tDQSH	0.45	0.55	0.45	0.55	0.45	0.55	CK	
DQS, DQS# falling setup to CK, CK# rising		tDSS	0.2	–	0.2	–	0.18	–	CK	25
DQS, DQS# falling hold from CK, CK# rising		tDSH	0.2	–	0.2	–	0.18	–	CK	25
DQS, DQS# differential WRITE preamble		tWPRE	0.9	–	0.9	–	0.9	–	CK	
DQS, DQS# differential WRITE postamble		tWPST	0.3	–	0.3	–	0.3	–	CK	

Table 4-47: Electrical Characteristics and AC Operating Conditions (Continued)

Notes 1–8 apply to the entire table

Parameter		Symbol	DDR3(L)-1066		DDR3(L)-1333		DDR3(L)-1600		Units	Notes
			Min	Max	Min	Max	Min	Max		
DQ Strobe Output Timing										
DQS, DQS# rising to/from rising CK,		tDQSCK	–300	300	–255	255	–225	225	ps	23
DQS, DQS# rising to/from rising CK,CK# when DLL is disabled		tDQSCK (DLL_DIS)	1	10	1	10	1	10	ns	26
DQS, DQS# differential output high time		tQSH	0.38	–	0.40	–	0.40	–	CK	21
DQS, DQS# differential output low time		tQSL	0.38	–	0.40	–	0.40	–	CK	21
DQS, DQS# Low-Z time (RL - 1)		tLZDQS	–600	300	–500	250	–450	225	ps	22, 23
DQS, DQS# High-Z time (RL + BL/2)		tHZDQS	–	300	–	250	–	225	ps	22, 23
DQS, DQS# differential READ preamble		tRPRE	0.9	Note 24	0.9	Note 24	0.9	Note 24	CK	23, 24
DQS, DQS# differential READ postamble		tRPST	0.3	Note 27	0.3	Note 27	0.3	Note 27	CK	23, 27
Command and Address Timing										
DLL locking time		tDLLK	512	–	512	–	512	–	CK	28
CTRL, CMD, ADDR setup to CK,CK#	Base (specification)	tIS (AC160)	140	–	80	–	60	–	ps	29, 30, 44
	V_{REF} @ 1 V/ns		300	–	240	–	220	–	ps	20, 30
CTRL, CMD, ADDR setup to CK,CK#	Base(specification)	tIS (AC135)	290	–	205	–	185	–	ps	29, 30, 44
	V_{REF} @ 1 V/ns		425	–	340	–	320	–	ps	20, 30
CTRL, CMD, ADDR from CK,CK#	Base (specification)	tIH (DC90)	210	–	150	–	130	–	ps	29, 30
	V_{REF} @ 1 V/ns		300	–	240	–	220	–	ps	20, 30
Minimum CTRL, CMD, ADDR		tIPW	780	–	620	–	560	–	ps	41
ACTIVATE to internal READ or WRITE		tRCD	See Speed Bin Tables for tRCD						ns	31
PRECHARGE command period		tRP	See Speed Bin Tables for tRP						ns	31
ACTIVATE-to-PRECHARGE command		tRAS	See Speed Bin Tables for tRAS						ns	31, 32
ACTIVATE-to-ACTIVATE command eriod		tRC	See Speed Bin Tables for tRC						CK	31, 43
ACTIVATE-to-ACTIVATE minimum command	2KB page size	tRRD	MIN = greater of 4CK or 10ns		MIN = greater of 4CK or 7.5ns				CK	31
Four ACTIVATEwindows	2KB page size	tFAW	50	–	45	–	40	–	ns	31
Write recovery time		tWR	MIN = 15ns; MAX = n/a						ns	31, 32,
Delay from start of internal WRITE transaction to internal READ command		tWTR	MIN = greater of 4CK or 7.5ns; MAX = n/a						CK	31, 34

Table 4-47: Electrical Characteristics and AC Operating Conditions (Continued)

Notes 1–8 apply to the entire table

Parameter		Symbol	DDR3(L)-1066		DDR3(L)-1333		DDR3(L)-1600		Units	Notes
			Max	Max	Max	Max	Max	Max		
READ-to-PRECHARGE time		$_tRTP$	MIN = greater of 4CK or 7.5ns; MAX = n/a						CK	31, 32
CAS#-to-CAS# command delay		$_tCCD$	MIN = 4CK; MAX = n/a						CK	
Auto precharge write recovery + precharge time		$_tDAL$	MIN = WR + $_tRP$/$_tCK$ (AVG); MAX = n/a						CK	
MODE REGISTER SET command cycle time		$_tMRD$	MIN = 4CK; MAX = n/a						CK	
MODE REGISTER SET command update delay		$_tMOD$	MIN = greater of 12CK or 15ns; MAX = n/a						CK	
MULTIPURPOSE REGISTER READ burst end to mode register set for		$_tMPRR$	MIN = 1CK; MAX = n/a						CK	
Calibration Timing										
ZQCL command: Long calibration time	POWER-UP and RESET	$_tZQinit$	512	–	512	–	512	–	CK	
	Normal	$_tZQoper$	256	–	256	–	256	–	CK	
ZQCS command: Short calibration time		$_tZQCS$	64	–	64	–	64	–	CK	
Initialization and Reset Timing										
Exit reset from CKE HIGH to a valid command		$_tXPR$	MIN = greater of 5CK or $_tRFC$ + 10ns; MAX = n/a						CK	
Begin power supply ramp to power supplies stable		$_tVDDPR$	MIN = n/a; MAX = 200						ms	
RESET# LOW to power supplies stable		$_tRPS$	MIN = 0; MAX = 200						ms	
RESET# LOW to I/O and R_{TT} High-Z		$_tIOZ$	MIN = n/a; MAX = 20						ns	35
Refresh Timing										
REFRESH-to-ACTIVATE or REFRESH command period		$_tRFC$ – 1Gb	MIN = 110; MAX = 70,200						ns	
		$_tRFC$ – 2Gb	MIN = 160; MAX = 70,200						ns	
		$_tRFC$ – 4Gb	MIN = 260; MAX = 70,200						ns	
		$_tRFC$ – 8Gb	MIN = 350; MAX = 70,200						ns	
Maximum refresh period	TC ≤ 85℃	–	64 (1X)						ms	36
	TC > 85℃		32 (2X)						ms	36
Maximum average periodic refresh	TC ≤ 85℃	$_tREFI$	7.8 (64ms/8192)						µs	36
	TC > 85℃		3.9 (32ms/8192)						µs	36

Table 4-47: Electrical Characteristics and AC Operating Conditions (Continued)

Notes 1–8 apply to the entire table

Parameter	Symbol	DDR3(L)-1066		DDR3(L)-1333		DDR3(L)-1600		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Self Refresh Timing									
Exit self refresh to commands not requiring a locked DLL	tXS	MIN = greater of 5CK or tRFC + 10ns; MAX = n/a						CK	
Exit self refresh to commands requiring a locked DLL	tXSDLL	MIN = tDLLK (MIN); MAX = n/a						CK	28
Minimum CKE low pulse width for self re-fresh entry to self refresh exit timing	tCKESR	MIN = tCKE (MIN) + CK; MAX = n/a						CK	
Valid clocks after self refresh entry or power-down entry	tCKSRE	MIN = greater of 5CK or 10ns; MAX = n/a						CK	
Valid clocks before self refresh exit, power-down exit, or reset exit	tCKSRX	MIN = greater of 5CK or 10ns; MAX = n/a						CK	
Power-Down Timing									
CKE MIN pulse width	tCKE (MIN)	Greater of 3CK or 5.625ns		Greater of 3CK or 5.625ns		Greater of 3CK or 5ns		CK	
Command pass disable delay	tCPDED	MIN = 1; MAX = n/a						CK	
Power-down entry to power-down exit tim-ing	tPD	MIN = tCKE (MIN); MAX = 9 * tREFI						CK	
Begin power-down period prior to CKE registered HIGH	tANPD	WL - 1CK						CK	
Power-down entry period: ODT either synchronous or asynchronous	PDE	Greater of tANPD or tRFC - REFRESH command to CKE LOW time						CK	
Power-down exit period: ODT either synchronous or asynchronous	PDX	tANPD + tXPDLL						CK	
Power-Down Entry Minimum Timing									
ACTIVATE command to power-down entry	tACTPDEN	MIN = 1						CK	
PRECHARGE/PRECHARGE ALL command to power-down entry	tPRPDEN	MIN = 1						CK	
REFRESH command to power-down entry	tREFPDEN	MIN = 1						CK	37
MRS command to power-down entry	tMRSPDEN	MIN = tMOD (MIN)						CK	
READ/READ with auto precharge command to power-down entry	tRDPDEN	MIN = RL + 4 + 1						CK	

Table 4-47: Electrical Characteristics and AC Operating Conditions (Continued)

Notes 1–8 apply to the entire table

Parameter		Symbol	DDR3(L)-1066		DDR3(L)-1333		DDR3(L)-1600		Unit	Notes
			Min	Max	Min	Max	Min	Max		
WRITE command to power-down entry	BL8 (OTF, MRS)	$_tWRPDEN$	MIN = WL + 4 + $_tWR/_tCK$ (AVG)						CK	
	BC4MRS	$_tWRPDEN$	MIN = WL + 2 + $_tWR/_tCK$ (AVG)						CK	
WRITE with auto precharge command to power-down entry	BL8 (OTF, MRS)	$_tWRAPDEN$	MIN = WL + 4 + WR + 1						CK	
	BC4MRS	$_tWRAPDEN$	MIN = WL + 2 + WR + 1						CK	
Power-Down Exit Timing										
DLL on, any valid command, or DLL off to commands not requiring locked DLL		$_tXP$	MIN = greater of 3CK or 7.5ns;		MIN = greater of 3CK or 6ns; MAX = n/a				CK	
Precharge power-down with DLL off to commands requiring a locked DLL		$_tXPDLL$	MIN = greater of 10CK or 24ns; MAX = n/a						CK	28
ODT Timing										
R_{TT} synchronous turn-on delay		ODTLon	CWL + AL - 2CK						CK	38
R_{TT} synchronous turn-off delay		ODTLoff	CWL + AL - 2CK						CK	40
R_{TT} turn-on from ODTL on reference		$_tAON$	–300	300	–250	250	–225	225	ps	23, 38
R_{TT} turn-off from ODTL off reference		$_tAOF$	0.3	0.7	0.3	0.7	0.3	0.7	CK	39, 40
Asynchronous R_{TT} turn-on delay (power-down with DLL off)		$_tAONPD$	MIN = 2; MAX = 8.5						ns	38
Asynchronous R_{TT} turn-off delay (power-down with DLL off)		$_tAOFPD$	MIN = 2; MAX = 8.5						ns	40
ODT HIGH time with WRITE command		ODTH8	MIN = 6; MAX = n/a						CK	
ODT HIGH time without WRITE command or with WRITE command and		ODTH4	MIN = 4; MAX = n/a						CK	
Dynamic ODT Timing										
$R_{TT,nom}$-to-$R_{TT(WR)}$ change skew		ODTLcnw	WL - 2CK						CK	
$R_{TT(WR)}$-to-$R_{TT,nom}$ change skew - BC4		ODTLcwn4	4CK + ODTLoff						CK	
$R_{TT(WR)}$-to-$R_{TT,nom}$ change skew - BL8		ODTLcwn8	6CK + ODTLoff						CK	
RTT dynamic change skew		$_tADC$	0.3	0.7	0.3	0.7	0.3	0.7	CK	39
Write Leveling Timing										
First DQS, DQS# rising edge		$_tWLMRD$	40	–	40	–	40	–	CK	
DQS, DQS# delay		$_tWLDQSEN$	25	–	25	–	25	–	CK	
Write leveling setup from rising CK, CK# crossing to rising DQS, DQS# crossing		$_tWLS$	245	–	195	–	165	–	ps	

Table 4-47: Electrical Characteristics and AC Operating Conditions (Continued)

Notes 1–8 apply to the entire table

Parameter	Symbol	DDR3(L)-1066		DDR3(L)-1333		DDR3(L)-1600		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write leveling hold from rising DQS, DQS# crossing to rising CK, CK#	$_{t}$WLH	245	–	195	–	165	–	ps	
Write leveling output delay	$_{t}$WLO	0	9	0	9	0	7.5	ns	
Write leveling output error	$_{t}$WLOE	0	2	0	2	0	2	ns	

Notes:

1. AC timing parameters are valid from specified TC MIN to TC MAX values.
2. All voltages are referenced to V_{SS}.
3. Output timings are only valid for R_{ON34} output buffer selection.
4. The unit tCK (AVG) represents the actual tCK (AVG) of the input clock under operation. The unit CK represents one clock cycle of the input clock, counting the actual clock edges.
5. AC timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 900mV in the test environment, but input timing is still referenced to V_{REF} (except tIS, tIH, tDS, and tDH use the AC/DC trip points and CK, CK# and DQS, DQS# use their crossing points). The minimum slew rate for the input signals used to test the device is 1 V/ns for single-ended inputs and 2 V/ns for differential inputs in the range between V_{IL}(AC) and V_{IH}(AC).
6. All timings that use time-based values (ns, us, ms) should use tCK (AVG) to determine the correct number of clocks (Table4-47 uses CK or tCK [AVG] interchangeably). In the case of noninteger results, all minimum limits are to be rounded up to the nearest whole integer, and all maximum limits are to be rounded down to the nearest whole integer.
7. Strobe or DQS_{diff} refers to the DQS and DQS# differential crossing point when DQS is the rising edge. Clock or CK refers to the CK and CK# differential crossing point when CK is the rising edge.
8. This output load is used for all AC timing (except ODT reference timing) and slew rates. The actual test load may be different.The output signal voltage reference point is V_{DDQ}/2 for single-ended signals and the crossing point for differential signals (seeFigure 4-18).
9. When operating in DLL disable mode, CHIPSIP does not warrant compliance with normal mode timings or functionality.
10. The clock's tCK (AVG) is the average clock over any 200 consecutive clocks and tCK (AVG) MIN is the smallest clock rate allowed, with the exception of a deviation due to clock jitter. Input clock jitter is allowed provided it does not exceed values specified and must be of a random Gaussian distribution in nature.
11. Spread spectrum is not included in the jitter specification values. However, the input clock can accommodate spread-spectrum at a sweep rate in the range of 20–60 kHz with an additional 1% of tCK (AVG) as a long-term jitter component; however, the spread spectrum may not use a clock rate below tCK (AVG) MIN.
12. The clock's tCH (AVG) and tCL (AVG) are the average half clock period over any 200 consecutive clocks and is the smallest clock half period allowed, with the exception of a deviation due to clock jitter. Input clock jitter is allowed provided it does not exceed values specified and must be of a random Gaussian distribution in nature.
13. The period jitter ($_{t}$JITper) is the maximum deviation in the clock period from the average or nominal clock. It is allowed in either the positive or negative direction.
14. tCH (ABS) is the absolute instantaneous clock high pulse width as measured from one rising edge to the following falling edge.
15. $_{t}$CL (ABS) is the absolute instantaneous clock low pulse width as measured from one falling edge to the following rising edge.

16. The cycle-to-cycle jitter tJITcc is the amount the clock period can deviate from one cycle to the next. It is important to keep cycle-to-cycle jitter at a minimum during the DLL locking time.
17. The cumulative jitter error tERRnper, where n is the number of clocks between 2 and 50, is the amount of clock time allowed to accumulate consecutively away from the average clock over n number of clock cycles.
18. tDS (base) and tDH (base) values are for a single-ended 1 V/ns slew rate DQs and 2 V/ns slew rate differential DQS, DQS#;
    when DQ single-ended slew rate is 2V/ns, the DQS differential slew rate is 4V/ns.
19. These parameters are measured from a data signal (DM, DQ0, DQ1, and so forth) transition edge to its respective data strobe signal (DQS, DQS#) crossing.
20. The setup and hold times are listed converting the base specification values (to which derating tables apply) to V_{REF} when the slew rate is 1 V/ns. These values, with a slew rate of 1 V/ns, are for reference only.
21. When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJITper (larger of tJITper
    (MIN) or tJITper (MAX) of the input clock (output deratings are relative to the SDRAM input clock).
22. Single-ended signal parameter.
23. The DRAM output timing is aligned to the nominal or average clock. Most output parameters must be derated by the actual jitter error when input clock jitter is present, even when within specification. This results in each parameter becoming larger. The following parameters are required to be derated by subtracting tERR10per (MAX): tDQSCK (MIN), tLZDQS (MIN), tLZDQ (MIN), and tAON (MIN). The following parameters are required to be derated by subtracting tERR10per (MIN): tDQSCK (MAX), tHZ (MAX), tLZDQS (MAX), tLZDQ MAX, and tAON (MAX). The parameter tRPRE (MIN) is derated by subtracting tJITper (MAX), while tRPRE (MAX) is derated by subtracting tJITper (MIN).
24. The maximum preamble is bound by tLZDQS (MAX).
25. These parameters are measured from a data strobe signal (DQS, DQS#) crossing to its respective clock signal (CK, CK#) crossing. The specification values are not affected by the amount of clock jitter applied, as these are relative to the clock signal crossing. These parameters should be met whether clock jitter is present.
26. The tDQSCK (DLL_DIS) parameter begins CL + AL - 1 cycle after the READ command.
27. The maximum postamble is bound by tHZDQS (MAX).
28. Commands requiring a locked DLL are: READ (and RDAP) and synchronous ODT commands. In addition, after any change of latency tXPDLL, timing must be met.
29. tIS (base) and tIH (base) values are for a single-ended 1 V/ns control/command/address slew rate and 2 V/ns CK, CK#
    differential slew rate.
30. These parameters are measured from a command/address signal transition edge to its respective clock (CK, CK#) signal crossing. The specification values are not affected by the amount of clock jitter applied as the setup and hold times are relative to the clock signal crossing that latches the command/address. These parameters should be met whether clock jitter is present.
31. For these parameters, the DDR3(L) SDRAM device supports t*n*PARAM (*n*CK) = RU(tPARAM [ns]/tCK[AVG] [ns]), assuming all input clock jitter specifications are satisfied. For example, the device will support t*n*RP (*n*CK) = RU(tRP/tCK[AVG]) if all input clock jitter specifications are met.
32. During READs and WRITEs with auto precharge, the DDR3(L) SDRAM will hold off the internal PRECHARGE command until

tRAS (MIN) has been satisfied.

33. When operating in DLL disable mode, the greater of 4CK or 15ns is satisfied for tWR.
34. The start of the write recovery time is defined as follows:
    • For BL8 (fixed by MRS or OTF): Rising clock edge four clock cycles after WL
    • For BC4 (OTF): Rising clock edge four clock cycles after WL
    • For BC4 (fixed by MRS): Rising clock edge two clock cycles after WL
35. RESET# should be LOW as soon as power starts to ramp to ensure the outputs are in High-Z. Until RESET# is LOW, the outputs are at risk of driving and could result in excessive current, depending on bus activity.
36. The refresh period is 64ms when T_C is less than or equal to 85℃. This equates to an average refresh rate of 7.8125us.
    However, nine REFRESH commands should be asserted at least once every 70.3us. When T_C is greater than 85℃, the refresh period is 32ms.
37. Although CKE is allowed to be registered LOW after a REFRESH command when tREFPDEN (MIN) is satisfied, there are cases where additional time such as tXPDLL (MIN) is required.
38. ODT turn-on time MIN is when the device leaves High-Z and ODT resistance begins to turn on. ODT turn-on time maximum is when the ODT resistance is fully on. The ODT reference load is shown in Figure 4-11. This output load is used for ODT timings (see Figure 4-18). Designs that were created prior to JEDEC tightening the maximum limit from 9ns to 8.5ns will be allowed to have a 9ns maximum.
39. Half-clock output parameters must be derated by the actual tERR10per and tJITdty when input clock jitter is present. This results in each parameter becoming larger. The parameters tADC (MIN) and tAOF (MIN) are each required to be derated by subtracting both tERR10per (MAX) and tJITdty (MAX). The parameters tADC (MAX) and tAOF (MAX) are required to be derated by subtracting both tERR10per (MAX) and tJITdty (MAX).
40. ODT turn-off time minimum is when the device starts to turn off ODT resistance. ODT turn-off time maximum is when the DRAM buffer is in High-Z. The ODT reference load is shown in Figure 4-11. This output load is used for ODT timings (see Figure 4-18).
41. Pulse width of a input signal is defined as the width between the first crossing of $V_{REF(DC)}$ and the consecutive crossing of $V_{REF(DC)}$.
42. Should the clock rate be larger than tRFC (MIN), an AUTO REFRESH command should have at least one NOP command between it and another AUTO REFRESH command. Additionally, if the clock rate is slower than 40ns (25 MHz), all REFRESH commands should be followed by a PRECHARGE ALL command.
43. DRAM devices should be evenly addressed when being accessed. Disproportionate accesses to a particular row address may result in a reduction of REFRESH characteristics or product lifetime.
44. When two V1H(AC) values (and two corresponding V1L(AC) values) are listed for a specific speed bin the user may choose either value for the input AC level. Whichever value is used the associated setup time for that AC level must also be used. Additionally one V1H(AC) value may be used for address/command inputs and the other V1H(AC) value may be used for data inputs.

Command and Address Setup, Hold, and Derating

The total tIS (setup time) and tIH (hold time) required is calculated by adding the data sheet tIS (base) and tIH (base) values (see Table 4-48 and Table 4-52; values come from Table 4-47) to the ΔtIS and ΔtIH derating values (see Table 4-49, Table 4-50, Table 4-53 and Table 4-54), respectively. Example: tIS (total setup time) = tIS (base) + ΔtIS. For a valid transition, the input signal has to remain above/below $V_{IH(AC)}/V_{IL(AC)}$ for some time tVAC (see Table 4-51 and Table 4-55).

Although the total setup time for slow slew rates might be negative (for example, a valid input signal will not have reached $V_{IH(AC)}/V_{IL(AC)}$ at the time of the rising clock transition), a valid input signal is still required to complete the transition and to reach $V_{IH(AC)}/V_{IL(AC)}$ (see Figure 4-2 for input signal requirements). For slew rates that fall between the values listed in Table 4-49 and Table 4-53, the derating values may be obtained by linear interpolation.

Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IH(AC)min}$. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IL(AC)max}$. If the actual signal is always earlier than the nominal slew rate line between the shaded $V_{REF(DC)}$-to-AC region, use the nominal slew rate for derating value (see Figure 4-21). If the actual signal is later than the nominal slew rate line anywhere between the shaded $V_{REF(DC)}$-to-AC region, the slew rate of a tangent line to the actual signal from the AC level to the DC level is used for derating value (see Figure 4-23).

Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC)max}$ and the first crossing of $V_{REF(DC)}$. Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC)min}$ and the first crossing of $V_{REF(DC)}$. If the actual signal is always later than the nominal slew rate line between the shaded DC-to-$V_{REF(DC)}$ region, use the nominal slew rate for derating value (see Figure 4-22). If the actual signal is earlier than the nominal slew rate line anywhere between the shaded DC-to-$V_{REF(DC)}$ region, the slew rate of a tangent line to the actual signal from the DC level to the $V_{REF(DC)}$ level is used for derating value (see Figure 4-24).

Table 4-48: Command and Address Setup and Hold Values 1 V/ns Referenced – AC/DC-Based (DDR3L)

Symbol	DDR3L-1066	DDR3L-1333	DDR3L-1600	Unit	Reference
tIS(base, AC160)	140	80	60	ps	$V_{IH(AC)}/V_{IL(AC)}$
tIS(base, AC135)	290	205	185	ps	$V_{IH(AC)}/V_{IL(AC)}$
tIS(base, AC125)	–	–	–	ps	$V_{IH(AC)}/V_{IL(AC)}$
tIH(base, DC90)	210	150	130	ps	$V_{IH(DC)}/V_{IL(DC)}$

Table 4-49: Derating Values for tIS/tIH – AC160/DC90-Based (DDR3L)

ΔtIS, ΔtIH Derating (ps) – AC/DC-Based																
CMD/ ADDR	CK, CK# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
2.0	80	45	80	45	80	45	88	53	96	61	104	69	112	79	120	95
1.5	53	30	53	30	53	30	61	38	69	46	77	54	85	64	93	80
1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
0.9	–1	–3	–1	–3	–1	–3	7	5	15	13	23	21	31	31	39	47
0.8	–3	–8	–3	–8	–3	–8	5	1	13	9	21	17	29	27	37	43
0.7	–5	–13	–5	–13	–5	–13	3	–5	11	3	19	11	27	21	35	37
0.6	–8	–20	–8	–20	–8	–20	0	–12	8	–4	16	4	24	14	32	30
0.5	–20	–30	–20	–30	–20	–30	–12	–22	–4	–14	4	–6	12	4	20	20
0.4	–40	–45	–40	–45	–40	–45	–32	–37	–24	–29	–16	–21	–8	–11	0	5

Table 4-50: Derating Values for tIS/tIH – AC135/DC90-Based (DDR3L)

ΔtIS, ΔtIH Derating (ps) – AC/DC-Based																
CMD/ ADDR	CK, CK# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
2.0	68	45	68	45	68	45	76	53	84	61	92	69	100	79	108	95
1.5	45	30	45	30	45	30	53	38	61	46	69	54	77	64	85	80
1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
0.9	2	–3	2	–3	2	–3	10	5	18	13	26	21	34	31	42	47
0.8	3	–8	3	–8	3	–8	11	1	19	9	27	17	35	27	43	43
0.7	6	–13	6	–13	6	–13	14	–5	22	3	30	11	38	21	46	37
0.6	9	–20	9	–20	9	–20	17	–12	25	–4	33	4	41	14	49	30
0.5	5	–30	5	–30	5	–30	13	–22	21	–14	29	–6	37	4	45	20
0.4	–3	–45	–3	–45	–3	–45	6	–37	14	–29	22	–21	30	–11	38	5

Table 4-51: Minimum Required Time tVAC Above $V_{IH(AC)}$ (Below $V_{IL[AC]}$) for Valid ADD/CMD Transition (DDR3L)

Slew Rate (V/ns)	DDR3L-1066/1333/1600	
	tVAC at 160mV (ps)	tVAC at 135mV (ps)
>2.0	200	213
2.0	200	213
1.5	173	190
1.0	120	145
0.9	102	130
0.8	80	111
0.7	51	87
0.6	13	55
0.5	Note 1	10
<0.5	Note 1	10

Note:

1. Rising input signal shall become equal to or greater than $V_{IH(ac)}$ level and Falling input signal shall become equal to or less than

   $V_{IL(ac)}$ level.

Table 4-52: Command and Address Setup and Hold Values 1 V/ns Referenced – AC/DC-Based (DDR3)

Symbol	DDR3-1066	Unit	Reference
tIS(base, AC175)	125	ps	$V_{IH(AC)}/V_{IL(AC)}$
tIS(base, AC150)	275	ps	$V_{IH(AC)}/V_{IL(AC)}$
tIS(base, AC135)	–	ps	$V_{IH(AC)}/V_{IL(AC)}$
tIS(base, AC125)	–	ps	$V_{IH(AC)}/V_{IL(AC)}$
tIH(base, DC100)	200	ps	$V_{IH(DC)}/V_{IL(DC)}$

Table 4-53: Derating Values for tIS/tIH – AC175/DC100-Based (DDR3)

ΔtIS, ΔtIH Derating (ps) – AC/DC-Based AC175 Threshold: $V_{IH(AC)} = V_{REF(DC)} + 175mV$, $V_{IL(AC)} = V_{REF(DC)} - 175mV$																
CMD/ ADDR	CK, CK# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
Slew	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
2.0	88	50	88	50	88	50	96	58	104	66	112	74	120	84	128	100
1.5	59	34	59	34	59	34	67	42	75	50	83	58	91	68	99	84
1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
0.9	–2	–4	–2	–4	–2	–4	6	4	14	12	22	20	30	30	38	46
0.8	–6	–10	–6	–10	–6	–10	2	–2	10	6	18	14	26	24	34	40
0.7	–11	–16	–11	–16	–11	–16	–3	–8	5	0	13	8	21	18	29	34
0.6	–17	–26	–17	–26	–17	–26	–9	–18	–1	–10	7	–2	15	8	23	24
0.5	–35	–40	–35	–40	–35	–40	–27	–32	–19	–24	–11	–16	–2	–6	5	10
0.4	–62	–60	–62	–60	–62	–60	–54	–52	–46	–44	–38	–36	–30	–26	–22	–10

Table 4-54: Derating Values for tIS/tIH – AC150/DC100-Based (DDR3)

ΔtIS, ΔtIH Derating (ps) – AC/DC-Based AC150 Threshold: $V_{IH(AC)} = V_{REF(DC)} + 150mV$, $V_{IL(AC)} = V_{REF(DC)} - 150mV$																
CMD/ ADDR	CK, CK# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
Slew	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
2.0	75	50	75	50	75	50	83	58	91	66	99	74	107	84	115	100
1.5	50	34	50	34	50	34	58	42	66	50	74	58	82	68	90	84
1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
0.9	0	–4	0	–4	0	–4	8	4	16	12	24	20	32	30	40	46
0.8	0	–10	0	–10	0	–10	8	–2	16	6	24	14	32	24	40	40
0.7	0	–16	0	–16	0	–16	8	–8	16	0	24	8	32	18	40	34
0.6	–1	–26	–1	–26	–1	–26	7	–18	15	–10	23	–2	31	8	39	24
0.5	–10	–40	–10	–40	–10	–40	–2	–32	6	–24	14	–16	22	–6	30	10
0.4	–25	–60	–25	–60	–25	–60	–17	–52	–9	–44	–1	–36	7	–26	15	–10

Table 4-55: Minimum Required Time tVAC Above $V_{IH(AC)}$ or Below $V_{IL(AC)}$ for Valid Transition (DDR3)

Slew Rate (V/ns)	DDR3-1066	
	tVAC at 175mV (ps)	tVAC at 150mV (ps)
>2.0	75	175
2.0	57	170
1.5	50	167
1.0	38	163
0.9	34	162
0.8	29	161
0.7	22	159
0.6	13	155
0.5	0	150
<0.5	0	150

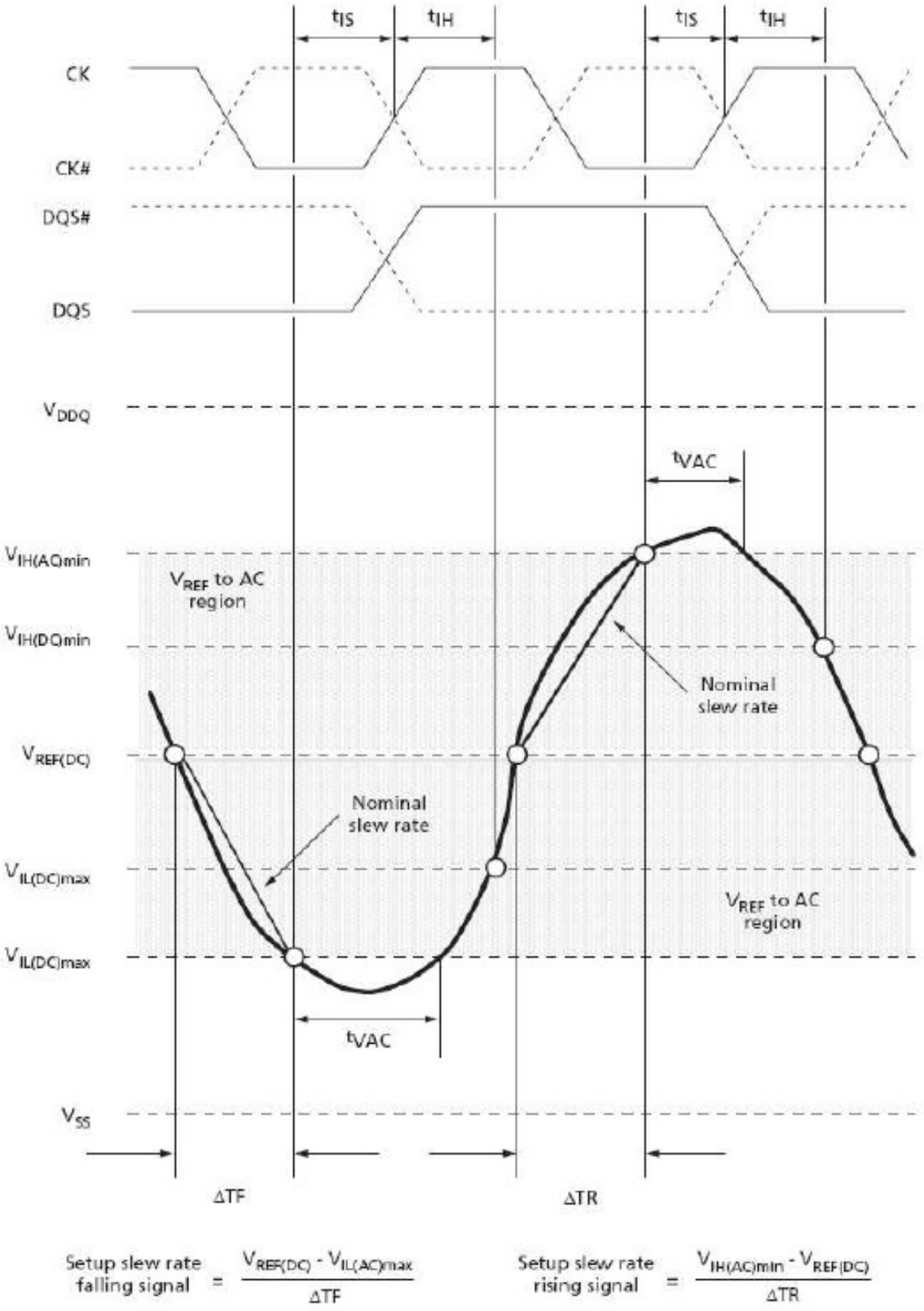


Figure 4-21: Nominal Slew Rate and tVAC for tIS (Command and Address – Clock)

NOTE:

1. The clock and the strobe are drawn on different time scales

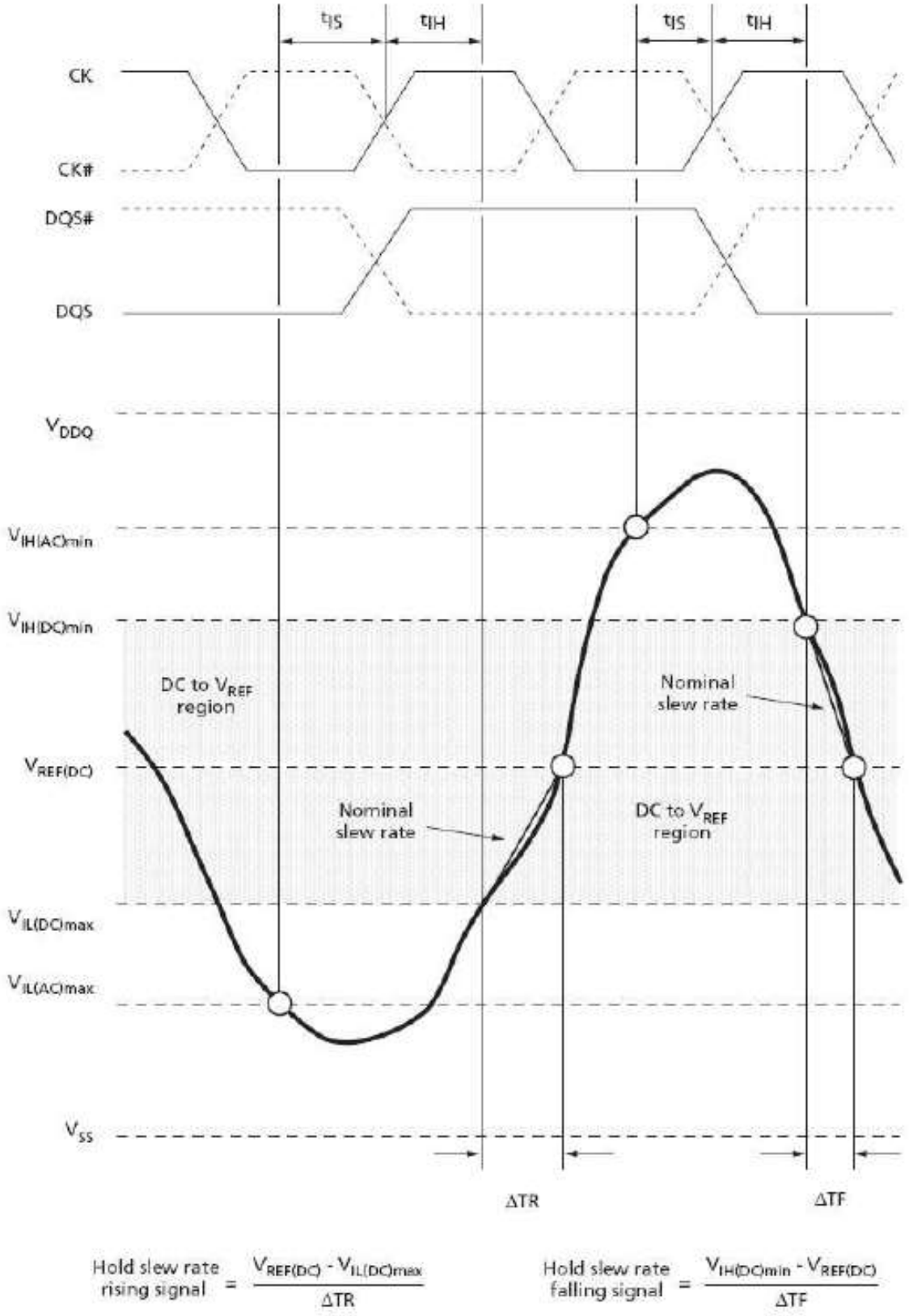
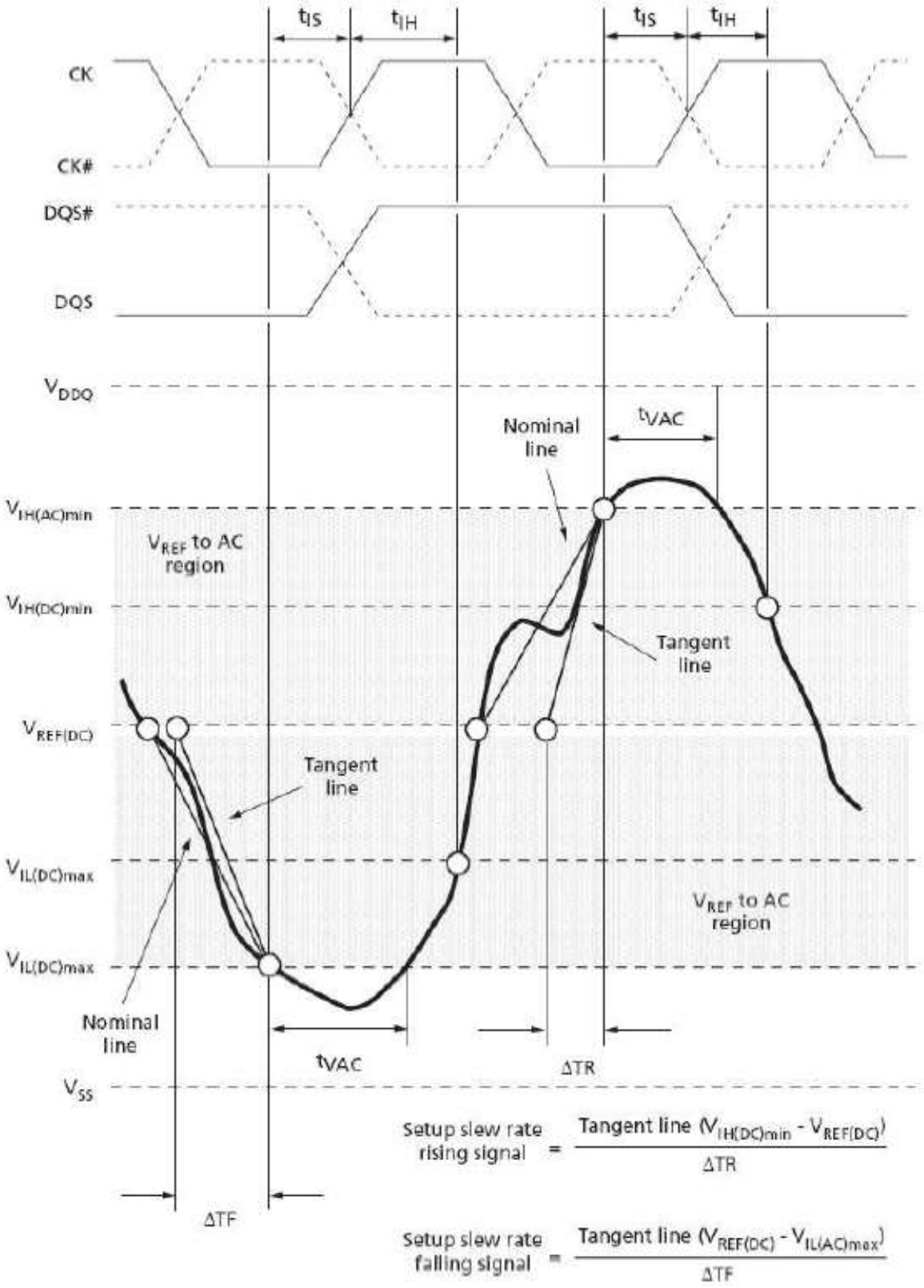


Figure 4-22: Nominal Slew Rate for tIH (Command and Address – Clock)

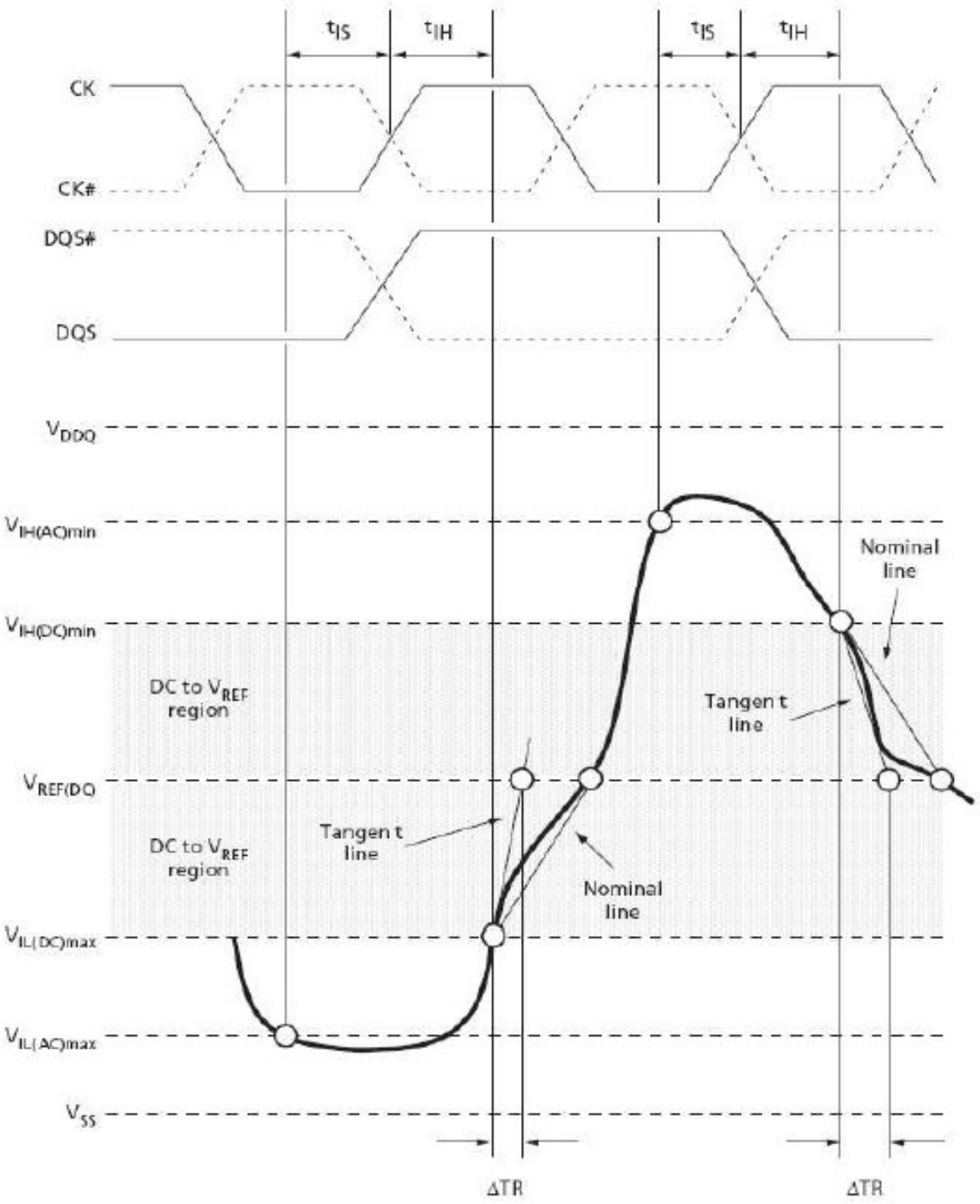
NOTE:

1. The clock and the strobe are drawn on different time scales



NOTE:

1. The clock and the strobe are drawn on different time scales.



$$\text{Hold slew rate rising signal} = \frac{\text{Tangent line } (V_{REF(DC)} - V_{IL(DC)max})}{\Delta TR}$$

$$\text{Hold slew rate falling signal} = \frac{\text{Tangent line } (V_{IH(DC)min} - V_{REF(DC)})}{\Delta TF}$$

NOTE:

1. The clock and the strobe are drawn on different time scales.

Data Setup, Hold, and Derating

The total tDS (setup time) and tDH (hold time) required is calculated by adding the data sheet tDS (base) and tDH (base) values (see Table 4-56; values come from Table 4-47) to the ΔtDS and ΔtDH derating values (see Table 4-57, Table 4-58 ,Table 4-61, Table 4-62) respectively. Example: tDS (total setup time) = tDS (base) + ΔtDS. For a valid transition, the input signal has to remain above/below $V_{IH(AC)}/V_{IL(AC)}$ for some time tVAC (see Table 4-59, Table 4-63).

Although the total setup time for slow slew rates might be negative (for example, a valid input signal will not have reached $V_{IH(AC)}/V_{IL(AC)}$) at the time of the rising clock transition), a valid input signal is still required to complete the transition and to reach $V_{IH}/V_{IL(AC)}$. For slew rates that fall between the values listed in Table 4-57, Table 4-58 ,Table 4-61, Table 4-62, the derating values may obtained by linear interpolation.

Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IH(AC)min}$. Setup (tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IL(AC)max}$. If the actual signal is always earlier than the nominal slew rate line between the shaded $V_{REF(DC)}$-to-AC region, use the nominal slew rate for derating value (see Figure 4-25). If the actual signal is later than the nominal slew rate line anywhere between the shaded $V_{REF(DC)}$-to-AC region, the slew rate of a tangent line to the actual signal from the AC level to the DC level is used for derating value (see Figure 4-27).

Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC)max}$ and the first crossing of $V_{REF(DC)}$. Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC)min}$ and the first crossing of $V_{REF(DC)}$. If the actual signal is always later than the nominal slew rate line between the shaded DC-to-$V_{REF(DC)}$ region, use the nominal slew rate for derating value (see Figure 4-26). If the actual signal is earlier than the nominal slew rate line anywhere between the shaded DC-to-$V_{REF(DC)}$ region, the slew rate of a tangent line to the actual signal from the DC-to-$V_{REF(DC)}$ region is used for derating value (see Figure 4-28).

Table 4-56: Data Setup and Hold Values at 1 V/ns (DQS, DQS# at 2 V/ns) – AC/DC-Based (DDR3L)

Symbol	DDR3L-1066	DDR3L-1333	DDR3L-1600	Unit	Reference
tDS (base) AC160	40	–	–	ps	$V_{IH(AC)}/V_{IL(AC)}$
tDS (base) AC135	90	45	45	ps	$V_{IH(AC)}/V_{IL(AC)}$
tDS (base) AC130	–	–	–	ps	$V_{IH(AC)}/V_{IL(AC)}$
tDH (base) DC90	110	75	55	ps	$V_{IH(DC)}/V_{IL(DC)}$
Slew Rate Referenced	1	1	1	V/ns	

Table 4-57: Derating Values for tDS/tDH – AC160/DC90-Based (DDR3L)

ΔtDS, ΔtDH Derating (ps) – AC/DC-Based																
DQ Slew	DQS, DQS# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
2.0	80	45	80	45	80	45										
1.5	53	30	53	30	53	30	61	38								
1.0	0	0	0	0	0	0	8	8	16	16						
0.9			–1	–3	–1	–3	7	5	15	13	23	21				
0.8					–3	–8	5	1	13	9	21	17	29	27		
0.7							–3	–5	11	3	19	11	27	21	35	37
0.6									8	–4	16	4	24	14	32	30
0.5											4	6	12	4	20	20
0.4													–8	–11	0	5

Table 4-58: Derating Values for tDS/tDH – AC135/DC90-Based (DDR3L)

ΔtDS, ΔtDH Derating (ps) – AC/DC-Based																
DQ Slew	DQS, DQS# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
2.0	68	45	68	45	68	45										
1.5	45	30	45	30	45	30	53	38								
1.0	0	0	0	0	0	0	8	8	16	16						
0.9			2	–3	2	–3	10	5	18	13	26	21				
0.8					3	–8	11	1	19	9	27	17	35	27		
0.7							14	–5	22	3	30	11	38	21	46	37
0.6									25	–4	33	4	41	14	49	30
0.5											39	–6	37	4	45	20
0.4													30	–11	38	5

Table 4-59: Minimum Required Time tVAC Above $V_{IH(AC)}$ (Below $V_{IL(AC)}$) for Valid DQ Transition (DDR3L)

Slew Rate (V/ns)	DDR3L-1066 160mV (ps)	DDR3L-1066/1333 135mV (ps)
	Min	Min
>2.0	165	113
2.0	165	113
1.5	138	90
1.0	85	45
0.9	67	30
0.8	45	11
0.7	16	Note 1
0.6	Note 1	Note 1
0.5	Note 1	Note 1
<0.5	Note 1	Note 1

Note:

1. Rising input signal shall become equal to or greater than $V_{IH(AC)}$ level and Falling input signal shall become equal to or less than $V_{IL(AC)}$ level.

Table 4-60: Data Setup and Hold Values at 1 V/ns (DQS, DQS# at 2 V/ns) – AC/DC-Based (DDR3)

Symbol	DDR3-1066	Unit	Reference
tDS (base) AC175	25	ps	$V_{IH(AC)}/V_{IL(AC)}$
tDS (base) AC150	75	ps	$V_{IH(AC)}/V_{IL(AC)}$
tDS (base) AC135	–	ps	$V_{IH(AC)}/V_{IL(AC)}$
tDH (base) DC100	100	ps	$V_{IH(DC)}/V_{IL(DC)}$

Table 4-61: Derating Values for tDS/tDH – AC175/DC100-Based (DDR3)

Shaded cells indicate slew rate combinations not supported

ΔtDS, ΔtDH Derating (ps) – AC/DC-Based																
DQ Slew Rate V/ns	DQS, DQS# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
2.0	88	50	88	50	88	50										
1.5	59	34	59	34	59	34	67	42								
1.0	0	0	0	0	0	0	8	8	16	16						
0.9			–2	–4	–2	–4	6	4	14	12	22	20				
0.8					–6	–10	2	–2	10	6	18	14	26	24		
0.7							–3	–8	5	0	13	8	21	18	29	34
0.6									–1	–10	7	–2	15	8	23	24
0.5											–11	–16	–2	–6	5	10
0.4													–30	–26	–22	–10

Table 4-62: Derating Values for tDS/tDH – AC150/DC100-Based (DDR3)

Shaded cells indicate slew rate combinations not supported

ΔtDS, ΔtDH Derating (ps) – AC/DC-Based																
DQ Slew Rate V/ns	DQS, DQS# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
2.0	75	50	75	50	75	50										
1.5	50	34	50	34	50	34	58	42								
1.0	0	0	0	0	0	0	8	8	16	16						
0.9			0	–4	0	–4	8	4	16	12	24	20				
0.8					0	–10	8	–2	16	6	24	14	32	24		
0.7							8	–8	16	0	24	8	32	18	40	34
0.6									15	–10	23	–2	31	8	39	24
0.5											14	–16	22	–6	30	10
0.4													7	–26	15	–10

Table 4-63: Required Minimum Time tVAC Above $V_{IH(AC)}$ (Below $V_{IL(AC)}$) for Valid DQ Transition (DDR3)

Slew Rate (V/ns)	tVAC at 175mV (ps)	tVAC at 150mV (ps)
	Min	Min
>2.0	75	175
2.0	57	170
1.5	50	167
1.0	38	163
0.9	34	162
0.8	29	161
0.7	22	159
0.6	13	155
0.5	0	150
<0.5	0	150

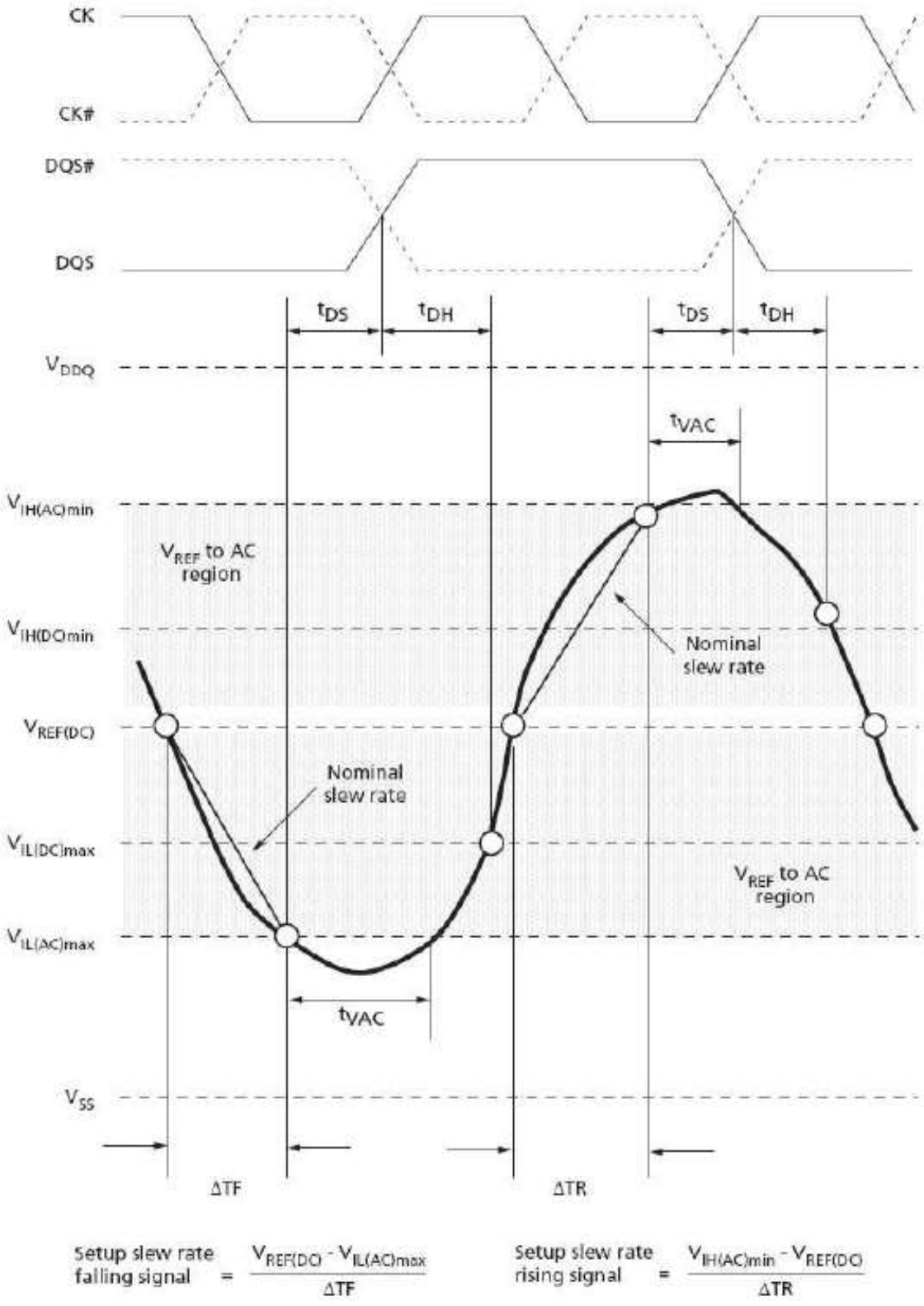


Figure 4-25: Nominal Slew Rate and tVAC for tDS (DQ – Strobe)

NOTE:

1. The clock and the strobe are drawn on different time scales.

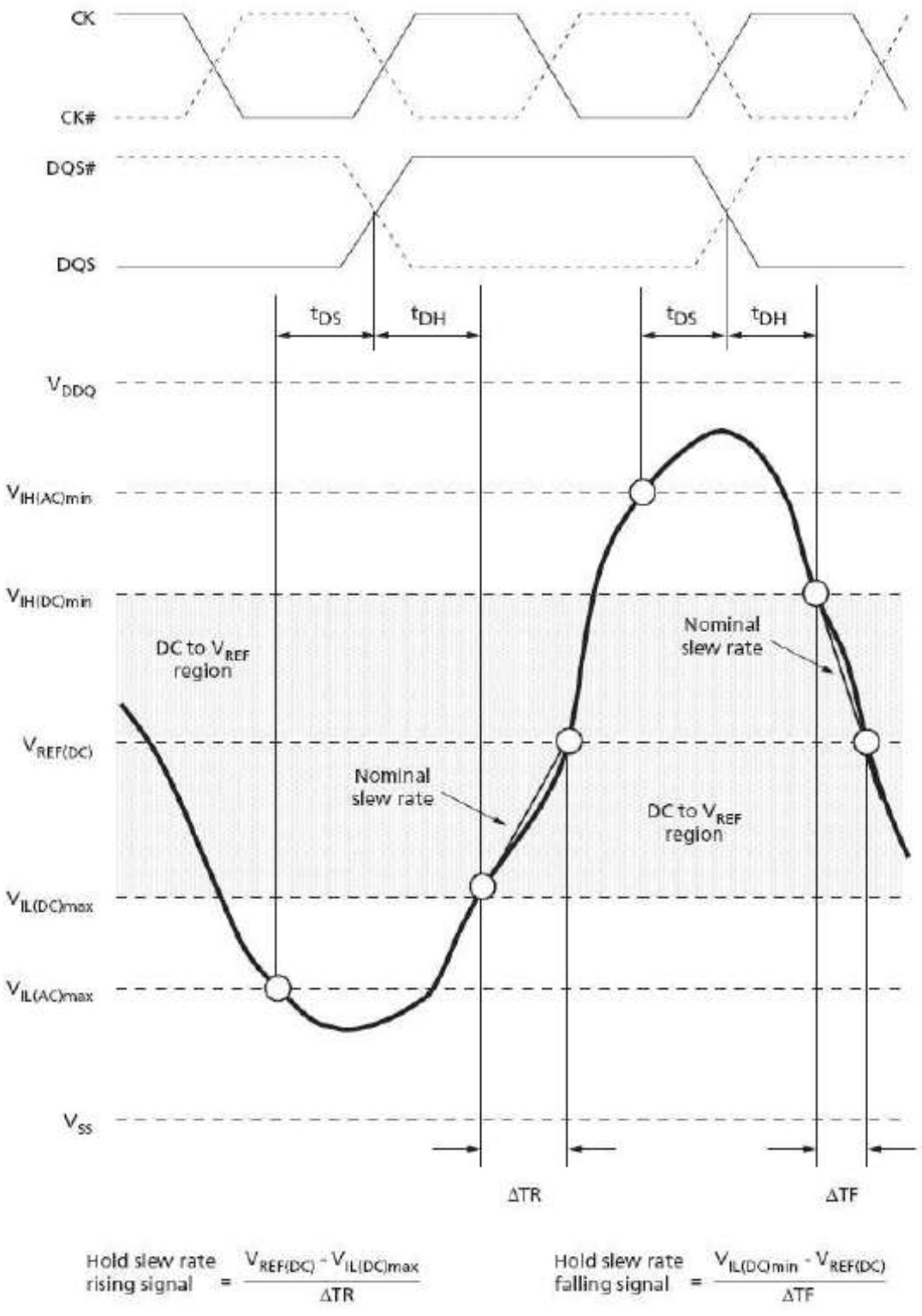


Figure 4-26: Nominal Slew Rate for tDH (DQ – Strobe)

NOTE:

1. The clock and the strobe are drawn on different time scales.

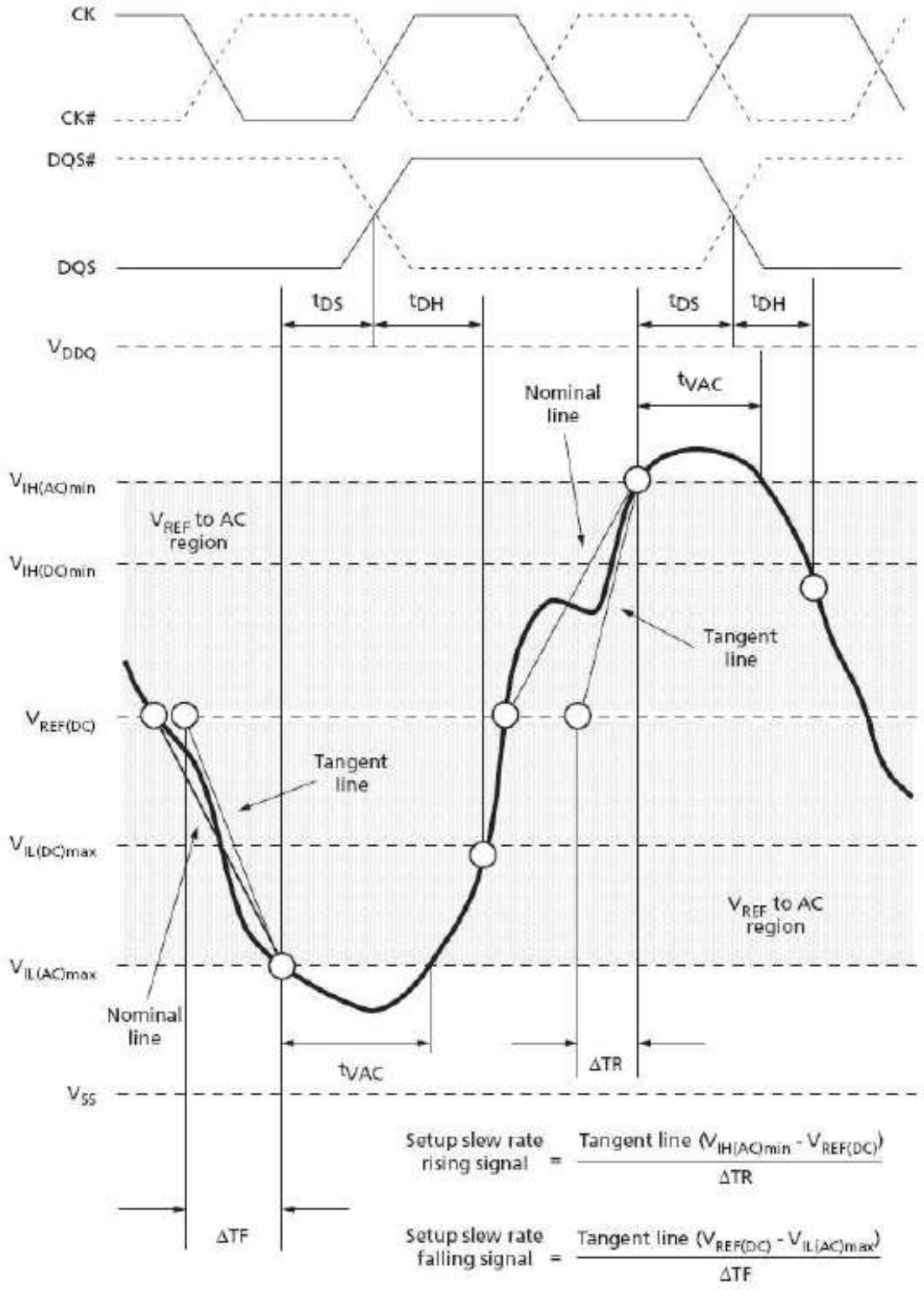


Figure 4-27: Tangent Line for tD5 (DQ – 5trobe)

NOTE:

1. The clock and the strobe are drawn on different time scales.

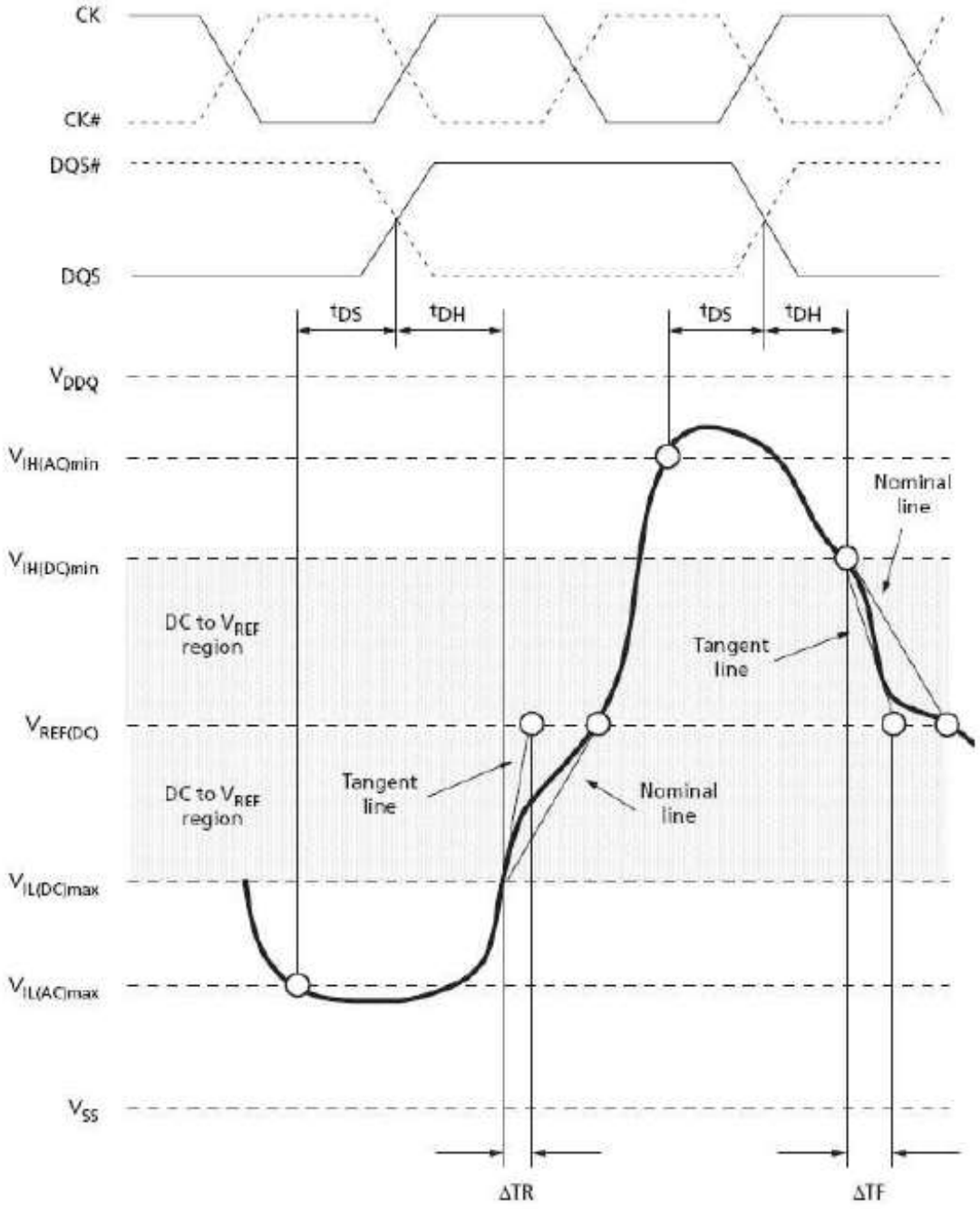


Figure 4-28: Tangent Line for tDH (DQ – 5trobe)

NOTE:

1. The clock and the strobe are drawn on different time scales

Commands – Truth Tables

Table 4-64: Truth Table – Command

Notes 1–5 apply to the entire table

Function		Symbol	CKE		CS#	RAS#	CAS#	WE#	BA [2:0]	An	A12	A10	A[11, 9:0]	Notes
			Prev.	Next										
MODE REGISTER SET		MRS	H	H	L	L	L	L	BA	OP code				
REFRESH		REF	H	H	L	L	L	H	V	V	V	V	V	
Self refresh entry		SRE	H	L	L	L	L	H	V	V	V	V	V	6
Self refresh exit		SRX	L	H	H	V	V	V	V	V	V	V	V	6,7
					L	H	H	H						
Single-bank PRECHARGE		PRE	H	H	L	L	H	L	BA	V	V	L	V	
PRECHARGE all banks		PREA	H	H	L	L	H	L	V		V	H	V	
Bank ACTIVATE		ACT	H	H	L	L	H	H	BA	Row address (RA)				
WRITE	BL8MRS,	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	8
	BC4OTF	WRS4	H	H	L	H	L	L	BA	RFU	L	L	CA	8
	BL8OTF	WRS8	H	H	L	H	L	L	BA	RFU	H	L	CA	8
WRITE with auto	BL8MRS,	WRAP	H	H	L	H	L	L	BA	RFU	V	H	CA	8
	BC4OTF	WRAPS4	H	H	L	H	L	L	BA	RFU	L	H	CA	8
	BL8OTF	WRAPS8	H	H	L	H	L	L	BA	RFU	H	H	CA	8
READ	BL8MRS,	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	8
	BC4OTF	RDS4	H	H	L	H	L	H	BA	RFU	L	L	CA	8
	BL8OTF	RDS8	H	H	L	H	L	H	BA	RFU	H	L	CA	8
READ with auto	BL8MRS,	RDAP	H	H	L	H	L	H	BA	RFU	V	H	CA	8
	BC4OTF	RDAPS4	H	H	L	H	L	H	BA	RFU	L	H	CA	8
	BL8OTF	RDAPS8	H	H	L	H	L	H	BA	RFU	H	H	CA	8
NO OPERATION		NOP	H	H	L	H	H	H	V	V	V	V	V	9
Device DESELECTED		DES	H	H	H	X	X	X	X	X	X	X	X	10
Power-down entry		PDE	H	L	L	H	H	H	V	V	V	V	V	6
					H	V	V	V						
Power-down exit		PDX	L	H	L	H	H	H	V	V	V	V	V	6,11
					H	V	V	V						
ZQ CALIBRATION LONG		ZQCL	H	H	L	H	H	L	X	X	X	H	X	12
ZQ CALIBRATION		ZQCS	H	H	L	H	H	L	X	X	X	L	X	

Notes:

1. Commands are defined by the states of CS#, RAS#, CAS#, WE#, and CKE at the rising edge of the clock. The MSB of BA, RA, and CA are device-, density-, and configuration-dependent.
2. RESET# is enabled LOW and used only for asynchronous reset. Thus, RESET# must be held HIGH during any normal operation.
3. The state of ODT does not affect the states described in this table.
4. Operations apply to the bank defined by the bank address. For MRS, BA selects one of four mode registers.
5. “V” means “H” or “L” (a defined logic level), and “X” means “Don’t Care”
6. See Table 4-65 for additional information on CKE transition.
7. Self refresh exit is asynchronous.

8. Burst READs or WRITEs cannot be terminated or interrupted. MRS (fixed) and OTF BL/BC are defined in MR0.
9. The purpose of the NOP command is to prevent the DRAM from registering any unwanted commands. A NOP will not terminate an operation that is executing.
10. The DES and NOP commands perform similarly.
11. The power-down mode does not perform any REFRESH operations.
12. ZQ CALIBRATION LONG is used for either ZQinit (first ZQCL command during initialization) or ZQoper (ZQCL command after initialization).

Table 4-65: Truth Table – CKE

Notes 1–2 apply to the entire table; see Table 4-64 for additional command details

Current State[3]	CKE		Command[5] (RAS#, CAS#, WE#, CS#)	Action[5]	Notes
	Previous Cycle[4] (*n* - 1)	Present Cycle[4] (*n*)			
Power-down	L	L	"Don't Care"	Maintain power-down	
	L	H	DES or NOP	Power-down exit	
Self refresh	L	L	"Don't Care"	Maintain self refresh	
	L	H	DES or NOP	Self refresh exit	
Bank(s) active	H	L	DES or NOP	Active power-down entry	
Reading	H	L	DES or NOP	Power-down entry	
Writing	H	L	DES or NOP	Power-down entry	
Precharging	H	L	DES or NOP	Power-down entry	
Refreshing	H	L	DES or NOP	Precharge power-down entry	
All banks idle	H	L	DES or NOP	Precharge power-down entry	6
	H	L	REFRESH	Self refresh	

Notes:

1. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.

2. tCKE (MIN) means CKE must be registered at multiple consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the required number of registration clocks. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of tIS + tCKE (MIN) + tIH.

3. Current state = The state of the DRAM immediately prior to clock edge n.

4. CKE (*n*) is the logic state of CKE at clock edge n; CKE (*n* - 1) was the state of CKE at the previous clock edge.

5. COMMAND is the command registered at the clock edge (must be a legal command as defined in Table 4-64. Action is a result of COMMAND. ODT does not affect the states described in this table and is not listed.

6. Idle state = All banks are closed, no data bursts are in progress, CKE is HIGH, and all timings from previous operations are satisfied. All self refresh exit and power-down exit parameters are also satisfied.

Commands Deselect

The DESELT (DES) command (CS# HIGH) prevents new commands from being executed by the DRAM. Operations already in progress are not affected.

NO OPERATION

The NO OPERATION (NOP) command (CS# LOW) prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

ZQ CALIBRATION LONG

The ZQ CALIBRATION LONG (ZQCL) command is used to perform the initial calibration during a power-up initialization and reset sequence (see Figure 4-37). This command may be issued at any time by the controller, depending on the system environment. The ZQCL command triggers the calibration engine inside the DRAM. After calibration is achieved, the calibrated values are transferred from the calibration engine to the DRAM I/O, which are reflected as updated R_{ON} and ODT values.

The DRAM is allowed a timing window defined by either tZQinit or tZQoper to perform a full calibration and transfer of values. When ZQCL is issued during the initialization sequence, the timing parameter tZQinit must be satisfied. When initialization is complete, subsequent ZQCL commands require the timing parameter tZQoper to be satisfied.

ZQ CALIBRATION SHORT

The ZQ CALIBRATION SHORT (ZQCS) command is used to perform periodic calibrations to account for small voltage and temperature variations. A shorter timing window is provided to perform the reduced calibration and transfer of values as defined by timing parameter tZQCS. A ZQCS command can effectively correct a minimum of 0.5% R_{ON} and R_{TT} impedance error within 64 clock cycles, assuming the maximum sensitivities specified in Table4-36 and Table4-37.

ACTIVATE

The ACTIVATE command is used to open (or activate) a row in a particular bank for a subsequent access.

The value on the BA[2:0] inputs selects the bank, and the address provided on inputs A[*n*:0] selects the row. This row remains open (or active) for accesses until a PRECHARGE command is issued to that bank.

A PRECHARGE command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The address provided on inputs A[2:0] selects the starting column address, depending on the burst length and burst type selected (see Burst Order table for additional information). The value on input A10 determines whether auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the READ burst. If auto precharge is not selected, the row will remain open for subsequent accesses. The value on input A12 (if enabled in the mode register) when the READ command is issued determines whether BC4 (chop) or BL8 is used. After a READ command is issued, the READ burst may not be interrupted.

Table 4-66: READ Command Summary

Function		Symbol	CKE		CS#	RAS#	CAS#	WE#	BA [2:0]	An	A12	A10	A[11, 9:0]
			Prev. Cycle	Next Cycle									
READ	BL8MRS, BC4MRS	RD	H		L	H	L	H	BA	RFU	V	L	CA
	BC4OTF	RDS4	H		L	H	L	H	BA	RFU	L	L	CA
	BL8OTF	RDS8	H		L	H	L	H	BA	RFU	H	L	CA
READ with auto precharge	BL8MRS, BC4MRS	RDAP	H		L	H	L	H	BA	RFU	V	H	CA
	BC4OTF	RDAPS4	H		L	H	L	H	BA	RFU	L	H	CA
	BL8OTF	RDAPS8	H		L	H	L	H	BA	RFU	H	H	CA

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA[2:0] inputs selects the bank. The value on input A10 determines whether auto precharge is used. The value on input A12 (if enabled in the MR) when the WRITE command is issued determines whether BC4 (chop) or BL8 is used. Input data appearing on the DQ is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory. If the DM signal is registered HIGH, the corresponding data inputs will be ignored and a WRITE will not be executed to that byte/column location.

Table 4-67: WRITE Command Summary

Function		Symbol	CKE		CS#	RAS#	CAS#	WE#	BA [2:0]	An	A12	A10	A[11, 9:0]
			Prev. Cycle	Next Cycle									
WRITE	BL8MRS, BC4MRS	WR	H		L	H	L	L	BA	RFU	V	L	CA
	BC4OTF	WRS4	H		L	H	L	L	BA	RFU	L	L	CA
	BL8OTF	WRS8	H		L	H	L	L	BA	RFU	H	L	CA
WRITE with auto	BL8MRS, BC4MRS	WRAP	H		L	H	L	L	BA	RFU	V	H	CA
	BC4OTF	WRAPS4	H		L	H	L	L	BA	RFU	L	H	CA
	BL8OTF	WRAPS8	H		L	H	L	L	BA	RFU	H	H	CA

PRECHARGE

The PRECHARGE command is used to de-activate the open row in a particular bank or in all banks. The bank(s) are available for a subsequent row access a specified time (tRP) after the PRECHARGE command is issued, except in the case of concurrent auto precharge. A READ or WRITE command to a different bank is allowed during a concurrent auto precharge as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Input A10 determines whether one or all banks are precharged. In the case where only one bank is precharged, inputs BA[2:0] select the bank; otherwise, BA[2:0] are treated as “Don’t Care”.

After a bank is precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command is treated as a NOP if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. However, the precharge period is determined by the last PRECHARGE command issued to the bank.

REFRESH

The REFRESH command is used during normal operation of the DRAM and is analogous to CAS#-before-RAS# (CBR) refresh or auto refresh. This command is nonpersistent, so it must be issued each time a refresh is required. The addressing is generated by the internal refresh controller. This makes the address bits a “Don’t Care” during a REFRESH command. The DRAM requires REFRESH cycles at an average interval of 7.8us (maximum when $T_C \leq 85℃$ or 3.9us maximum when $T_C \leq 95℃$). The REFRESH period begins when the REFRESH command is registered and ends tRFC (MIN) later.

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight REFRESH commands can be posted to any given DRAM, meaning that the maximum absolute interval between any REFRESH command and the next REFRESH command is nine times the maximum average interval refresh rate. Self refresh may be entered with up to eight REFRESH commands being posted. After exiting self refresh (when entered with posted REFRESH commands), additional posting of REFRESH commands is allowed to the extent that the maximum number of cumulative posted REFRESH commands (both preand post-self refresh) does not exceed eight REFRESH commands.

At any given time, a maximum of 16 REFRESH commands can be issued within 2 x tREFI.

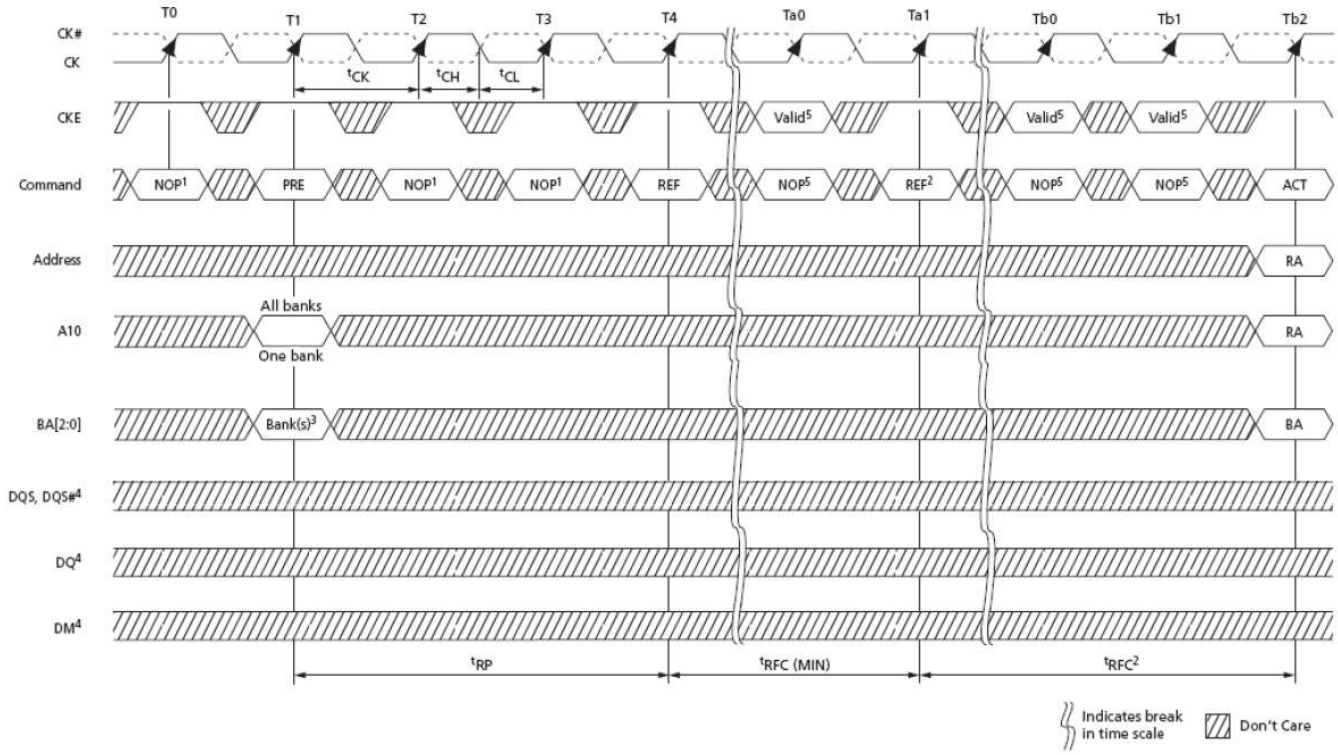


Figure 4-29: Refresh Mode

NOTES:

1. NOP commands are shown for ease of illustration; other valid commands may be possible at these times. CKE must be active during the PRECHARGE, ACTIVATE, and REFRESH commands, but may be inactive at other times (see section: Power-Down Mode).
2. The second REFRESH is not required, but two back-to-back REFRESH commands are shown.
3. "Don't Care" if A10 is HIGH at this point; however, A10 must be HIGH if more than one bank is active (must precharge all active banks).
4. For operations shown, DM, DQ, and DQS signals are all "Don't Care"/High-Z.
5. Only NOP and DES commands are allowed after a REFRESH command and until tRFC (MIN) is satisfied.

SELF REFRESH

The SELF REFRESH command is used to retain data in the DRAM, even if the rest of the system is powered down. When in self refresh mode, the DRAM retains data without external clocking. Self refresh mode is also a convenient method used to enable/disable the DLL as well as to change the clock frequency within the allowed synchronous operating range (see section: Input Clock Frequency Change). All power supply inputs (including V_{REFCA} and V_{REFDQ}) must be maintained at valid levels upon entry/exit and during self refresh mode operation. All power supply inputs (including V_{REFCA} and V_{REFDQ}) must be maintained at valid levels upon entry/exit and during self refresh mode operation. V_{REFDQ} may float or not drive $V_{DDQ}/2$ while in self refresh mode under the following conditions: • V_{SS} < V_{REFDQ} < V_{DD} is maintained

- V_{REFDQ} is valid and stable prior to CKE going back HIGH
- The first WRITE operation may not occur earlier than 512 clocks after V_{REFDQ} is valid
- All other self refresh mode exit timing requirements are met

DLL Disable Mode

If the DLL is disabled by the mode register (MR1[0] can be switched during initialization or later), the DRAM is targeted, but not guaranteed, to operate similarly to the normal mode, with a few notable exceptions:

- The DRAM supports only one value of CAS latency (CL = 6) and one value of CAS WRITE latency (CWL = 6).
- DLL disable mode affects the read data clock-to-data strobe relationship (tDQSCK), but not the read data-to-data strobe relationship (tDQSQ, tQH). Special attention is required to line up the read data with the controller time domain when the DLL is disabled.
- In normal operation (DLL on), tDQSCK starts from the rising clock edge AL + CL cycles after the READ command. In DLL disable mode, tDQSCK starts AL + CL - 1 cycles after the READ command. Additionally, with the DLL disabled, the value of tDQSCK could be larger than tCK.

The ODT feature (including dynamic ODT) is not supported during DLL disable mode. The ODT resistors must be disabled by continuously registering the ODT ball LOW by programming $R_{TT,nom}$ MR1[9, 6, 2] and $R_{TT(WR)}$ MR2[10, 9] to 0 while in the DLL disable mode.

Specific steps must be followed to switch between the DLL enable and DLL disable modes due to a gap in the allowed clock rates between the two modes (tCK [AVG] MAX and tCK [DLL_DIS] MIN, respectively). The only time the clock is allowed to cross this clock rate gap is during self refresh mode. Thus, the required procedure for switching from the DLL enable mode to the DLL disable mode is to change frequency during self refresh:

1. Starting from the idle state (all banks are precharged, all timings are fulfilled, ODT is turned off, and $R_{TT,nom}$ and $R_{TT(WR)}$ are High-Z), set MR1[0] to 1 to disable the DLL.
2. Enter self refresh mode after tMOD has been satisfied.
3. After tCKSRE is satisfied, change the frequency to the desired clock rate.
4. Self refresh may be exited when the clock is stable with the new frequency for tCKSRX. After tXS is satisfied, update the mode registers with appropriate values.
5. The DRAM will be ready for its next command in the DLL disable mode after the greater of tMRD or tMOD has been satisfied. A ZQCL command should be issued with appropriate timings met.

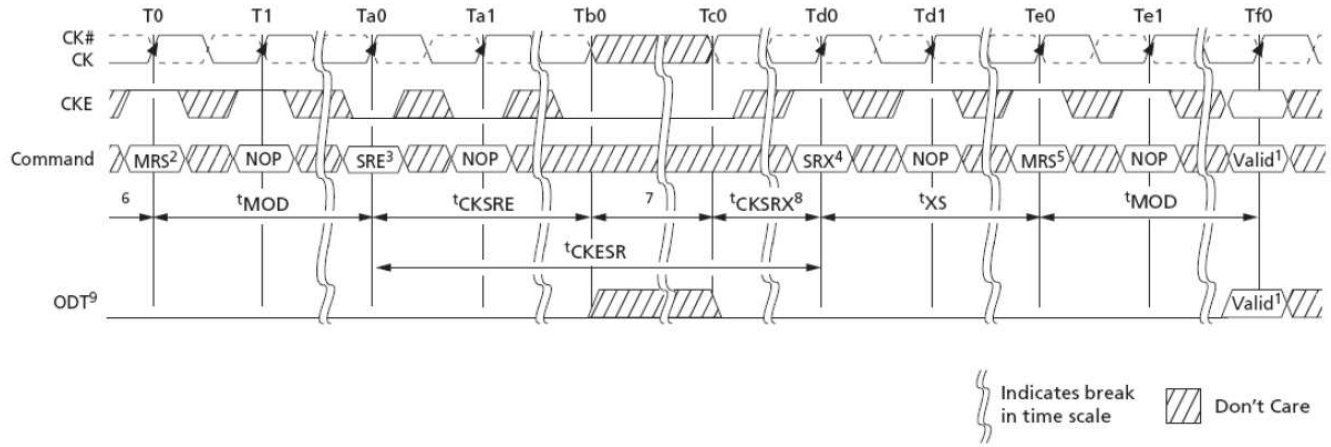


Figure 4-30: DLL Enable Mode to DLL Disable Mode

NOTES:

1. Any valid command.
2. Disable DLL by setting MR1[0] to 1.
3. Enter SELF REFRESH.
4. Exit SELF REFRESH.
5. Update the mode registers with the DLL disable parameters setting.
6. Starting with the idle state, R_{TT} is in the High-Z state.
7. Change frequency.
8. Clock must be stable tCKSRX.
9. Static LOW in the case that $R_{TT,nom}$ or $R_{TT(WR)}$ is enabled; otherwise, static LOW or HIGH.

A similar procedure is required for switching from the DLL disable mode back to the DLL enable mode. This also requires changing the frequency during self refresh mode (see Figure 4-31).

1. Starting from the idle state (all banks are precharged, all timings are fulfilled, ODT is turned off, and $R_{TT,nom}$ and $R_{TT(WR)}$ are High-Z), enter self refresh mode.
2. After tCKSRE is satisfied, change the frequency to the new clock rate.
3. Self refresh may be exited when the clock is stable with the new frequency for tCKSRX. After tXS is satisfied, update the mode registers with the appropriate values. At a minimum, set MR1[0] to 0 to enable the DLL. Wait tMRD, then set MR0[8] to 1 to enable DLL RESET.
4. After another tMRD delay is satisfied, update the remaining mode registers with the appropriate values.
5. The DRAM will be ready for its next command in the DLL enable mode after the greater of tMRD or tMOD has been satisfied. However, before applying any command or function requiring a locked DLL, a delay of tDLLK after DLL RESET must be satisfied. A ZQCL command should be issued with the appropriate timings met.

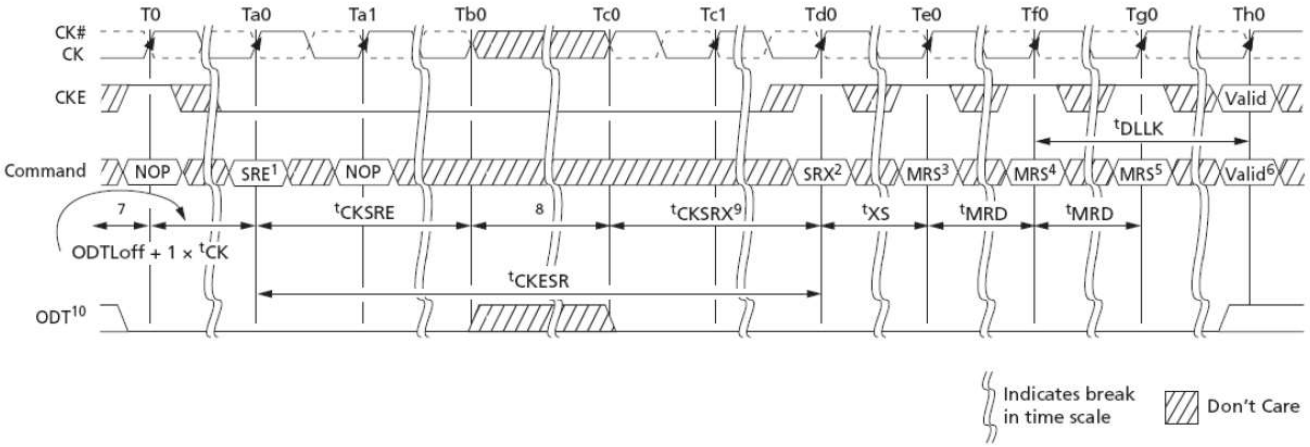


Figure 4-31: DLL Disable Mode to DLL Enable Mode

NOTES:

1. Enter SELF REFRESH.
2. Exit SELF REFRESH.
3. Wait tXS, then set MR1[0] to 0 to enable DLL.
4. Wait tMRD, then set MR0[8] to 1 to begin DLL RESET.
5. Wait tMRD, update registers (CL, CWL, and write recovery may be necessary).
6. Wait tMOD, any valid command.
7. Starting with the idle state.
8. Change frequency.
9. Clock must be stable at least tCKSRX.
10. Static LOW in the case that $R_{TT,nom}$ or $R_{TT(WR)}$ is enabled; otherwise, static LOW or HIGH.

The clock frequency range for the DLL disable mode is specified by the parameter tCK (DLL_DIS). Due to latency counter and timing restrictions, only CL = 6 and CWL = 6 are supported.

DLL disable mode will affect the read data clock to data strobe relationship (tDQSCK) but not the data strobe to data relationship (tDQSQ, tQH). Special attention is needed to line up read data to the controller time domain.

Compared to the DLL on mode where tDQSCK starts from the rising clock edge AL + CL cycles after the READ command, the DLL disable mode tDQSCK starts AL + CL - 1 cycles after the READ command.

WRITE operations function similarly between the DLL enable and DLL disable modes; however, ODT functionality is not allowed with DLL disable mode.

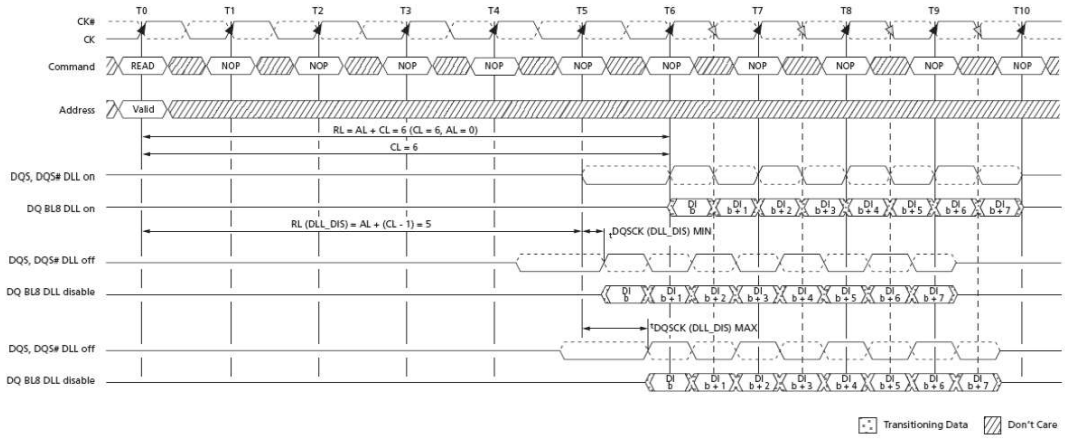


Figure 4-32: DLL Disable Tdqsck

Table 4-68: READ Electrical Characteristics, DLL Disable Mode

Parameter	Symbol	Min	Max	Unit
Access window of DQS from CK, CK#	tDQSCK (DLL_DIS)	1	10	ns

Input Clock Frequency Change

When the DDR3(L) SDRAM is initialized, the clock must be stable during most normal states of operation. This means that after the clock frequency has been set to the stable state, the clock period is not allowed to deviate, except for what is allowed by the clock jitter and spread spectrum clocking (SSC) specifications.

The input clock frequency can be changed from one stable clock rate to another under two conditions: self refresh mode and precharge power-down mode. It is illegal to change the clock frequency outside of those two modes. For the self refresh mode condition, when the DDR3(L) SDRAM has been successfully placed into self refresh mode and tCKSRE has been satisfied, the state of the clock becomes a “Don’t Care” When the clock becomes a “Don’t Care,” changing the clock frequency is permissible if the new clock frequency is stable prior to tCKSRX. When entering and exiting self refresh mode for the sole purpose of changing the clock frequency, the self refresh entry and exit specifications must still be met.

The precharge power-down mode condition is when the DDR3(L) SDRAM is in precharge power-down mode (either fast exit mode or slow exit mode). Either ODT must be at a logic LOW or $R_{TT,nom}$ and $R_{TT(WR)}$ must be disabled via MR1 and MR2. This ensures $R_{TT,nom}$ and $R_{TT(WR)}$ are in an off state prior to entering precharge power-down mode, and CKE must be at a logic LOW. A minimum of tCKSRE must occur after CKE goes LOW before the clock frequency can change. The DDR3(L) SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade (tCK [AVG] MIN to tCK [AVG] MAX). During the input clock frequency change, CKE must be held at a stable LOW level. When the input clock frequency is changed, a stable clock must be provided to the DRAM tCKSRX before precharge power-down may be exited. After precharge power-down is exited and tXP has been satisfied, the DLL must be reset via the MRS. Depending on the new clock frequency, additional MRS commands may need to be issued. During the DLL lock time, $R_{TT,nom}$ and $R_{TT(WR)}$ must remain in an off state. After the DLL lock time, the DRAM is ready to operate with a new clock frequency.

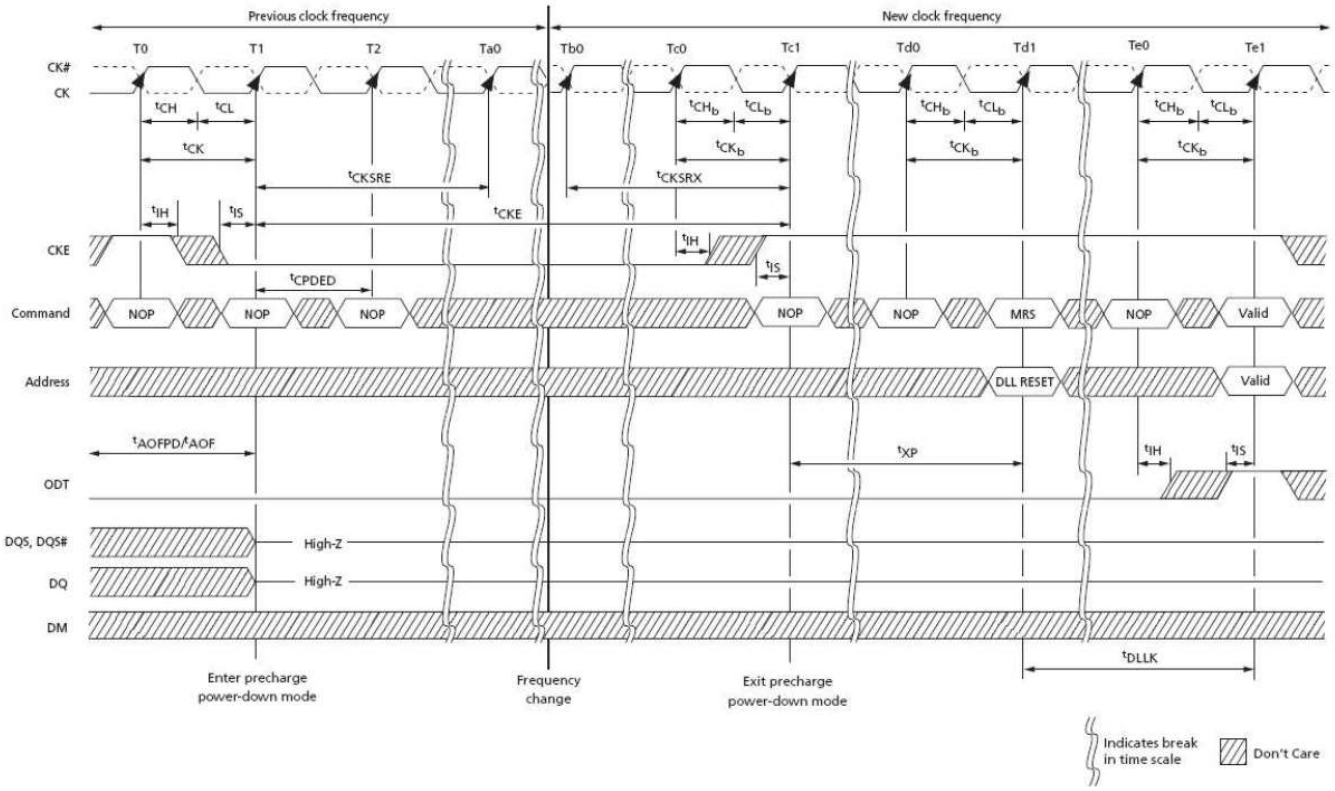


Figure 4-33: Change Frequency During Precharge Power-Down

NOTES:

1. Applicable for both SLOW-EXIT and FAST-EXIT precharge power-down modes.
2. tAOFPD and tAOF must be satisfied and outputs High-Z prior to T1 (see section: On-Die Termination (ODT) for exact requirements).
3. If the $R_{TT,nom}$ feature was enabled in the mode register prior to entering precharge power-down mode, the ODT signal must be continuously registered LOW, ensuring R_{TT} is in an off state. If the $R_{TT,nom}$ feature was disabled in the mode register prior to entering precharge power-down mode, R_{TT} will remain in the off state. The ODT signal can be registered LOW or HIGH in this case.

Write Leveling

For better signal integrity, DDR3(L) SDRAM memory modules have adopted fly-by topology for the commands, addresses, control signals, and clocks. Write leveling is a scheme for the memory controller to adjust or de-skew the DQS strobe (DQS, DQS#) to CK relationship at the DRAM with a simple feedback feature provided by the DRAM. Write leveling is generally used as part of the initialization process, if required. For normal DRAM operation, this feature must be disabled. This is the only DRAM operation where the DQS functions as an input (to capture the incoming clock) and the DQ function as outputs (to report the state of the clock). Note that nonstandard ODT schemes are required.

The memory controller using the write leveling procedure must have adjustable delay settings on its DQS strobe to align the rising edge of DQS to the clock at the DRAM pins. This is accomplished when the DRAM asynchronously feeds back the CK status via the DQ bus and samples with the rising edge of DQS. The controller repeatedly delays the DQS strobe until a CK transition from 0 to 1 is detected. The DQS delay established by this procedure helps ensure tDQSS, tDSS, and tDSH specifications in systems that use fly-by topology by de-skewing the trace length mismatch. A conceptual timing of this procedure is shown in Figure 4-34.

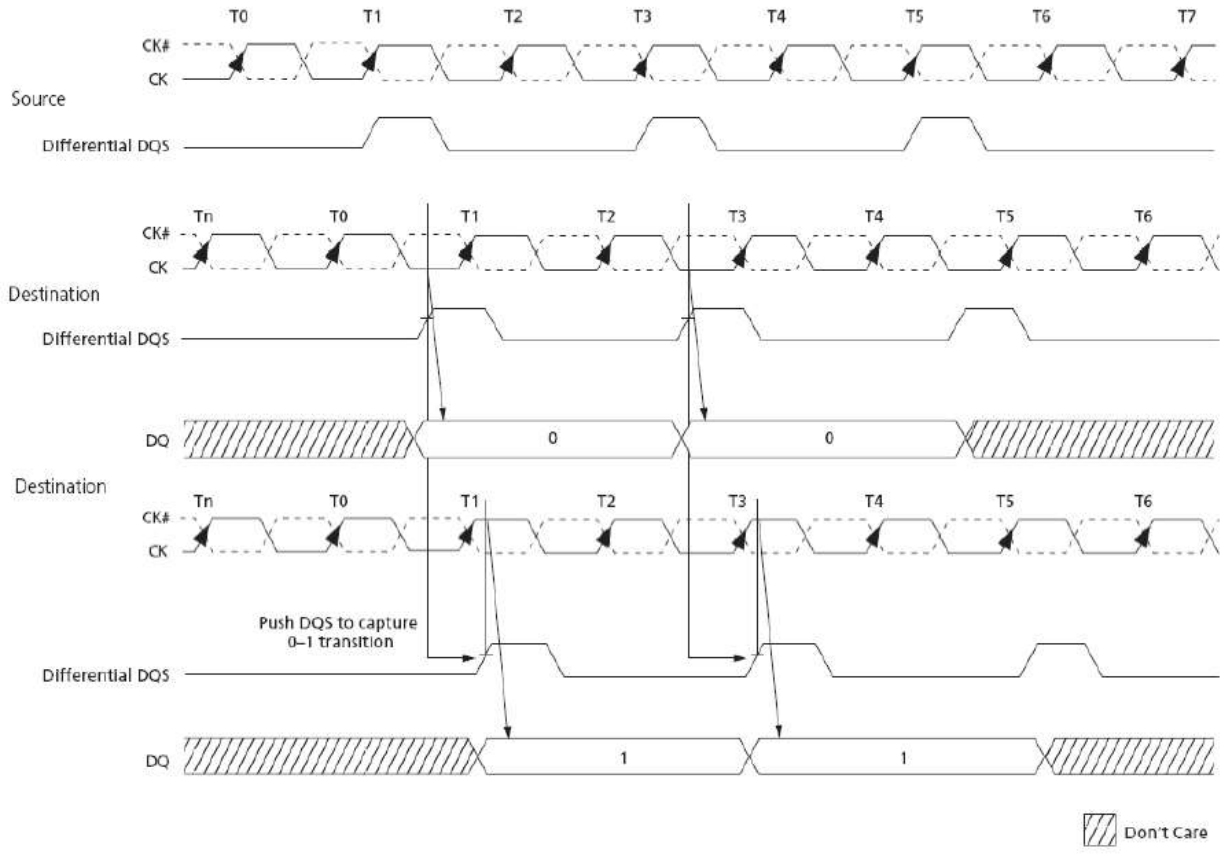


Figure 4-34: Write Leveling Concept

When write leveling is enabled, the rising edge of DQS samples CK, and the prime DQ outputs the sampled CK's status.

The write leveling mode register interacts with other mode registers to correctly configure the write leveling functionality. Besides using MR1[7] to disable/enable write leveling, MR1[12] must be used to enable/disable the output buffers. The ODT value, burst length, and so forth need to be selected as well. This interaction is shown in Table 4-69. It should also be noted that when the outputs are enabled during write leveling mode, the DQS buffers are set as inputs, and the DQ are set as outputs. Additionally, during write leveling mode, only the DQS strobe terminations are activated and deactivated via the ODT ball. The DQ remain disabled and are not affected by the ODT ball.

Table 4-69: WriteLeveling Matrix

Note 1 applies to the entire table

MR1[7]	MR1[12]	MR1 [2, 6, 9]	DRAM ODT Ball	DRAM $R_{TT,nom}$		DRAM State	Case	Notes
Write Leveling	Output Buffers	$R_{TT,nom}$ Value		DQS	DQ			
Disabled	See normal operations					Write leveling not enabled	0	
Enabled (1)	Disabled (1)	N/A	Low	Off	Off	DQS not receiving: not terminated Prime DQ High-Z: not terminated Other DQ High-Z: not terminated	1	2
		20Ω,30Ω, 40Ω,60Ω, or 120Ω	High	On		DQS not receiving: terminated by R_{TT} Prime DQ High-Z: not terminated	2	
	Enabled (0)	N/A	Low	Off		DQS receiving: not terminated Prime DQ driving CK state: not terminated Other DQ driving LOW: not terminated	3	3
		40Ω,60Ω, or 120Ω	High	On		DQS receiving: terminated by R_{TT} Prime DQ driving CK state: not terminated Other DQ driving LOW: not terminated	4	

Notes:

1. Expected usage if used during write leveling: Case 1 may be used when DRAM are on a dual-rank module and on the rank not being leveled or on any rank of a module not being leveled on a multislot system. Case 2 may be used when DRAM are on any rank of a module not being leveled on a multislot system. Case 3 is generally not used. Case 4 is generally used when DRAM are on the rank that is being leveled.
2. Since the DRAM DQS is not being driven (MR1[12] = 1), DQS ignores the input strobe, and all $R_{TT,nom}$ values are allowed. This simulates a normal standby state to DQS.
3. Since the DRAM DQS is being driven (MR1[12] = 0), DQS captures the input strobe, and only some $R_{TT,nom}$ values are allowed. This simulates a normal write state to DQS.

Write Leveling Procedure

A memory controller initiates the DRAM write leveling mode by setting MR1[7] to 1, assuming the other programable features (MR0, MR1, MR2, and MR3) are first set and the DLL is fully reset and locked. The DQ balls enter the write leveling mode going from a High-Z state to an undefined driving state, so the DQ bus should not be driven. During write leveling mode, only the NOP or DES commands are allowed. The memory controller should attempt to level only one rank at a time; thus, the outputs of other ranks should be disabled by setting MR1[12] to 1 in the other ranks. The memory controller may assert ODT after a tMOD delay, as the DRAM will be ready to process the ODT transition. ODT should be turned on prior to DQS being driven LOW by at least ODTLon delay (WL - 2 tCK), provided it does not violate the aforementioned tMOD delay requirement.

The memory controller may drive DQS LOW and DQS# HIGH after tWLDQSEN has been satisfied. The controller may begin to toggle DQS after tWLMRD (one DQS toggle is DQS transitioning from a LOW state to a HIGH state with DQS# transitioning from a HIGH state to a LOW state, then both transition back to their original states). At a minimum, ODTLon and tAON must be satisfied at least one clock prior to DQS toggling.

After tWLMRD and a DQS LOW preamble (tWPRE) have been satisfied, the memory controller may provide either a single DQS toggle or multiple DQS toggles to sample CK for a given DQS-to-CK skew. Each DQS toggle must not violate tDQSL (MIN) and tDQSH (MIN) specifications. tDQSL (MAX) and tDQSH (MAX) specifications are not applicable during write leveling mode. The DQS must be able to distinguish the CK's rising edge within tWLS and tWLH. The prime DQ will output the CK's status asynchronously from the associated DQS rising edge CK capture within tWLO. The remaining DQ that always drive LOW when DQS is toggling must be LOW within tWLOE after the first tWLO is satisfied (the prime DQ going LOW). As previously noted, DQS is an input and not an output during this process. Figure 4-35 depicts the basic timing parameters for the overall write leveling procedure.

The memory controller will most likely sample each applicable prime DQ state and determine whether to increment or decrement its DQS delay setting. After the memory controller performs enough DQS toggles to detect the CK's 0-to-1 transition, the memory controller should lock the DQS delay setting for that DRAM. After locking the DQS setting is locked, leveling for the rank will have been achieved, and the write leveling mode for the rank should be disabled or reprogrammed (if write leveling of another rank follows).

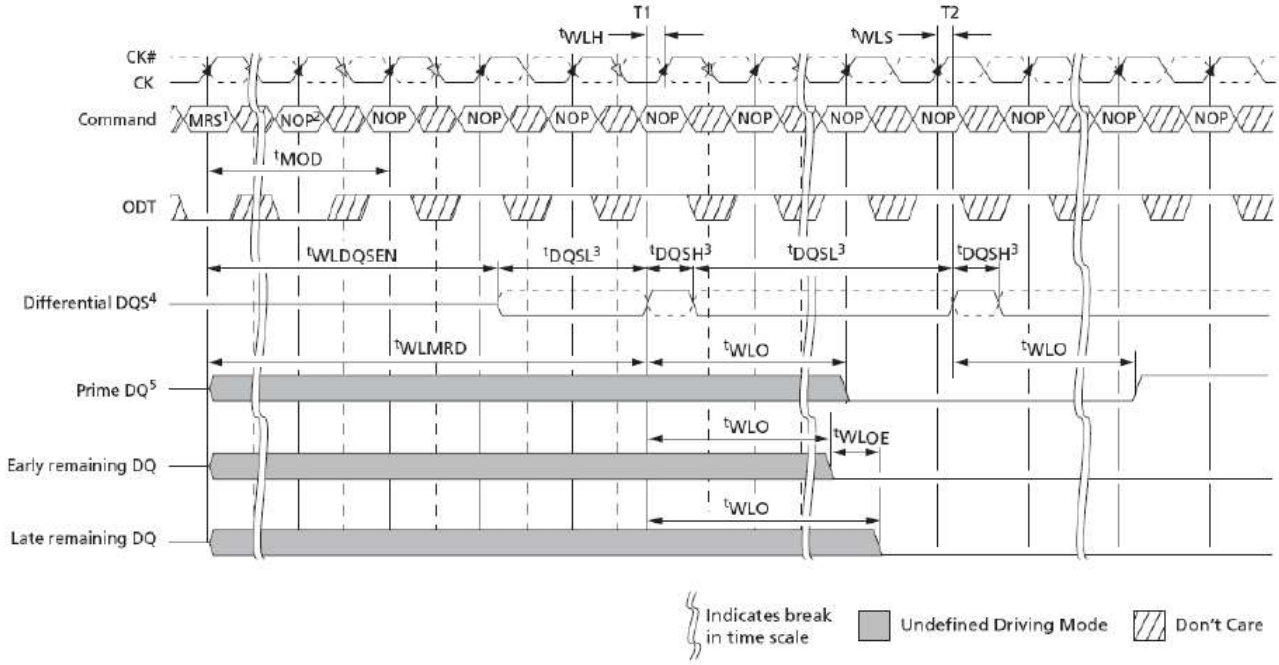


Figure 4-35: Write Leveling Sequence

NOTES:

1. MRS: Load MR1 to enter write leveling mode.
2. NOP: NOP or DES.
3. DQS, DQS# needs to fulfill minimum pulse width requirements tDQSH (MIN) and tDQSL (MIN) as defined for regular writes. The maximum pulse width is system-dependent.
4. Differential DQS is the differential data strobe (DQS, DQS#). Timing reference points are the zero crossings. The solid line represents DQS; the dotted line represents DQS#.
5. DRAM drives leveling feedback on a prime DQ. The remaining DQ are driven LOW and remain in this state throughout the leveling procedure.

Write Leveling Mode Exit Procedure

After the DRAM are leveled, they must exit from write leveling mode before the normal mode can be used. Figure4-36 depicts a general procedure for exiting write leveling mode. After the last rising DQS (capturing a 1 at T0), the memory controller should stop driving the DQS signals after tWLO (MAX) delay plus enough delay to enable the memory controller to capture the applicable prime DQ state (at ~Tb0). The DQ balls become undefined when DQS no longer remains LOW, and they remain undefined until tMOD after the MRS command (at Te1).

The ODT input should be de-asserted LOW such that ODTLoff (MIN) expires after the DQS is no longer driving LOW. When ODT LOW satisfies tIS, ODT must be kept LOW (at ~Tb0) until the DRAM is ready for either another rank to be leveled or until the normal mode can be used. After DQS termination is switched off, write level mode should be disabled via the MRS command (at Tc2). After tMOD is satisfied (at Te1), any valid command may be registered by the DRAM. Some MRS commands may be issued after tMRD (at Td1).

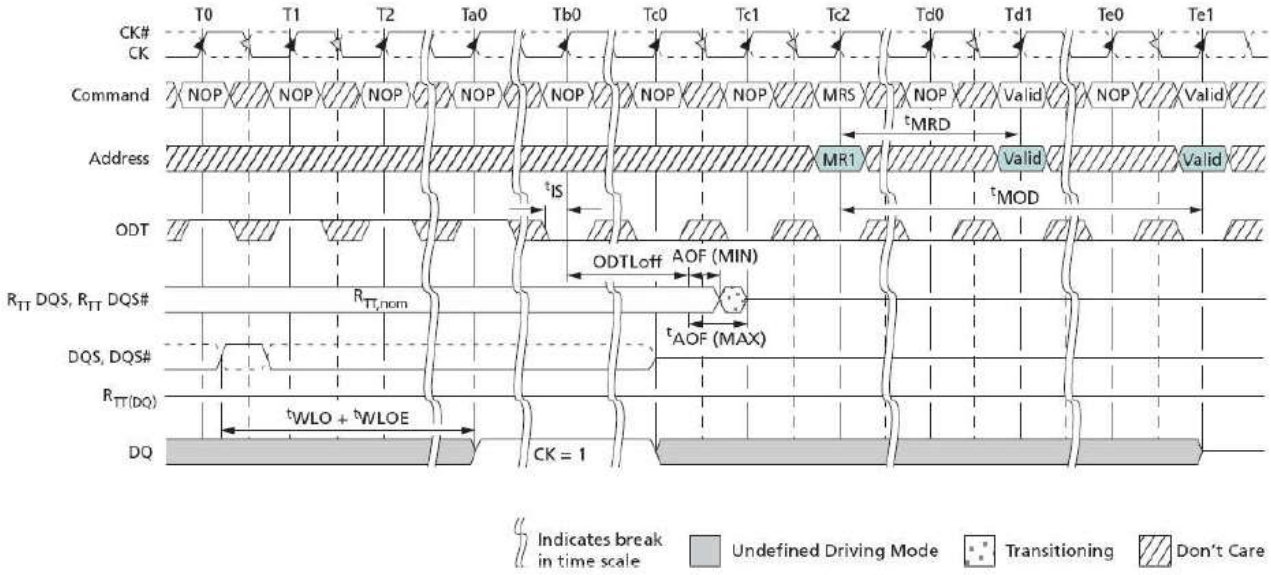


Figure 4-36: Write Leveling Exit Procedure

NOTE:

1. The DQ result, = 1, between Ta0 and Tc0, is a result of the DQS, DQS# signals capturing CK HIGH just after the T0 state.

Initialization

The following sequence is required for power-up and initialization, as shown in Figure 4-37:

1. Apply power. RESET# is recommended to be below 0.2 × V_{DDQ} during power ramp to ensure the outputs remain disabled (High-Z) and ODT off (R_{TT} is also High-Z).

   All other inputs, including ODT, may be undefined.

   During power-up, either of the following conditions may exist and must be met:

   • Condition A:

   – V_{DD} and V_{DDQ} are driven from a single-power converter output and are ramped with a maximum delta voltage between them of $\Delta V \leq 300mV$. Slope reversal of any power supply signal is allowed. The voltage levels on all balls other than V_{DD}, V_{DDQ}, V_{SS}, V_{SSQ} must be less than or equal to V_{DDQ} and V_{DD} on one side, and must be greater than or equal to V_{SSQ} and V_{SS} on the other side.

   – Both V_{DD} and V_{DDQ} power supplies ramp to $V_{DD,min}$ and $V_{DDQ,min}$ within tV_{DDPR} = 200ms.

   – V_{REFDQ} tracks V_{DD} × 0.5, V_{REFCA} tracks V_{DD} × 0.5.

   – V_{TT} is limited to 0.95V when the power ramp is complete and is not applied directly to the device; however, tVTD should be greater than or equal to 0 to avoid device latchup.

   • Condition B:

   – V_{DD} may be applied before or at the same time as V_{DDQ}.

   – V_{DDQ} may be applied before or at the same time as V_{TT}, V_{REFDQ}, and V_{REFCA}.

   – No slope reversals are allowed in the power supply ramp for this condition.

2. Until stable power, maintain RESET# LOW to ensure the outputs remain disabled (High-Z). After the power is stable, RESET# must be LOW for at least 200us to begin the initialization process. ODT will remain in the High-Z state while RESET# is LOW and until CKE is registered HIGH.
3. CKE must be LOW 10ns prior to RESET# transitioning HIGH.
4. After RESET# transitions HIGH, wait 500us (minus one clock) with CKE LOW.

5. After the CKE LOW time, CKE may be brought HIGH (synchronously) and only NOP or DES commands may be issued. The clock must be present and valid for at least 10ns (and a minimum of five clocks) and ODT must be driven LOW at least tIS prior to CKE being registered HIGH. When CKE is registered HIGH, it must be continuously registered HIGH until the full initialization process is complete.
6. After CKE is registered HIGH and after tXPR has been satisfied, MRS commands may be issued. Issue an MRS (LOAD MODE) command to MR2 with the applicable settings (provide LOW to BA2 and BA0 and HIGH to BA1).
7. Issue an MRS command to MR3 with the applicable settings.
8. Issue an MRS command to MR1 with the applicable settings, including enabling the DLL and configuring ODT.
9. Issue an MRS command to MR0 with the applicable settings, including a DLL RESET command. tDLLK (512) cycles of clock input are required to lock the DLL.
10. Issue a ZQCL command to calibrate R_{TT} and R_{ON} values for the process voltage temperature (PVT). Prior to normal operation, tZQinit must be satisfied.
11. When tDLLK and tZQinit have been satisfied, the DDR3(L) SDRAM will be ready for normal operation.

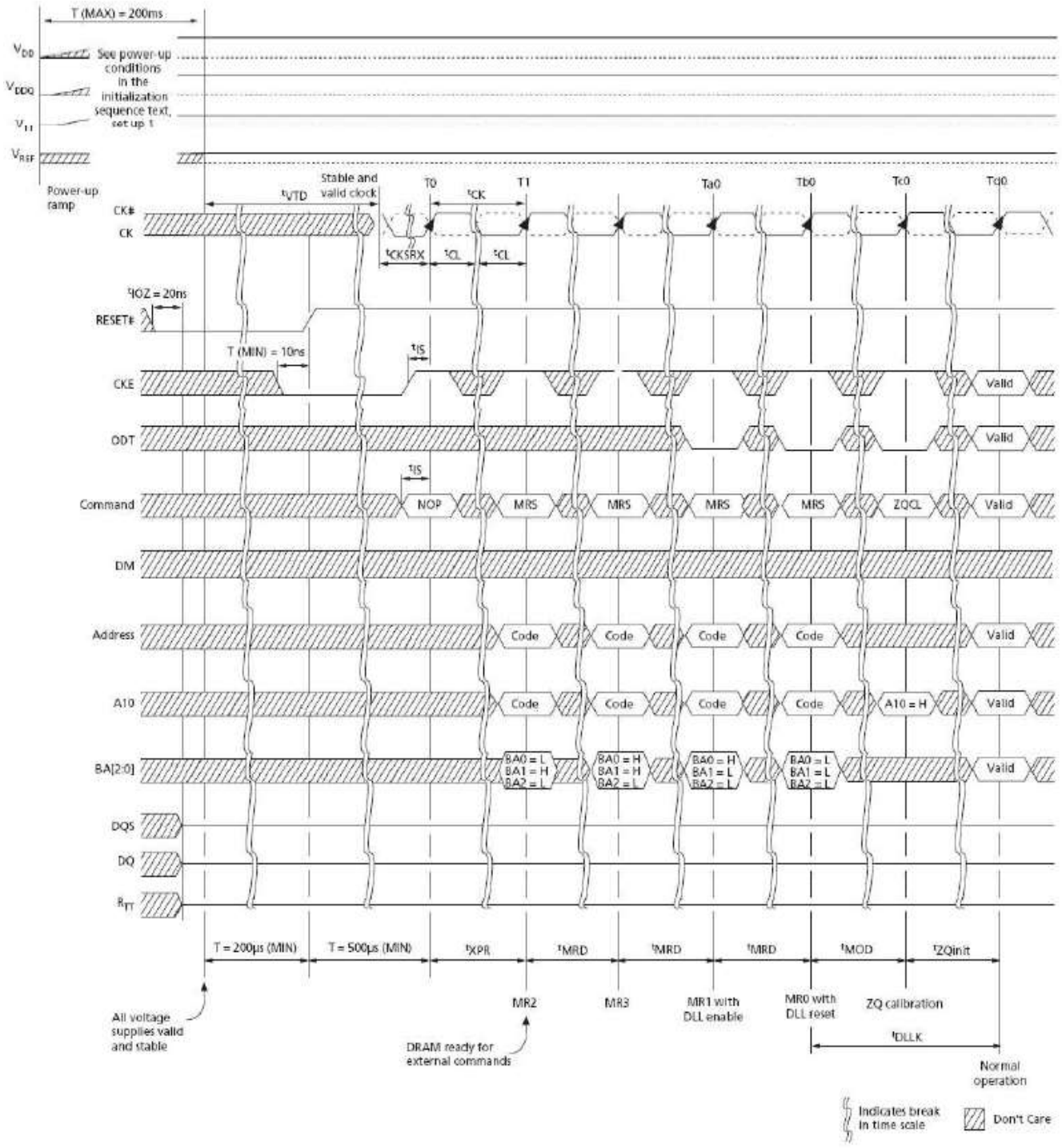


Figure 4-37: Initialization Sequence

Voltage Initialization / Change

If the SDRAM is powered up and initialized for the 1.35V operating voltage range, voltage can be increased to the 1.5V operating range provided the following conditions aremet (See Figure 4-38):

- Just prior to increasing the 1.35V operating voltages, no further commands are issued, other than NOPs or COMMAND INHIBITs, and all banks are in the precharge state.
- The 1.5V operating voltages are stable prior to issuing new commands, other than NOPs or COMMAND INHIBITs.
- The DLL is reset and relocked after the 1.5V operating voltages are stable and prior to any READ command.
- The ZQ calibration is performed. tZQinit must be satisfied after the 1.5V operating voltages are stable and prior to any READ command.

If the SDRAM is powered up and initialized for the 1.5V operating voltage range, voltage can be reduced to the 1.35V operation range provided the following conditions are met (See Figure 4-38):

- Just prior to reducing the 1.5V operating voltages, no further commands are issued, other than NOPs or COMMAND INHIBITs, and all banks are in the precharge state.
- The 1.35V operating voltages are stable prior to issuing new commands, other than NOPs or COMMAND INHIBITs.
- The DLL is reset and relocked after the 1.35V operating voltages are stable and prior to any READ command.
- The ZQ calibration is performed. tZQinit must be satisfied after the 1.35V operating voltages are stable and prior to any READ command.

V_{DD} Voltage Switching

After the DDR3(L) DRAM is powered up and initialized, the power supply can be altered between the DDR3L and DDR3 levels, provided the sequence in Figure 4-38 is maintained.

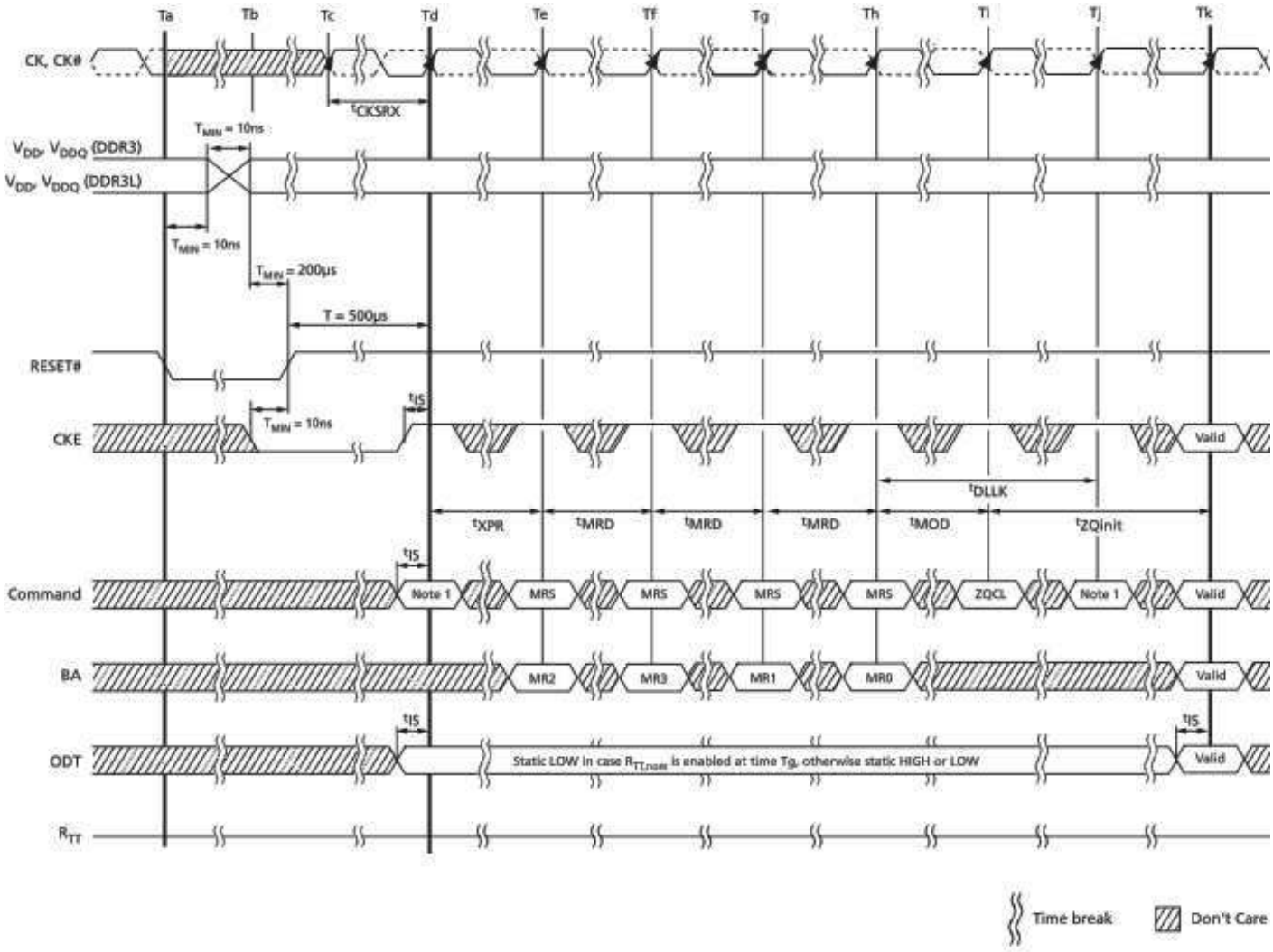


Figure 4-38: V_{DD} Voltage Switching

NOTE:

1. From time point Td until Tk, NOP or DES commands must be applied between MRS and ZQCL commands.

Mode Registers

Mode registers (MR0–MR3) are used to define various modes of programmable operations of the DDR3(L) SDRAM. A mode register is programmed via the mode register set (MRS) command during initialization, and it retains the stored information (except for MR0[8], which is self-clearing) until it is reprogrammed, RESET# goes LOW, the device loses power.

Contents of a mode register can be altered by re-executing the MRS command. Even if the user wants to modify only a subset of the mode register's variables, all variables must be programmed when the MRS command is issued. Reprogramming the mode register will not alter the contents of the memory array, provided it is performed correctly.

The MRS command can only be issued (or re-issued) when all banks are idle and in the precharged state (tRP is satisfied and no data bursts are in progress). After an MRS command has been issued, two parameters must be satisfied: tMRD and tMOD. The controller must wait tMRD before initiating any subsequent MRS commands.

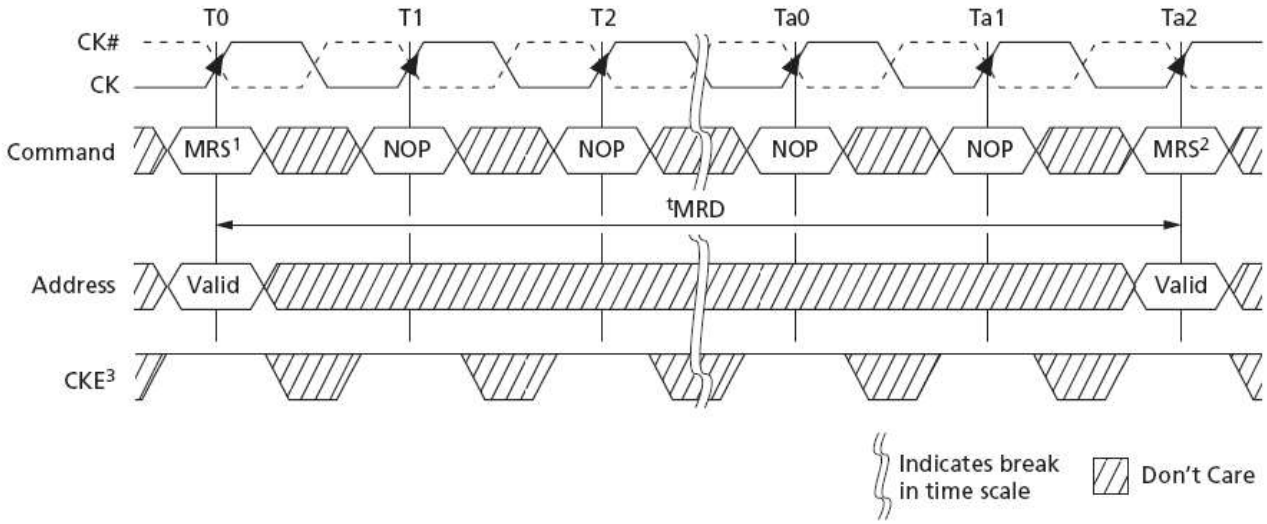


Figure 4-39: MRS to MRS Command Timing (tMRD)

NOTES:

1. Prior to issuing the MRS command, all banks must be idle and precharged, tRP (MIN) must be satisfied, and no data bursts can be in progress.
2. tMRD specifies the MRS to MRS command minimum cycle time.
3. CKE must be registered HIGH from the MRS command until tMRSPDEN (MIN) (see Power-Down Mode).
4. For a CAS latency change, tXPDLL timing must be met before any non-MRS command.

The controller must also wait tMOD before initiating any non-MRS commands (excluding NOP and DES). The DRAM requires tMOD in order to update the requested features, with the exception of DLL RESET, which requires additional time. Until tMOD has been satisfied, the updated features are to be assumed unavailable.

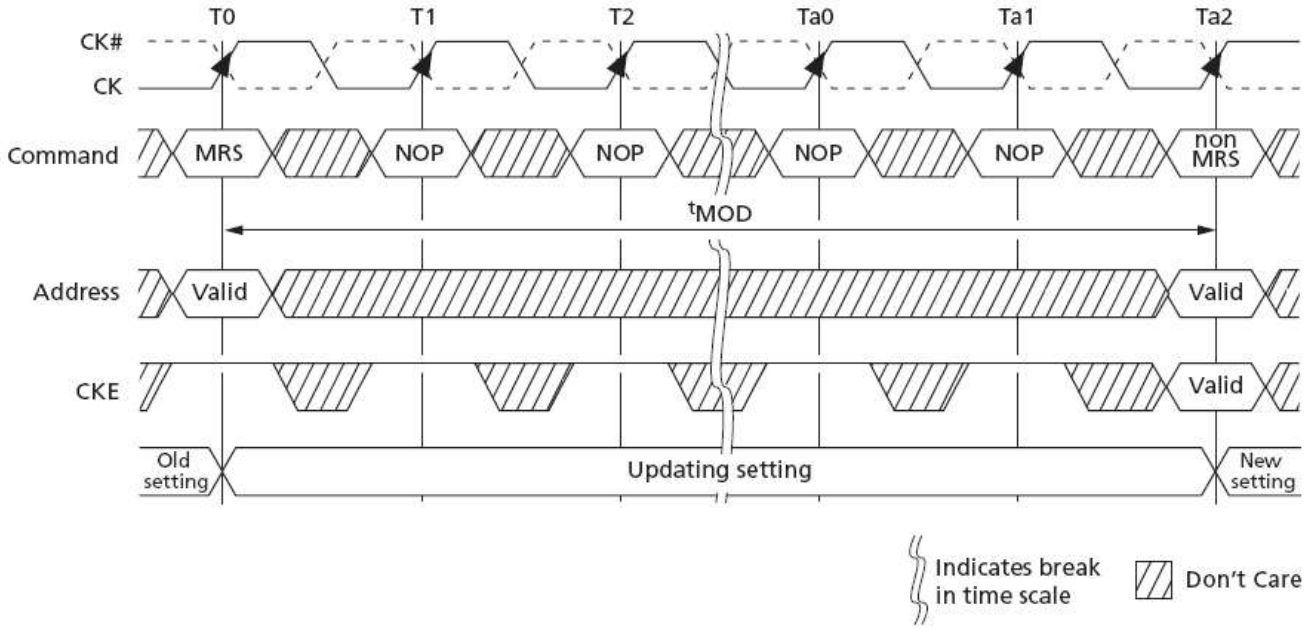


Figure 4-40: MRS to nonMRS Command Timing (tMOD)

NOTES:

1. Prior to issuing the MRS command, all banks must be idle (they must be precharged, tRP must be satisfied, and no data bursts can be in progress).
2. Prior to Ta2 when tMOD (MIN) is being satisfied, no commands (except NOP/DES) may be issued.
3. If R_{TT} was previously enabled, ODT must be registered LOW at T0 so that ODTL is satisfied prior to Ta1. ODT must also be registered LOW at each rising CK edge from T0 until tMODmin is satisfied at Ta2.
4. CKE must be registered HIGH from the MRS command until tMRSPDEN (MIN), at which time power-down may occur (see Power-Down Mode).

Mode Register 0 (MR0)

The base register, mode register 0 (MR0), is used to define various DDR3(L) SDRAM modes of operation. These definitions include the selection of a burst length, burst type, CAS latency, operating mode, DLL RESET, write recovery, and precharge power-down mode (see Figure 4-41).

Burst Length

Burst length is defined by MR0[1:0]. Read and write accesses to the DDR3(L) SDRAM are burst-oriented, with the burst length being programmable to 4 (chop mode), 8 (fixed mode), or selectable using A12 during a READ/WRITE command (on-the-fly). The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. When MR0[1:0] is set to 01 during a READ/WRITE command, if A12 = 0, then BC4 (chop) mode is selected. If A12 = 1, then BL8 mode is selected. Specific timing diagrams, and turnaround between READ/WRITE, are shown in the READ/WRITE sections of this document.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A[*i*:2] when the burst length is set to 4 and by A[*i*:3] when the burst length is set to 8 (where A*i* is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length
applies to both READ and WRITE bursts.

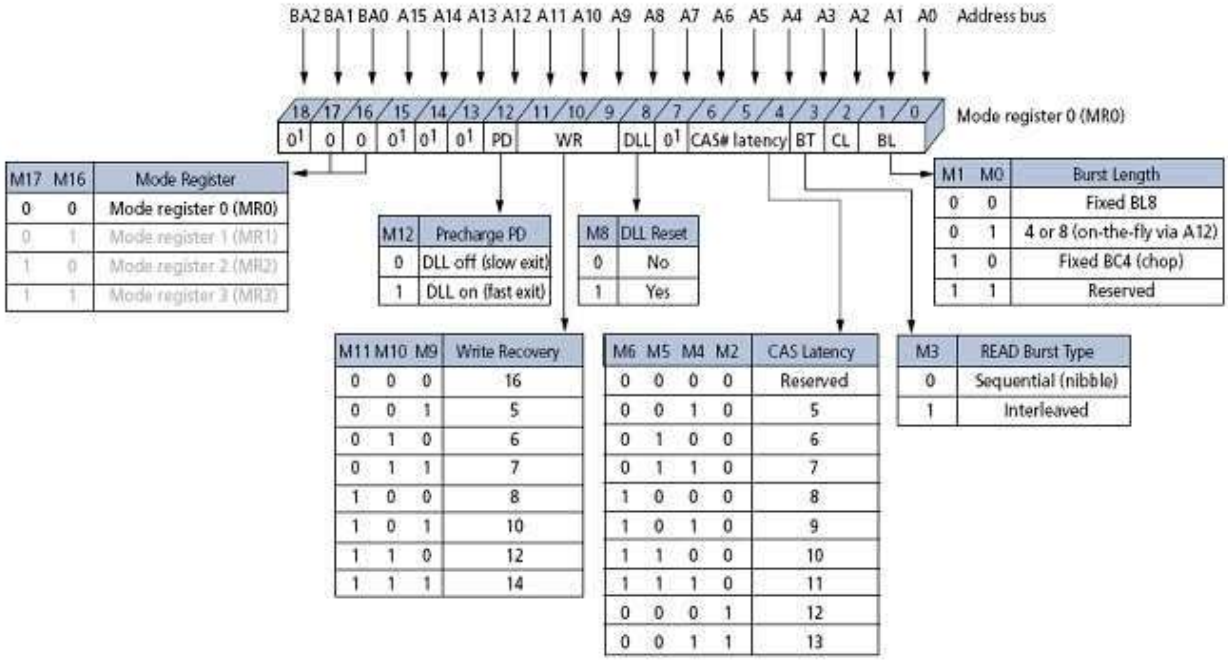


Figure 4-41: Mode Register 0 (MR0) Definitions

NOTE:

1. MR0[18, 15;13, 7] are reserved for future use and must be programmed to 0.

Burst Type

Accesses within a given burst can be programmed to either a sequential or an interleaved order. The burst type is selected via MR0[3] (see Figure 4-41). The ordering of accesses within a burst is determined by the burst length, the burst type, and the starting column address. DDR3(L) only supports 4-bit burst chop and 8-bit burst access modes. Full interleave address ordering is supported for READs, while WRITEs are restricted to nibble (BC4) or word (BL8) boundaries.

Table 4-70: Burst Order

Burst Length	READ/ WRITE	Starting Column Address (A[2, 1, 0])	Burst Type = Sequential (Decimal)	Burst Type = Interleaved (Decimal)	Notes
4 (chop)	READ	0 0 0	0, 1, 2, 3, Z, Z, Z, Z	0, 1, 2, 3, Z, Z, Z, Z	1, 2
		0 0 1	1, 2, 3, 0, Z, Z, Z, Z	1, 0, 3, 2, Z, Z, Z, Z	1, 2
		0 1 0	2, 3, 0, 1, Z, Z, Z, Z	2, 3, 0, 1, Z, Z, Z, Z	1, 2
		0 1 1	3, 0, 1, 2, Z, Z, Z, Z	3, 2, 1, 0, Z, Z, Z, Z	1, 2
		1 0 0	4, 5, 6, 7, Z, Z, Z, Z	4, 5, 6, 7, Z, Z, Z, Z	1, 2
		1 0 1	5, 6, 7, 4, Z, Z, Z, Z	5, 4, 7, 6, Z, Z, Z, Z	1, 2
		1 1 0	6, 7, 4, 5, Z, Z, Z, Z	6, 7, 4, 5, Z, Z, Z, Z	1, 2
		1 1 1	7, 4, 5, 6, Z, Z, Z, Z	7, 6, 5, 4, Z, Z, Z, Z	1, 2
	WRITE	0 V V	0, 1, 2, 3, X, X, X, X	0, 1, 2, 3, X, X, X, X	1, 3, 4
		1 V V	4, 5, 6, 7, X, X, X, X	4, 5, 6, 7, X, X, X, X	1, 3, 4
8 (fixed)	READ	0 0 0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	1
		0 0 1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6	1
		0 1 0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5	1
		0 1 1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4	1
		1 0 0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3	1
		1 0 1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2	1
		1 1 0	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1	1
		1 1 1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0	1
	WRITE	V V V	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	1, 3

NotesS:

1. Internal READ and WRITE operations start at the same point in time for BC4 as they do for BL8.
2. Z = Data and strobe output drivers are in tri-state.
3. V = A valid logic level (0 or 1), but the respective input buffer ignores level-on input pins.
4. X = “Don’t Care”.

DLL RESET

DLL RESET is defined by MR0[8] (see Figure 4-41). Programming MR0[8] to 1 activates the DLL RESET function. MR0[8] is self-clearing, meaning it returns to a value of 0 after the DLL RESET function has been initiated.

Anytime the DLL RESET function is initiated, CKE must be HIGH and the clock held stable for 512 (tDLLK) clock cycles before a READ command can be issued. This is to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization can result in invalid output timing specifications, such as tDQSCK timings.

Write Recovery

WRITE recovery time is defined by MR0[11:9] (see Figure 4-41). Write recovery values of 5, 6, 7, 8, 10, or 12 can be used by programming MR0[11:9]. The user is required to program the correct value of write recovery, which is calculated by dividing tWR (ns) by tCK (ns) and rounding up a noninteger value to the next integer:

WR (cycles) = roundup (tWR [ns]/tCK [ns]).

Precharge Power-Down (Precharge PD)

The precharge power-down (PD) bit applies only when precharge power-down mode is being used. When MR0[12] is set to 0, the DLL is off during precharge power-down, providing a lower standby current mode; however, tXPDLL must be satisfied when exiting. When MR0[12] is set to 1, the DLL continues to run during precharge power-down mode to enable a faster exit of precharge power-down mode; however, tXP must be satisfied when exiting (see section: Power-Down Mode).

CAS Latency (CL)

CAS latency (CL) is defined by MR0[6:4], as shown in Figure 4-41. CAS latency is the delay, in clock cycles, between the internal READ command and the availability of the first bit of output data. CL can be set to 5 through 14. DDR3(L) SDRAM do not support half-clock latencies.

Examples of CL = 6 and CL = 8 are shown below. If an internal READ command is regis-tered at clock edge n, and the CAS latency is m clocks, the data will be available nominally coincident with clock edge *n* + *m*. See Speed Bin Table for the CLs supported at various operating frequencies.

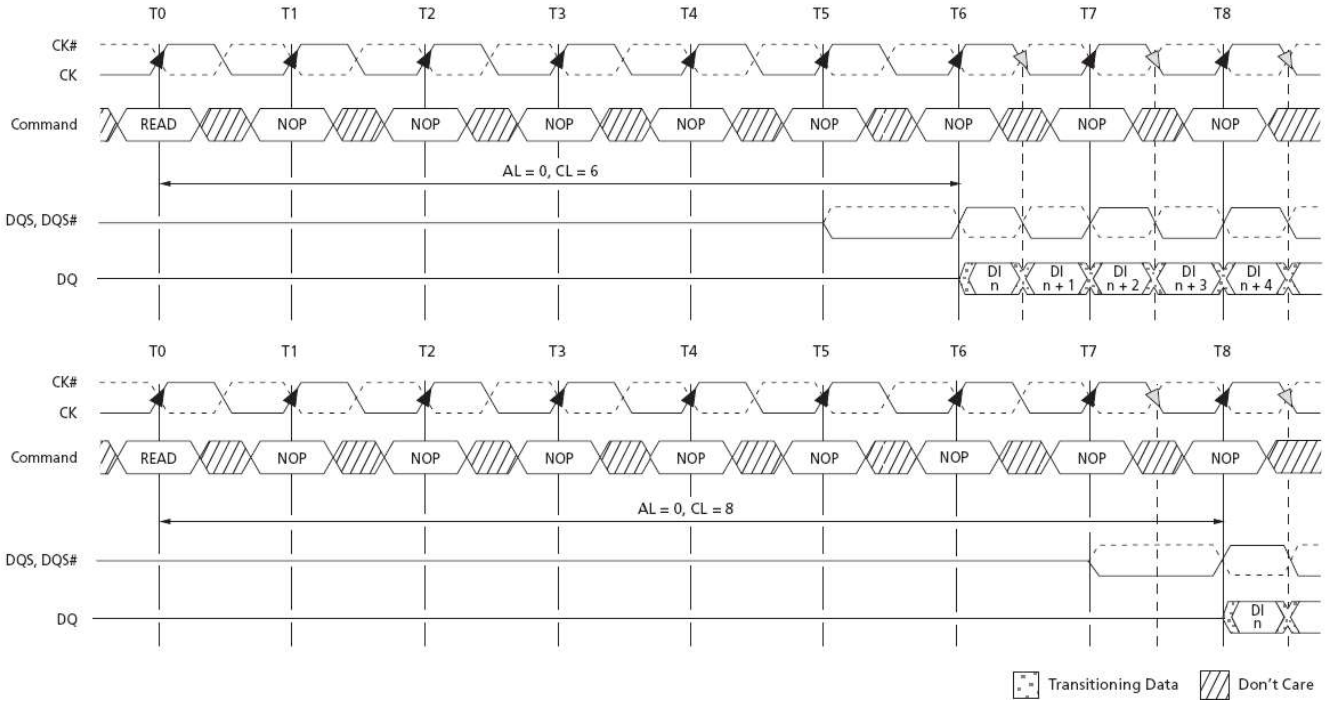


Figure 4-42: READ Latency

NOTES:

1. For illustration purposes, only CL = 6 and CL = 8 are shown. Other CL values are possible.

2. Shown with nominal tDQSCK and nominal tDSDQ.

Mode Register 1 (MR1)

The mode register 1 (MR1) controls additional features and functions not available in the other mode registers: Q OFF (OUTPUT DISABLE)), DLL ENABLE/DLL DISABLE, $R_{TT,nom}$ value (ODT), WRITE LEVELING, POSTED CAS ADDITIVE latency, and OUTPUT DRIVE STRENGTH. These functions are controlled via the bits shown in

Figure 4-43. The MR1 register is programmed via the MRS command and retains the stored information until it is reprogrammed, RESET# goes LOW, or the device loses power. Reprogramming the MR1 register will not alter the contents of the memory array, provided it is reprogrammed correctly.

The MR1 register must be loaded when all banks are idle and no bursts are in progress. The controller must satisfy the specified timing parameters tMRD and tMOD before initiating a subsequent operation.

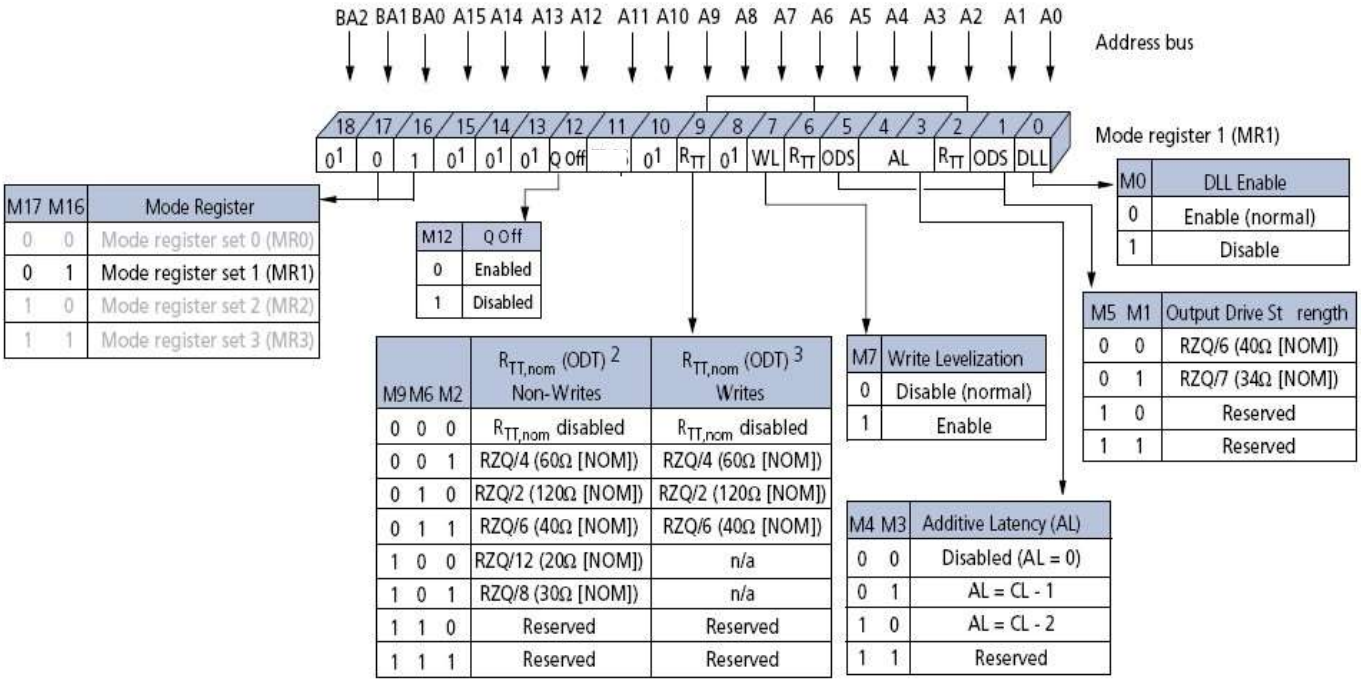


Figure 4-43: Mode Register 1 (MR1) Definition

NOTES:

1. MR1[18, 15:13, 10, 8] are reserved for future use and must be programmed to 0.
2. During write leveling, if MR1[7] and MR1[12] are 1, then all $R_{TT,nom}$ values are available for use.
3. During write leveling, if MR1[7] is a 1, but MR1[12] is a 0, then only $R_{TT,nom}$ write values are available for use.

DLL ENABLE/DISABLE

The DLL may be enabled or disabled by programming MR1[0] during the LOAD MODE command (see Figure 4-43). The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation, after having disabled the DLL for the purpose of debugging or evaluation. Enabling the DLL should always be followed by resetting the DLL using the appropriate LOAD MODE command.

If the DLL is enabled prior to entering self refresh mode, the DLL is automatically disabled when entering SELF REFRESH operation and is automatically re-enabled and reset upon exit of the SELF REFRESH operation. If the DLL is disabled prior to entering self refresh mode, the DLL remains disabled, even upon exit of the SELF REFRESH operation until it is re-enabled and reset.

The DRAM is not tested to check—nor does CHIPSIP warrant compliance with—normal mode timings or functionality when the DLL is disabled. An attempt has been made to have the DRAM operate in the normal mode where reasonably possible when the DLL has been disabled; however, by industry standard, a few known exceptions are defined:

• ODT is not allowed to be used.

• The output data is no longer edge-aligned to the clock.

• CL and CWL can only be six clocks.

When the DLL is disabled, timing and functionality can vary from the normal operation specifications when the DLL is enabled (see section: DLL Disable Mode). Disabling the DLL also implies the need to change the clock frequency (see section: Input Clock Frequency Change).

Output Drive Strength

The DDR3(L) SDRAM uses a programmable impedance output buffer. The drive strength mode register setting is defined by MR1[5, 1]. RZQ/7 (34Ω [NOM]) is the primary output driver impedance setting for DDR3(L) SDRAM devices. To calibrate the output driver impedance, an external precision resistor (RZQ) is connected between the ZQ ball and V_{SSQ}. The value of the resistor must be 240Ω±1%.

The output impedance is set during initialization. Additional impedance calibration updates do not affect device operation, and all data sheet timings and current specifications are met during an update.

To meet the 34Ω specification, the output drive strength must be set to 34Ω during initialization. To obtain a calibrated output driver impedance after power-up, the DDR3(L) SDRAM needs a calibration command that is part of the initialization and reset procedure.

OUTPUT ENABLE/DISABLE

The OUTPUT ENABLE/DISABLE function is defined by MR1[12] (see Figure 4-43). When enabled (MR1[12] = 0), all outputs (DQ, DQS, DQS#) function when in the normal mode of operation. When disabled (MR1[12] = 1), all DDR3(L) SDRAM outputs (DQ and DQS, DQS#) are High-Z. The output disable feature is intended to be used during I_{DD} characterization of the READ current and during tDQSS margining (write leveling) only.

On-Die Termination (ODT)

ODT resistance $R_{TT,nom}$ is defined by MR1[9, 6, 2] (see Figure 4-43). The R_{TT} termination value applies to the DQ, DM, DQS, DQS# balls. DDR3(L) supports multiple R_{TT} termination values based on RZQ/n where n can be 2, 4, 6, 8, or 12 and RZQ is 240Ω.

Unlike DDR3(L) ODT must be turned off prior to reading data out and must remain off during a READ burst. $R_{TT,nom}$ termination is allowed any time after the DRAM is initialized, calibrated, and not performing read accesses, or when it is not in self refresh mode. Additionally, write accesses with dynamic ODT ($R_{TT(WR)}$) enabled temporarily replaces $R_{TT, nom}$ with $R_{TT(WR)}$.

The actual effective termination, $R_{TT(EFF)}$, may be different from R_{TT} targeted due to nonlinearity of the termination. For $R_{TT(EFF)}$ values and calculations, (see section: On-Die Termination (ODT)).

The ODT feature is designed to improve signal integrity of the memory channel by enabling the DDR3(L) SDRAM controller to independently turn on/off ODT for any or all devices. The ODT input control pin is used to determine when R_{TT} is turned on (ODTLon) and off (ODTLoff), assuming ODT has been enabled via MR1[9, 6, 2].

Timings for ODT are detailed in On-Die Termination (ODT).

WRITE LEVELING

The WRITE LEVELING function is enabled by MR1[7] (see Figure 4-43). Write leveling is used (during initialization) to deskew the DQS strobe to clock offset as a result of fly-by topology designs. For better signal integrity, DDR3(L) SDRAM memory modules adopted fly-by topology for the commands, addresses, control signals, and clocks.

The fly-by topology benefits from a reduced number of stubs and their lengths. However, fly-by topology induces flight time skews between the clock and DQS strobe (and DQ) at each DRAM on the DIMM. Controllers will have a difficult time maintaining tDQSS, tDSS, and tDSH specifications without supporting write leveling in systems that use fly-by topology-based modules. Write leveling timing and detailed operation information is provided in Write Leveling.

Posted CAS Additive Latency (AL)

Posted CAS additive latency (AL) is supported to make the command and data bus efficient for sustainable bandwidths in DDR3(L) SDRAM. MR1[4, 3] define the value of AL (see Figure 4-44). MR1[4, 3] enable the user to program the DDR3(L) SDRAM with AL = 0, CL - 1, or CL - 2.

With this feature, the DDR3(L) SDRAM enables a READ or WRITE command to be issued after the ACTIVATE command for that bank prior to tRCD (MIN). The only restriction is ACTIVATE to READ or WRITE + AL ≥ tRCD (MIN) must be satisfied. Assuming tRCD (MIN) = CL, a typical application using this feature sets AL = CL - 1tCK = tRCD (MIN) – 1tCK. The READ or WRITE command is held for the time of the AL before it is released internally to the DDR3(L) SDRAM device. READ latency (RL) is controlled by the sum of the AL and CAS latency (CL), RL = AL + CL. WRITE latency (WL) is the sum of CAS WRITE latency and AL, WL = AL + CWL (see section: Mode Register 2 (MR2)). Examples of READ and WRITE latencies are shown in Figure 4-44 and Figure 4-46.

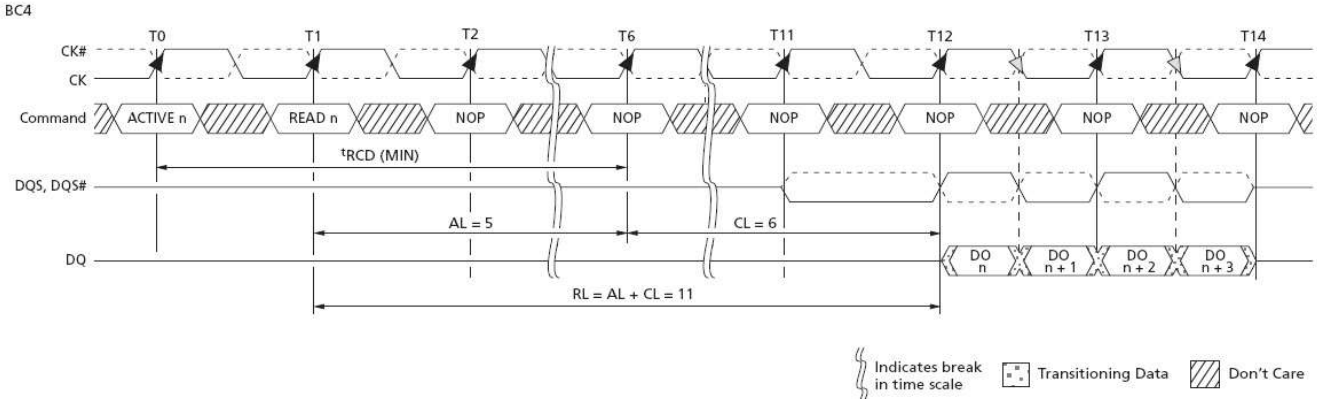


Figure 4-44: READ Latency (AL = 5, CL = 6)

Mode Register 2 (MR2)

The mode register 2 (MR2) controls additional functions and features not available in the other mode registers. These additional functions are CAS WRITE latency (CWL), AUTO SELF REFRESH (ASR), SELF REFRESH TEMPERATURE (SRT), and DYNAMIC ODT ($R_{TT(WR)}$). These functions are controlled via the bits shown in Figure 4-45. MR2 is programmed via the MRS command and will retain the stored information until it is programmed again or the device loses power. Reprogramming the MR2 register will not alter the contents of the memory array, provided it is reprogrammed correctly. The MR2 register must be loaded when all banks are idle and no data bursts are in progress, and the controller must wait the specified time tMRD and tMOD before initiating a subsequent operation.

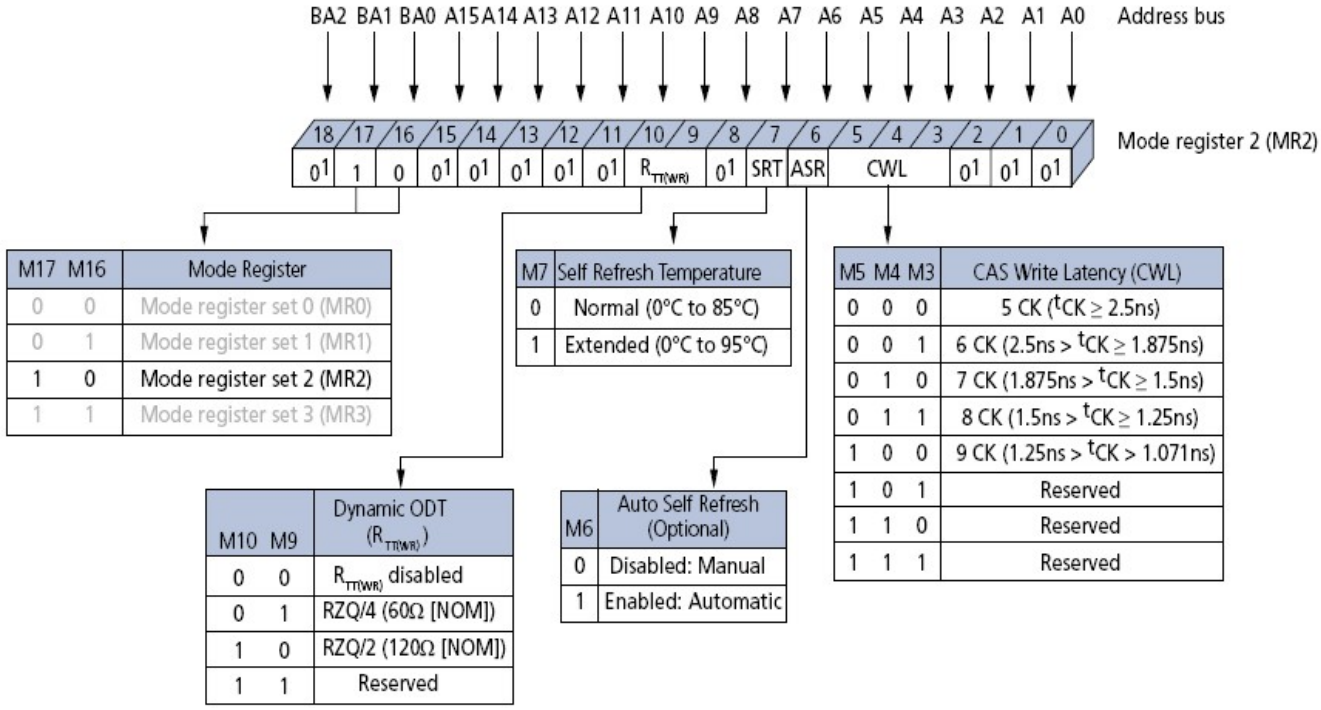


Figure 4-45: Mode Register 2 (MR2) Definition

NOTE:

1. MR2[18, 15:11, 8, and 2:0] are reserved for future use and must all be programmed to 0.

CAS WRITE Latency (CWL)

CWL is defined by MR2[5:3] and is the delay, in clock cycles, from the releasing of the internal write to the latching of the internal write to o the latching of the first data in. CWL must be correctly set to the corresponding operating clock frequency (see Figure 4-45). The overall WRITE latency (WL) is equal to CWL + AL (Figure 4-43).

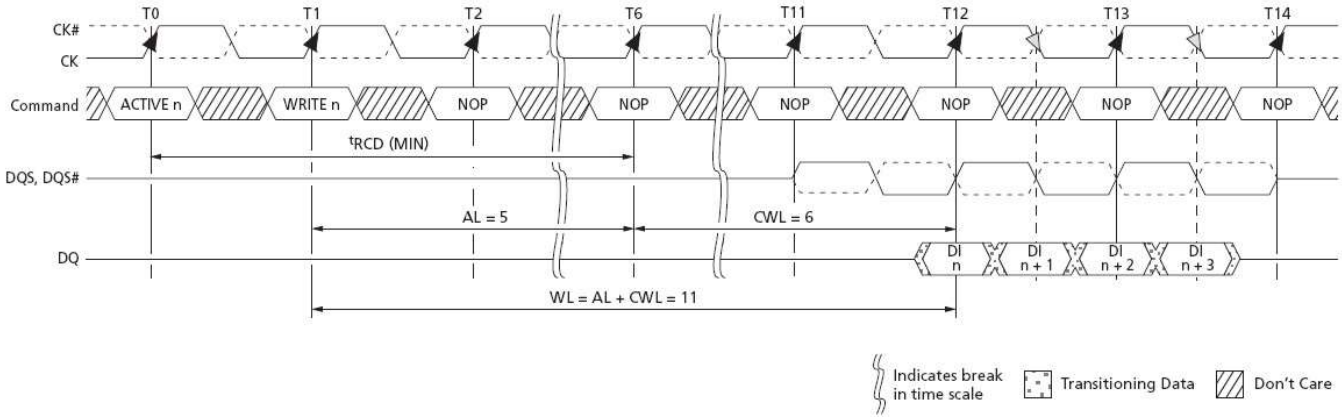


Figure 4-46: CAS WRITE Latency

AUTO SELF REFRESH (ASR)

Mode register MR2[6] is used to disable/enable the ASR function. When ASR is disabled, the self refresh mode's refresh rate is assumed to be at the normal 85℃ li mit (sometimes referred to as 1x refresh rate). In the disabled mode, ASR requires the user to ensure the DRAM never exceeds T_C of 85℃ while in self refresh unless the user enables the SRT feature listed below when the T_C is between 85℃ and 95℃.

Enabling ASR assumes the DRAM self refresh rate is changed automatically from 1x to 2x when the case temperature exceeds 85℃. This enables the user to operate the DRAM beyond the standard 85℃ limit up to the optional extended temperature range of 95℃ while i n self refresh mode.

The standard self refresh current test specifies test conditions for normal temperature (85℃) only, m eaning that if ASR is enabled, the standard self refresh current specifications do not apply (see section: Extended Temperature Usage).

SELF REFRESH TEMPERATURE (SRT)

Mode register MR2[7] is used to disable/enable the SRT function. When SRT is disabled, the self refresh mode's refresh rate is assumed to be at the normal 85℃ li mit (sometimes referred to as 1x refresh rate). In the disabled mode, SRT requires the user to ensure the DRAM never exceeds a T_C of 85℃ while in self refresh mode, unless the user enables ASR.

When SRT is enabled, the DRAM self refresh is changed internally from 1x to 2x, regardless of T_C. This enables the user to operate the DRAM beyond the standard 85℃ l imit up to the optional extended temperature range of 95℃ while in self refresh mode. The standard self refresh current test specifies test conditions for normal T_C (85℃) only, meaning that if SRT is enabled, the standard self refresh current specifications do not apply (see section: Extended Temperature Usage).

SRT vs.ASR

If the normal case temperature limit of 85℃ is not exceeded, then neither SRT nor ASR is required, and both can be disabled throughout operation. However, if the extended temperature option of 95℃ is needed, the user is required to provide a 2x refresh rate during (manual) refresh and to enable either the SRT or the ASR to ensure self refresh is performed at the 2x rate.

SRT forces the DRAM to switch the internal self refresh rate from 1x to 2x. Self refresh is performed at the 2x refresh rate regardless of the case temperature.

ASR automatically switches the DRAM's internal self refresh rate from 1x to 2x. However, while in self refresh mode, ASR enables the refresh rate to automatically adjust between 1x and 2x over the supported temperature range. One other disadvantage of ASR is the DRAM cannot always switch from a 1x to 2x refresh rate at an exact case temperature of 85℃. Although the DRAM will support data integrity when it switches from a 1x to 2x refresh rate, it may switch at a lower temperature than 85℃. Since only one mode is necessary, SRT and ASR cannot be enabled at the same time.

DYNAMIC ODT

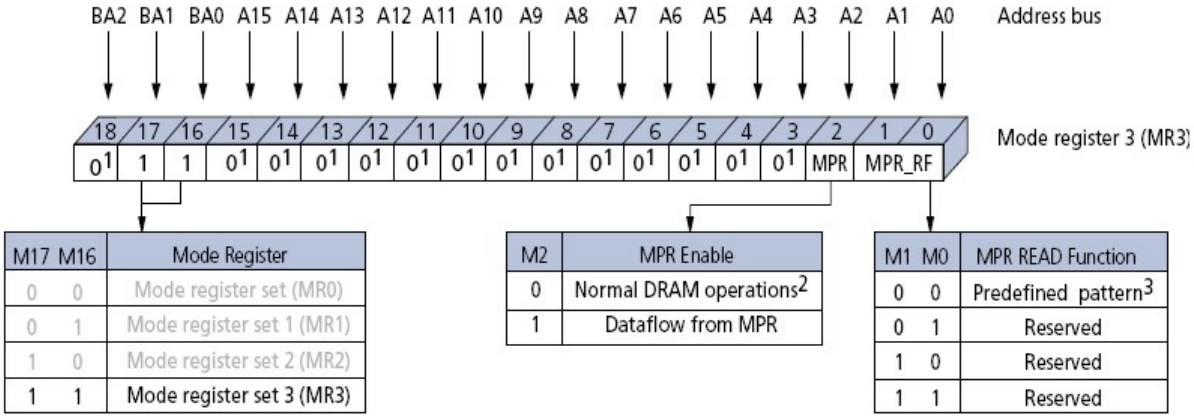
The dynamic ODT ($R_{TT(WR)}$) feature is defined by MR2[10, 9]. Dynamic ODT is enabled when a value is selected. This new DDR3(L) SDRAM feature enables the ODT termination resistance value to change without issuing an MRS command, essentially changing the ODT termination on-the-fly.

With dynamic ODT ($R_{TT(WR)}$) enabled, the DRAM switches from nominal ODT ($R_{TT,nom}$) to dynamic ODT ($R_{TT(WR)}$) when beginning a WRITE burst, and subsequently switches back to normal ODT ($R_{TT,nom}$) at the completion of the WRITE burst. If $R_{TT,nom}$ is disabled, the $R_{TT,nom}$ value will be High-Z. Special timing parameters must be adhered to when dynamic ODT ($R_{TT(WR)}$) is enabled: ODTLcnw, ODTLcwn4, ODTLcwn8, ODTH4, ODTH8, and tADC.

Dynamic ODT is only applicable during WRITE cycles. If normal ODT ($R_{TT,nom}$) is disabled, dynamic ODT ($R_{TT(WR)}$) is still permitted. $R_{TT,nom}$ and $R_{TT(WR)}$ can be used independent of one another. Dynamic ODT is not available during write leveling mode, regardless of the state of ODT ($R_{TT,nom}$). For details on dynamic ODT operation, refer to section Dynamic ODT.

Mode Register 3 (MR3)

The mode register 3 (MR3) controls additional functions and features not available in the other mode registers. Currently defined is the MULTIPURPOSE REGISTER (MPR). This function is controlled via the bits shown in Figure 4-47. The MR3 is programmed via the LOAD MODE command and retains the stored information until it is programmed again or until the device loses power. Reprogramming the MR3 register will not alter the contents of the memory array, provided it is performed correctly. The MR3 register must be loaded when all banks are idle and no data bursts are in progress, and the controller must wait the specified time tMRD and tMOD before initiating a subsequent operation.



M17	M16	Mode Register
0	0	Mode register set (MR0)
0	1	Mode register set 1 (MR1)
1	0	Mode register set 2 (MR2)
1	1	Mode register set 3 (MR3)

M2	MPR Enable
0	Normal DRAM operations[2]
1	Dataflow from MPR

M1	M0	MPR READ Function
0	0	Predefined pattern[3]
0	1	Reserved
1	0	Reserved
1	1	Reserved

Figure 4-47: Mode Register 3 (MR3) Definition

NOTES:

1. MR3[18 and 15:3] are reserved for future use and must all be programmed to 0.
2. When MPR control is set for normal DRAM operation, MR3[1, 0] will be ignored.
3. Intended to be used for READ synchronization.

MULTIPURPOSE REGISTER (MPR)

The MULTIPURPOSE REGISTER (MPR) function is used to output a predefined system timing calibration bit sequence. Bit 2 is the master bit that enables or disables access to the MPR register, and bits 1 and 0 determine which mode the MPR is placed in. The basic concept of the multipurpose register is shown in Figure 4-48.

If MR3[2] = 0, then MPR access is disabled, and the DRAM operates in normal mode. However, if MR3[2] is a 1, then the DRAM no longer outputs normal read data but outputs MPR data as defined by MR3[0, 1]. If MR3[0, 1] is equal to 00, then a predefined read pattern for system calibration is selected.

To enable the MPR, the MRS command is issued to MR3, and MR3[2] = 1. Prior to issuing the MRS command, all banks must be in the idle state (all banks are precharged, and tRP is met). When the MPR is enabled, any subsequent READ or RDAP commands are redirected to the multipurpose register. The resulting operation when either a READ or RDAP command is issued, is defined by MR3[1:0] when the MPR is enabled (see Table 4-72). When the MPR is enabled, only READ or RDAP commands are allowed until a subsequent MRS command is issued with the MPR disabled (MR3[2] = 0). Power-down mode, self refresh, and any other non-READ/RDAP commands are not allowed during MPR enable mode. The RESET function is supported during MPR enable mode.

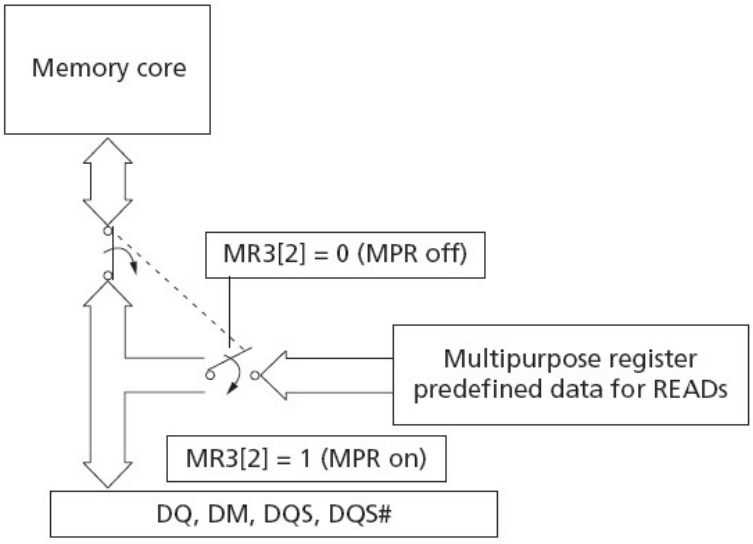


Figure 4-48: Multipurpose Register (MPR) Block Diagram

NOTES:

1. A predefined data pattern can be read out of the MPR with an external READ command.

2. MR3[2] defines whether the data flow comes from the memory core or the MPR. When the data flow is defined, the MPR

contents can be read out continuously with a regular READ or RDAP command.

Table 4-71: MPR Functional Description of MR3 Bits

MR3[2]	MR3[1:0]	Function
MPR	MPR READ Function	
0	"Don't Care"	Normal operation, no MPR transaction All subsequent READs come from the DRAM memory array
1	A[1:0] (see Table 4-72)	Enable MPR mode, subsequent READ/RDAP commands defined by bits 1 and 2

MPR Functional Description

The MPR JEDEC definition enables either a prime DQ to output the MPR data with the remaining DQ driven LOW, or all DQ to output the MPR data. The MPR readout supports fixed READ burst and READ burst chop (MRS and OTF via A12/BC#) with regular READ latencies and AC timings applicable, provided the DLL is locked as required.

MPR addressing for a valid MPR read is as follows:

- A[1:0] must be set to 00 as the burst order is fixed per nibble.
- A2 selects the burst order:
  - BL8, A2 is set to 0, and the burst order is fixed to 0, 1, 2, 3, 4, 5, 6, 7.
- For burst chop 4 cases, the burst order is switched on the nibble base along with the following:
  - A2 = 0; burst order = 0, 1, 2, 3
  - A2 = 1; burst order = 4, 5, 6, 7
- Burst order bit 0 (the first bit) is assigned to LSB, and burst order bit 7 (the last bit) is assigned to MSB.
- A[9:3] are "Don't Care".
- A10 is "Don't Care".
- A11 is "Don't Care".
- A12: Selects burst chop mode on-the-fly, if enabled within MR0.
- A13 is a "Don't Care".
- BA[2:0] are "Don't Care".

MPR Register Address Definitions and Bursting Order

The MPR currently supports a single data format. This data format is a predefined read pattern for system calibration. The predefined pattern is always a repeating 0– 1 bit pattern.

Examples of the different types of predefined READ pattern bursts are shown in the following figures.

Table 4-72: MPR Readouts and Burst Order Bit Mapping

MR3[2]	MR3[1:0]	Function	Burst Length	Read A[2:0]	Burst Order and Data Pattern
1	00	READ predefined pattern for system calibration	BL8	000	Burst order: 0, 1, 2, 3, 4, 5, 6, 7 Predefined pattern: 0, 1, 0, 1, 0, 1, 0, 1
			BC4	000	Burst order: 0, 1, 2, 3 Predefined pattern: 0, 1, 0, 1
			BC4	100	Burst order: 4, 5, 6, 7 Predefined pattern: 0, 1, 0, 1
1	01	RFU	N/A	N/A	N/A
			N/A	N/A	N/A
			N/A	N/A	N/A
1	10	RFU	N/A	N/A	N/A
			N/A	N/A	N/A
			N/A	N/A	N/A
1	11	RFU	N/A	N/A	N/A
			N/A	N/A	N/A
			N/A	N/A	N/A

Note:

1. Burst order bit 0 is assigned to LSB, and burst order bit 7 is assigned to MSB of the selected MPR agent.

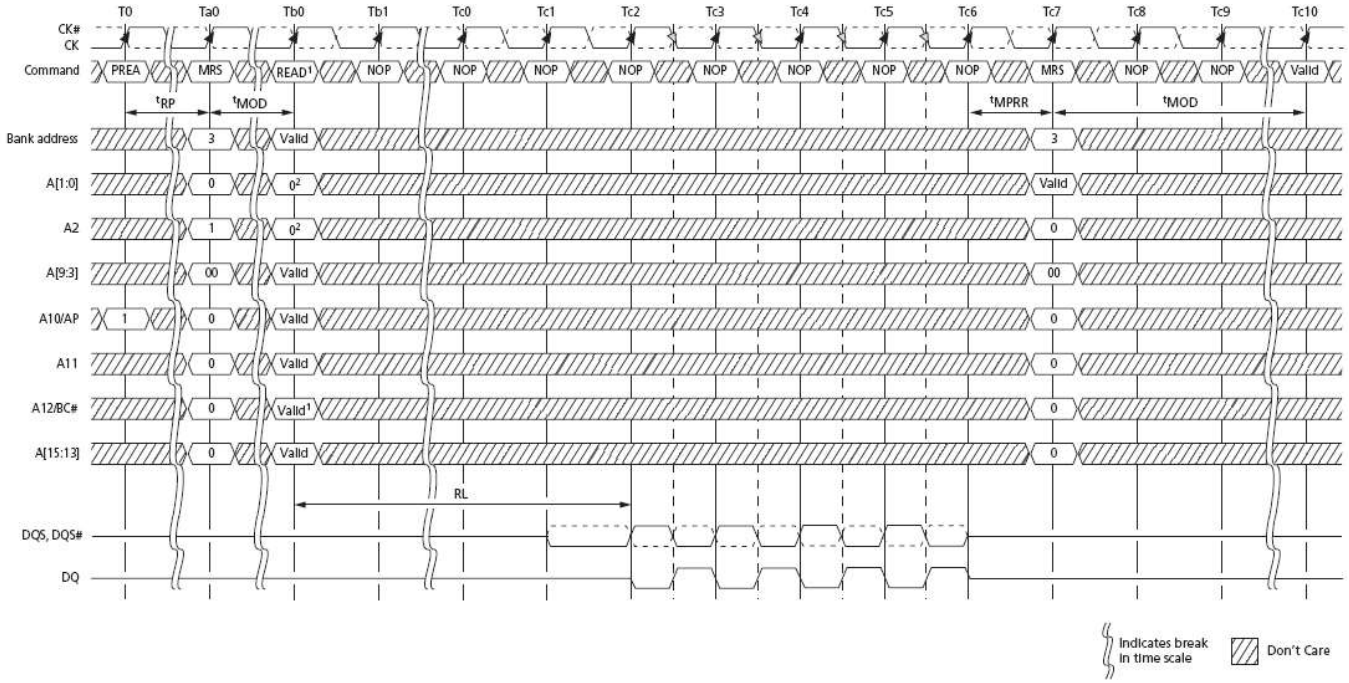


Figure 4-49: MPR System Read Calibration with BL8: Fixed Burst Order Single Readout

NOTES:

1. READ with BL8 either by MRS or OTF.

2. Memory controller must drive 0 on A[2:0].

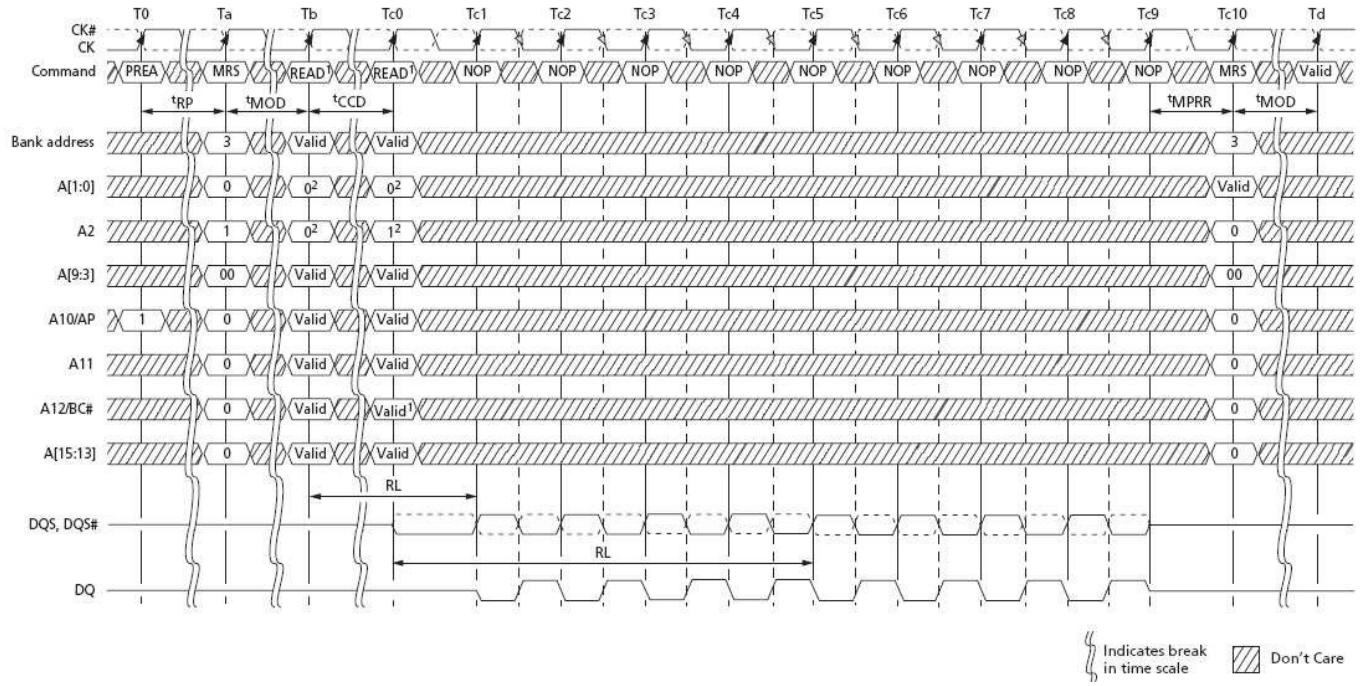


Figure 4-50: MPR System Read Calibration with BL8: Fixed Burst Order, Back-to-Back Readout

NOTES:

1. READ with BL8 either by MRS or OTF.

2. Memory controller must drive 0 on A[2:0].

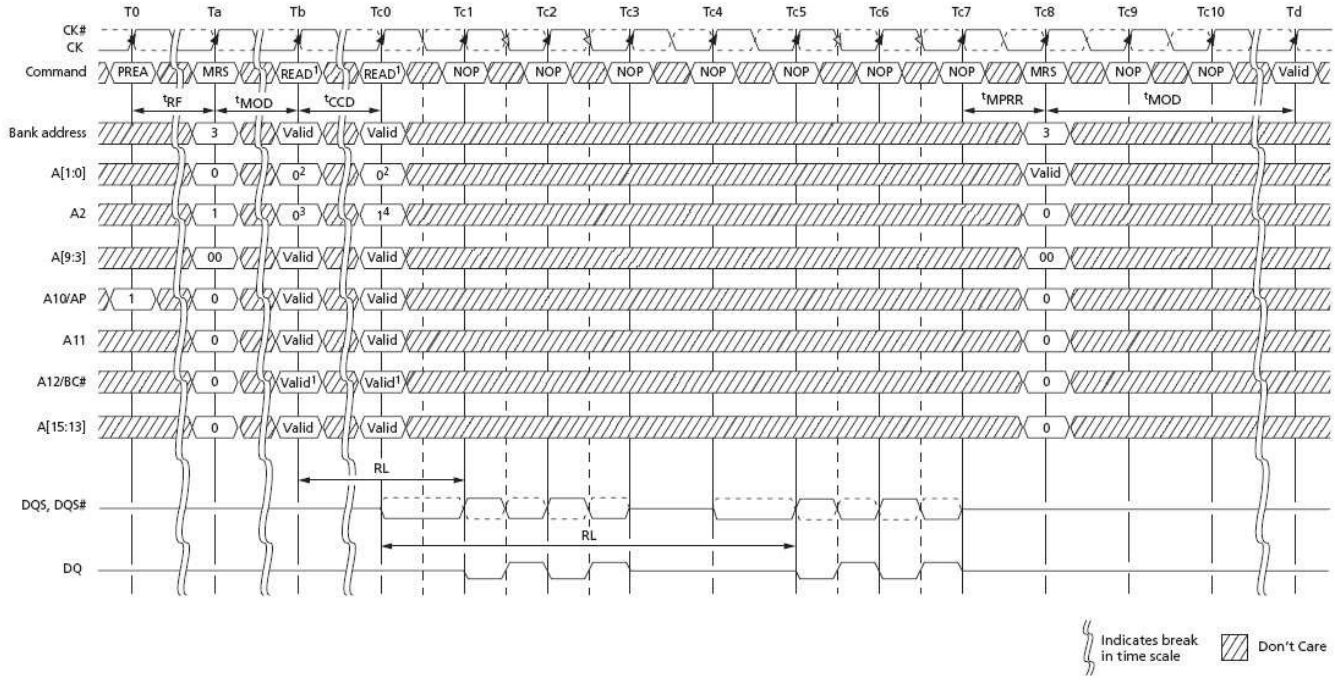


Figure 4-51: MPR System Read Calibration with BC4: Lower Nibble, Then Upper Nibble

NOTES:

1. READ with BC4 either by MRS or OTF.
2. Memory controller must drive 0 on A[1:0].
3. A2 = 0 selects lower 4 nibble bits 0 . . . 3.
4. A2 = 1 selects upper 4 nibble bits 4 . . . 7.

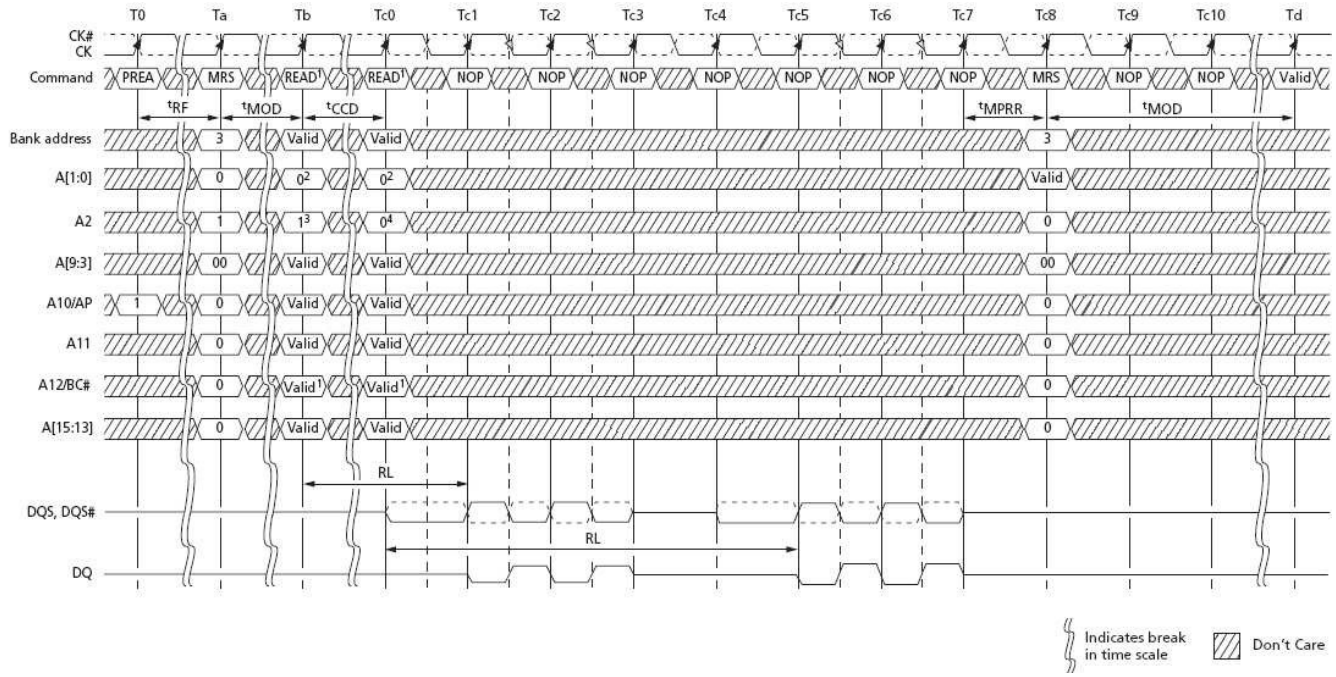


Figure 4-52: MPR System Read Calibration with BC4: Upper Nibble, Then Lower Nibble

NOTES:

1. READ with BC4 either by MRS or OTF.
2. Memory controller must drive 0 on A[1:0].
3. A2 = 1 selects upper 4 nibble bits 4 . . . 7.
4. A2 = 0 selects lower 4 nibble bits 0 . . . 3.

MPR Read Predefined Pattern

The predetermined read calibration pattern is a fixed pattern of 0, 1, 0, 1, 0, 1, 0, 1. The following is an example of using the predetermined read calibration pattern. The example is to perform multiple reads from the multipurpose register to do system level read timing calibration based on the predetermined standard pattern.

The following protocol outlines the steps used to perform the read calibration:

1. Precharge all banks.
2. After tRP is satisfied, set MRS, MR3[2] = 1 and MR3[1:0] = 00. This redirects all subsequent reads and loads the predefined pattern into the MPR. As soon as tMRD and tMOD are satisfied, the MPR is available.
3. Data WRITE operations are not allowed until the MPR returns to the normal DRAM state.
4. Issue a read with burst order information (all other address pins are “Don’t Care”):
   - A[1:0] = 00 (data burst order is fixed starting at nibble)
   - A2 = 0 (for BL8, burst order is fixed as 0, 1, 2, 3, 4, 5, 6, 7)
   - A12 = 1 (use BL8)
5. After RL = AL + CL, the DRAM bursts out the predefined read calibration pattern (01010101).
6. The memory controller repeats the calibration reads until read data capture at memory controller is optimized.
7. After the last MPR READ burst and after tMPRR has been satisfied, issue MRS, MR3[2] = 0, and MR3[1:0] = “Don’t Care” to the normal DRAM state. All subsequent read and write accesses will be regular reads and writes from/to the DRAM array.
8. When tMRD and tMOD are satisfied from the last MRS, the regular DRAM commands (such as activating a memory bank for regular read or write access) are permitted.

MODE REGISTER SET (MRS) Command

The mode registers are loaded via inputs BA[2:0], A[13:0]. BA[2:0] determine which mode register is programmed:

• BA2 = 0, BA1 = 0, BA0 = 0 for MR0.

• BA2 = 0, BA1 = 0, BA0 = 1 for MR1.

• BA2 = 0, BA1 = 1, BA0 = 0 for MR2.

• BA2 = 0, BA1 = 1, BA0 = 1 for MR3.

The MRS command can only be issued (or re-issued) when all banks are idle and in the precharged state (tRP is satisfied and no data bursts are in progress). The controller must wait the specified time tMRD before initiating a subsequent operation such as an ACTIVATE command (see Figure 4-39). There is also a restriction after issuing an MRS command with regard to when the updated functions become available. This parameter is specified by tMOD. Both tMRD and tMOD parameters are shown in Figure 4-39 and Figure 4-40. Violating either of these requirements will result in unspecified operation.

ZQ CALIBRATION Operation

The ZQ CALIBRATION command is used to calibrate the DRAM output drivers (R_{ON}) and ODT values (R_{TT}) over process, voltage, and temperature, provided a dedicated 240Ω (±1%) external resistor is connected from the DRAM's ZQ ball to V_{SSQ}.

DDR3(L) SDRAM require a longer time to calibrate R_{ON} and ODT at power-up initialization and self refresh exit, and a relatively shorter time to perform periodic calibrations. DDR3(L) SDRAM defines two ZQ CALIBRATION commands: ZQCL and ZQCS. An example of ZQ calibration timing is shown below.

All banks must be precharged and tRP must be met before ZQCL or ZQCS commands can be issued to the DRAM. No other activities (other than issuing another ZQCL or ZQCS command) can be performed on the DRAM channel by the controller for the duration of tZQinit or tZQoper. The quiet time on the DRAM channel helps accurately calibrate R_{ON} and ODT. After DRAM calibration is achieved, the DRAM should disable the ZQ ball's current consumption path to reduce power.

ZQ CALIBRATION commands can be issued in parallel to DLL RESET and locking time. Upon self refresh exit, an explicit ZQCL is required if ZQ calibration is desired.

In dual-rank systems that share the ZQ resistor between devices, the controller must not enable overlap of tZQinit, tZQoper, or tZQCS between ranks.

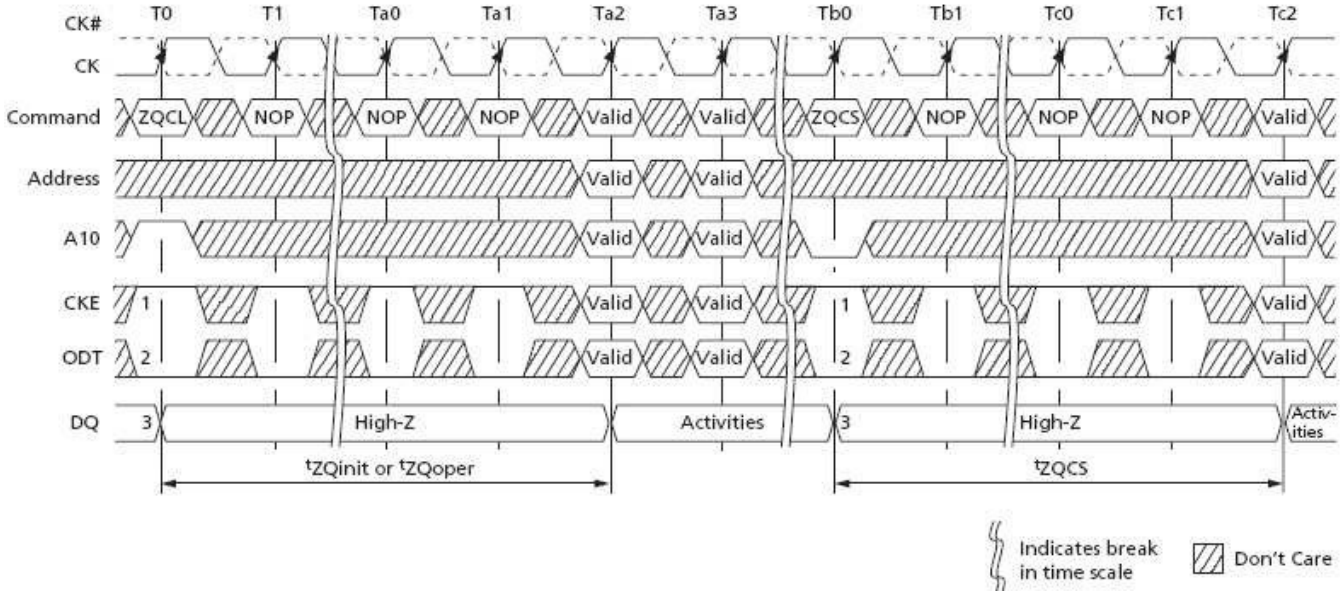


Figure 4-53: ZQ CALIBRATION Timing (ZQCL and ZQCS)

NOTES:

1. CKE must be continuously registered HIGH during the calibration procedure.
2. ODT must be disabled via the ODT signal or the MRS during the calibration procedure.
3. All devices connected to the DQ bus should be High-Z during calibration.

ACTIVATE Operation

Before any READ or WRITE commands can be issued to a bank within the DRAM, a row in that bank must be opened (activated). This is accomplished via the ACTIVATE command, which selects both the bank and the row to be activated.

After a row is opened with an ACTIVATE command, a READ or WRITE command may be issued to that row, subject to the tRCD specification. However, if the additive latency is programmed correctly, a READ or WRITE command may be issued prior to tRCD (MIN). In this operation, the DRAM enables a READ or WRITE command to be issued after the ACTIVATE command for that bank, but prior to tRCD (MIN) with the requirement that (ACTIVATE-to-READ/WRITE) + AL ≥ tRCD (MIN) (see Posted CAS Additive Latency). tRCD (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVATE command on which a READ or WRITE command can be entered. The same procedure is used to convert other specification limits from time units to clock cycles.

When at least one bank is open, any READ-to-READ command delay or WRITE-to-WRITE command delay is restricted to tCCD (MIN).

A subsequent ACTIVATE command to a different row in the same bank can only be issued after the previous active row has been closed (precharged). The minimum time interval between successive ACTIVATE commands to the same bank is defined by tRC.

A subsequent ACTIVATE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVATE commands to different banks is defined by tRRD. No more than four bank ACTIVATE commands may be issued in a given tFAW (MIN) period, and the tRRD (MIN) restriction still applies. The tFAW (MIN) parameter applies, regardless of the number of banks already opened or closed.

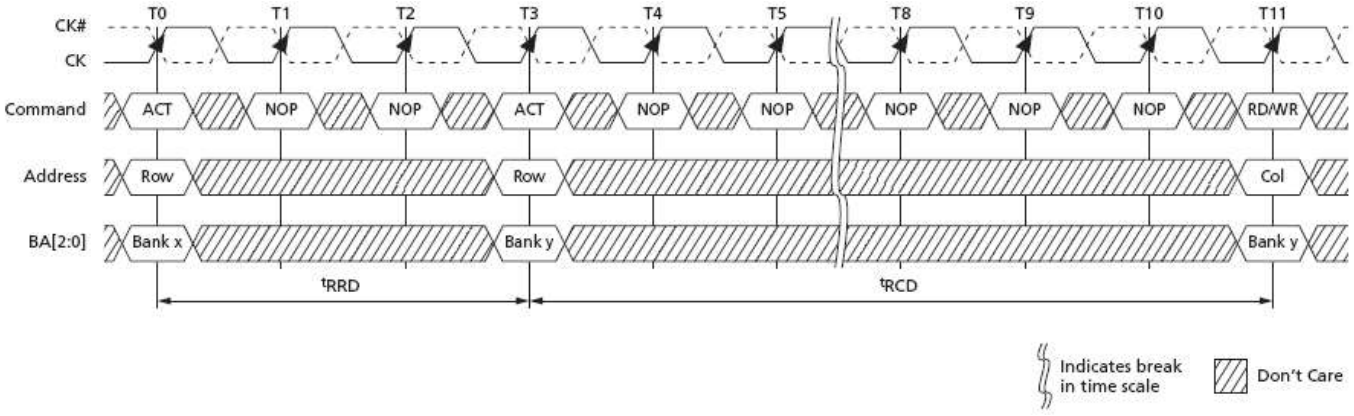


Figure 4-54: Example: Meeting tRRD (MIN) and tRCD (MIN)

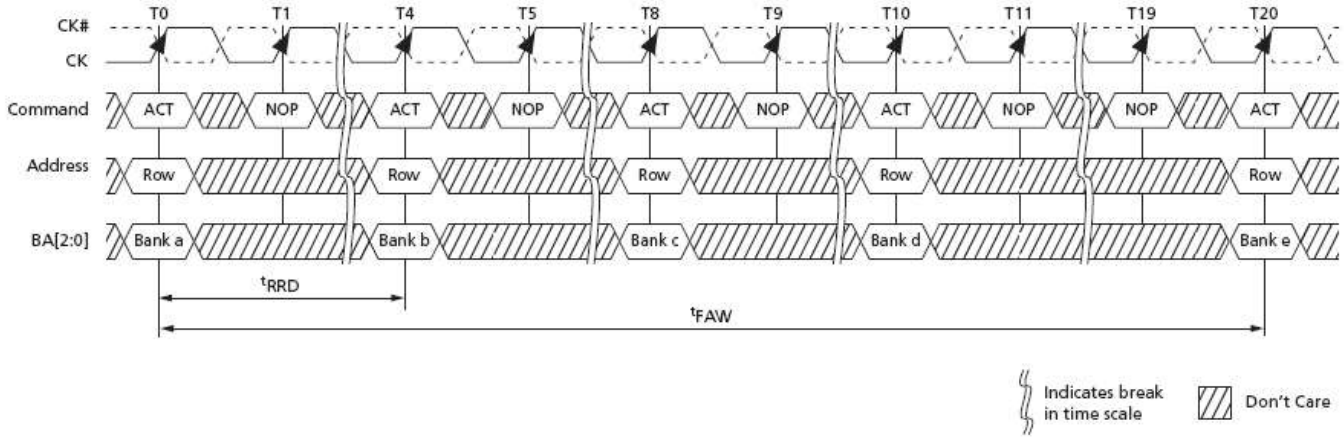


Figure 4-55: Example: tFAW

READ Operation

READ bursts are initiated with a READ command. The starting column and bank addresses are provided with the READ command and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is automatically precharged at the completion of the burst. If auto precharge is disabled, the row will be left open after the completion of the burst.

During READ bursts, the valid data-out element from the starting column address is available READ latency (RL) clocks later. RL is defined as the sum of posted CAS additive latency (AL) and CAS latency (CL) (RL = AL + CL). The value of AL and CL is programmable in the mode register via the MRS command. Each subsequent data-out element is valid nominally at the next positive or negative clock edge (that is, at the next crossing of CK and CK#). Figure 4-56 shows an example of RL based on a CL setting of 8 and an AL setting of 0.

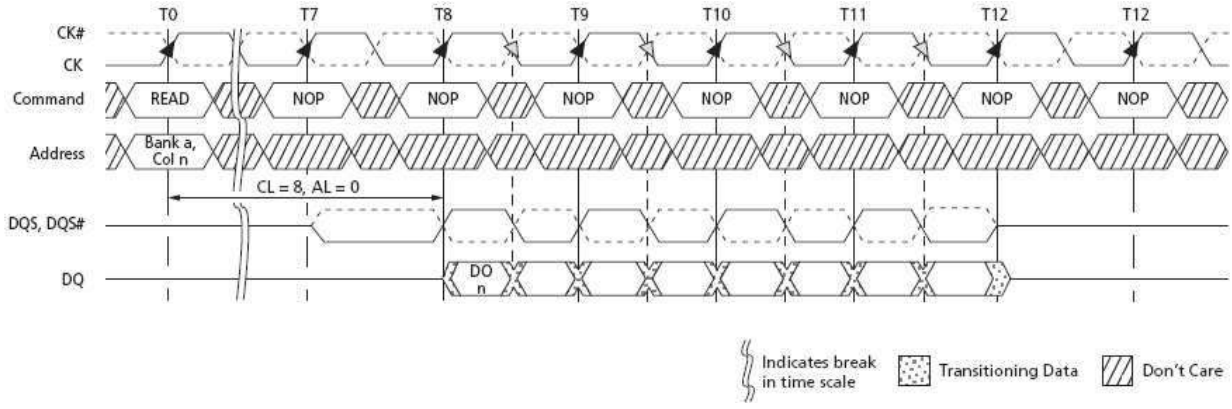


Figure 4-56: READ Latency

NOTES:

1. DO *n* = data-out from column *n*.
2. Subsequent elements of data-out appear in the programmed order following DO *n*.

DQS, DQS# is driven by the DRAM along with the output data. The initial LOW state on DQS and HIGH state on DQS# is known as the READ preamble (tRPRE). The LOW state on DQS and the HIGH state on DQS#, coincident with the last data-out element, is known as the READ postamble (tRPST). Upon completion of a burst, assuming no other commands have been initiated, the DQ goes High-Z. A detailed explanation of tDQSQ (valid data-out skew), tQH (data-out window hold), and the valid data window are depicted in Figure 4-67. A detailed explanation of tDQSCK (DQS transition skew to CK) is also depicted in Figure 4-67.

Data from any READ burst may be concatenated with data from a subsequent READ command to provide a continuous flow of data. The first data element from the new burst follows the last element of a completed burst. The new READ command should be issued tCCD cycles after the first READ command. This is shown for BL8 in Figure 4-57. If BC4 is enabled, tCCD must still be met, which will cause a gap in the data output, as shown in Figure 4-58. Nonconsecutive READ data is reflected in Figure 4-59. DDR3(L) SDRAM does not allow interrupting or truncating any READ burst.

Data from any READ burst must be completed before a subsequent WRITE burst is allowed. An example of a READ burst followed by a WRITE burst for BL8 is shown in Figure 4-60 (BC4 is shown in Figure 4-61). To ensure the READ data is completed before the WRITE data is on the bus, the minimum READ-to-WRITE timing is RL + tCCD - WL + 2tCK.

A READ burst may be followed by a PRECHARGE command to the same bank, provided auto precharge is not activated. The minimum READ-to-PRECHARGE command spacing to the same bank is four clocks and must also satisfy a minimum analog time from the READ command. This time is called tRTP (READ-to-PRECHARGE). tRTP starts AL cycles later than the READ command. Examples for BL8 are shown in Figure 4-62 and BC4 in Figure 4-63. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met. The PRECHARGE command followed by another PRECHARGE command to the same bank is allowed. However, the precharge period will be determined by the last PRECHARGE command issued to the bank.

If A10 is HIGH when a READ command is issued, the READ with auto precharge function is engaged. The DRAM starts an auto precharge operation on the rising edge, which is AL + tRTP cycles after the READ command. DRAM support a tRAS lockout feature (see Figure 4-65). If tRAS (MIN) is not satisfied at the edge, the starting point of the auto precharge operation will be delayed until tRAS (MIN) is satisfied. If tRTP (MIN) is not satisfied at the edge, the starting point of the auto precharge operation is delayed until tRTP (MIN) is satisfied. In case the internal precharge is pushed out by tRTP, tRP starts at the point at which the internal precharge happens (not at the next rising clock edge after this event). The time from READ with auto precharge to the next ACTIVATE command to the same bank is AL + (tRTP + tRP)*, where * means rounded up to the next integer. In any event, internal precharge does not start earlier than four clocks after the last 8*n*-bit prefetch.

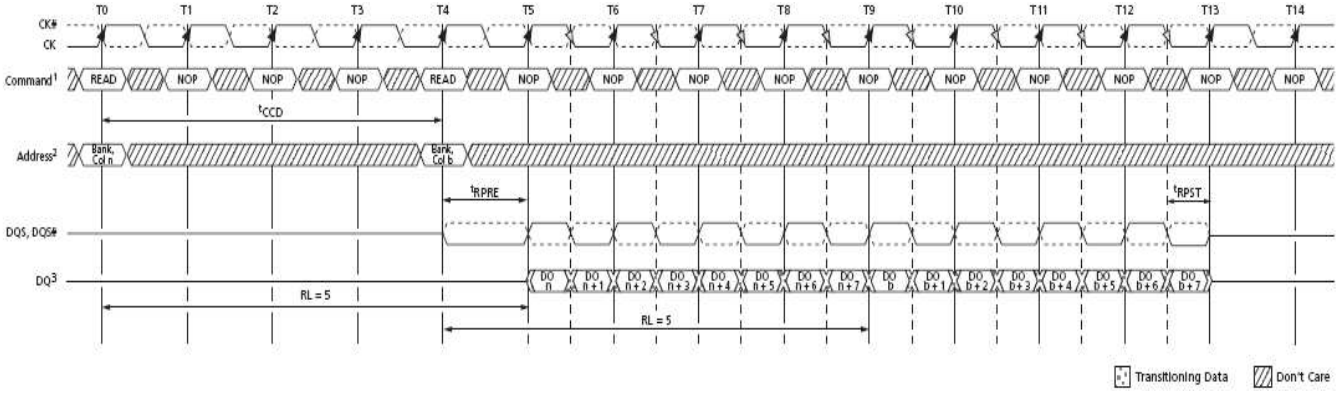


Figure 4-57: Consecutive READ Bursts (BL8)

NOTES:

1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. The BL8 setting is activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ command at T0 and T4.
3. DO *n* (or *b*) = data-out from column *n* (or column *b*).
4. BL8, RL = 5 (CL = 5, AL = 0).

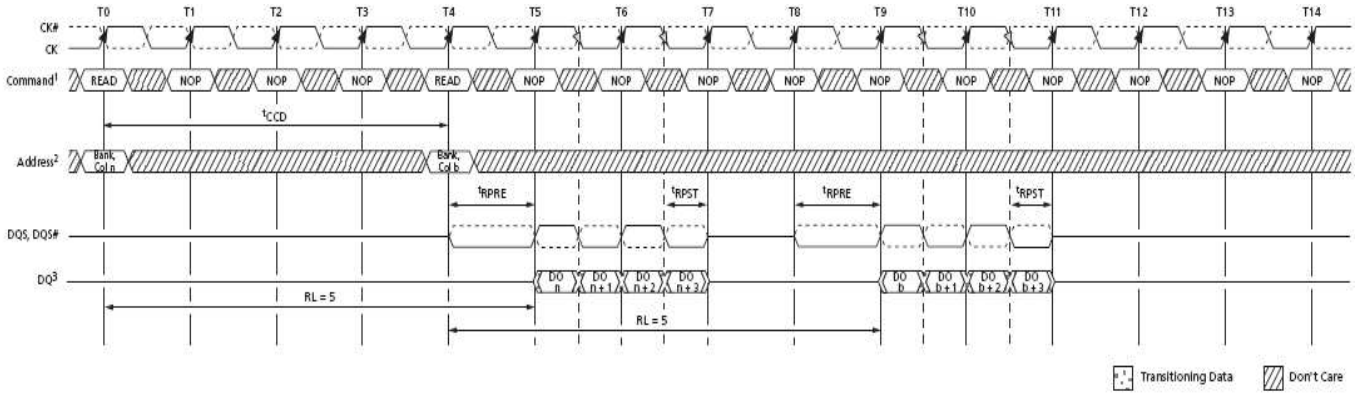


Figure 4-58: Consecutive READ Bursts (BC4)

NOTES:

1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. The BC4 setting is activated by either MR0[1:0] = 10 or MR0[1:0] = 01 and A12 = 0 during READ command at T0 and T4.
3. DO *n* (or *b*) = data-out from column *n* (or column *b*).
4. BC4, RL = 5 (CL = 5, AL = 0).

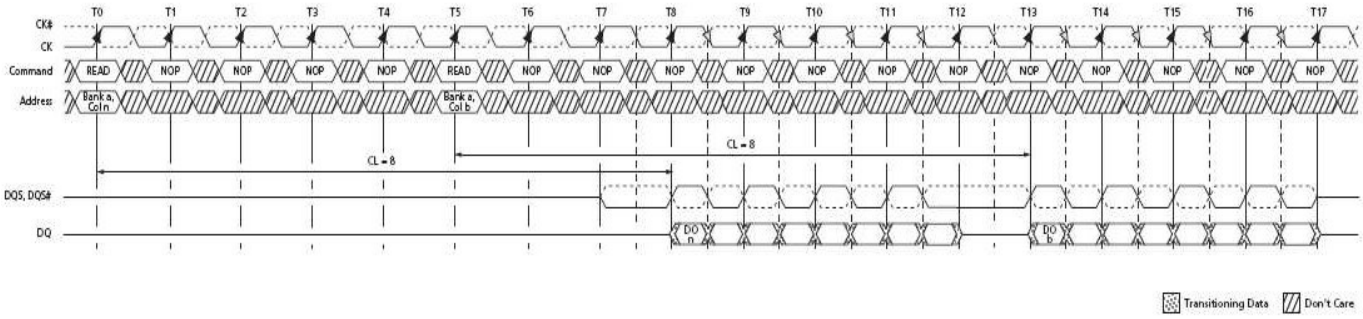


Figure 4-59: Nonconsecutive READ Bursts

Notes:

1. AL = 0, RL = 8.
2. DO *n* (or *b*) = data-out from column *n* (or column *b*).
3. Seven subsequent elements of data-out appear in the programmed order following DO *n*.
4. Seven subsequent elements of data-out appear in the programmed order following DO *b*.

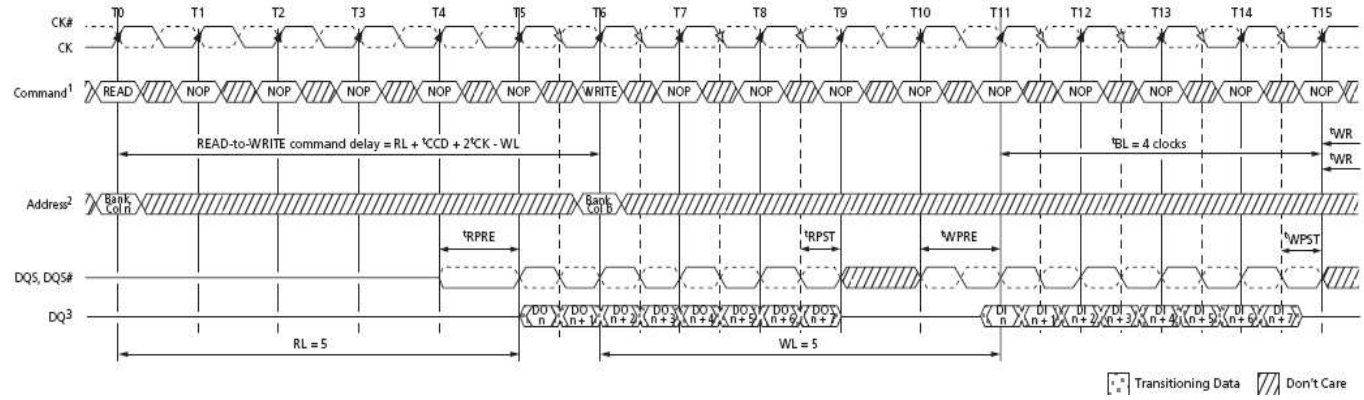


Figure 4-60: READ (BL8) to WRITE (BL8)

Notes:

1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. The BL8 setting is activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during the READ command at T0, and the WRITE command at T6.
3. DO *n* = data-out from column, DI *b* = data-in for column *b*.
4. BL8, RL = 5 (AL = 0, CL = 5), WL = 5 (AL = 0, CWL = 5).

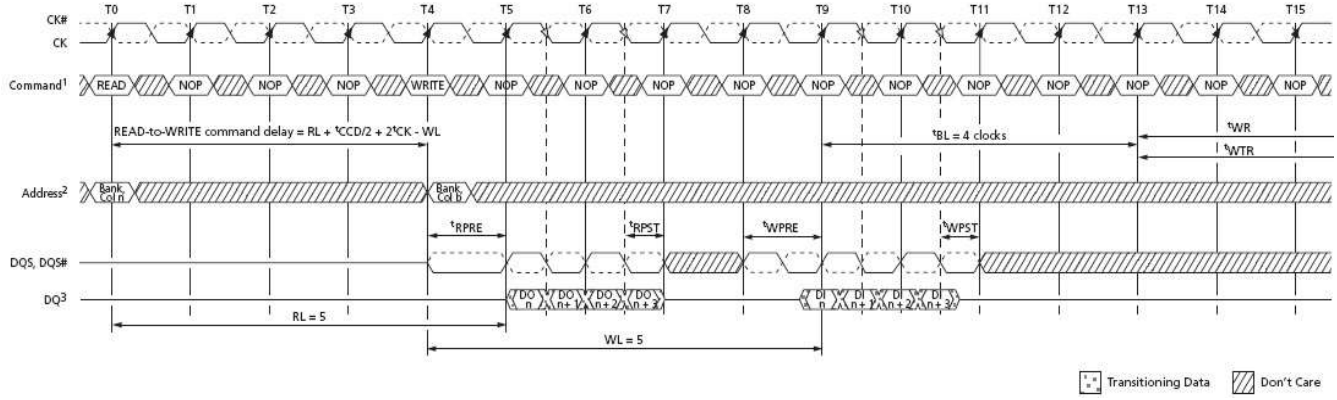


Figure 4-61: READ (BC4) to WRITE (BC4) OTF

Notes:

1. NOP commands are shown for ease of illustration; other commands may be valid at these times.

2. The BC4 OTF setting is activated by MR0[1:0] and A12 = 0 during READ command at T0 and WRITE command at T4.

3. DO *n* = data-out from column *n*; DI *n* = data-in from column *b*.

4. BC4, RL = 5 (AL - 0, CL = 5), WL = 5 (AL = 0, CWL = 5).

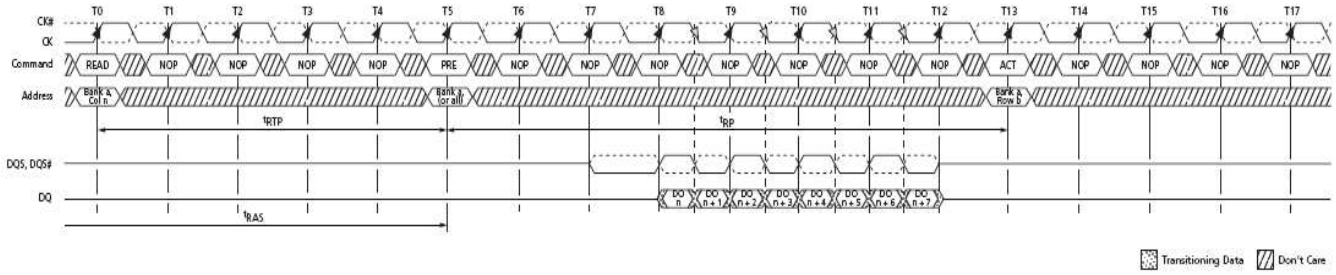


Figure 4-62: READ to PRECHARGE (BL8)

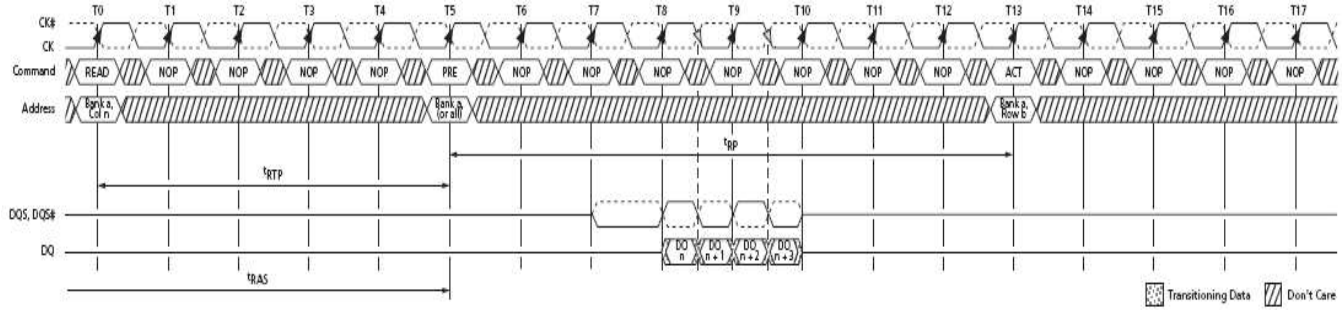


Figure 4-63: READ to PRECHARGE (BC4)

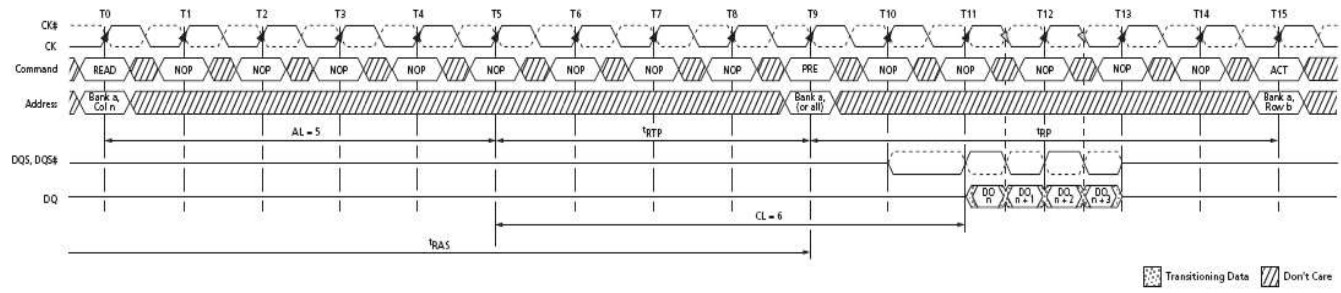


Figure 4-64: READ to PRECHARGE (AL = 5, CL = 6)

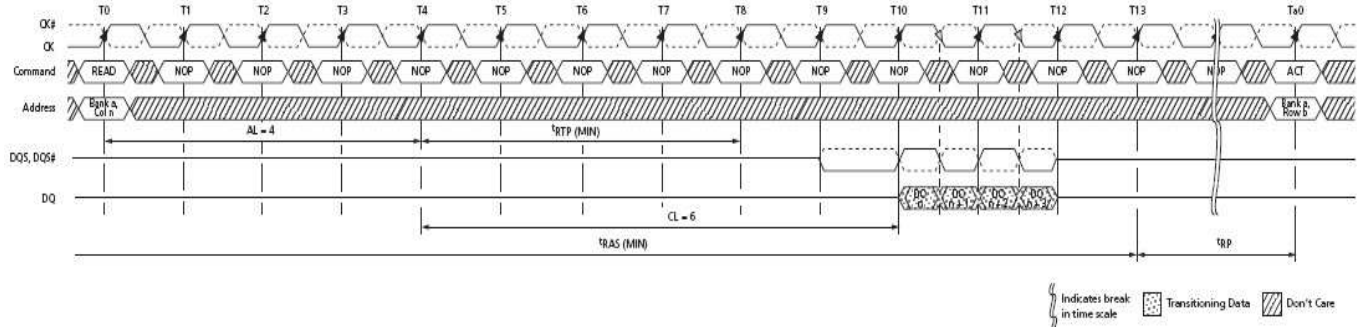


Figure 4-65: READ with Auto Precharge (AL = 4, CL = 6)

DQS to DQ output timing is shown in Figure 4-66. The DQ transitions between valid data outputs must be within tDQSQ of the crossing point of DQS, DQS#. DQS must also maintain a minimum HIGH and LOW time of tQSH and tQSL. Prior to the READ preamble, the DQ balls will either be floating or terminated, depending on the status of the ODT signal.

Figure 4-67 shows the strobe-to-clock timing during a READ. The crossing point DQS, DQS# must transition within ±tDQSCK of the clock crossing point. The data out has no timing relationship to CK, only to DQS, as shown in Figure4-67. Figure 4-67 also shows the READ preamble and postamble. Typically, both DQS and DQS# are High-Z to save power (V_{DDQ}). Prior to data output from the DRAM, DQS is driven LOW and DQS# is HIGH for tRPRE. This is known as the READ preamble.

The READ postamble, tRPST, is one half clock from the last DQS, DQS# transition. During the READ postamble, DQS is driven LOW and DQS# is HIGH. When complete, the DQ is disabled or continues terminating, depending on the state of the ODT signal. Figure 4-70 demonstrates how to measure tRPST.

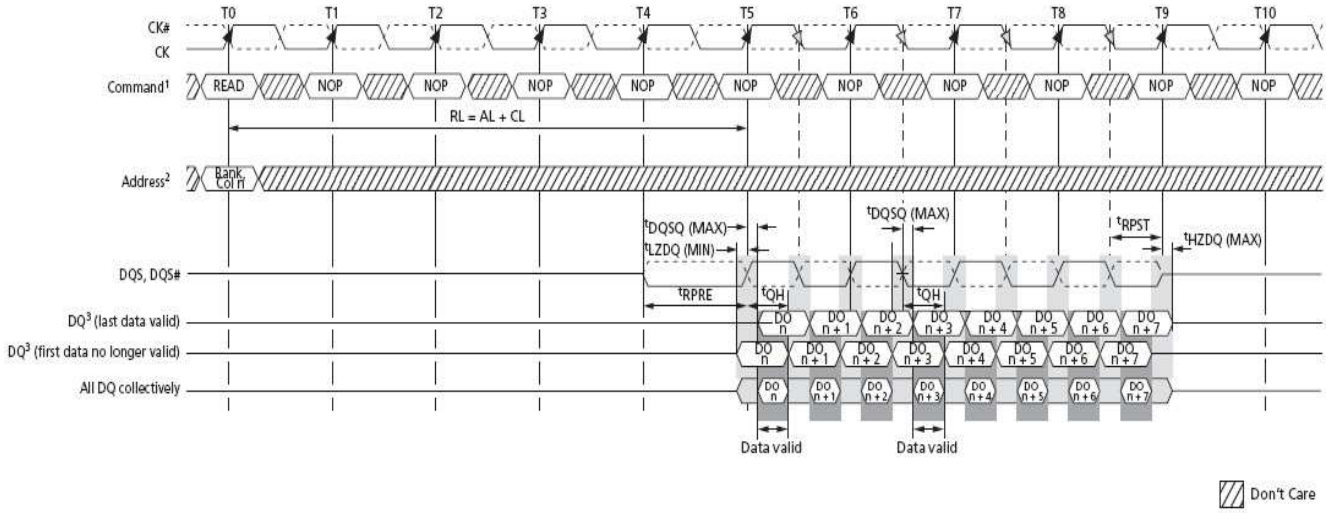


Figure 4-66: Data Output Timing – tDQSQ and Data Valid Window

Notes:

1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. The BL8 setting is activated by either MR0[1, 0] = 0, 0 or MR0[0, 1] = 0, 1 and A12 = 1 during READ command at T0.
3. DO *n* = data-out from column *n*.
4. BL8, RL = 5 (AL = 0, CL = 5).
5. Output timings are referenced to $V_{DDQ}/2$ and DLL on and locked.
6. tDQSQ defines the skew between DQS, DQS# to data and does not define DQS, DQS# to CK.
7. Early data transitions may not always happen at the same DQ. Data transitions of a DQ can be early or late within a burst.

tHZ and tLZ transitions occur in the same access time as valid data transitions. These parameters are referenced to a specific voltage level that specifies when the device output is no longer driving tHZDQS and tHZDQ, or begins driving tLZDQS, tLZDQ. Figure4-68 shows a method of calculating the point when the device is no longer driving tHZDQS and tHZDQ, or begins driving tLZDQS, tLZDQ, by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. The parameters tLZDQS, tLZDQ, tHZDQS, and tHZDQ are defined as single-ended.

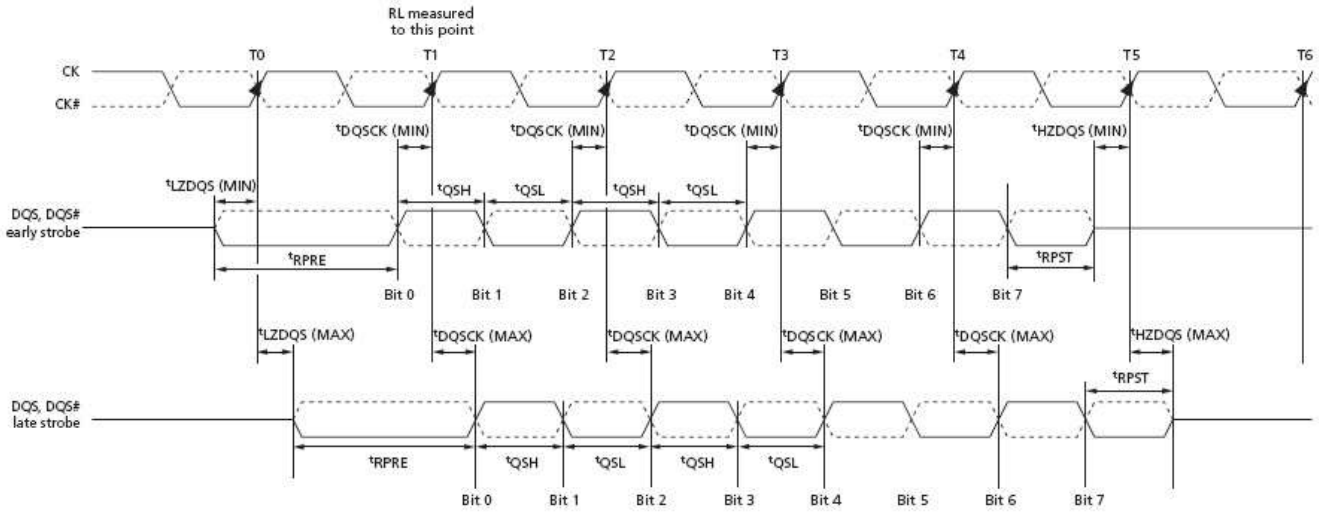


Figure 4-67: Data Strobe Timing – READs

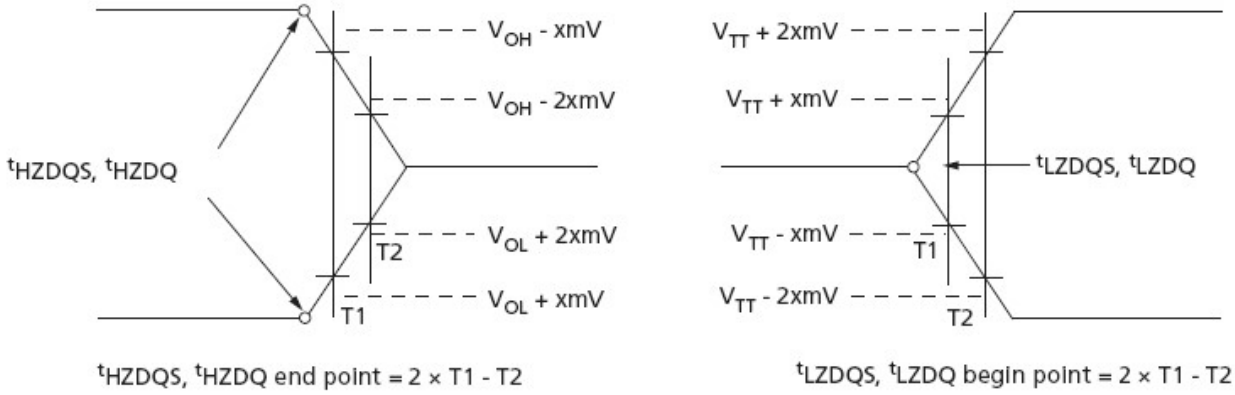


Figure 4-68: Method for Calculating tLZ and tHZ

Notes:

1. Within a burst, the rising strobe edge is not necessarily fixed at tDQSCK (MIN) or tDQSCK (MAX). Instead, the rising strobe edge can vary between tDQSCK (MIN) and tDQSCK (MAX).
2. The DQS HIGH pulse width is defined by tQSH, and the DQS LOW pulse width is defined by tQSL. Likewise, tLZDQS (MIN) and tHZDQS (MIN) are not tied to tDQSCK (MIN) (early strobe case), and tLZDQS (MAX) and tHZDQS (MAX) are not tied to tDQSCK (MAX) (late strobe case); however, they tend to track one another.
3. The minimum pulse width of the READ preamble is defined by tRPRE (MIN). The minimum pulse width of the READ postamble is defined by tRPST (MIN).

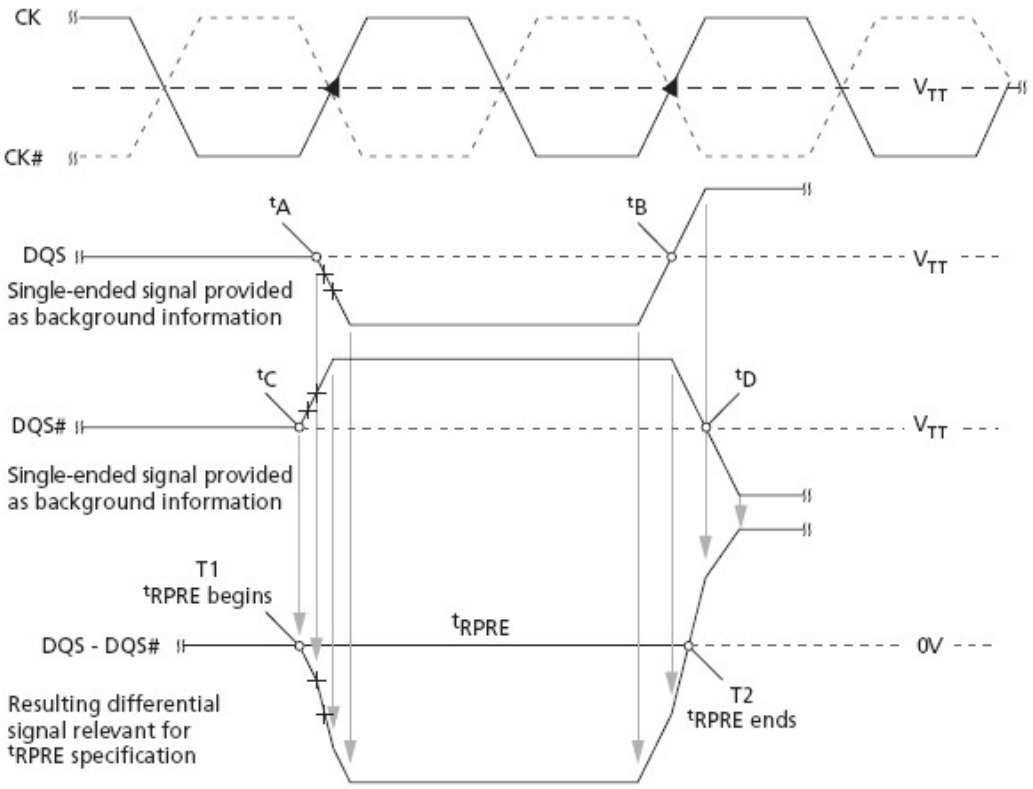


Figure 4-69: tRPRE Timing

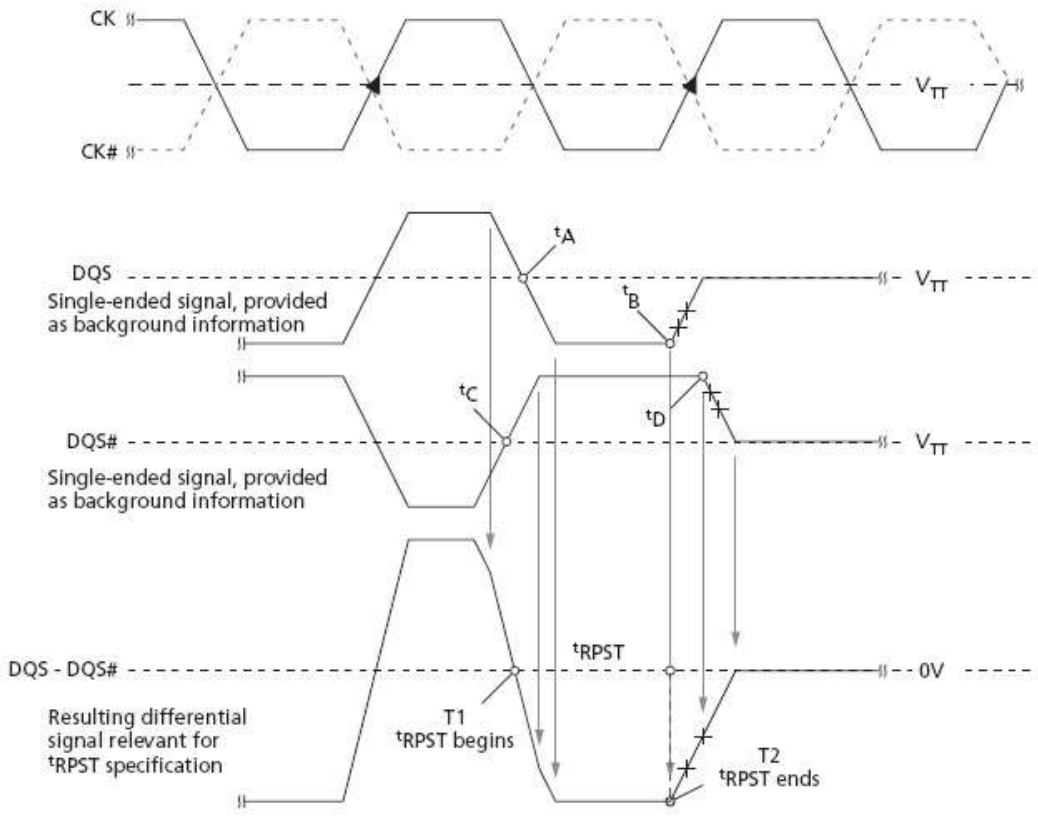


Figure 4-70: tRPST Timing

Write Operation

WRITE bursts are initiated with a WRITE command. The starting column and bank addresses are provided with the WRITE command, and auto precharge is either enabled or disabled for that access. If auto precharge is selected, the row being accessed is precharged at the end of the WRITE burst. If auto precharge is not selected, the row will remain open for subsequent accesses. After a WRITE command has been issued, the WRITE burst may not be interrupted. For the generic WRITE commands used in Figure 4-73 through Figure 4-81, auto precharge is disabled.

During WRITE bursts, the first valid data-in element is registered on a rising edge of DQS following the WRITE latency (WL) clocks later and subsequent data elements will be registered on successive edges of DQS. WRITE latency (WL) is defined as the sum of posted CAS additive latency (AL) and CAS WRITE latency (CWL): WL = AL + CWL. The values of AL and CWL are programmed in the MR0 and MR2 registers, respectively. Prior to the first valid DQS edge, a full cycle is needed (including a dummy crossover of DQS, DQS#) and specified as the WRITE preamble shown in Figure 4-73. The half cycle on DQS following the last data-in element is known as the WRITE postamble.

The time between the WRITE command and the first valid edge of DQS is WL clocks ±tDQSS. Figure 4-74 through Figure 4-81 show the nominal case where tDQSS = 0ns; however, Figure 4-73 includes tDQSS (MIN) and tDQSS (MAX) cases.

Data may be masked from completing a WRITE using data mask. The data mask occurs on the DM ball aligned to the WRITE data. If DM is LOW, the WRITE completes normally. If DM is HIGH, that bit of data is masked.

Upon completion of a burst, assuming no other commands have been initiated, the DQ will remain High-Z, and any additional input data will be ignored.

Data for any WRITE burst may be concatenated with a subsequent WRITE command to provide a continuous flow of input data. The new WRITE command can be tCCD clocks following the previous WRITE command. The first data element from the new burst is applied after the last element of a completed burst. Figure 4-74 and Figure 4-75 show concatenated bursts. An example of nonconsecutive WRITEs is shown in Figure 4-76.

Data for any WRITE burst may be followed by a subsequent READ command after tWTR has been met (see Figure4-77, Figure 4-78, and Figure 4-79).

Data for any WRITE burst may be followed by a subsequent PRECHARGE command, providing tWR has been met, as shown in Figure 4-80 and Figure 4-81. Both tWTR and tWR starting time may vary, depending on the mode register settings (fixed BC4, BL8 versus OTF).

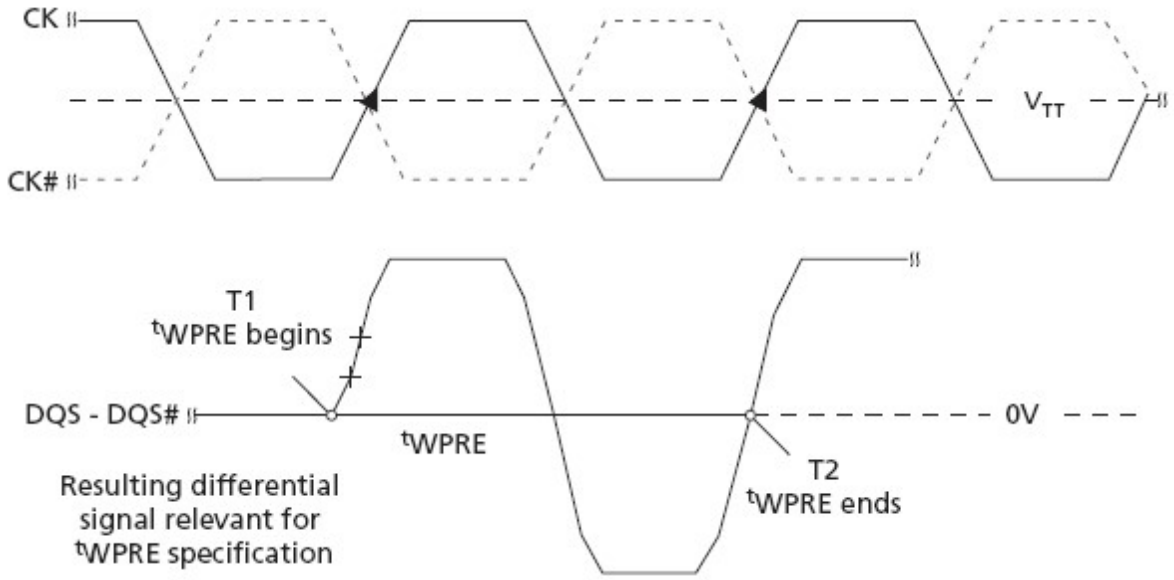


Figure 4-71: $_{t}$WPRE Timing

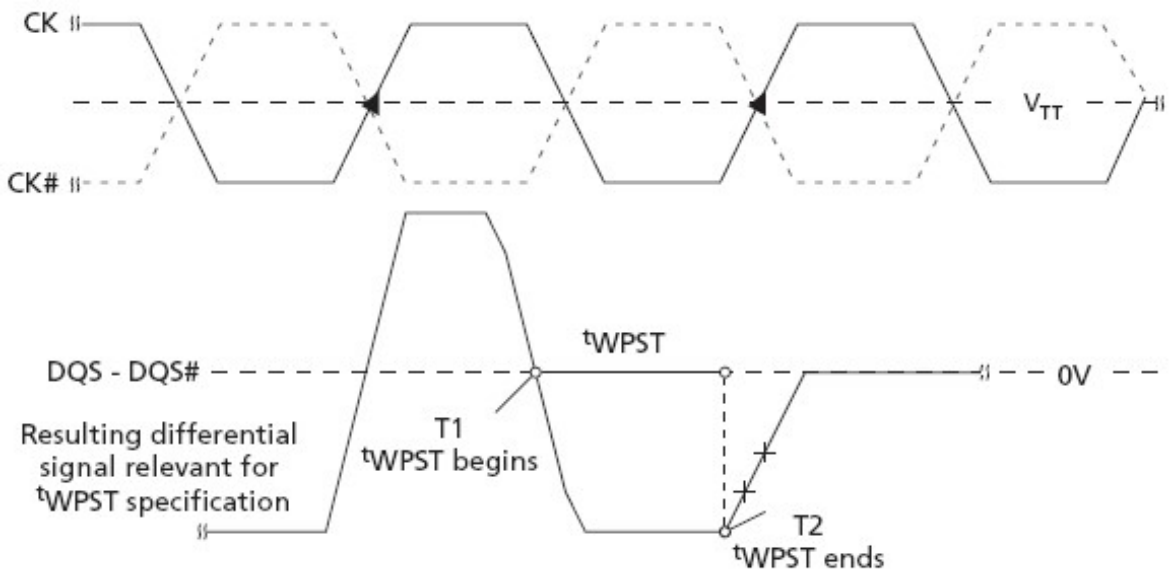


Figure 4-72: $_{t}$WPST Timing

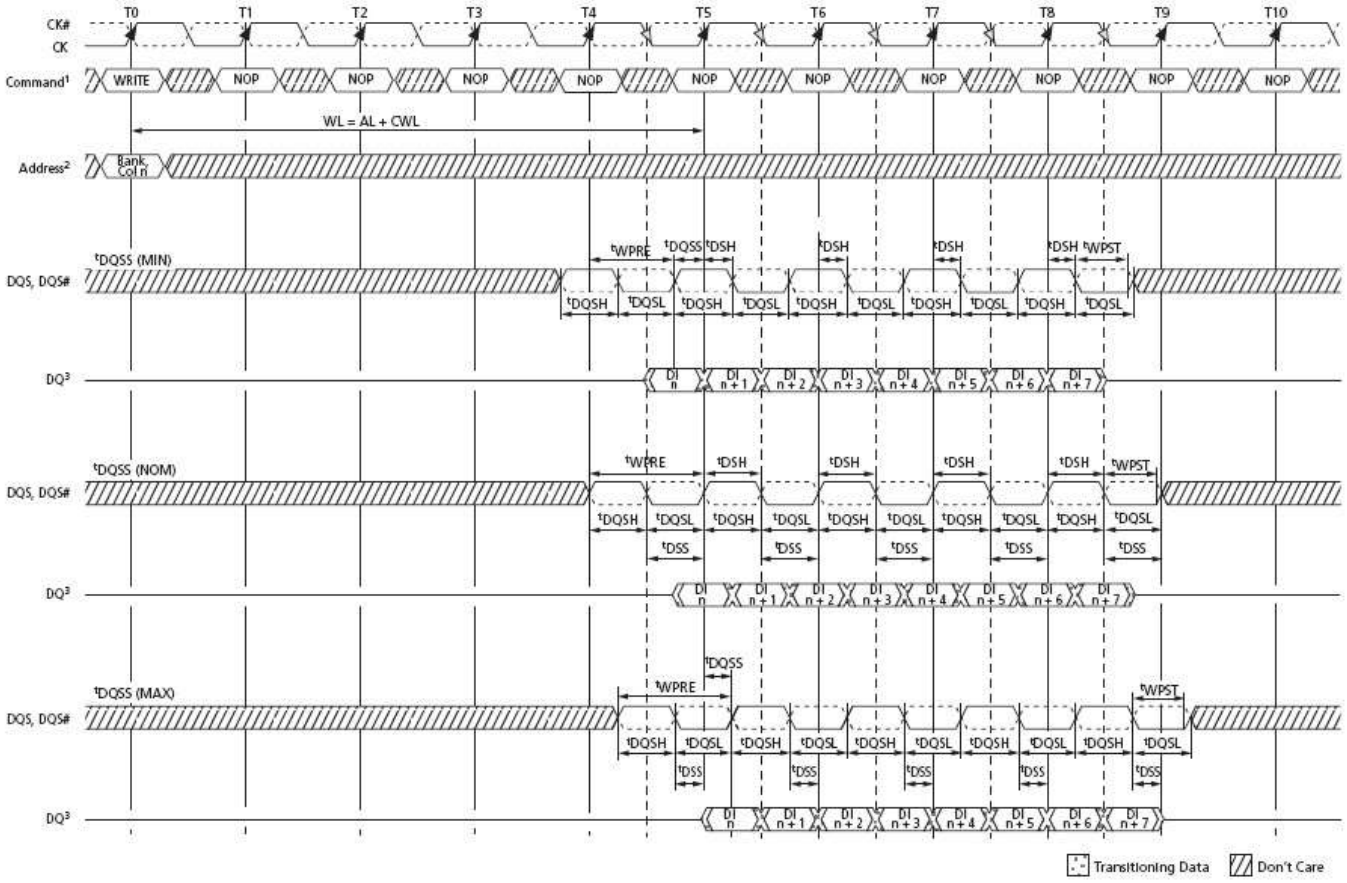


Figure 4-73: WRITE Burst

Notes:

1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. The BL8 setting is activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during the WRITE command at T0.
3. DI *n* = data-in for column *n*.
4. BL8, WL = 5 (AL = 0, CWL = 5).
5. tDQSS must be met at each rising clock edge.
6. tWPST is usually depicted as ending at the crossing of DQS, DQS#; however, tWPST actually ends when DQS no longer drives LOW and DQS# no longer drives HIGH.

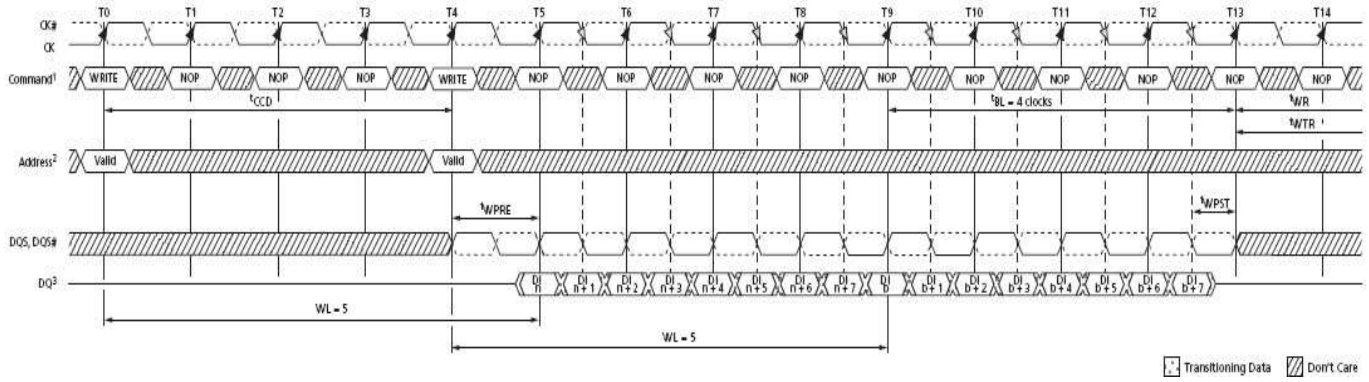


Figure 4-74: Consecutive WRITE (BL8) to WRITE (BL8)

Notes:

1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. The BL8 setting is activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during the WRITE commands at T0 and T4.
3. DI *n* (or b) = data-in for column *n* (or column *b*).
4. BL8, WL = 5 (AL = 0, CWL = 5).

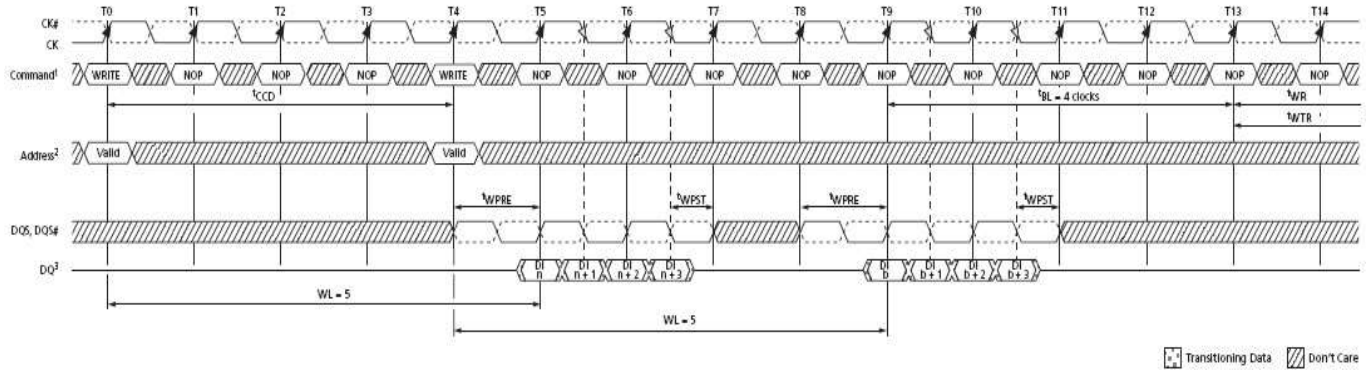


Figure 4-75: Consecutive WRITE (BC4) to WRITE (BC4) via OTF

Notes:

1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. BC4, WL = 5 (AL = 0, CWL = 5).
3. DI *n* (or *b*) = data-in for column *n* (or column *b*).
4. The BC4 setting is activated by MR0[1:0] = 01 and A12 = 0 during the WRITE command at T0 and T4.
5. If set via MRS (fixed) tWR and tWTR would start T11 (2 cycles earlier).

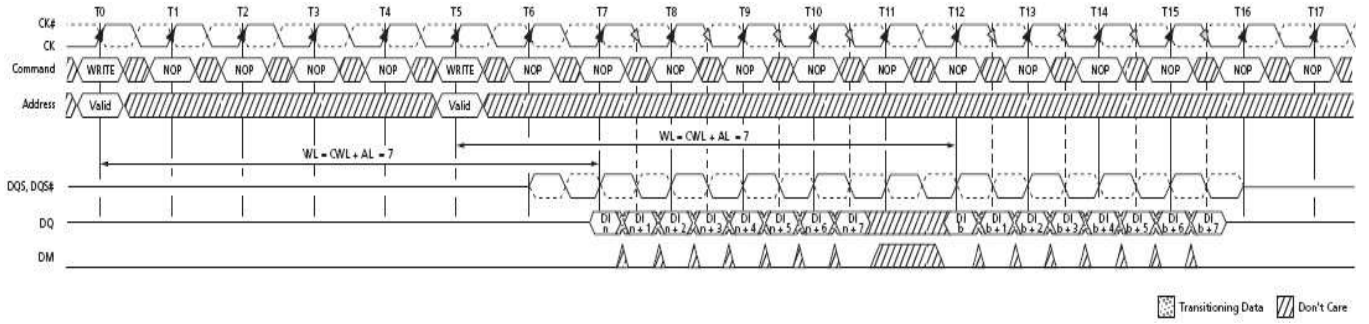


Figure 4-76: Nonconsecutive WRITE to WRITE

Notes:

1. DI *n* (or *b*) = data-in for column *n* (or column *b*).
2. Seven subsequent elements of data-in are applied in the programmed order following DO *n*.
3. Each WRITE command may be to any bank.
4. Shown for WL = 7 (CWL = 7, AL = 0).

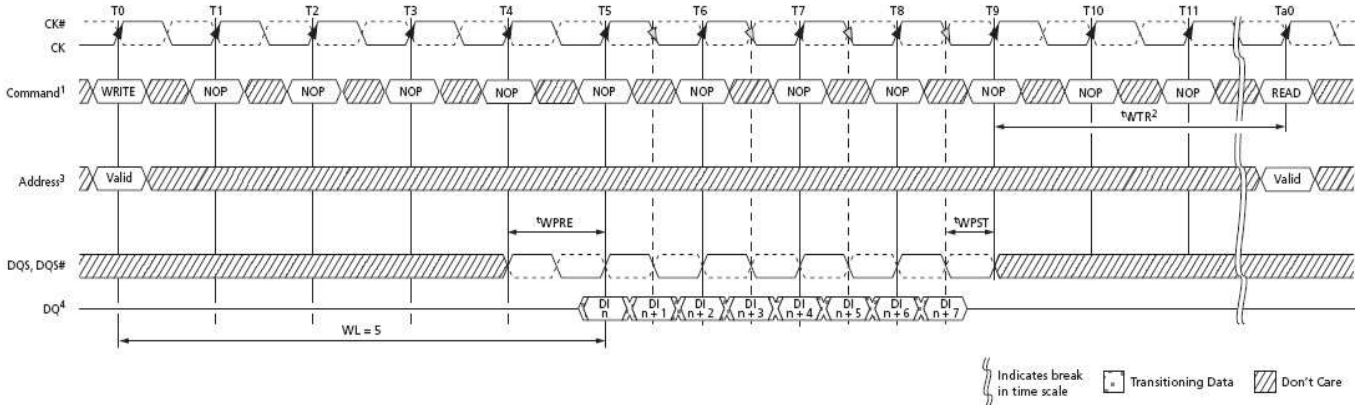


Figure 4-77: WRITE (BL8) to READ (BL8)

Notes:

1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. tWTR controls the WRITE-to-READ delay to the same device and starts with the first rising clock edge after the last write data shown at T9.
3. The BL8 setting is activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and MR0[12] = 1 during the WRITE command at T0. The READ command at Ta0 can be either BC4 or BL8, depending on MR0[1:0] and the A12 status at Ta0.
4. DI *n* = data-in for column *n*.
5. RL = 5 (AL = 0, CL = 5), WL = 5 (AL = 0, CWL = 5).

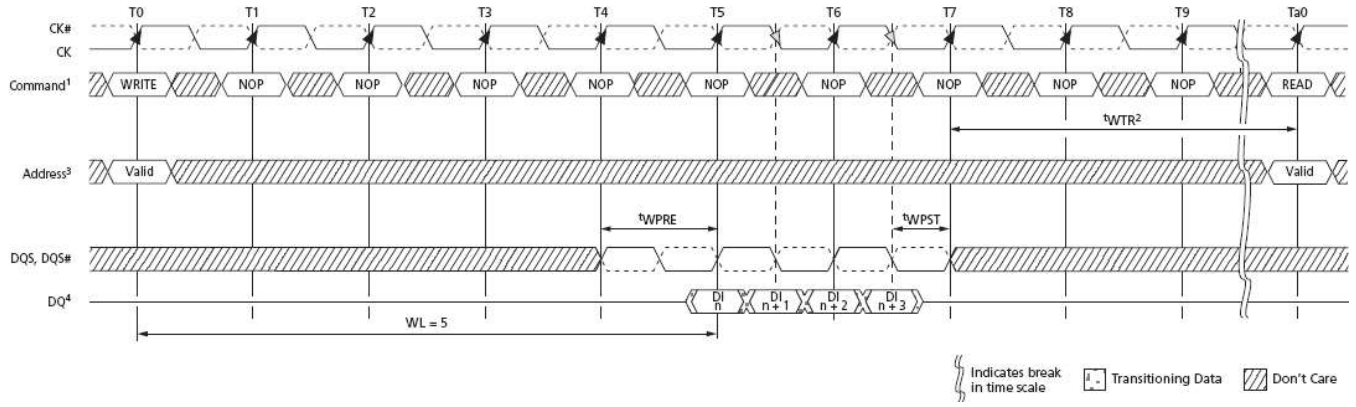


Figure 4-78: WRITE to READ (BC4 Mode Register Setting)

Notes:

1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. tWTR controls the WRITE-to-READ delay to the same device and starts with the first rising clock edge after the last write data shown at T7.
3. The fixed BC4 setting is activated by MR0[1:0] = 10 during the WRITE command at T0 and the READ command at Ta0.
4. DI *n* = data-in for column *n*.
5. BC4 (fixed), WL = 5 (AL = 0, CWL = 5), RL = 5 (AL = 0, CL = 5).

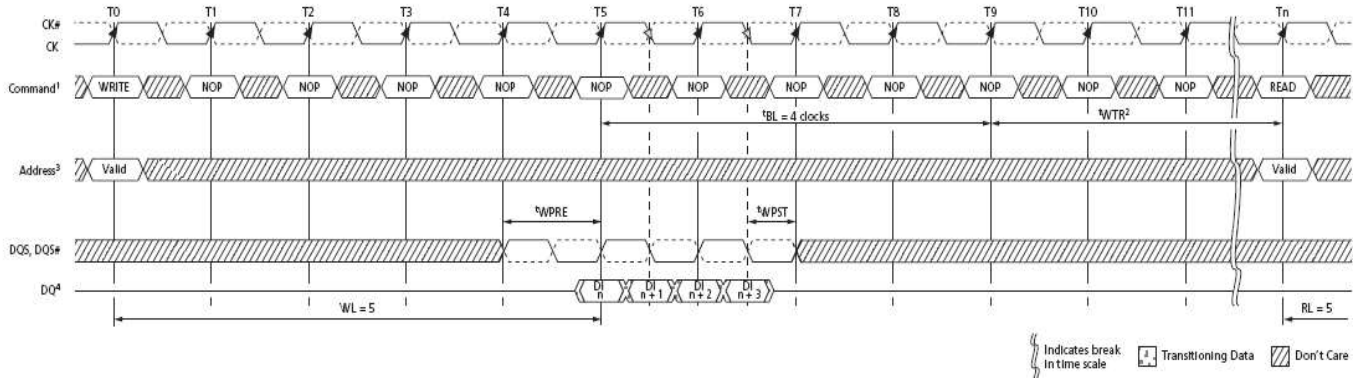


Figure 4-79: WRITE (BC4 OTF) to READ (BC4 OTF)

Notes:

1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. tWTR controls the WRITE-to-READ delay to the same device and starts after tBL.
3. The BC4 OTF setting is activated by MR0[1:0] = 01 and A12 = 0 during the WRITE command at T0 and the READ command atT*n*.
4. DI *n* = data-in for column *n*.
5. BC4, RL = 5 (AL = 0, CL = 5), WL = 5 (AL = 0, CWL = 5).

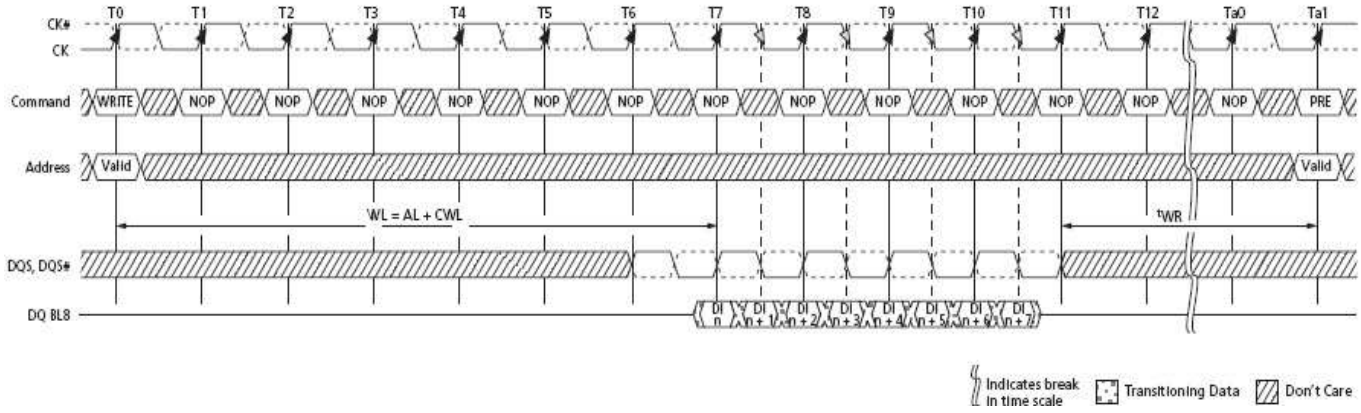


Figure 4-80: WRITE (BL8) to PRECHARGE

Notes:

1. DI *n* = data-in from column *n*.
2. Seven subsequent elements of data-in are applied in the programmed order following DO *n*.
3. Shown for WL = 7 (AL = 0, CWL = 7).

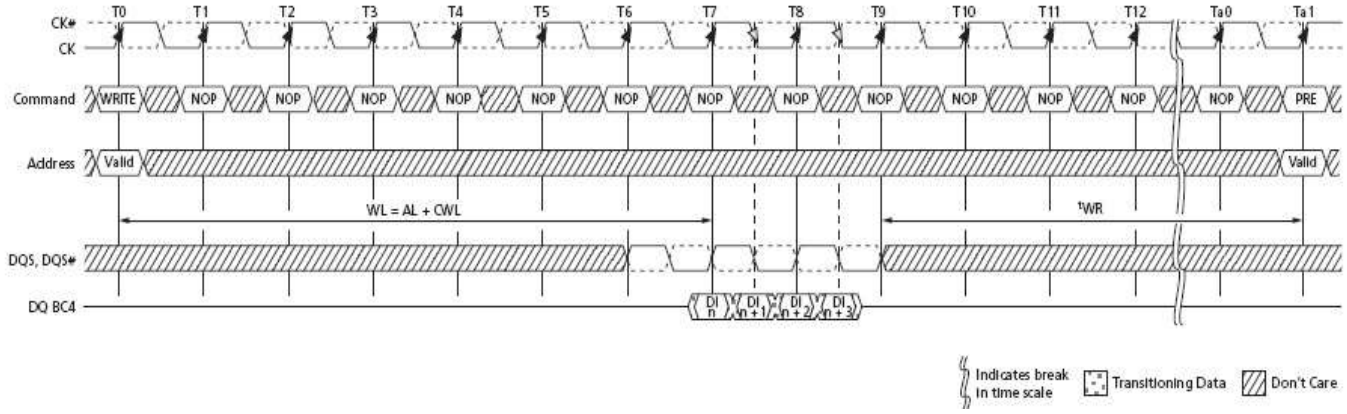


Figure 4-81: WRITE (BC4 Mode Register Setting) to PRECHARGE

Notes:

1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. The write recovery time (tWR) is referenced from the first rising clock edge after the last write data is shown at T7. tWR specifies the last burst WRITE cycle until the PRECHARGE command can be issued to the same bank.
3. The fixed BC4 setting is activated by MR0[1:0] = 10 during the WRITE command at T0.
4. DI *n* = data-in for column *n*.
5. BC4 (fixed), WL = 5, RL = 5.

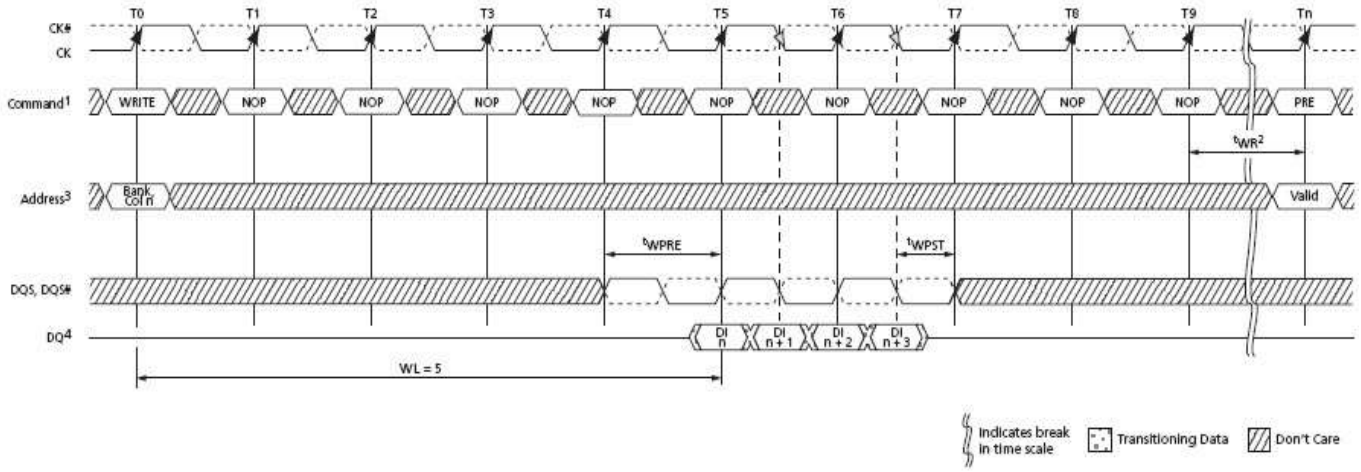


Figure 4-82: WRITE (BC4 OTF) to PRECHARGE

Notes:

1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. The write recovery time (tWR) is referenced from the rising clock edge at T9. tWR specifies the last burst WRITE cycle until the PRECHARGE command can be issued to the same bank.
3. The BC4 setting is activated by MR0[1:0] = 01 and A12 = 0 during the WRITE command at T0.
4. DI *n* = data-in for column *n*.
5. BC4 (OTF), WL = 5, RL = 5.

DQ Input Timing

Figure 4-73 shows the strobe-to-clock timing during a WRITE burst. DQS, DQS# must transition within 0.25tCK of the clock transitions, as limited by tDQSS. All data and data mask setup and hold timings are measured relative to the DQS, DQS# crossing, not the clock crossing.

The WRITE preamble and postamble are also shown in Figure 4-73. One clock prior to data input to the DRAM, DQS must be HIGH and DQS# must be LOW. Then for a half clock, DQS is driven LOW (DQS# is driven HIGH) during the WRITE preamble, tWPRE. Likewise, DQS must be kept LOW by the controller after the last data is written to the DRAM during the WRITE postamble, tWPST.

Data setup and hold times are also shown in Figure 4-73. All setup and hold times are measured from the crossing points of DQS and DQS#. These setup and hold values pertain to data input and data mask input.

Additionally, the half period of the data input strobe is specified by tDQSH and tDQSL.

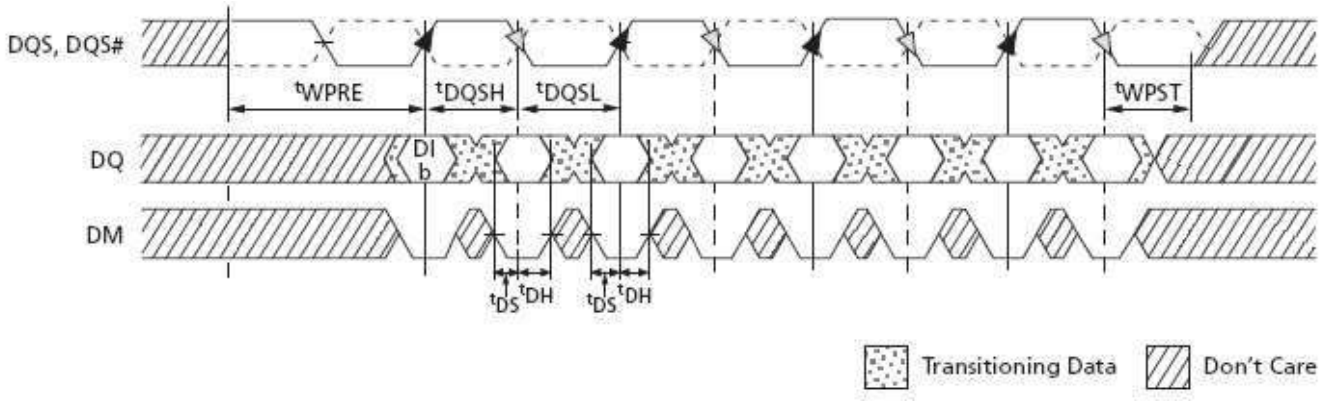


Figure 4-83: Data Input Timing

PRECHARGE Operation

Input A10 determines whether one bank or all banks are to be precharged and, in the case where only one bank is to be precharged, inputs BA[2:0] select the bank.

When all banks are to be precharged, inputs BA[2:0] are treated as “Don’t Care” After a bank is precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued.

SELF REFRESH Operation

The SELF REFRESH operation is initiated like a REFRESH command except CKE is LOW. The DLL is automatically disabled upon entering SELF REFRESH and is automatically enabled and reset upon exiting SELF REFRESH.

All power supply inputs (including V_{REFCA} and V_{REFDQ}) must be maintained at valid levels upon entry/exit and during self refresh mode operation. V_{REFDQ} may float or not drive $V_{DDQ}/2$ while in self refresh mode under certain conditions:

- V_{SS} < V_{REFDQ} < V_{DD} is maintained.
- V_{REFDQ} is valid and stable prior to CKE going back HIGH.
- The first WRITE operation may not occur earlier than 512 clocks after V_{REFDQ} is valid.
- All other self refresh mode exit timing requirements are met.

The DRAM must be idle with all banks in the precharge state (tRP is satisfied and no bursts are in progress) before a self refresh entry command can be issued. ODT must also be turned off before self refresh entry by registering the ODT ball LOW prior to the self refresh entry command (see section: On-Die Termination (ODT) (for timing requirements)). If $R_{TT,nom}$ and $R_{TT(WR)}$ are disabled in the mode registers, ODT can be a “Don’t Care” After the self refresh entry command is registered, CKE must be held LOW to keep the DRAM in self refresh mode.

After the DRAM has entered self refresh mode, all external control signals, except CKE and RESET#, are “Don’t Care” The DRAM initiates a minimum of one REFRESH command internally within the tCKE period when it enters self refresh mode.

The requirements for entering and exiting self refresh mode depend on the state of the clock during self refresh mode. First and foremost, the clock must be stable (meeting tCK specifications) when self refresh mode is entered. If the clock remains stable and the frequency is not altered while in self refresh mode, then the DRAM is allowed to exit self refresh mode after tCKESR is satisfied (CKE is allowed to transition HIGH tCKESR later than when CKE was registered LOW). Since the clock remains stable in self refresh mode (no frequency change), tCKSRE and tCKSRX are not required. However, if the clock is altered during self refresh mode (if it is turned-off or its frequency changes), then tCKSRE and tCKSRX must be satisfied. When entering self refresh mode, tCKSRE must be satisfied prior to altering the clock's frequency. Prior to exiting self refresh mode, tCKSRX must be satisfied prior to registering CKE HIGH.

When CKE is HIGH during self refresh exit, NOP or DES must be issued for tXS time. tXS is required for the completion of any internal refresh already in progress and must be satisfied before a valid command not requiring a locked DLL can be issued to the device. tXS is also the earliest time self refresh re-entry may occur. Before a command requiring a locked DLL can be applied, a ZQCL command must be issued, tZQOPER timing must be met, and tXSDLL must be satisfied. ODT must be off during tXSDLL.

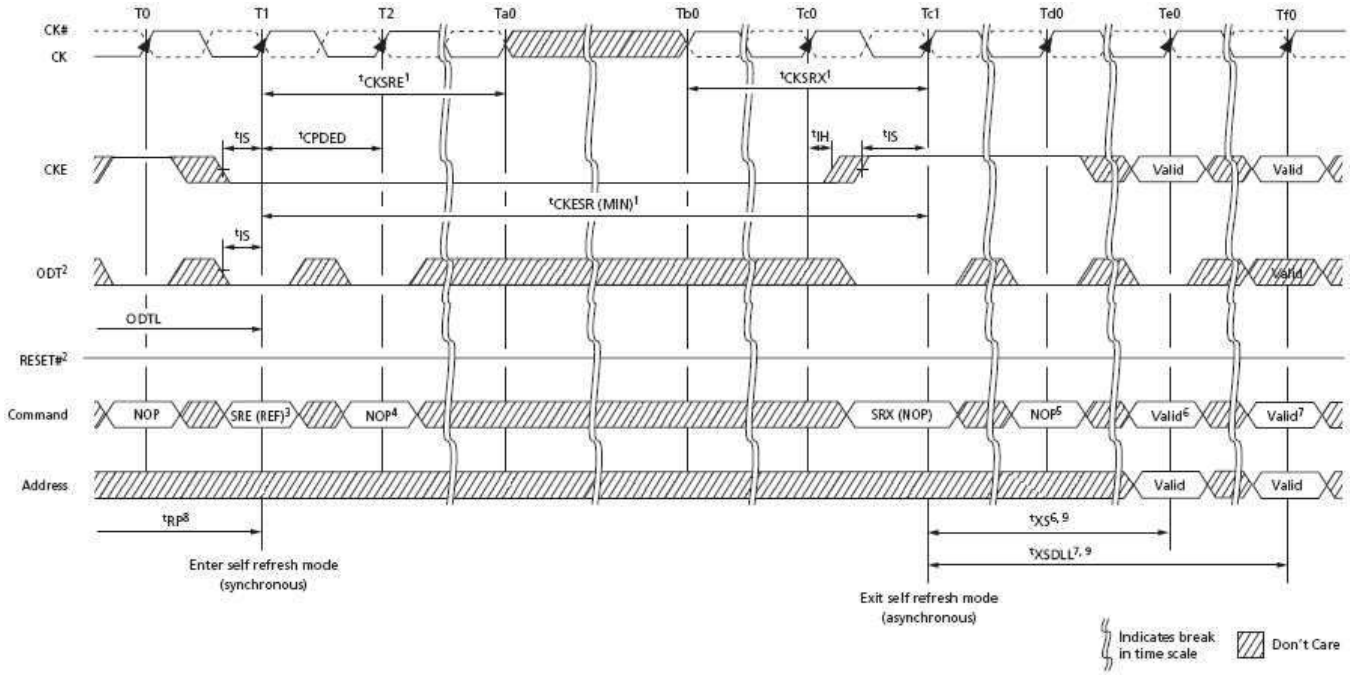


Figure 4-84: Self Refresh Entry/Exit Timing

Notes:

1. The clock must be valid and stable, meeting tCK specifications at least tCKSRE after entering self refresh mode, and at least tCKSRX prior to exiting self refresh mode, if the clock is stopped or altered between states Ta0 and Tb0. If the clock remains valid and unchanged from entry and during self refresh mode, then tCKSRE and tCKSRX do not apply; however, tCKESR must be satisfied prior to exiting at SRX.
2. ODT must be disabled and R_{TT} off prior to entering self refresh at state T1. If both $R_{TT,nom}$ and $R_{TT(WR)}$ are disabled in the mode registers, ODT can be a “Don’t Care”.
3. Self refresh entry (SRE) is synchronous via a REFRESH command with CKE LOW.
4. A NOP or DES command is required at T2 after the SRE command is issued prior to the inputs becoming “Don’t Care”.
5. NOP or DES commands are required prior to exiting self refresh mode until state Te0.
6. tXS is required before any commands not requiring a locked DLL.
7. tXSDLL is required before any commands requiring a locked DLL.
8. The device must be in the all banks idle state prior to entering self refresh mode. For example, all banks must be precharged, tRP must be met, and no data bursts can be in progress.
9. Self refresh exit is asynchronous; however, tXS and tXSDLL timings start at the first rising clock edge where CKE HIGH satisfies tISXR at Tc1. tCKSRX timing is also measured so that tISXR is satisfied at Tc1.

Extended Temperature Usage

DDR3(L) SDRAM support the optional extended case temperature (T_C) range of -10℃ to 95℃. Thus, the SRT and ASR options must be used at a minimum.

The extended temperature range DRAM must be refreshed externally at 2x (double refresh) anytime the case temperature is above 85℃ (and does not exceed 95℃). The external refresh requirement is accomplished by reducing the refresh period from 64ms to 32ms. However, self refresh mode requires either ASR or SRT to support the extended temperature. Thus, either ASR or SRT must be enabled when T_C is above 85℃ or self refresh cannot be used until T_C is at or below 85℃. Table 4-73 summarizes the two extended temperature options and Table 4-74 summarizes how the two extended temperature options relate to one another.

Table 4-73: Self Refresh Temperature and Auto Self Refresh Description

Field	MR2 Bits	Description
Self Refresh Temperature (SRT)		
SRT	7	If ASR is disabled (MR2[6]= 0), SRT must be programmed to indicate T_{OPER} during self refresh: *MR2[7]= 0: Normal operating temperature range (-10℃ to 85℃) *MR2[7]= 1: Extended operating temperature range (-10℃ to 95℃) If ASR is enabled (MR2[7]= 1), SRT must be set to 0, even if the extended temperature range is
Auto Self Refresh (ASR)		
ASR	6	When ASR is enabled, the DRAM automatically provides SELF REFRESH power management functions, (refresh rate for all supported operating temperature values) *MR2[6] = 1: ASR is enabled (M7 must = 0) When ASR is not enabled, the SRT bit must be programmed to indicate T_{OPER} during SELF REFRESH

Table 4-74: Self Refresh Mode Summary

MR2[6] (ASR)	MR2[7] (SRT)	SELF REFRESH Operation	Permitted Operating Temperature Range for Self Refresh Mode
0	0	Self refresh mode is supported in the normal temperature range	Normal (-10℃ to 85℃)
0	1	Self refresh mode is supported in normal and extended temperature ranges; When SRT is enabled, it increases self	Normal and extended (-10℃ to 95℃)
1	0	Self refresh mode is supported in normal and extended temperature ranges; Self refresh power consumption may be	Normal and extended (-10℃ to 95℃)
1	1	Illegal	

Power-Down Mode

Power-down is synchronously entered when CKE is registered LOW coincident with a NOP or DES command. CKE is not allowed to go LOW while an MRS, MPR, ZQCAL, READ, or WRITE operation is in progress. CKE is allowed to go LOW while any of the other legal operations (such as ROW ACTIVATION, PRECHARGE, auto precharge, or REFRESH) are in progress. However, the power-down I_{DD} specifications are not applicable until such operations have completed. Depending on the previous DRAM state and the command issued prior to CKE going LOW, certain timing constraints must be satisfied (as noted in Table 4-75). Timing diagrams detailing the different power-down mode entry and exits are shown in Figure 4-85 through Figure 4-94.

Table 4-75: Command to Power-Down Entry Parameters

DRAM Status	Last Command Prior to CKE LOW[1]	Parameter (Min)	Parameter Value	Figure
Idle or active	ACTIVATE	tACTPDEN	1tCK	Figure 4-92
Idle or active	PRECHARGE	tPRPDEN	1tCK	Figure 4-93
Active	READ or READAP	tRDPDEN	RL + 4tCK + 1tCK	Figure 4-88
Active	WRITE: BL8OTF,BL8MRS,BC4OTF	tWRPDEN	WL + 4tCK + tWR/tCK	Figure 4-89
Active	WRITE: BC4MRS		WL + 2tCK + tWR/tCK	Figure 4-89
Active	WRITEAP:BL8OTF,BL8MRS,BC4OTF	tWRAPDEN	WL + 4tCK + WR + 1tCK	Figure 4-90
Active	WRITEAP: BC4MRS		WL + 2tCK + WR + 1tCK	Figure 4-90
Idle	REFRESH	tREFPDEN	1tCK	Figure 4-91
Power-down	REFRESH	tXPDLL	Greater of 10tCK or 24ns	Figure 4-95
Idle	MODE REGISTER SET	tMRSPDEN	tMOD	Figure 4-94

Note:

1. If slow-exit mode precharge power-down is enabled and entered, ODT becomes asynchronous tANPD prior to CKE going LOW and remains asynchronous until tANPD + tXPDLL after CKE goes HIGH.

Entering power-down disables the input and output buffers, excluding CK, CK#, ODT,CKE, and RESET#. NOP or DES commands are required until tCPDED has been satisfied, at which time all specified input/output buffers are disabled. The DLL should be in a locked state when power-down is entered for the fastest power-down exit timing. If the DLL is not locked during power-down entry, the DLL must be reset after exiting power-down mode for proper READ operation as well as synchronous ODT operation.

During power-down entry, if any bank remains open after all in-progress commands are complete, the DRAM will be in active power-down mode. If all banks are closed after all in-progress commands are complete, the DRAM will be in precharge power-down mode. Precharge power-down mode must be programmed to exit with either a slow exit mode or a fast exit mode. When entering precharge power-down mode, the DLL is turned off in slow exit mode or kept on in fast exit mode.

The DLL also remains on when entering active power-down. ODT has special timing constraints when slow exit mode precharge power-down is enabled and entered. Refer to section: Asynchronous ODT Mode for detailed ODT usage requirements in slow exit mode precharge power-down. A summary of the two power-down modes is listed in Table 4-76.

While in either power-down state, CKE is held LOW, RESET# is held HIGH, and a stable clock signal must be maintained. ODT must be in a valid state but all other input signals are “Don’t Care” If RESET# goes LOW during power-down, the DRAM will switch out of power-down mode and go into the reset state. After CKE is registered LOW, CKE must remain LOW until tPD (MIN) has been satisfied. The maximum time allowed for powerdown duration is tPD (MAX) (9 × tREFI).

The power-down states are synchronously exited when CKE is registered HIGH (with a required NOP or DES command). CKE must be maintained HIGH until tCKE has been satisfied. A valid, executable command may be applied after power-down exit latency, tXP, and tXPDLL have been satisfied. A summary of the power-down modes is listed below.

For specific CKE-intensive operations, such as repeating a power-down-exit-to-refresh-to-power-down-entry sequence, the number of clock cycles between power-down exit and power-down entry may not be sufficient to keep the DLL properly updated. In addition to meeting tPD when the REFRESH command is used between power-down exit and power-down entry, two other conditions must be met. First, tXP must be satisfied before issuing the REFRESH command. Second, tXPDLL must be satisfied before the next power-down may be entered. An example is shown in Figure 4-95.

Table 4-76: Power-Down Modes

DRAM State	MR1[12]	DLL State	Power-Down Exit	Relevant Parameters
Active (any bank open)	“Don’t Care”	On	Fast	tXP to any other valid command
Precharged (all banks precharged)	1	On	Fast	tXP to any other valid command
	0	Off	slow	tXPDLL to commands that require the DLL to be locked (READ, RDAP, or ODT on);

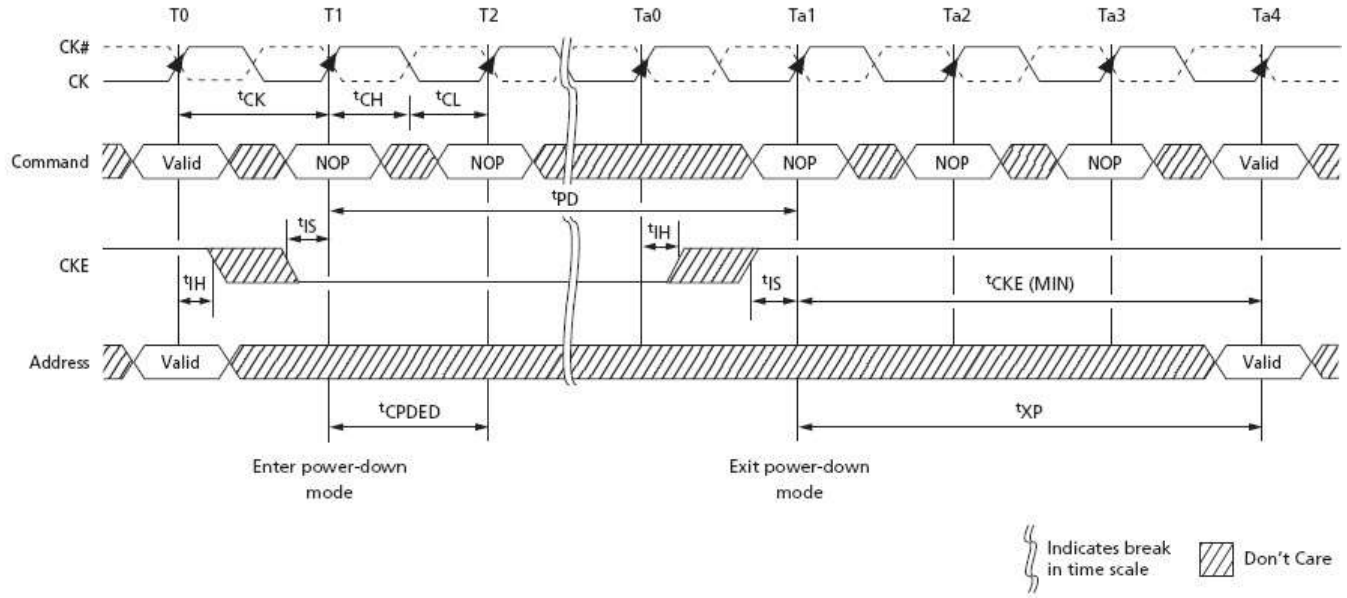


Figure 4-85: Active Power-Down Entry and Exit

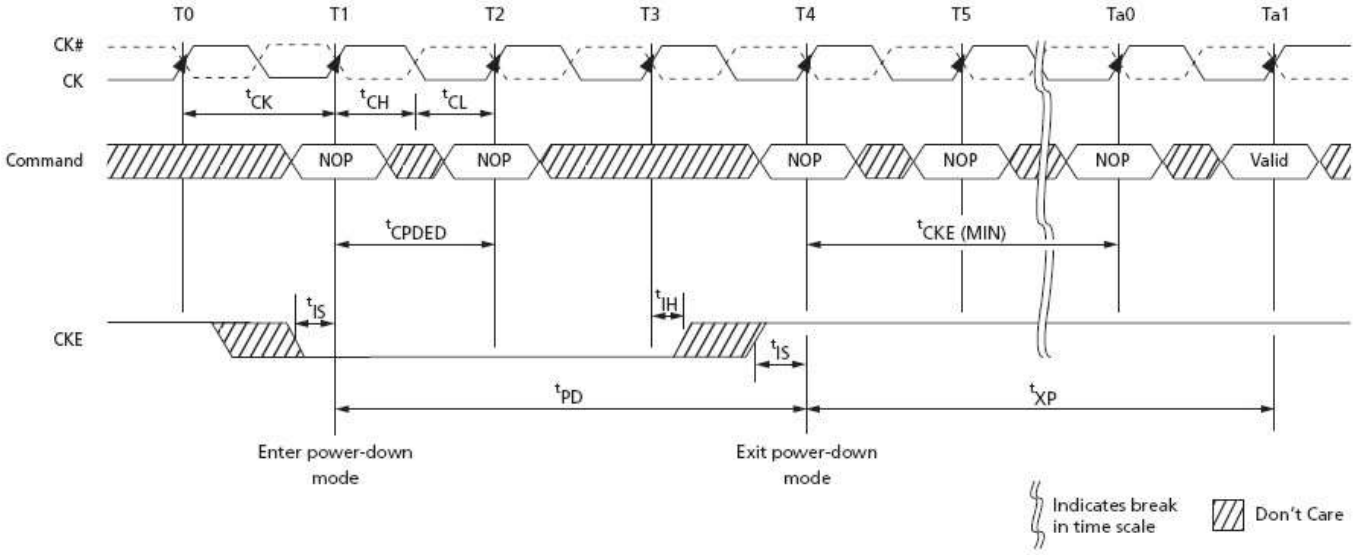


Figure 4-86: Precharge Power-Down (Fast-Exit Mode) Entry and Exit

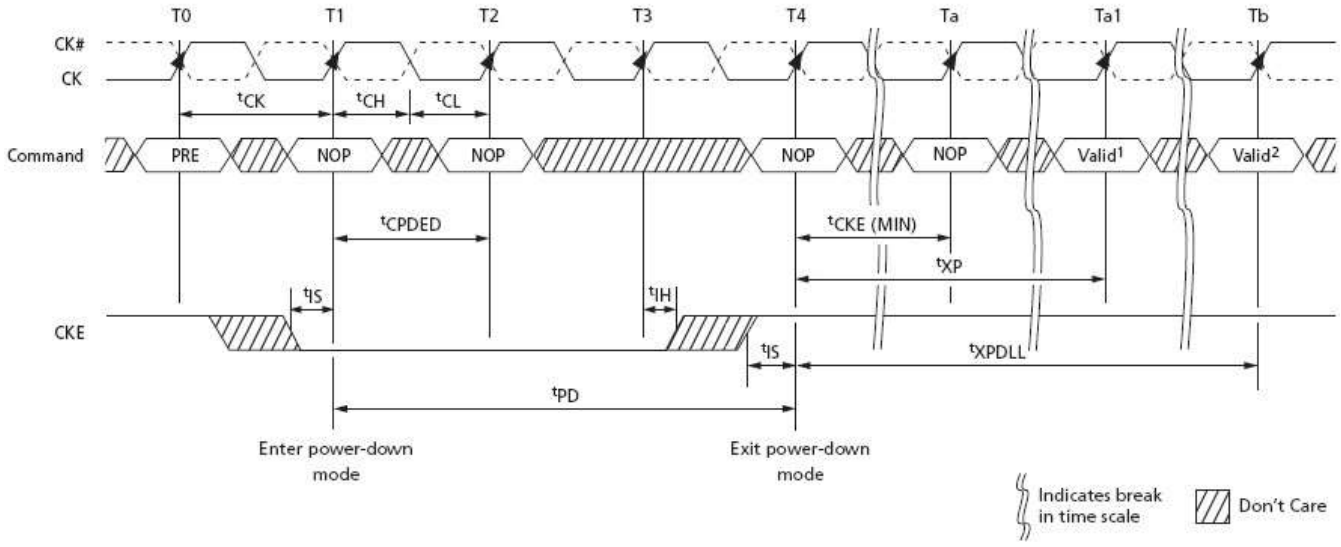


Figure 4-87: Precharge Power-Down (Slow-Exit Mode) Entry and Exit

Notes:

1. Any valid command not requiring a locked DLL.
2. Any valid command requiring a locked DLL.

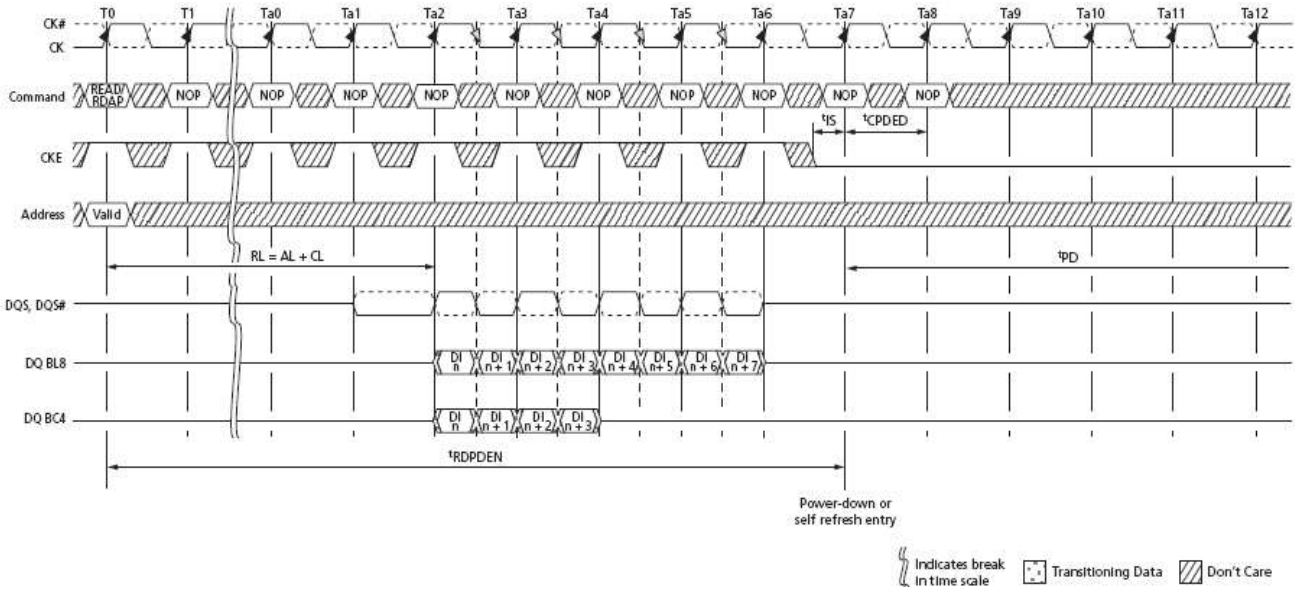


Figure 4-88: Power-Down Entry After READ or READ with Auto Precharge (RDAP)

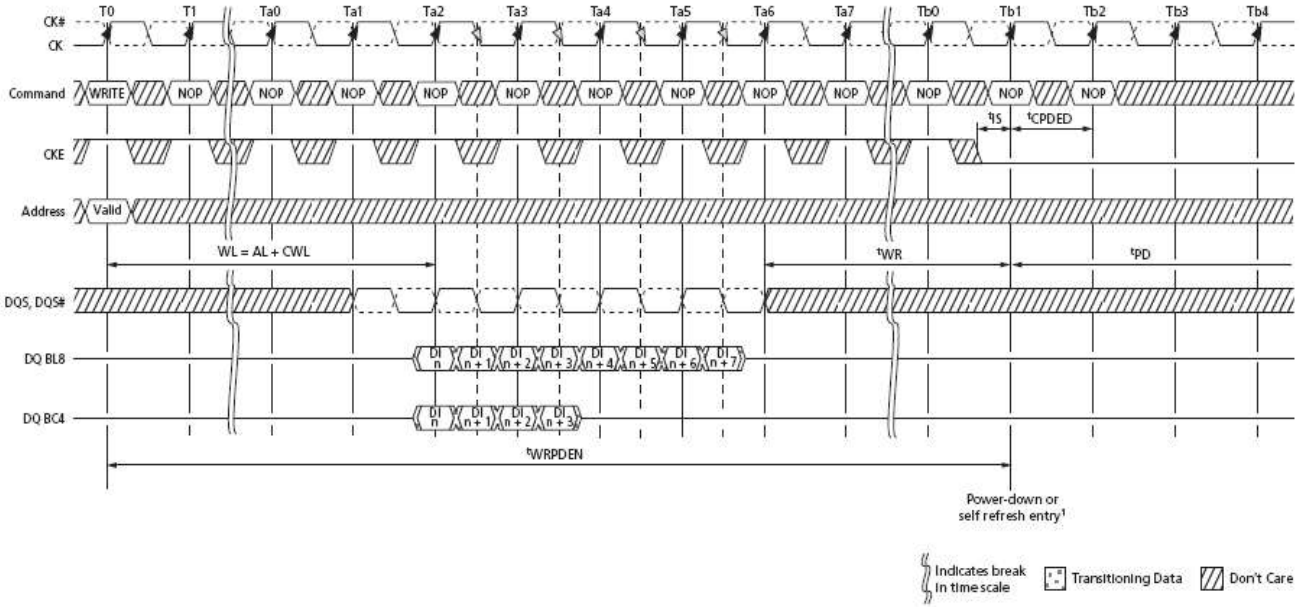


Figure 4-89: Power-Down Entry After WRITE

Note:

1. CKE can go LOW 2tCK earlier if BC4MRS.

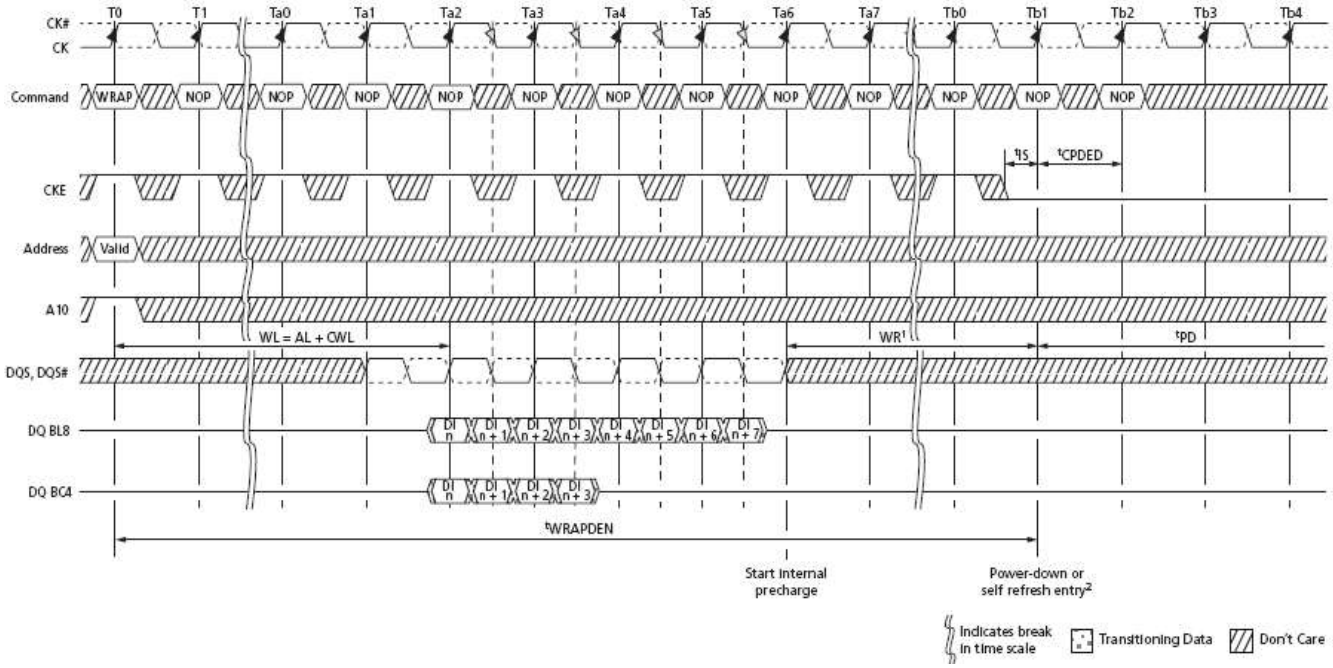


Figure 4-90: Power-Down Entry After WRITE with Auto Precharge (WRAP)

Notes:

1. tWR is programmed through MR0[11:9] and represents tWRmin (ns)/tCK rounded up to the next integer tCK.
2. CKE can go LOW 2tCK earlier if BC4MRS.

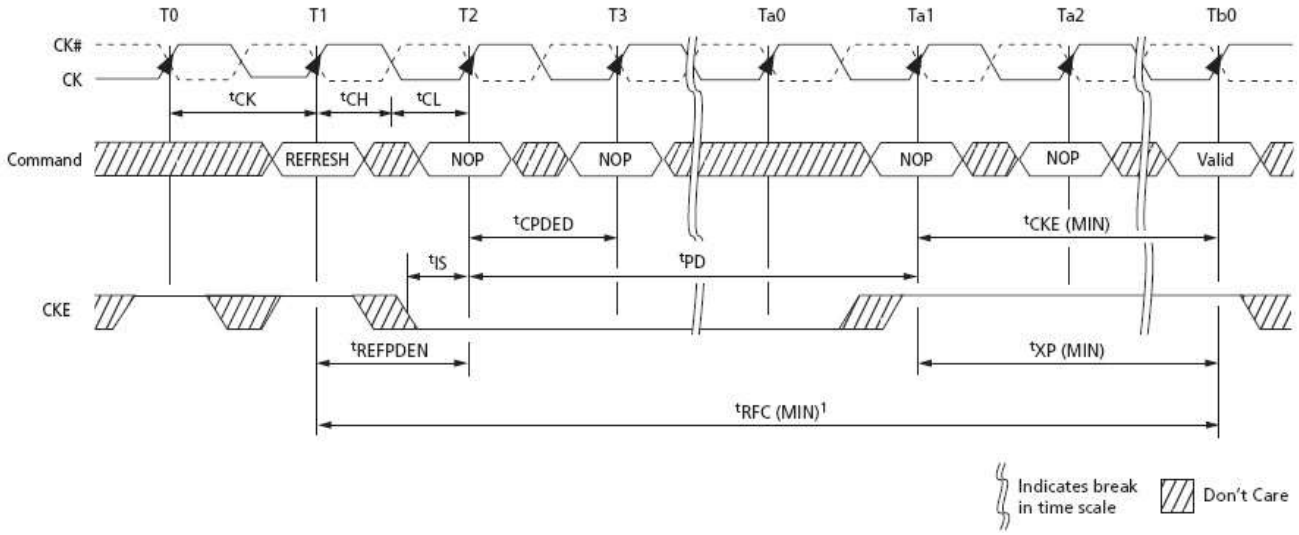


Figure 4-91: REFRESH to Power-Down Entry

Note:

1. After CKE goes HIGH during tRFC, CKE must remain HIGH until tRFC is satisfied.

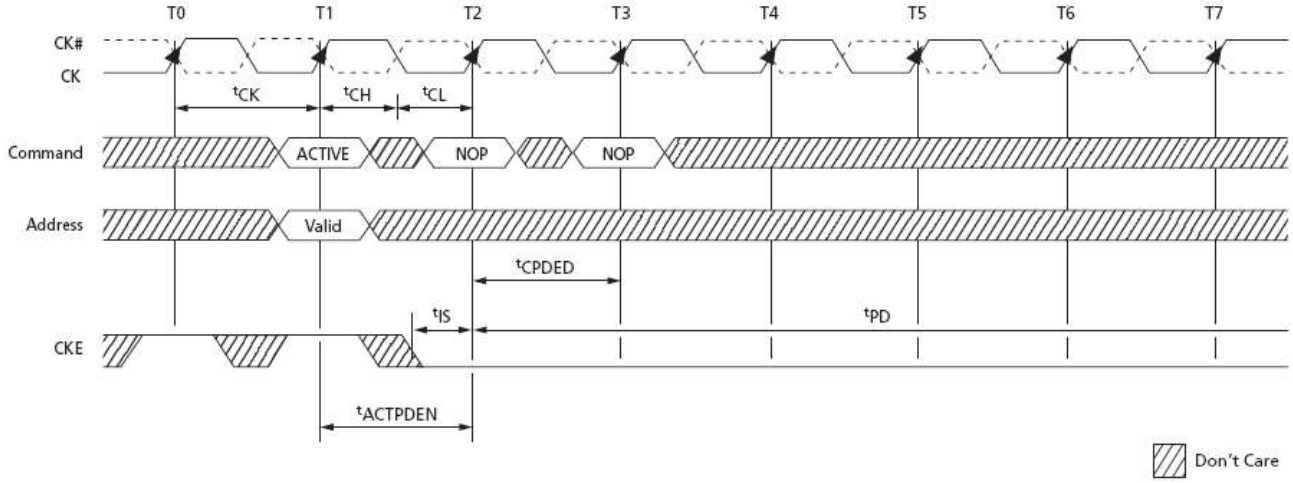


Figure 4-92: ACTIVATE to Power-Down Entry

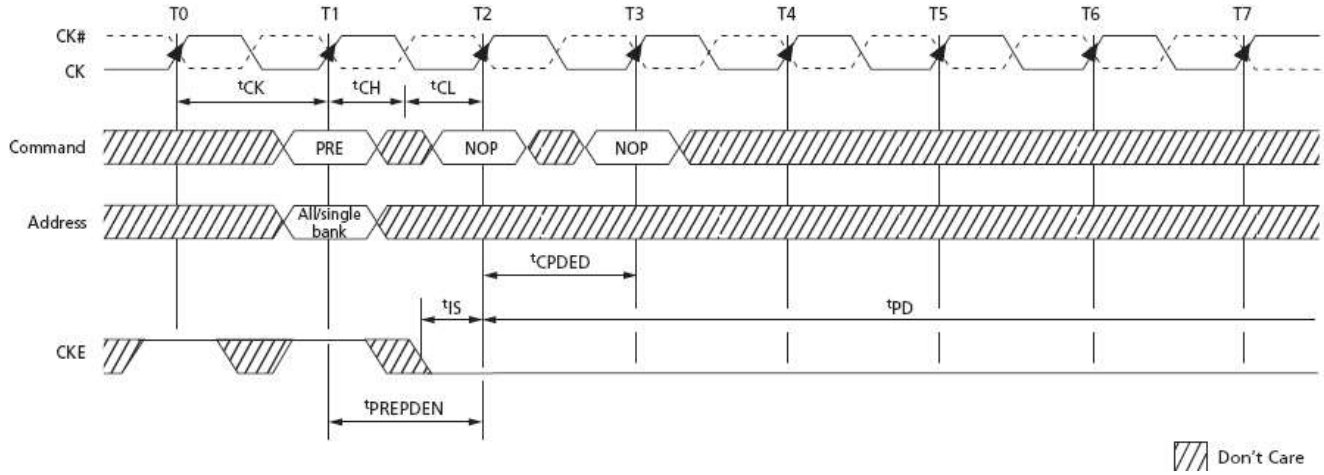


Figure 4-93: PRECHARGE to Power-Down Entry

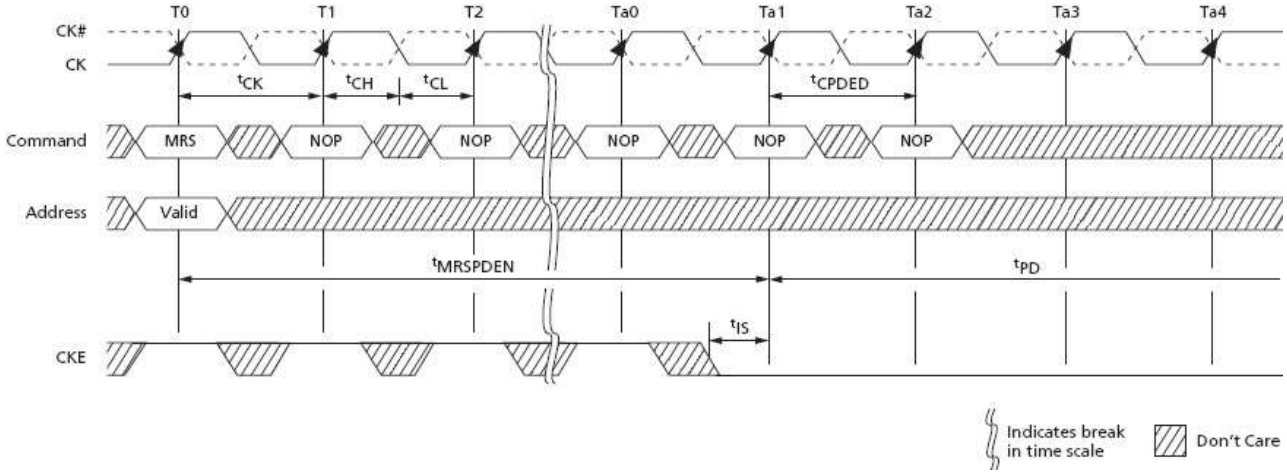


Figure 4-94: MRS Command to Power-Down Entry

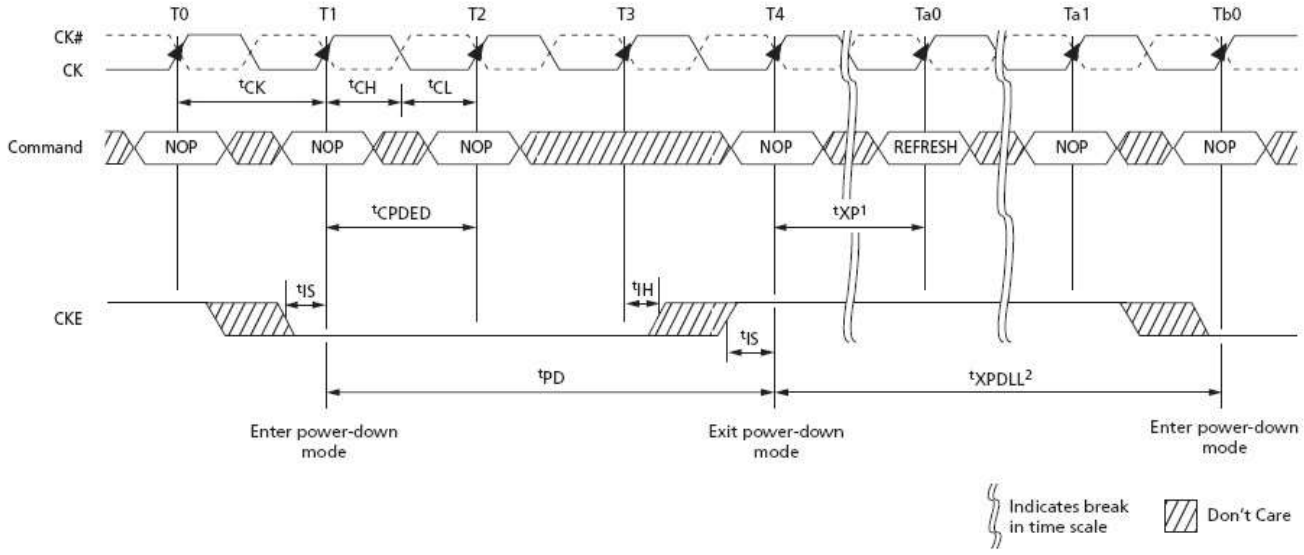


Figure 4-95: Power-Down Exit to Refresh to Power-Down Entry

Notes:

1. tXP must be satisfied before issuing the command.
2. tXPDLL must be satisfied (referenced to the registration of power-down exit) before the next power-down can be entered.

RESET Operation

The RESET signal (RESET#) is an asynchronous reset signal that triggers any time it drops LOW, and there are no restrictions about when it can go LOW. After RESET# goes LOW, it must remain LOW for 100ns. During this time, the outputs are disabled, ODT (R_{TT}) turns off (High-Z), and the DRAM resets itself. CKE should be driven LOW prior to RESET# being driven HIGH. After RESET# goes HIGH, the DRAM must be re-initialized as though a normal power-up was executed. All counters, except refresh counters on the DRAM are reset, and data stored in the DRAM is assumed unknown after RESET# has gone LOW.

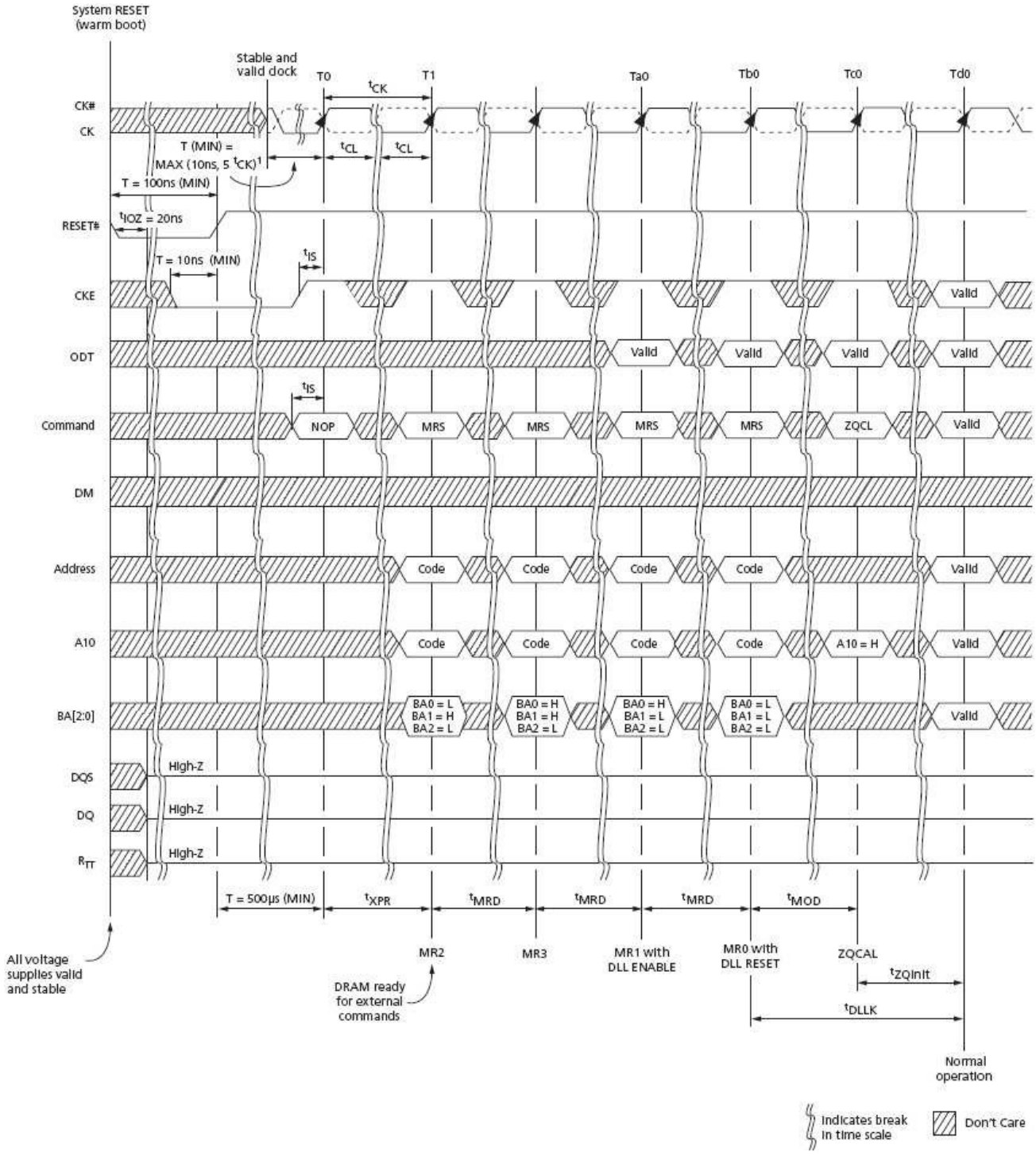


Figure 4-96: RESET Sequence

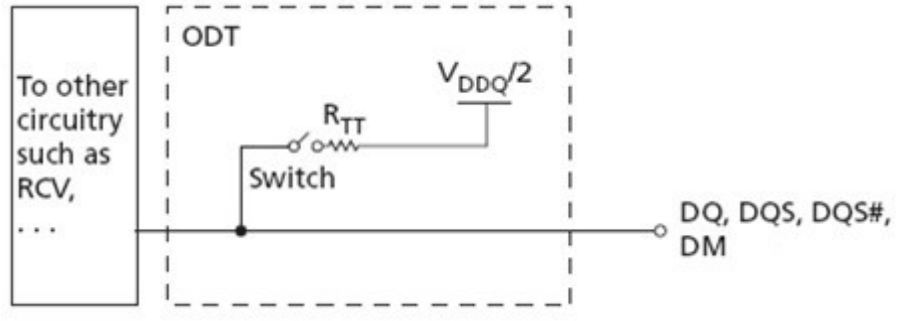
Note:

1. The minimum time required is the longer of 10ns or 5 clocks.

On-Die Termination (ODT)

On-die termination (ODT) is a feature that enables the DRAM to enable/disable and turn on/off termination resistance for each DQ, DQS and DQS#.

ODT is designed to improve signal integrity of the memory channel by enabling the DRAM controller to independently turn on/off the DRAM's internal termination resistance for any grouping of DRAM devices. ODT is not supported during DLL disable mode (simple functional representation shown below). The switch is enabled by the internal ODT control logic, which uses the external ODT ball and other control information.



Functional Representation of ODT

The value of R_{TT} (ODT termination resistance value) is determined by the settings of several mode register bits (see Table 4-82). The ODT ball is ignored while in self refresh mode (must be turned off prior to self refresh entry) or if mode registers MR1 and MR2 are programmed to disable ODT. ODT is comprised of nominal ODT and dynamic ODT modes and either of these can function in synchronous or asynchronous mode (when the DLL is off during precharge power-down or when the DLL is synchronizing). Nominal ODT is the base termination and is used in any allowable ODT state. Dynamic ODT is applied only during writes and provides OTF switching from no R_{TT} or $R_{TT,nom}$ to $R_{TT(WR)}$.

The actual effective termination, $R_{TT(EFF)}$, may be different from R_{TT} targeted due to nonlinearity of the termination. For $R_{TT(EFF)}$ values and calculations, see Table 4-26 .

Nominal ODT

ODT (NOM) is the base termination resistance for each applicable ball; it is enabled or disabled via MR1[9, 6, 2] (see section: Mode Register 1 (MR1) Definition), and it is turned on or off via the ODT ball.

Table 4-77: Truth Table – ODT (Nominal)

Note 1 applies to the entire table

MR1[9, 6, 2]	ODT Pin	DRAM Termination State	DRAM State	Notes
000	0	$R_{TT,nom}$ disabled, ODT off	Any valid	2
000	1	$R_{TT,nom}$ disabled, ODT on	Any valid except self refresh, read	3
000–101	0	$R_{TT,nom}$ enabled, ODT off	Any valid	2
000–101	1	$R_{TT,nom}$ enabled, ODT on	Any valid except self refresh, read	3
110 and 111	X	$R_{TT,nom}$ reserved, ODT on or off	Illegal	

Notes:

1. Assumes dynamic ODT is disabled (see section: Dynamic ODT) when enabled).
2. ODT is enabled and active during most writes for proper termination, but it is not illegal for it to be off during writes.
3. ODT must be disabled during reads. The $R_{TT,nom}$ value is restricted during writes. Dynamic ODT is applicable if enabled.

Nominal ODT resistance $R_{TT,nom}$ is defined by MR1[9, 6, 2], as shown in Mode Register 1 (MR1) Definition. The $R_{TT,nom}$ termination value applies to the output pins previously mentioned. DDR3(L) SDRAM supports multiple $R_{TT,nom}$ values based on RZQ/n where n can be 2, 4, 6, 8, or 12 and RZQ is 240Ω. $R_{TT,nom}$ termination is allowed any time after the DRAM is initialized, calibrated, and not performing read access, or when it is not in self refresh mode.

Write accesses use $R_{TT,nom}$ if dynamic ODT ($R_{TT(WR)}$) is disabled. If $R_{TT,nom}$ is used during writes, only RZQ/2, RZQ/4, and RZQ/6 are allowed (see Table 4-81. ODT timings are summarized in Table 4-76, as well as listed in Table 4-47.

Examples of nominal ODT timing are shown in conjunction with the synchronous mode of operation in section: Synchronous ODT Mode.

Table 4-78: ODT Parameters

Symbol	Description	Begins at	Defined to	Definition for All DDR3(L) Speed Bins	Unit
ODTLon	ODT synchronous turn-on delay	ODT registered HIGH	$R_{TT(ON)}$ ±tAON	CWL + AL - 2	tCK
ODTLoff	ODT synchronous turn-off delay	ODT registered HIGH	$R_{TT(OFF)}$ ±tAOF	CWL + AL - 2	tCK
tAONPD	ODT asynchronous turn-on delay	ODT registered HIGH	$R_{TT(ON)}$	2–8.5	ns
tAOFPD	ODT asynchronous turn-off delay	ODT registered HIGH	$R_{TT(OFF)}$	2–8.5	ns
ODTH4	ODT minimum HIGH time after ODT assertion or write (BC4)	ODT registered HIGH or write registration with	ODT registered LOW	4tCK	tCK
ODTH8	ODT minimum HIGH time after write (BL8)	Write registration with ODT HIGH	ODT registered LOW	6tCK	tCK
tAON	ODT turn-on relative to ODTLon completion	Completion of ODTLon	$R_{TT(ON)}$	See Table 4-47	ps
tAOF	ODT turn-off relative to ODTLoff completion	Completion of ODTLoff	$R_{TT(OFF)}$	0.5tCK ± 0.2tCK	tCK

Dynamic ODT

In certain application cases, and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3(L) SDRAM can be changed without issuing an MRS command, essentially changing the ODT termination on the fly. With dynamic ODT $R_{TT(WR)}$ enabled, the DRAM switches from nominal ODT $R_{TT,nom}$ to dynamic ODT $R_{TT(WR)}$ when beginning a WRITE burst and subsequently switches back to nominal ODT $R_{TT,nom}$) at the completion of the WRITE burst. This requirement is supported by the dynamic ODT feature, as described below.

Dynamic ODT Special Use Case

When DDR3(L) devices are architect as a single rank memory array, dynamic ODT offers a special use case: the ODT ball can be wired high (via a current limiting resistor preferred) by having $R_{TT,nom}$ disabled via MR1 and $R_{TT(WR)}$ enabled via MR2. This will allow the ODT signal not to have to be routed yet the DRAM can provide ODT coverage during write accesses.

When enabling this special use case, some standard ODT spec conditions may be violated: ODT is sometimes supposed to be held low. Such ODT spec violation (ODT not LOW) is allowed under this special use case. Most notably, if Write Leveling is used, this would appear to be a problem since $R_{TT(WR)}$ can not be used (should be disabled) and $R_{TT(NOM)}$ should be used. For Write leveling during this special use case, with the DLL locked, then $R_{TT(NOM)}$ maybe enabled when entering Write Leveling mode and disabled when exiting Write Leveling mode. More so, $R_{TT(NOM)}$ must be enabled when enabling Write Leveling, via same MR1 load, and disabled when disabling Write Leveling, via same MR1 load if $R_{TT(NOM)}$ is to be used.

ODT will turn-on within a delay of ODTLon + tAON + tMOD + 1CK (enabling via MR1) or turn-off within a delay of ODTLoff + tAOF + tMOD + 1CK. As seen in the table below, between the Load Mode of MR1 and the previously specified delay, the value of ODT is uncertain. this means the DQ ODT termination could turn-on and then turn-off again during the period of stated uncertainty.

Table 4-79: Write Leveling with Dynamic ODT Special Case

Begin $R_{TT,nom}$ Uncertainty	End $R_{TT,nom}$ Uncertainty	I/Os	$R_{TT,nom}$ Final State
MR1 load mode command: Enable Write Leveling and $R_{TT(NOM)}$	ODTLon + tAON + tMOD + 1CK	DQS, DQS#	Drive $R_{TT,nom}$ value
		DQs	No $R_{TT,nom}$
MR1 load mode command: Disable Write Leveling and $R_{TT(NOM)}$	ODTLoff + tAOFF + tMOD + 1CK	DQS, DQS#	No $R_{TT,nom}$
		DQs	No $R_{TT,nom}$

Functional Description

The dynamic ODT mode is enabled if either MR2[9] or MR2[10] is set to 1. Dynamic ODT is not supported during

DLL disable mode so $R_{TT(WR)}$ must be disabled. The dynamic ODT function is described below:

• Two R_{TT} values are available—$R_{TT,nom}$ and $R_{TT(WR)}$.
  – The value for $R_{TT,nom}$ is preselected via MR1[9, 6, 2].
  – The value for $R_{TT(WR)}$ is preselected via MR2[10, 9].
• During DRAM operation without READ or WRITE commands, the termination is controlled.
  – Nominal termination strength $R_{TT,nom}$ is used.
  – Termination on/off timing is controlled via the ODT ball and latencies ODTLon and ODTLoff.
• When a WRITE command (WR, WRAP, WRS4, WRS8, WRAPS4, WRAPS8) is registered, and if dynamic ODT is enabled, the ODT termination is controlled.
  – A latency of ODTLcnw after the WRITE command: termination strength $R_{TT,nom}$ switches to $R_{TT(WR)}$.
  – A latency of ODTLcwn8 (for BL8, fixed or OTF) or ODTLcwn4 (for BC4, fixed or OTF) after the WRITE
    command: termination strength $R_{TT(WR)}$ switches back to $R_{TT,nom}$.
  – On/off termination timing is controlled via the ODT ball and determined by ODTLon, ODTLoff, ODTH4, and ODTH8.
  – During the tADC transition window, the value of R_{TT} is undefined.

ODT is constrained during writes and when dynamic ODT is enabled (see Table 4-80) ODT timings listed in Table
4-78 also apply to dynamic ODT mode.

Table 4-80: Dynamic ODT Specific Parameters

Symbol	Description	Begins at	Defined to	Definition for All DDR3(L) Speed	Unit
ODTLcnw	Change from $R_{TT,nom}$ to $R_{TT(WR)}$	Write registration	R_{TT} switched from $R_{TT,nom}$ to $R_{TT(WR)}$	WL - 2	tCK
ODTLcwn4	Change from $R_{TT(WR)}$ to $R_{TT,nom}$ (BC4)	Write registration	R_{TT} switched from $R_{TT(WR)}$ to $R_{TT,nom}$	4tCK + ODTL off	tCK
ODTLcwn8	Change from $R_{TT(WR)}$ to $R_{TT,nom}$ (BL8)	Write registration	R_{TT} switched from $R_{TT(WR)}$ to $R_{TT,nom}$	6tCK + ODTL off	tCK
tADC	R_{TT} change skew	ODTLcnw completed	R_{TT} transition complete	0.5tCK ± 0.2tCK	tCK

Table 4-81: Mode Registers for $R_{TT,nom}$

MR1 ($R_{TT,nom}$)			$R_{TT,nom}$ (RZQ)	$R_{TT,nom}$ (Ohm)	$R_{TT,nom}$ Mode Restriction
M9	M6	M2			
0	0	0	Off	Off	N/A
0	0	1	RZQ/4	60	Self refresh
0	1	0	RZQ/2	120	
0	1	1	RZQ/6	40	
1	0	0	RZQ/12	20	Self refresh, write
1	0	1	RZQ/8	30	
1	1	0	Reserved	Reserved	N/A
1	1	1	Reserved	Reserved	N/A

Note:

1. RZQ = 240Ω. If $R_{TT,nom}$ is used during WRITEs, only RZQ/2, RZQ/4, RZQ/6 are allowed.

Table 4-82: Mode Registers for $R_{TT(WR)}$

MR2 ($R_{TT(WR)}$)		$R_{TT(WR)}$ (RZQ)	$R_{TT(WR)}$ (Ohm)
M10	M9		
0	0	Dynamic ODT off: WRITE does not affect $R_{TT,nom}$	
0	1	RZQ/4	60
1	0	RZQ/2	120
1	1	Reserved	Reserved

Table 4-83: Timing Diagrams for Dynamic ODT

Figure	Title
Figure 4-98	Dynamic ODT: ODT Asserted Before and After the WRITE, BC4
Figure 4-99	Dynamic ODT: Without WRITE Command
Figure 4-100	Dynamic ODT: ODT Pin Asserted Together with WRITE Command for 6 Clock Cycles, BL8
Figure 4-101	Dynamic ODT: ODT Pin Asserted with WRITE Command for 6 Clock Cycles, BC4
Figure 4-102	Dynamic ODT: ODT Pin Asserted with WRITE Command for 4 Clock Cycles, BC4

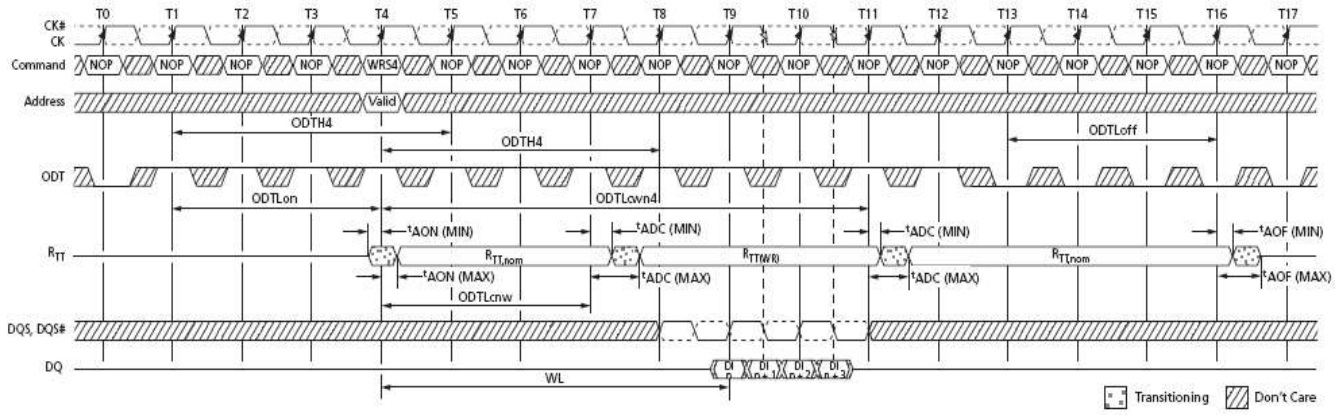


Figure 4-98: Dynamic ODT: ODT Asserted Before and After the WRITE, BC4

Notes:

1. Via MRS or OTF. AL = 0, CWL = 5. $R_{TT,nom}$ and $R_{TT(WR)}$ are enabled.
2. ODTH4 applies to first registering ODT HIGH and then to the registration of the WRITE command. In this example, ODTH4 is satisfied if ODT goes LOW at T8 (four clocks after the WRITE command).

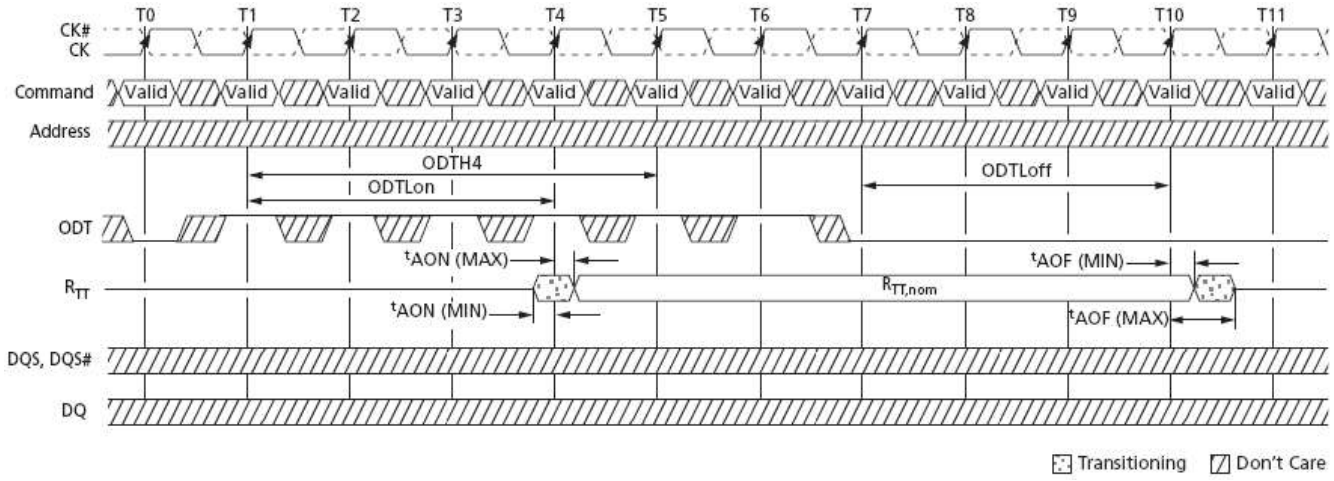


Figure 4-99: Dynamic ODT: Without WRITE Command

Notes:

1. AL = 0, CWL = 5. $R_{TT,nom}$ is enabled and $R_{TT(WR)}$ is either enabled or disabled.
2. ODTH4 is defined from ODT registered HIGH to ODT registered LOW; in this example, ODTH4 is satisfied. ODT registered LOW at T5 is also legal.

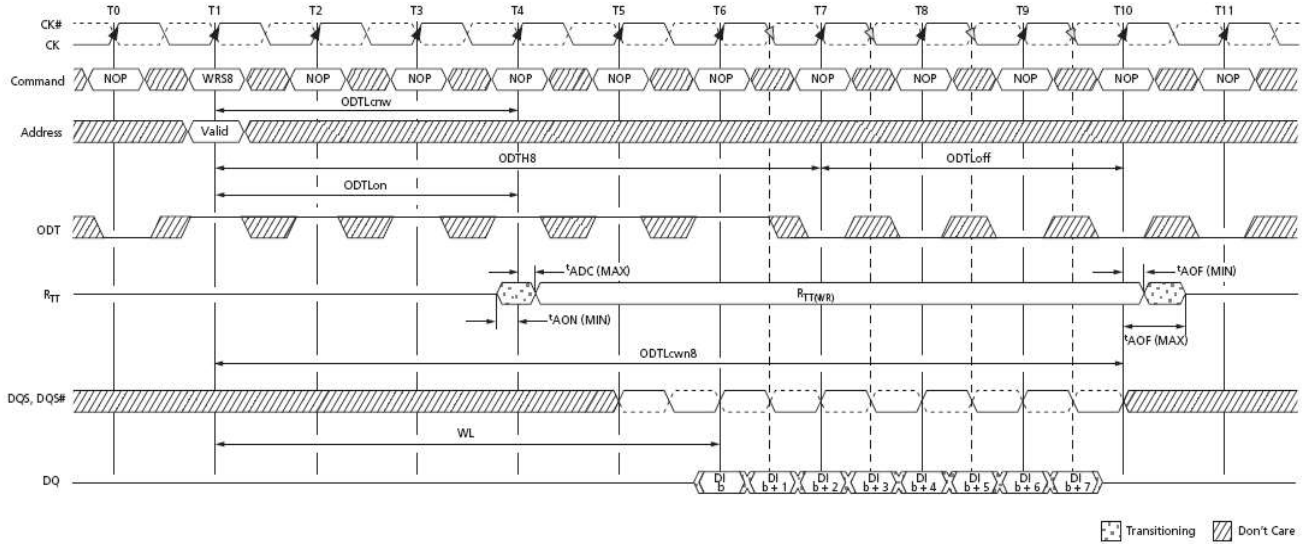


Figure 4-100: Dynamic ODT: ODT Pin Asserted Together with WRITE Command for 6 Clock Cycles, BL8

Notes:

1. Via MRS or OTF; AL = 0, CWL = 5. If $R_{TT,nom}$ can be either enabled or disabled, ODT can be HIGH. $R_{TT(WR)}$ is enabled.
2. In this example, ODTH8 = 6 is satisfied exactly.

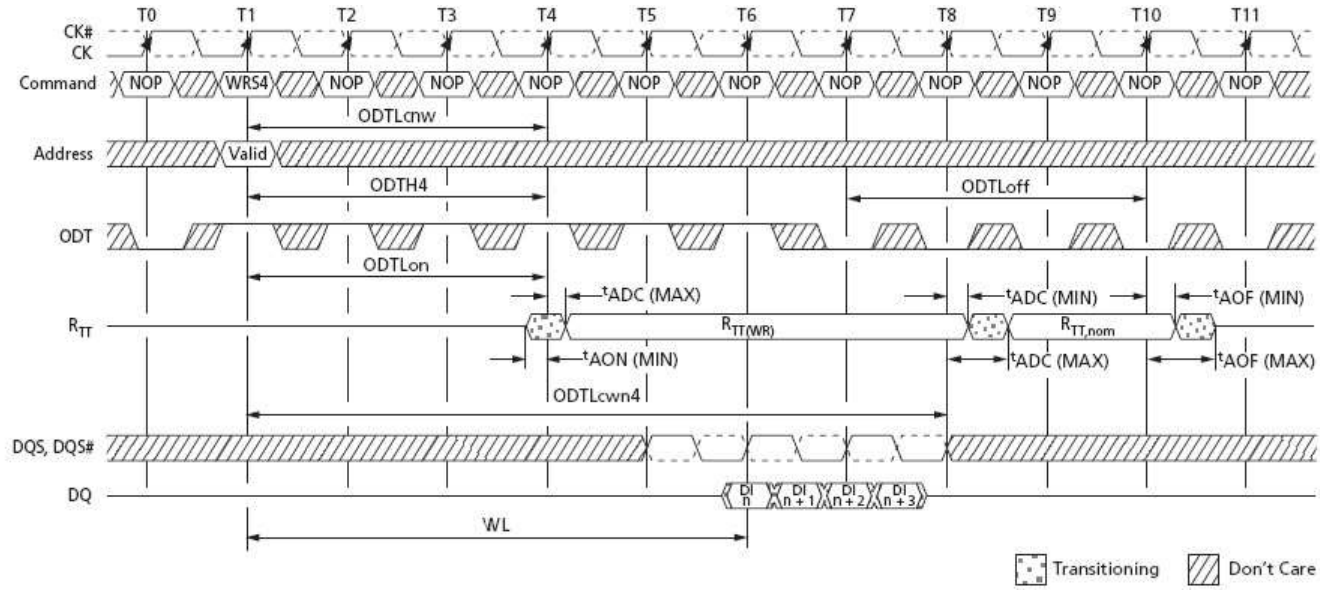


Figure 4-101: Dynamic ODT: ODT Pin Asserted with WRITE Command for 6 Clock Cycles, BC4

Notes:

1. Via MRS or OTF. AL = 0, CWL = 5. $R_{TT,nom}$ and $R_{TT(WR)}$ are enabled.
2. ODTH4 is defined from ODT registered HIGH to ODT registered LOW, so in this example, ODTH4 is satisfied. ODT registered LOW at T5 is also legal.

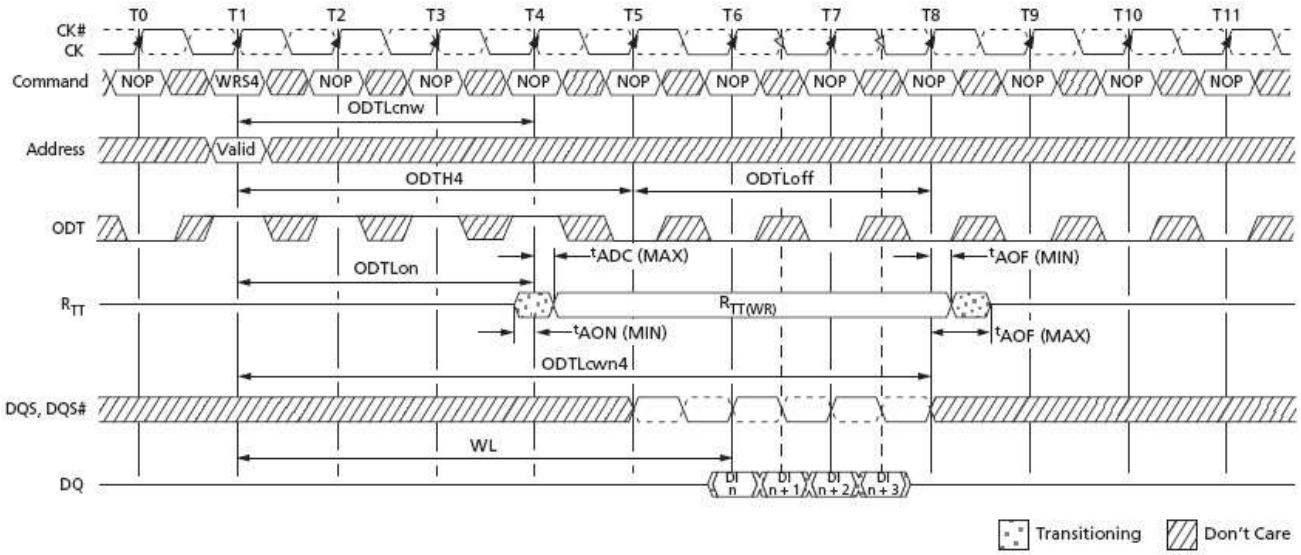


Figure 4-102: Dynamic ODT: ODT Pin Asserted with WRITE Command for 4 Clock Cycles, BC4

Notes:

1. Via MRS or OTF. AL = 0, CWL = 5. $R_{TT,nom}$ can be either enabled or disabled. If disabled, ODT can remain HIGH. $R_{TT(WR)}$ is enabled.
2. In this example ODTH4 = 4 is satisfied exactly.

Synchronous ODT Mode

Synchronous ODT mode is selected whenever the DLL is turned on and locked and when either $R_{TT,nom}$ or $R_{TT(WR)}$ is enabled. Based on the power-down definition, these modes are:

- Any bank active with CKE HIGH.
- Refresh mode with CKE HIGH.
- Idle mode with CKE HIGH.
- Active power-down mode (regardless of MR0[12]).
- Precharge power-down mode if DLL is enabled by MR0[12] during precharge power-down.

ODT Latency and Posted ODT

In synchronous ODT mode, R_{TT} turns on ODTLon clock cycles after ODT is sampled HIGH by a rising clock edge and turns off ODTLoff clock cycles after ODT is registered LOW by a rising clock edge. The actual on/off times varies by tAON and tAOF around each clock edge (see Table 4-84). The ODT latency is tied to the WRITE latency (WL) by ODTLon = WL - 2 and ODTLoff = WL - 2.

Since write latency is made up of CAS WRITE latency (CWL) and additive latency (AL), the AL programmed into the mode register (MR1[4, 3]) also applies to the ODT signal. The device's internal ODT signal is delayed a number of clock cycles defined by the AL relative to the external ODT signal. Thus, ODTLon = CWL + AL - 2 and ODTLoff = CWL + AL - 2.

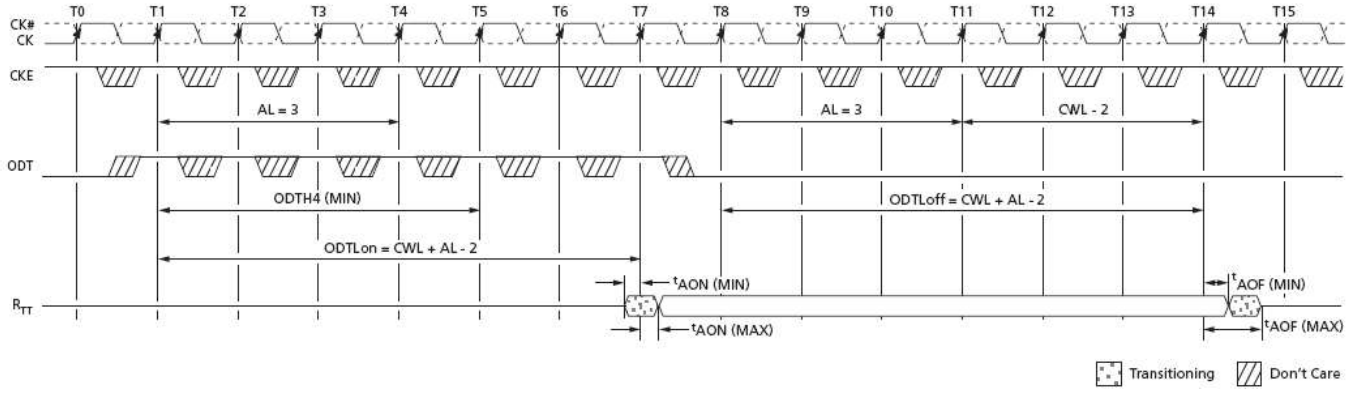
Timing Parameters

Synchronous ODT mode uses the following timing parameters: ODTLon, ODTLoff, ODTH4, ODTH8, tAON, and tAOF. The minimum R_{TT} turn-on time (tAON [MIN]) is the point at which the device leaves High-Z and ODT resistance begins to turn on. Maximum R_{TT} turn-on time (tAON [MAX]) is the point at which ODT resistance is fully on. Both are measured relative to ODTLon. The minimum R_{TT} turn-off time (tAOF [MIN]) is the point at which the device starts to turn off ODT resistance. The maximum R_{TT} turn off time (tAOF [MAX]) is the point at which ODT has reached High-Z. Both are measured from ODTLoff.

When ODT is asserted, it must remain HIGH until ODTH4 is satisfied. If a WRITE command is registered by the DRAM with ODT HIGH, then ODT must remain HIGH until ODTH4 (BC4) or ODTH8 (BL8) after the WRITE command (see Figure 4-104). ODTH4 and ODTH8 are measured from ODT registered HIGH to ODT registered LOW or from the registration of a WRITE command until ODT is registered LOW.

Table 4-84: Synchronous ODT Parameters

Symbol	Description	Begins at	Defined to	Definition for All DDR3(L) Speed Bins	Unit
ODTLon	ODT synchronous turn-on delay	ODT registered HIGH	$R_{TT(ON)}$ ±tAON	CWL + AL - 2	tCK
ODTLoff	ODT synchronous turn-off delay	ODT registered HIGH	$R_{TT(OFF)}$ ±tAOF	CWL +AL - 2	tCK
ODTH4	ODT minimum HIGH time after ODT assertion or	ODT registered HIGH or write regis-tration with ODT	ODT registered LOW	4tCK	tCK
ODTH8	ODT minimum HIGH time after WRITE (BL8)	Write registration with ODT HIGH	ODT registered LOW	6tCK	tCK
tAON	ODT turn-on relative to ODTLon completion	Completion of ODTLon	$R_{TT(ON)}$	See Table 4-47	ps
tAOF	ODT turn-off relative to ODTLoff completion	Completion of ODTLoff	$R_{TT(OFF)}$	0.5tCK ± 0.2tCK	tCK



Note:

1. AL = 3; CWL = 5; ODTLon = WL = 6.0; ODTLoff = WL - 2 = 6. $R_{TT,nom}$ is enabled.

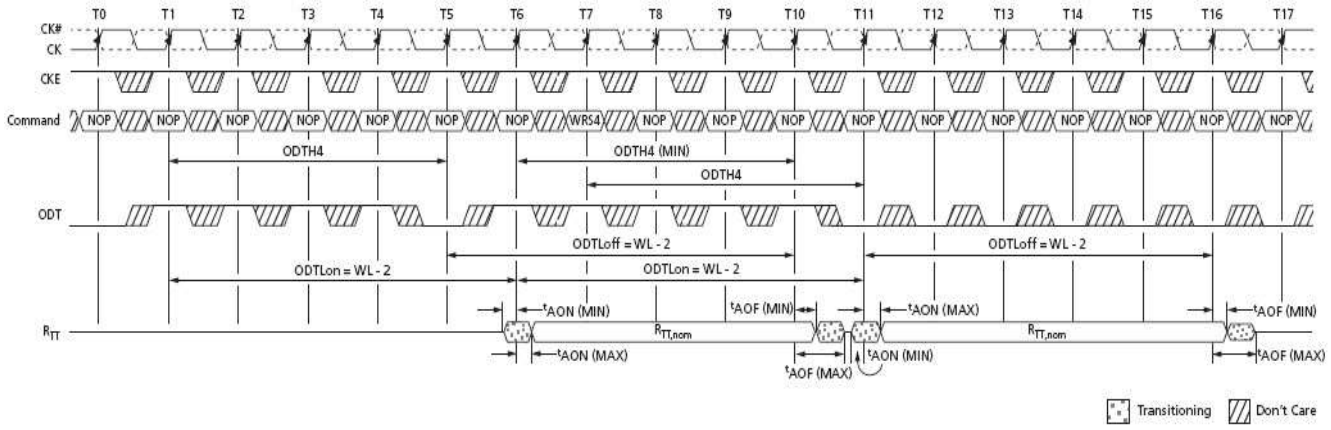


Figure 4-104: Synchronous ODT (BC4)

Notes:

1. WL = 7. RTT,nom is enabled. RTT(WR) is disabled.

2. ODT must be held HIGH for at least ODTH4 after assertion (T1).

3. ODT must be kept HIGH ODTH4 (BC4) or ODTH8 (BL8) after the WRITE command (T7).

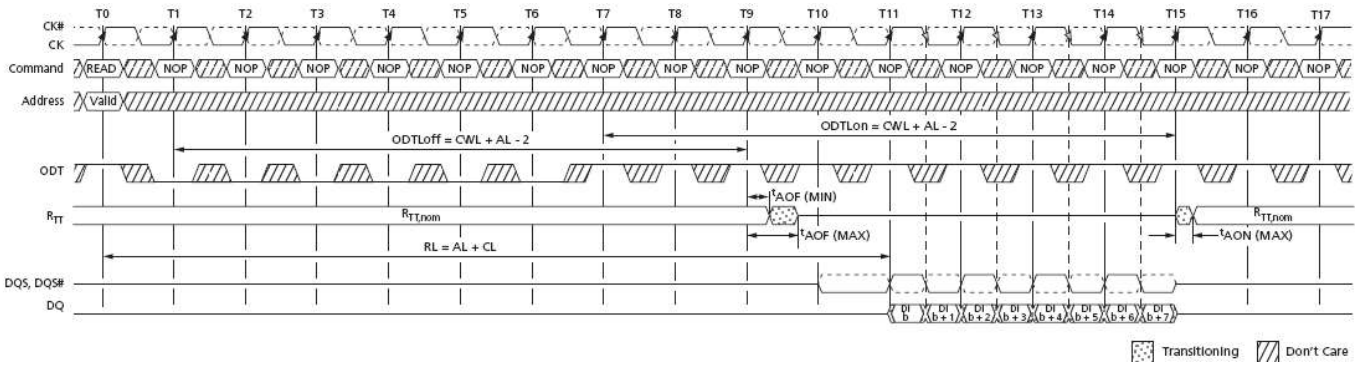
4. ODTH is measured from ODT first registered HIGH to ODT first registered LOW or from the registration of the WRITE command with ODT HIGH to ODT registered LOW.

5. Although ODTH4 is satisfied from ODT registered HIGH at T6, ODT must not go LOW before T11 as ODTH4 must also be satisfied from the registration of the WRITE command at T7.

ODT Off During READs

Because the device cannot terminate and drive at the same time, R_{TT} must be disabled at least one-half clock cycle before the READ preamble by driving the ODT ball LOW (if either $R_{TT,nom}$ or $R_{TT(WR)}$ is enabled). R_{TT} may not be enabled until the end of the postamble, as shown in the following example.

Note: ODT may be disabled earlier and enabled later than shown in Figure 4-105.



Note:

1. ODT must be disabled externally during READs by driving ODT LOW. For example, CL = 6; AL = CL - 1 = 5; RL = AL + CL = 11; CWL = 5; ODTLon = CWL + AL - 2 = 8; ODTLoff = CWL + AL - 2 = 8. RTT,nom is enabled. RTT(WR) is a “Don’t Care”.

Asynchronous ODT Mode

Asynchronous ODT mode is available when the DRAM runs in DLL on mode and when either $R_{TT,nom}$ or $R_{TT(WR)}$ is enabled; however, the DLL is temporarily turned off in precharged power-down standby (via MR0[12]). Additionally, ODT operates asynchronously when the DLL is synchronizing after being reset. See section: Power-Down Mode for definition and guidance over power-down details.

In asynchronous ODT timing mode, the internal ODT command is not delayed by AL relative to the external ODT command. In asynchronous ODT mode, ODT controls R_{TT} by analog time. The timing parameters tAONPD and tAOFPD replace ODTLon/tAON and ODTLoff/tAOF, respectively, when ODT operates asynchronously.

The minimum R_{TT} turn-on time (tAONPD [MIN]) is the point at which the device termination circuit leaves High-Z and ODT resistance begins to turn on. Maximum R_{TT} turnon time (tAONPD [MAX]) is the point at which ODT resistance is fully on. tAONPD (MIN) and tAONPD (MAX) are measured from ODT being sampled HIGH.

The minimum R_{TT} turn-off time (tAOFPD [MIN]) is the point at which the device termination circuit starts to turn off ODT resistance. Maximum R_{TT} turn-off time (tAOFPD [MAX]) is the point at which ODT has reached High-Z. tAOFPD (MIN) and tAOFPD (MAX) are measured from ODT being sampled LOW.

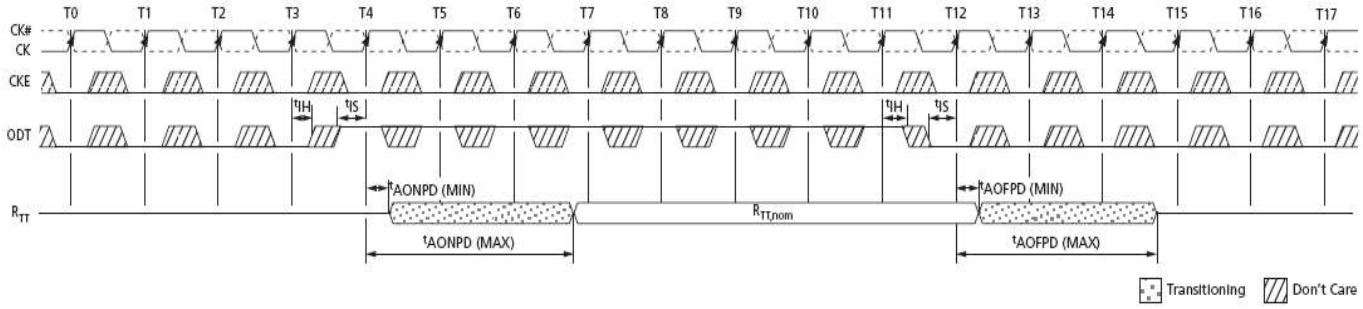


Figure 4-106: Asynchronous ODT Timing with Fast ODT Transition

Note:

1. AL is ignored.

Table 4-85: Asynchronous ODT Timing Parameters for All Speed Bins

Symbol	Description	Min	Max	Unit
tAONPD	Asynchronous R_{TT} turn-on delay (power-down with DLL off)	2	8.5	ns
tAOFPD	Asynchronous R_{TT} turn-off delay (power-down with DLL off)	2	8.5	ns

Synchronous to Asynchronous ODT Mode Transition (Power-Down Entry)

There is a transition period around power-down entry (PDE) where the DRAM's ODT may exhibit either synchronous or asynchronous behavior. This transition period occurs if the DLL is selected to be off when in precharge power-down mode by the setting MR0[12] = 0. Power-down entry begins tANPD prior to CKE first being registered LOW, and ends when CKE is first registered LOW. tANPD is equal to the greater of ODTLoff + 1tCK or ODTLon + 1tCK. If a REFRESH command has been issued, and it is in progress when CKE goes LOW, power-down entry ends tRFC after the REFRESH command, rather than when CKE is first registered LOW. Power-down entry then becomes the greater of tANPD and tRFC - REFRESH command to CKE registered LOW.

ODT assertion during power-down entry results in an R_{TT} change as early as the lesser of tAONPD (MIN) and ODTLon × tCK + tAON (MIN), or as late as the greater of tAONPD (MAX) and ODTLon × tCK + tAON (MAX). ODT de-assertion during power-down entry can result in an R_{TT} change as early as the lesser of tAOFPD (MIN) and ODTLoff × tCK + tAOF (MIN), or as late as the greater of tAOFPD (MAX) and ODTLoff × tCK + tAOF (MAX). Table 4-86 summarizes these parameters.

If AL has a large value, the uncertainty of the state of R_{TT} becomes quite large. This is because ODTLon and
ODTLoff are derived from the WL; and WL is equal to CWL + AL. Figure 4-107 shows three different cases:

- ODT_A: Synchronous behavior before tANPD.
- ODT_B: ODT state changes during the transition period with tAONPD (MIN) <ODTLon × tCK + tAON (MIN) and tAONPD (MAX) > ODTLon × tCK + tAON (MAX).
- ODT_C: ODT state changes after the transition period with asynchronous behavior.

Table 4-86: ODT Parameters for Power-Down (DLL Off) Entry and Exit Transition Period

Description	Min	Max
Power-down entry transition period (power-down entry)	Greater of: tANPD or tRFC - refresh to CKE LOW	
Power-down exit transition period (power-down exit)	tANPD + tXPDLL	
ODT to R_{TT} turn-on delay (ODTLon = WL - 2)	Lesser of: tAONPD (MIN) (2ns) or ODTLon x tCK + tAON (MIN)	Greater of: tAONPD (MAX) (8.5ns) or ODTLon x tCK + tAON (MAX)
ODT to R_{TT} turn-off delay (ODTLoff = WL - 2)	Lesser of: tAOFPD (MIN) (2ns) or ODTLoff x tCK + tAOF (MIN)	Greater of: tAOFPD (MAX) (8.5ns) or ODTLoff x tCK + tAOF (MAX)
tANPD	WL - 1 (greater of ODTLoff + 1 or ODTLon + 1)	

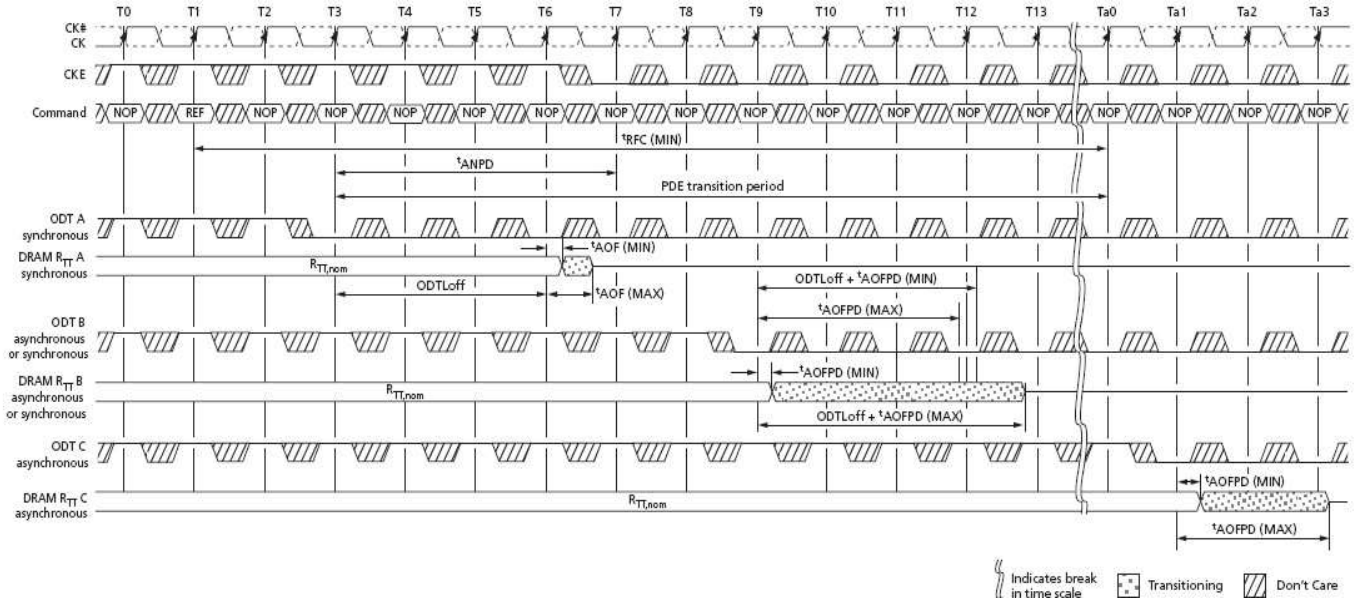


Figure 4-107: Synchronous to Asynchronous Transition During Precharge Power-Down (DLL Off) Entry

Note:

1. AL = 0; CWL = 5; ODTL(off) = WL - 2 = 3.

Asynchronous to Synchronous ODT Mode Transition (Power-Down Exit)

The DRAM's ODT can exhibit either asynchronous or synchronous behavior during power-down exit (PDX). This transition period occurs if the DLL is selected to be off when in precharge power-down mode by setting MR0[12] to 0. Power-down exit begins tANPD prior to CKE first being registered HIGH, and ends tXPDLL after CKE is first registered HIGH. tANPD is equal to the greater of ODTLoff + 1tCK or ODTLon + 1tCK. The transition period is tANPD + tXPDLL.

ODT assertion during power-down exit results in an R_{TT} change as early as the lesser of tAONPD (MIN) and ODTLon × tCK + tAON (MIN), or as late as the greater of tAONPD (MAX) and ODTLon × tCK + tAON (MAX). ODT de-assertion during power-down exit may result in an R_{TT} change as early as the lesser of tAOFPD (MIN) and ODTLoff × tCK + tAOF (MIN), or as late as the greater of tAOFPD (MAX) and ODTLoff × tCK + tAOF (MAX). Table 4-86 summarizes these parameters.

If AL has a large value, the uncertainty of the R_{TT} state becomes quite large. This is because ODTLon and ODTLoff are derived from WL, and WL is equal to CWL + AL. Figure 4-108 shows three different cases:

• ODT C: Asynchronous behavior before tANPD.

• ODT B: ODT state changes during the transition period, with tAOFPD (MIN) < ODTLoff × tCK + tAOF (MIN), and ODTLoff × tCK + tAOF (MAX) > tAOFPD (MAX).

• ODT A: ODT state changes after the transition period with synchronous response.

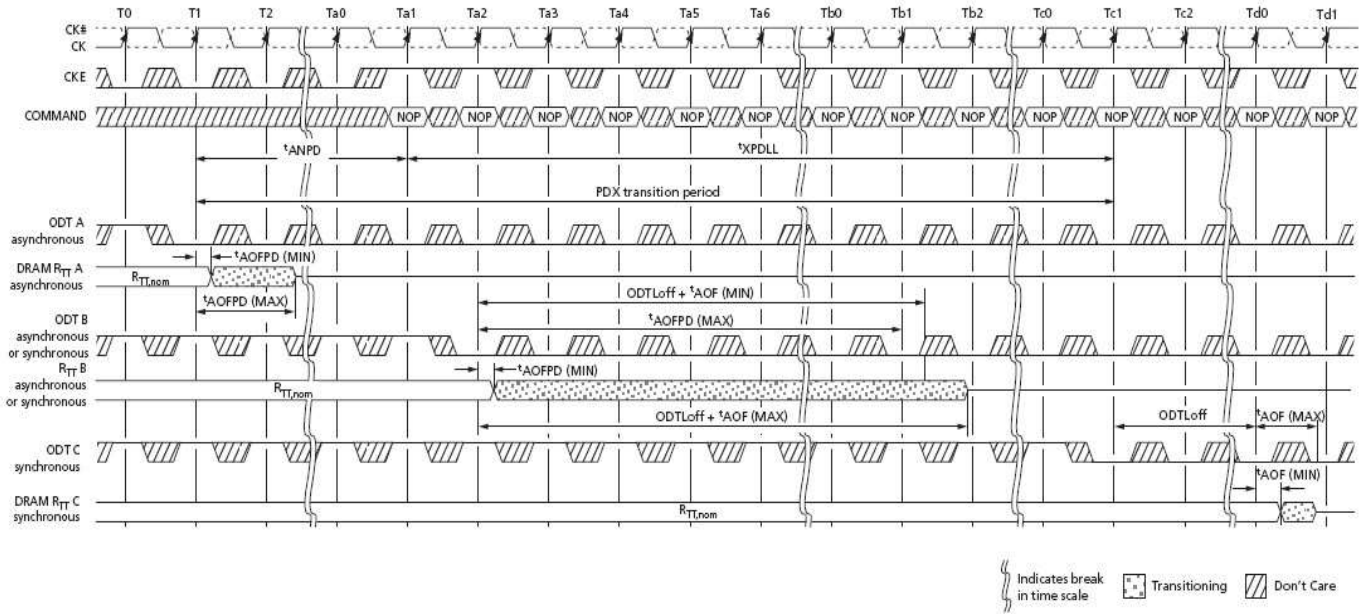


Figure 4-108: Asynchronous to Synchronous Transition During Precharge Power-Down (DLL Off) Exit

Note:

1. CL = 6; AL = CL - 1; CWL = 5; ODTLoff = WL - 2 = 8.

Asynchronous to Synchronous ODT Mode Transition (Short CKE Pulse)

If the time in the precharge power-down or idle states is very short (short CKE LOW pulse), the power-down entry and power-down exit transition periods overlap. When overlap occurs, the response of the DRAM's R_{TT} to a change in the ODT state can be synchronous or asynchronous from the start of the power-down entry transition period to the end of the power-down exit transition period, even if the entry period ends later than the exit period.

If the time in the idle state is very short (short CKE HIGH pulse), the power-down exit and power-down entry transition periods overlap. When this overlap occurs, the response of the DRAM's R_{TT} to a change in the ODT state may be synchronous or asynchronous from the start of power-down exit transition period to the end of the powerdown entry transition period.

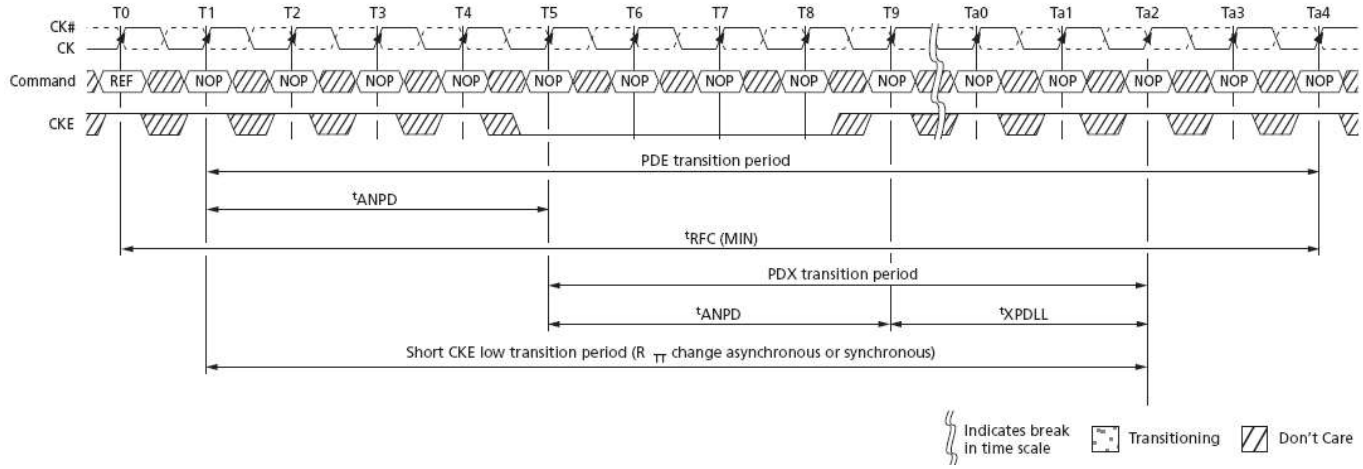


Figure 4-109: Transition Period for Short CKE LOW Cycles with Entry and Exit Period Overlapping

Note:

1. AL = 0, WL = 5, tANPD = 4.

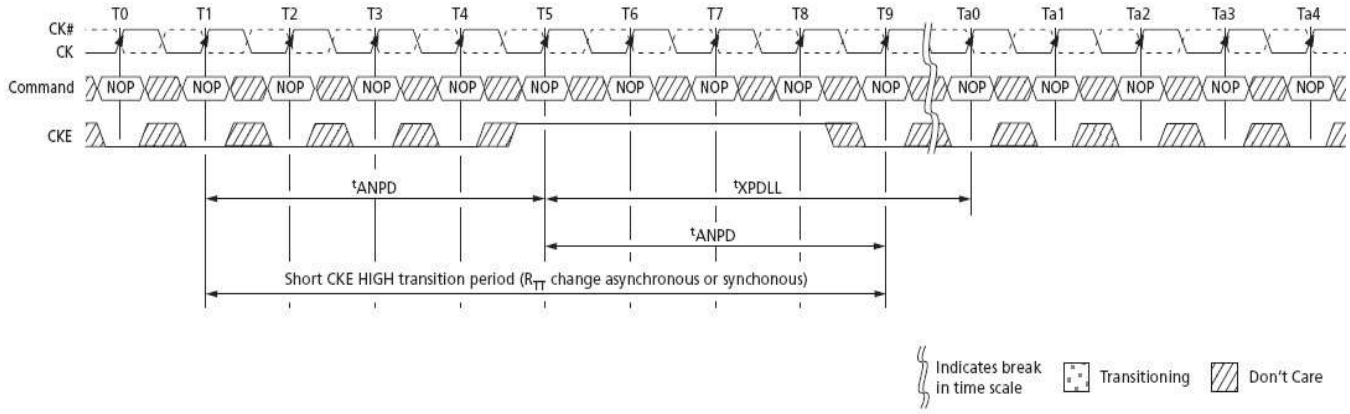


Figure 4-110: Transition Period for Short CKE HIGH Cycles with Entry and Exit Period Overlapping

Note:

1. AL = 0, WL = 5, tANPD = 4.

NAND FLASH SPECIFICATION

General Description

The XC3D31BAH-DINA NAND FLASH memory provides a storage solution for embedded systems with limited space, pins and power. It is ideal for code shadowing to RAM, solid state applications and storing media data such as, voice, video, text and photos. The device operates on a single 2.7V to 3.6V power supply with active current consumption as low as 25mA at 3V and 10uA for CMOS standby current.

The memory array totals 276,824,064bytes, and organized into 2,048 erasable blocks of 135,168bytes. Each block consists of 64 programmable pages of 2,112bytes each. Each page consists of 2,048bytes for the main data storage area and 64bytes for the spare data area (The spare area is typically used for error management functions).

The XC3D31BAH-DINA supports the standard NAND FLASH memory interface using the multiplexed 8-bit bus to transfer data, addresses, and command instructions. The five control signals, CLE, ALE, CE#, RE# and WE# handle the bus interface protocol. Also, the device has two other signal pins, the WP# (Write Protect) and the R/B# (Ready/Busy) for monitoring the device status.

Addressing

Table 5-1 Address Cycle Map

Bus cycle	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st Cycle	A7	A6	A5	A4	A3	A2	A1	A0
2nd Cycle	L	L	L	L	A11	A10	A9	A8
3rd Cycle	A19	A18	A17	A16	A15	A14	A13	A12
4th Cycle	A27	A26	A25	A24	A23	A22	A21	A20
5th Cycle	L	L	L	L	L	L	L	A28

Notes:

1. “L” indicates a low condition, which must be held during the address cycle to insure correct processing.
2. A0 to A11 during the 1st and 2nd cycles are column addresses. A12 to A28 during the 3rd, 4th and 5th cycles are row addresses.
3. A18 is plane address
4. The device ignores any additional address inputs that exceed the device’s requirement.

MODE SELECTION TABLE

Table 5-2 Mode Selection

MODE		CLE	ALE	CE#	WE#	RE#	WP#
Read mode	Command input	H	L	L		H	X
	Address input	L	H	L		H	X
Program Erase mode	Command input	H	L	L		H	H
	Address input	L	H	L		H	H
Data input		L	L	L		H	H
Sequential Read and Data output		L	L	L	H		X
During read (busy)		X	X	X	X	H	X
During program (busy)		X	X	X	X	X	H
During erase (busy)		X	X	X	X	X	H
Write protect		X	X	X	X	X	L
Standby		X	X	H	X	X	0V/Vcc

Notes:

1. “H” indicates a HIGH input level, “L” indicates a LOW input level, and “X” indicates a Don’t Care Level.

2. WP# should be biased to CMOS HIGH or LOW for standby.

COMMAND TABLE

Table 5-3 Command Table

COMMAND	1st CYCLE	2nd CYCLE	3rd CYCLE	4th CYCLE	Acceptable during busy
PAGE READ	00h	30h			
READ for COPY BACK	00h	35h			
SEQUENTIAL CACHE READ	31h				
RANDOM CACHE READ	00h	31h			
LAST ADDRESS CACHE READ	3Fh				
READ ID	90h				
READ STATUS	70h				Yes
RESET	FFh				Yes
PAGE PROGRAM	80h	10h			
PROGRAM for COPY BACK	85h	10h			
CACHE PROGRAM	80h	15h			
BLOCK ERASE	60h	D0h			
RANDOM DATA INPUT*1	85h				
RANDOM DATA OUTPUT*1	05h	E0h			
READ PARAMETER PAGE	ECh				
READ UNIQUE ID	EDh				
GET FEATURES	EEh				
SET FEATURES	EFh				
READ STATUS ENHANCED	78h				Yes
TWO PLANE READ PAGE	00h	00h	30h		
TWO PLANE READ FOR COPY BACK	00h	00h	35h		
TWO PLANE RANDOM DATA READ	06h	E0h			
TWO PLANE PROGRAM(TRADITIONAL)	80h	11h	81h	10h	
TWO PLANE PROGRAM(ONFI)	80h	11h	80h	10h	
TWO PLANE CACHE PROGRAM(START/CONTINUE)(TRADITIONAL)	80h	11h	81h	15h	
TWO PLANE CACHE PROGRAM(START/CONTINUE) (ONFI)	80h	11h	80h	15h	
TWO PLANE CACHE PROGRAM(END)(TRADITIONAL)	80h	11h	81h	10h	
TWO PLANE CACHE PROGRAM(END)(ONFI)	80h	11h	80h	10h	
TWO PLANE PROGRAM FOR COPY BACK(TRADITIONAL)	85h	11h	81h	10h	
TWO PLANE PROGRAM FOR COPY BACK(ONFI)	85h	11h	85h	10h	
TWO PLANE BLOCK ERASE(TRADITIONAL)	60h	60h	D0h		
TWO PLANE BLOCK ERASE(ONFI)	60h	D1h	60h	D0h	

Notes:

1. RANDOM DATA INPUT and RANDOM DATA OUTPUT command is only to be used within a page.

2. Any commands that are not in the above table are considered as undefined and are prohibited as inputs.

3. Do not cross plane address boundaries when using Copy Back Read and Program for copy back.

Device Operations

READ Operation

PAGE READ (00h-30h)

When the device powers on, 00h command is latched to command register. Therefore, system only issues five address cycles and 30h command for initial read from the device. This operation can also be entered by writing 00h command to the command register, and then write five address cycles, followed by writing 30h command. After writing 30h command, the data is transferred from NAND array to Data Register during $_{t}$R. Data transfer progress can be done by monitoring the status of the R/B# signal output. R/B# signal will be LOW during data transfer. Also, there is an alternate method by using the READ STATUS (70h) command. If the READ STATUS command is issued during read operation, the Read (00h) command must be re-issued to read out the data from Data Register. When the data transfer is complete, R/B# signal goes HIGH, and the data can be read from Data Register by toggling RE#. Read is sequential from initial column address to the end of the page. (See Figure 5-1)

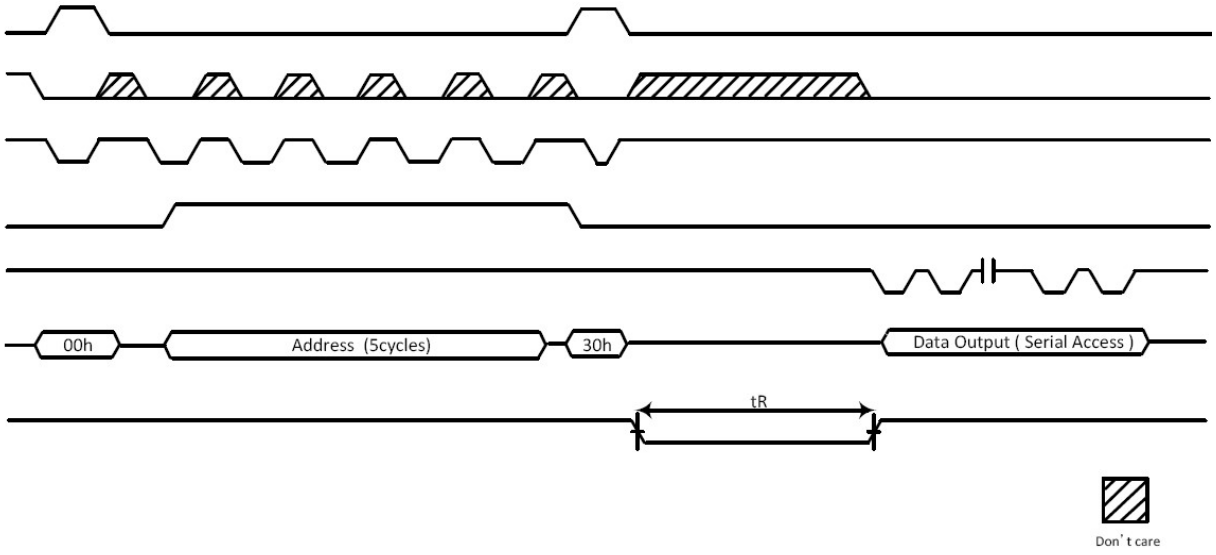


Figure 5-1 Page Read Operations

CACHE READ OPERATIONS

To obtain a higher degree of performance read operations, the device's Cache and Data Register can be used independent of each other. Data can be read out from the Cache Register, while array data is transferred from the NAND Array to the Data Register.

The CACHE READ mode starts with issuing a PAGE READ command (00h-30h) to transfer a page of data from NAND array to the Cache Register. R/B# signal will go LOW during data transfer indicating a busy status. Copying the next page of data from the NAND array to the Data Register while making the Cache Register page data available is done by issuing either a SEQUENTIAL CACHE READ (31h) or RANDOM CACHE READ (00h-31h) command. The SEQUENTIAL CACHE READ mode will copy the next page of data in sequence from the NAND array to the Data Register or use the RANDOM CACHE READ mode (00h-31h) to copy a random page of data from NAND array to the Data Register. The R/B# signal goes LOW for a period of t_{RCBSY} during the page data transfer from NAND array to the Data Register. When R/B# goes HIGH, this means that the Cache Register data is available and can be read out of the Cache Register by with toggling RE#, which starts at address column 0. If it is desired to start at a different column address, a RANDOM DATA OUTPUT (05h-E0h) command can be used to change the column address to read out the data.

At this point in the procedure when completing the read of the desired number of bytes, one of two things can be chosen. Continue CACHE READ (31h or 00h-31h) operations or end the CACHE READ mode with a LAST ADDRESS CACHE READ (3Fh) command.

To continue with the read operations, execute the CACHE READ (31h or 00h-31h) command. The R/B# signal goes LOW for the period of t_{RCBSY} while data is copied from Data Register to the Cache Register and the next page of data starts being copied from the NAND array to the Data Register. When R/B# signal goes HIGH signifying that the Cache Register data is available, at this time RE# can start toggling to output the desired data starting at column 0 address or using the RANDOM DATA OUTPUT command for random column address access.

To terminate the CACHE READ operations a LAST ADDRESS CACHE READ (3Fh) command is issued, R/B# signal goes LOW and the Data Register contents is copied to the Cache Register. At the completion of the Data Register to Cache Register transfer, R/B# goes HIGH indicating data is available at the output of the Cache Register. At this point Data can be read by toggling RE# starting at column address 0 or using the RANDOM DATA OUTPUT command for random column address access. The device NAND array is ready for next command set.

SEQUENTIAL CACHE READ (31h)

The SEQUENTIAL CACHE READ (31h) copies the next page of data in sequence within block to the Data Register while the previous page of data in the Cache Register is available for output. This is done by issuing the command (31h), R/B# signal goes LOW and the SR bits 6 and 5 = “00” for the period of $_{t}$RCBSY. When R/B# signal goes HIGH and SR bits 6 and 5 = “10”, data at the Cache Register is available. The data can be read out from the Cache Register by toggling RE#, starting address is column 0 or by using the RANDOM DATA OUTPUT command for random column address access.

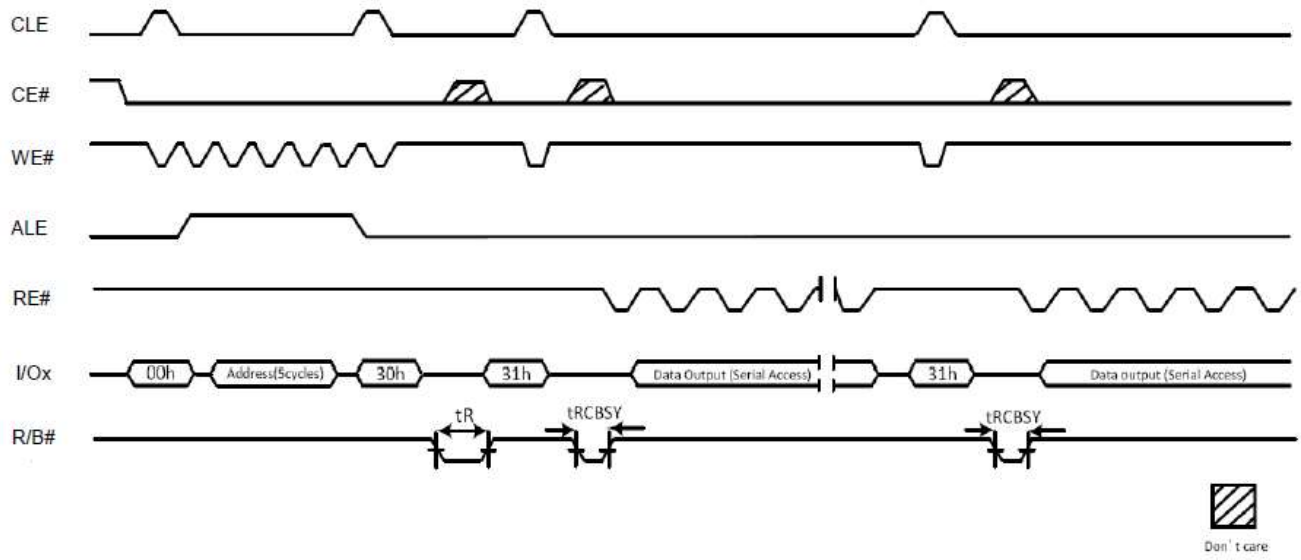


Figure 5-2 Sequential Cache Read Operations

RANDOM CACHE READ (00h-31h)

The RANDOM CACHE READ (00h-31h) will copy a particular page from NAND array to the Data Register while the previous page of data is available at the Cache Register output. Perform this function by first issuing the 00h command to the Command Register, then writing the five address cycles for the desired page of data to the Address Register. Then write the 31h command to the Command Register. Note; the column address bits are ignored.

After the RANDOM CACHE READ command is issued, R/B# signal goes LOW and SR bits 6 and 5 equal “00” for the period of $_{t}$RCBSY. When R/B# signal goes HIGH and SR bits 6 and 5 equal “10”, the page data in the Cache Register is available. The data can read out from the Cache Register by toggling RE#, the starting column address will be 0 or use the RANDOM DATA OUTPUT (05h-E0h) command change the column address to start reading out the data.

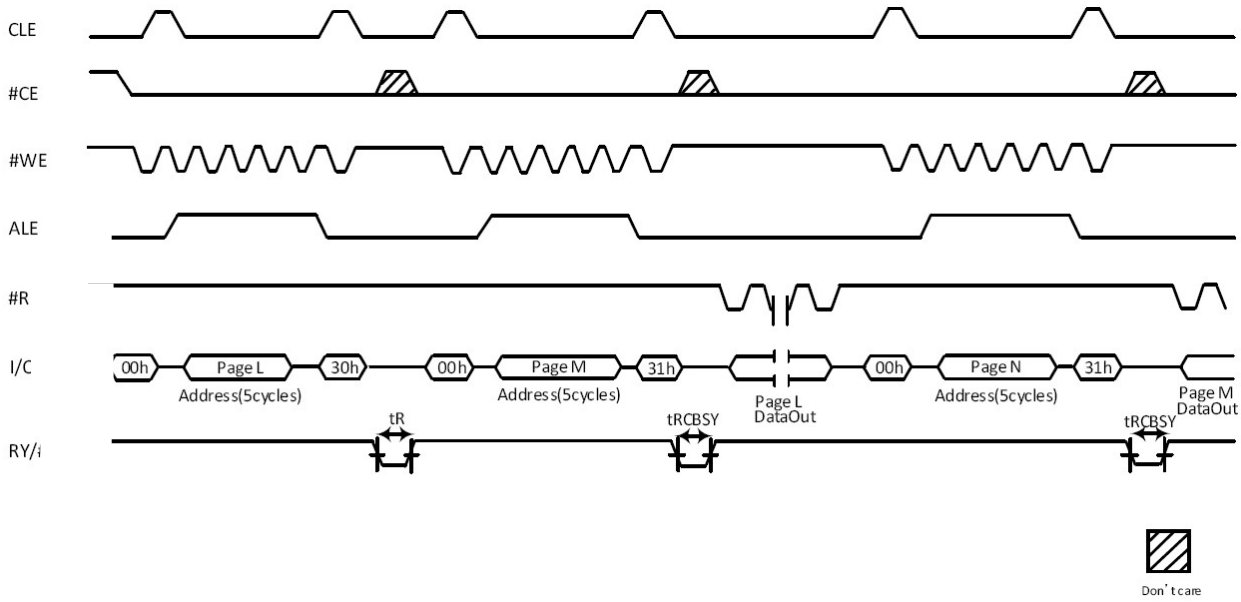


Figure 5-3 Random Cache Read Operation

LAST ADDRESS CACHE READ (3Fh)

The LAST ADDRESS CACHE READ (3Fh) copies a page of data from the Data Register to the Cache Register without starting the another cache read. After writing the 3Fh command, R/B# signal goes LOW and SR bits 6 and 5 equals “00” for the period of $_{t}$RCBSY. When R/B# signal goes HIGH and SR bits 6 and 5 equals “11”, the Cache Register data is available, and the device NAND array is in ready state. The data can read out from the Cache Register by toggling RE#, starting at address column 0 or us RANDOM DATA OUTPUT (05h-E0h) command to change the column address to read out the data.

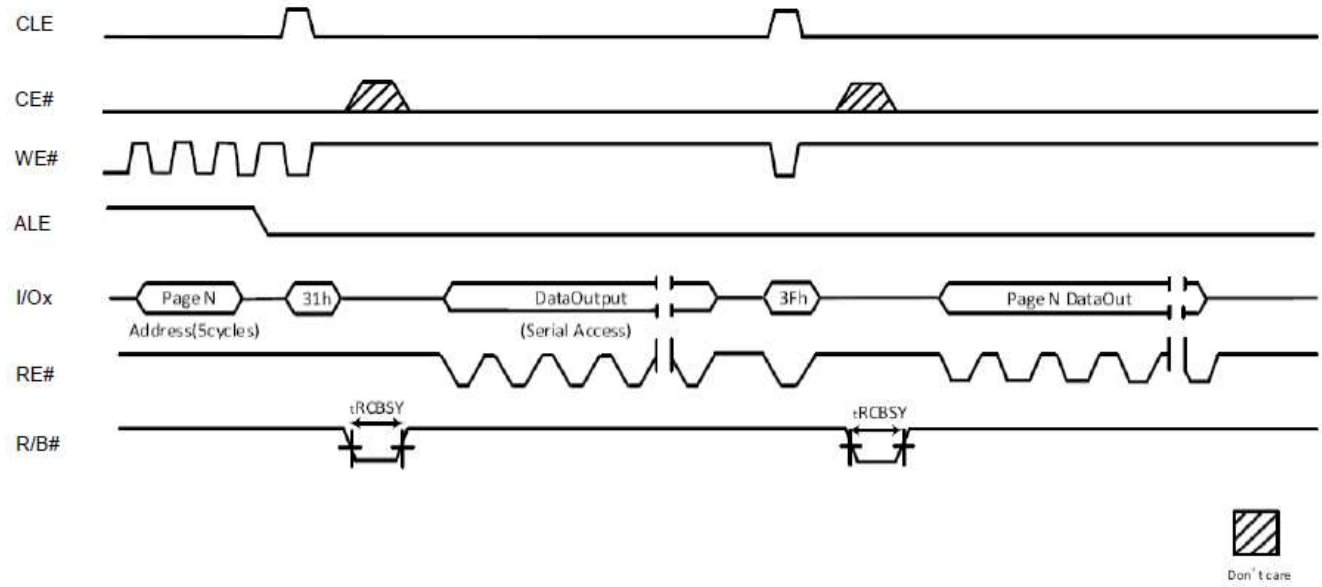


Figure 5-4 Last Address Cache Read Operation

TWO PLANE READ (00h-00h-30h)

TWO PLANE READ (00h-00h-30h) transfers two pages data from the NAND array to the data registers. Each page address have to be indicated different plane address.

To set the TWO PLANE READ mode, write the 00h command to the command register, and then write five address cycles for plane 0. Secondly, write the 00h command to the command register, and five address cycles for plane 1. Finally, the 30h command is issued. The first-plane and second-plane addresses must be identical for all of issued address except plane address.

After the 30h command is written, page data is transferred from both planes to their respective data registers in $_{t}$R. R/B# goes LOW while these are transferred. When the transfers are complete, R/B# goes HIGH. To read out the data, at first, system writes TWO PLANE RAMDOM DATA READ (06h-E0h) command to select a plane, next, repeatedly pulse RE# to read out the data from selected plane. To change the plane address, issues TWO PLANE RANDOM DATA READ (06h-E0h) command to select another plane address, then repeatedly pulse RE# to read out the data from the selected plane data register.

Alternatively, data transfers can be monitored by the READ STATUS (70h). When the transfers are complete, SR bit 6 is set to 1. To read data from the first of the two planes even when READ STATUS ENHANCED (78h) command is used, the system must issue the TWO PLANE RANDOM DATA READ (06h-E0h) command at first and pulse RE# repeatedly.

Write a TWO PLANE RANDOM DATA READ (06h-E0h) command to select the other plane, after the data cycle is complete. Pulse RE# repeatedly to output the data beginning at the specified column address,

During TWO PLANE READ operation, the READ STATUS ENHANCED (78h) command is prohibited.

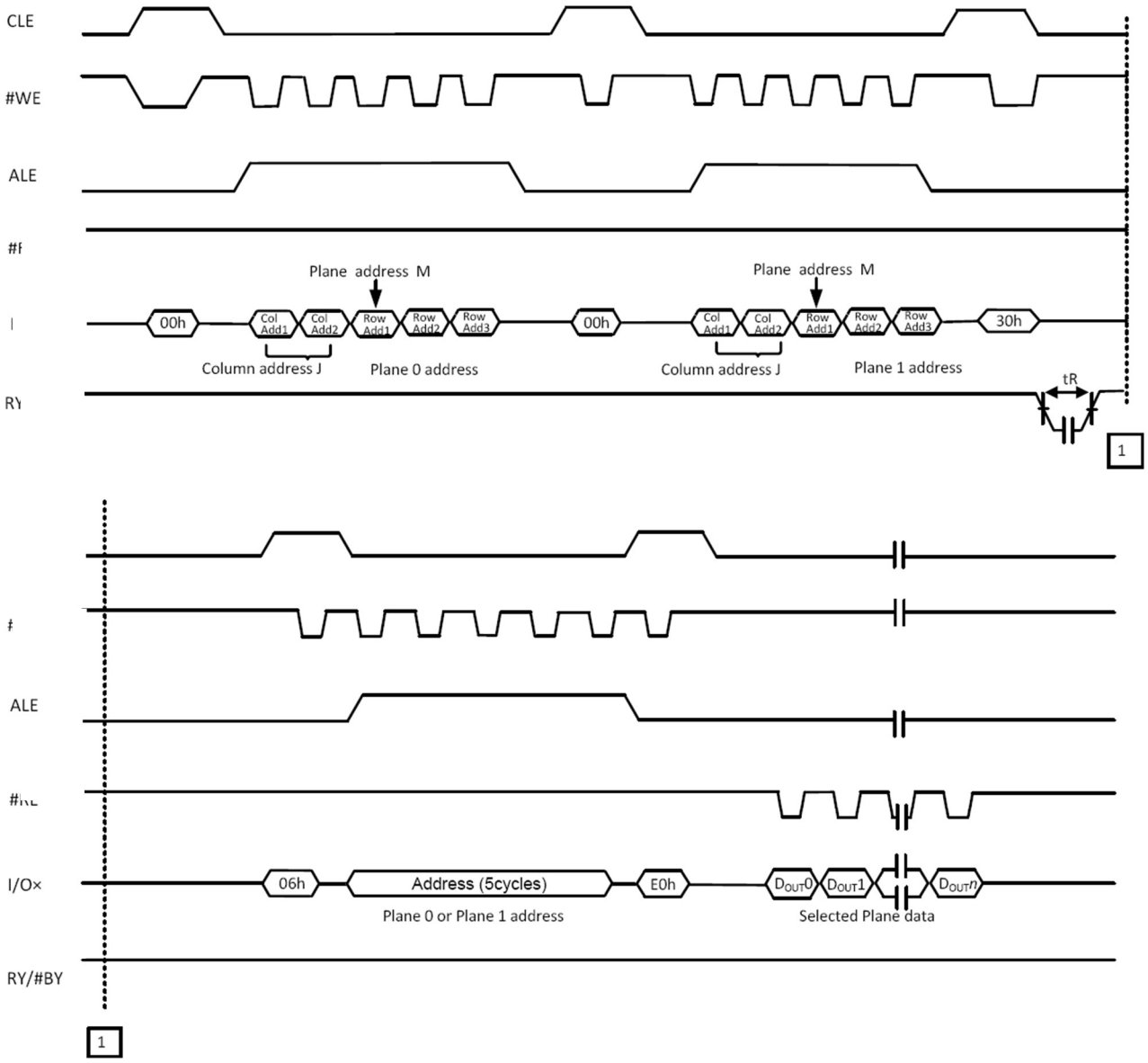


Figure 5-5 Two Plane Read Page (00h-00h-30h) Operation

RANDOM DATA OUTPUT (05h-E0h)

The RANDOM DATA OUTPUT allows the selection of random column addresses to read out data from a single or multiple of addresses. The use of the RANDOM DATA OUTPUT command is available after the PAGE READ (00h-30h) sequence by writing the 05h command following by the two cycle column address and then the E0h command. Toggling RE# will output data sequentially. The RANDOM DATA OUTPUT command can be issued multiple times, but limited to the current loaded page.

Figure 5-6 Random Data Output

TWO PLANE RANDOM DATA OUTPUT (06h-E0h)

TWO PLANE RANDOM DATA READ (06h-E0h) command can indicate to specified plane and column address on cache register. This command is accepted by a device when it is ready. Issuing 06h to the command register, two column address cycles, three row address cycles, E0h are followed, this enables data output mode on the address device's cache register at the specified column address. After the E0h command, the host have to wait at least t_{WHR} before requesting data output. The selected device is in data output mode until another valid command is issued.

The TWO PLANE RANDOM DATA READ (06h-E0h) command is used to select the cache register to be enabled for data output. When the data output is complete on the selected plane, the command can be issued again to start data output on another plane.

If there is a need to update the column address without selecting a new cache register, the RANDOM DATA READ (05h-E0h) command can be used instead.

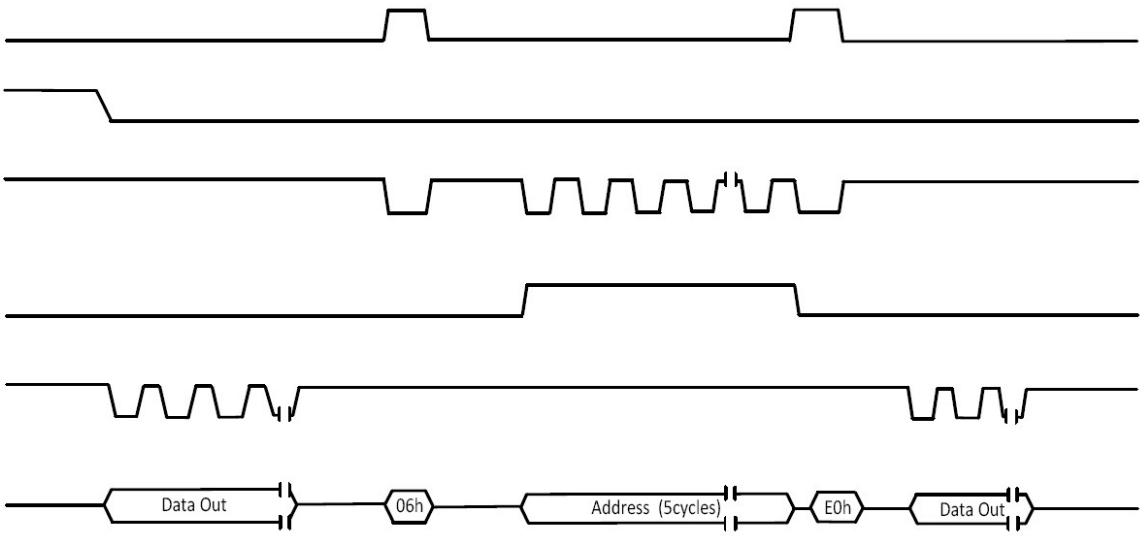


Figure 5-7 Two Plane Random Data Read (06h-E0h) Operation

READ ID (90h)

READ ID command is comprised of two modes determined by the input address, device (00h) or ONFI (20h) identification information. To enter the READ ID mode, write 90h to the Command Register followed by a 00h address cycle, then toggle RE# for 5 single byte cycles, XC3D31BAH-DINA. The pre-programmed code includes the Manufacturer ID, Device ID, and Product-Specific Information (see Table 5-4). If the READ ID command is followed by 20h address, the output code includes 4 single byte cycles of ONFI identifying information (See Table 5-5). The device remains in the READ ID Mode until the next valid command is issued.

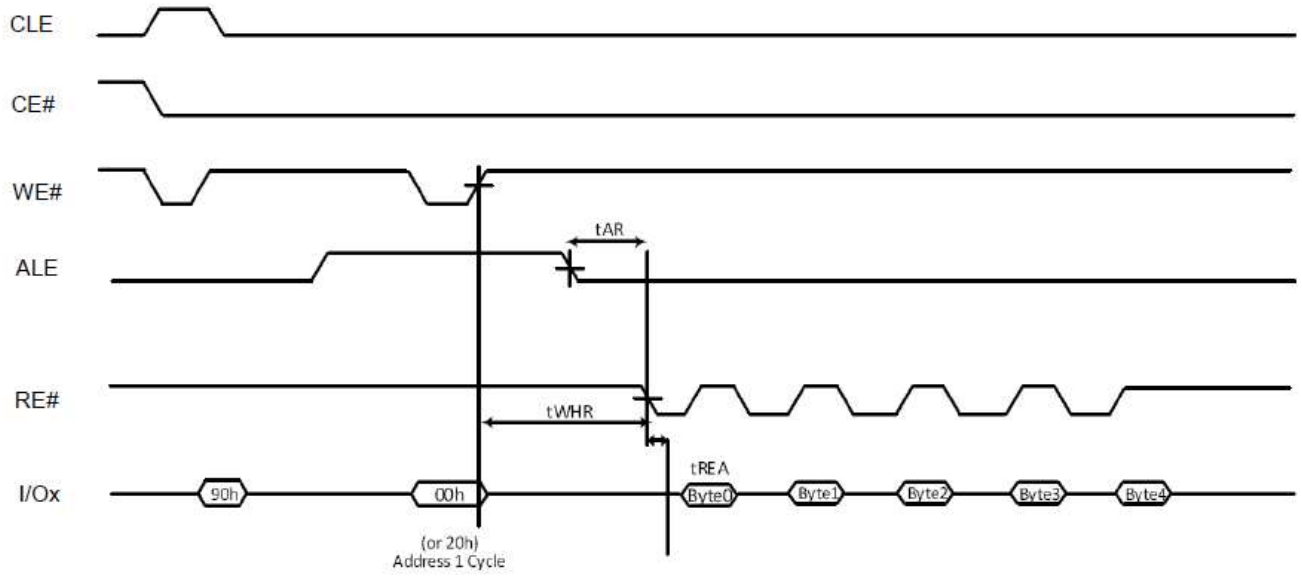


Figure 5-8 Read ID

Table 5-4 Device ID and configuration codes for Address 00h

Part Number	1st Byte/Cycle	2nd Byte/Cycle	3rd Byte/Cycle	4th Byte/Cycle	5th Byte/Cycle
XC3D31BAH-DINA	EFh	DAh	90h	95h	04h
Description	MFR ID	Device ID	Cache Programming Supported	Page Size:2KB Spare Area Size:64b BLK Size w/o Spare:128KB	

Table 5-5 ONFI identifying codes for Address 20h

Part Number	1st Byte/Cycle	2nd Byte/Cycle	3rd Byte/Cycle	4th Byte/Cycle
XC3D31BAH-DINA	4Fh	4Eh	46h	49h

READ PARAMETER PAGE (ECh)

READ PARAMETER PAGE can read out the device's parameter data structure, such as, manufacturer information, device organization, timing parameters, key features, and other pertinent device parameters. The data structure is stored with at least three copies in the device's parameter page. Figure 5-9 shows the READ PARAMETER PAGE timing. The RANDOM DATA OUTPUT (05h- E0h) command is supported during data output.

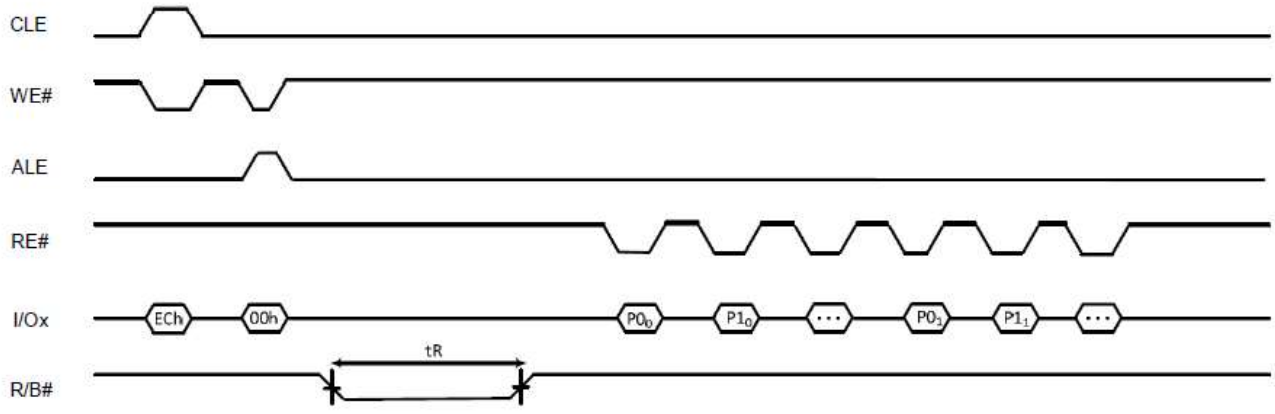


Figure 5-9 Read Parameter Page

Table 5-6 Parameter Page Output Value

Byte	Description		Value
0-3	Parameter page signature		4Fh, 4Eh, 46h, 49h
4-5	Revision number		02h, 00h
6-7	Features supported		18h,00h
8-9	Optional commands supported		3Fh,00h
10-31	Reserved		00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
32-43	Device manufacturer		57h, 49h, 4Eh, 42h, 4Fh, 4Eh, 44h, 20h, 20h, 20h, 20h, 20h
44-63	Device model	XC3D31BAH-DINA	57h,32h,39h,4Eh,30h,32h,47h,56h,20h,20h,20h,20h,20h,20h,20h, 20h, 20h, 20h, 20h, 20h, 20h
64	Manufacturer ID		EFh
65-66	Date code		00h, 00h
67-79	Reserved		00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
80-83	# of data bytes per page		00h, 08h, 00h, 00h
84-85	# of spare bytes per page		40h, 00h
86-89	# of data bytes per partial page		00h, 02h, 00h, 00h
90-91	# of spare bytes per partial page		10h, 00h
92-95	# of pages per block		40h, 00h, 00h, 00h
96-99	# of blocks per unit		00h, 08h, 00h, 00h
100	# of logical units		01h
101	# of address cycles		23h
102	# of bits per cell		01h
103-104	Bad blocks maximum per unit		28h, 00h
105-106	Block endurance		01h, 05h
107	Guaranteed valid blocks at beginning of target		01h
108-109	Block endurance for guaranteed valid blocks		00h, 00h
110	# of programs per page		04h
111	Partial programming attributes		00h
112	# of ECC bits		01h
113	# of interleaved address bits		01h
114	Interleaved operation attributes		0Ch
115-127	Reserved		00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h

Table 5-6 Parameter Page Output Value

Byte	Description	Value
128	I/O pin capacitance	0Ah
129-130	Timing mode support	1Fh, 00h
131-132	Program cache timing	1Fh, 00h
133-134	Maximum page program time	BCh, 02h
135-136	Maximum block erase time	10h, 27h
137-138	Maximum random read time	19h, 00h
139-140	$_t$CCS minimum	46h, 00h
141-163	Reserved	00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
164-165	Vendor specific revision #	01h,00h
166-253	Vendor specific	00h
254-255	Integrity CRC	Set at shipment
256-511	Value of bytes 0-255	
512-767	Value of bytes 0-255	
>767	Additional redundant parameter pages	

READ STATUS (70h)

The XC3D31BAH-DINA has an 8-bit Status Register which can be read during device operation. Refer to Table 5-6 for specific Status Register definitions. After writing 70h command to the Command Register, read cycles will only read from the Status Register. The status can be read from I/O [7:0] outputs, as long as CE# and RE# are LOW. Note; RE# does not need to be toggled for Status Register read. The Command Register remains in status read mode until another command is issued. To change to normal read mode, issue the PAGE READ (00h) command. After the PAGE READ command is issued, data output starts from the initial column address.

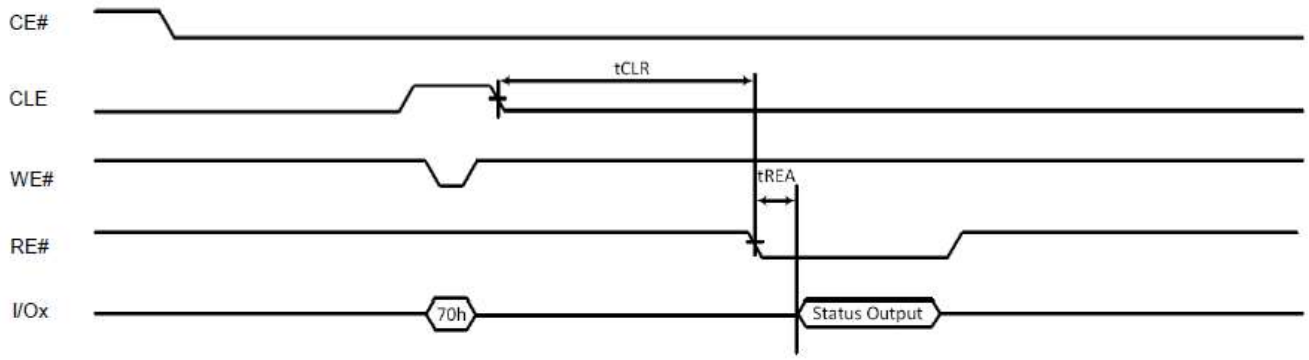


Figure 5-10 Read Status Operation

Table 5-7 Status Register Bit Definition

SR bit	Page Read	Cache Read	Page Program	Cache Program	Block Erase	Definition
I/O 0	Not Use	Not Use	Pass/Fail	Pass/Fail(N)	Pass/Fail	0=Successful Program/Erase 1=Error in Program/Erase
I/O 1	Not Use	Not Use	Not Use	Pass/Fail(N-1)	Not Use	0=Successful Program 1=Error in Program
I/O 2	Not Use	Not Use	Not Use	Not Use	Not Use	0
I/O 3	Not Use	Not Use	Not Use	Not Use	Not Use	0
I/O 4	Not Use	Not Use	Not Use	Not Use	Not Use	0
I/O 5	Ready/Busy	Ready/Busy1	Ready/Busy	Ready/Busy	Ready/Busy	Ready = 1 Busy = 0
I/O 6	Ready/Busy	Cache Ready/Busy2	Ready/Busy	Cache Ready/Busy	Ready/Busy	Ready = 1 Busy = 0
I/O 7	Write Protect	Write Protect	Write Protect	Write Protect	Write Protect	Unprotected = 1 Protected = 0

Notes:

1. SR bit 5 is 0 during the actual programming operation. If cache mode is used, this bit will be 1 when all internal operations are complete.

2. SR bit 6 is 1 when the Cache Register is ready to accept new data. R/B# follows bit 6.

READ STATUS ENHANCED (78h)

The READ STATUS ENHANCED (78h) command returns the status of the addressed plane on a target even when it is busy (SR bit 6 = 0).

Writing 78h to the command register, followed by three row address cycles containing the page, plane and block addresses that is same as executed addresses, puts the device into read status mode. The device stays in this mode until another valid command is issued.

The device status is returned when the host requests data output. The SR bit 6 and SR bit 5 bits of the status register are shared for all planes on the device. The SR bit 1 and SR bit 0 bits are specific to the plane specified in the row address.

The READ STATUS ENHANCED (78h) command also enables the device for data output. To begin data output following a READ operation after the device is ready (SR bit 6 = 1), issue the READ MODE (00h) command, then begin data output. If the host needs to change the cache register that will output data, use the TWO PLANE RANDOMDATA READ (06h-E0h) command after the device is ready

Use of the READ STATUS ENHANCED (78h) command is prohibited when OTP mode is enabled. It is also prohibited following some of the other reset, identification.

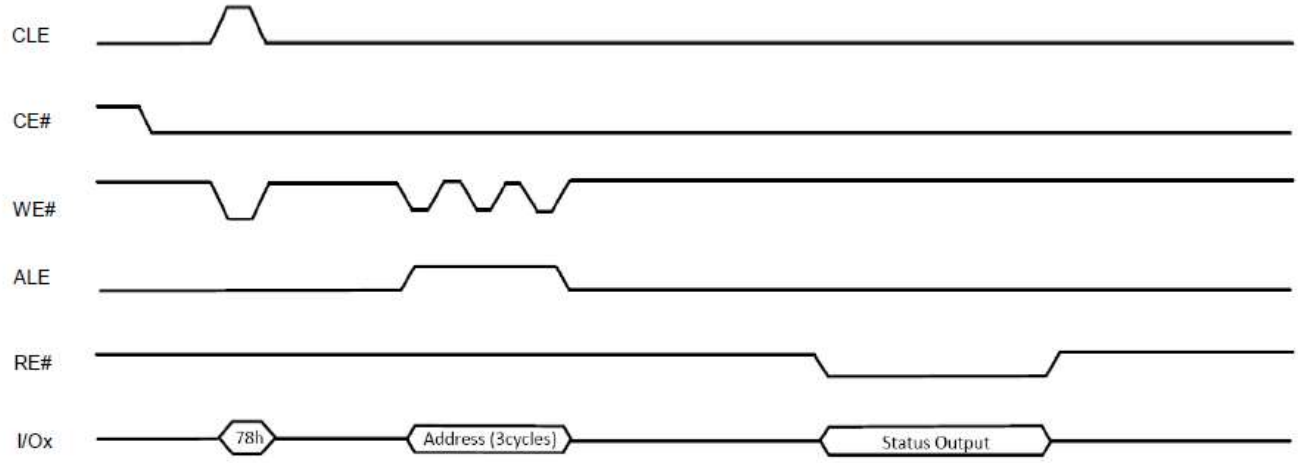


Figure 5-11 Read Status Enhanced (78h) Operation

READ UNIQUE ID (EDh)

The XC3D31BAH-DINA NAND FLASH device has a method to uniquely identify each NAND FLASH device by using the READ UNIQUE ID command. The format of the ID is limitless, but the ID for every NAND FLASH device manufactured, will be guaranteed to be unique.

Numerous NAND controllers typically use proprietary error correction code (ECC) schemes. In these cases CHIPSIP cannot protect unique ID data with factory programmed ECC. However, to ensure data reliability, CHIPSIP will program the NAND FLASH devices with 16 bytes of unique ID code, starting at byte 0 on the page, immediately followed by 16 bytes of the complement of that unique ID. The combination of these two actions is then repeated 16 times. This means the final copy of the unique ID will resides at location byte 511. At this point an XOR or exclusive operation can be performed on the first copy of the unique ID and its complement. If the unique ID is good, the results should yield all the bits as 1s. In the event that any of the bits are 0 after the XOR operation, the procedure can be repeated on a subsequent copy of the unique ID data.

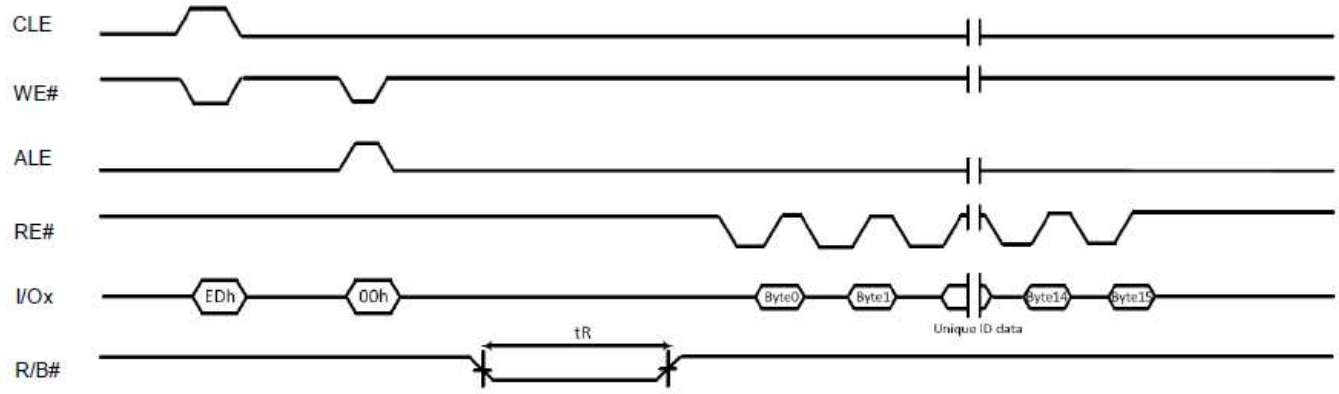


Figure 5-12 Read Unique ID

PROGRAM Operation

PAGE PROGRAM (80h-10h)

The XC3D31BAH-DINA Page Program command will program pages sequentially within a block, from the lower order page address to higher order page address. Programming pages out of sequence is prohibited. The XC3D31BAH-DINA supports partial-page programming operations up to 4 times before an erase is required if partitioning a page. Note; programming a single bit more than once without first erasing it is not supported.

SERIAL DATA INPUT (80h)

Page Program operation starts with the execution of the Serial Data Input command (80h) to the Command Register, following next by inputting five address cycles and then the data is loaded. Serial data is loaded to Cache Register with each WE# cycle. The Program command (10h) is written to the Command Register after the serial data input is finished. At this time the internal write state controller automatically executes the algorithms for program and verifies operations. Once the programming starts, determining the completion of the program process can be done by monitoring the R/B# output or the SR bit 6, which will follow the R/B# signal. R/B# will stay LOW during the internal array programming operation during the period of ($_t$PROG). During page program operation, only two commands are available, READ STATUS (70h) and RESET (FFh). When the device status goes to the ready state, SR bit 0 (I/O0) indicates whether the program operation passed (Bit0=0) or failed (Bit0=1), (see Figure 5-13). The Command Register remains in read status mode until the next command is issued.

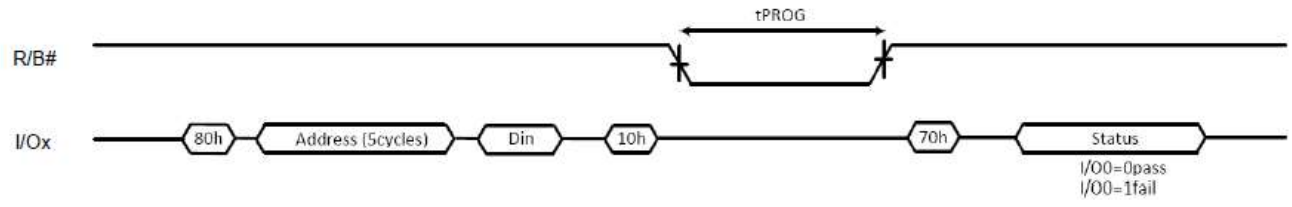


Figure 5-13 Page Program

RANDOM DATA INPUT (85h)

After the Page Program (80h) execution of the initial data has been loaded into the Cache Register, if the need for additional writing of data is required, using the RANDOM DATA INPUT (85h) command can perform this function to a new column address prior to the Program (10h) command. The RANDOM DATA INPUT command can be issued multiple times in the same page (See Figure 5-14).

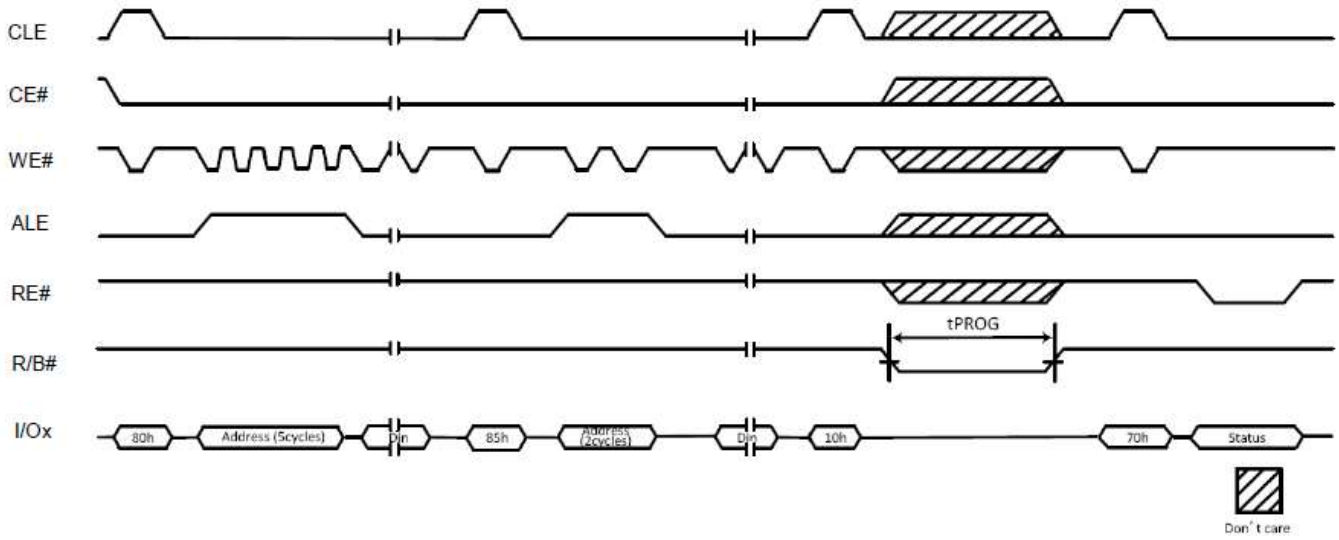


Figure 5-14 Random Data Input

CACHE PROGRAM (80h-15h)

CACHE PROGEAM (80h) command is started by writing the command to the Command Register. The next writes should be five cycles of address, and then either writing a full or partial page of input data into the Cache Register. Issuing the CACHE PROGRAM (15h) command to the Command Register, starting transferring data from the Cache Register to the Data Register on the rising edge of WE# and R/B# will go LOW. Programming to the array starts after the data has been copied into the Data Register and R/B# returns to HIGH.

When R/B# returns to HIGH, the next input data can be written to the Cache Register by issuing another CACHE PROGRAM command series. The time R/B# goes LOW, is typical controlled by the actual programming time. The time for the first programming pass equals the time it takes to transfer the data from the Cache Register to the Data Register. On the second and subsequent programming passes, data transfer from the Cache Register to the Data Register is held until Data Register content is programming into the NAND array.

The CACHE PROGRAM command can cross block address boundaries. RANDOM DATA INPUT (85h) commands are permitted with CACHE PROGRAM operations. Status Register's Cache R/B# Bit 6 (I/O6) can be read after issuing the READ STATUS (70h) command for confirming when the Cache Register is ready or busy. R/B#, always follows SR bit 6 (I/O6). Status Register's R/B# Bit 5 (I/O5) can be polled to determine whether the array programming is in progress or completed for the current programming cycle.

If only R/B# is used for detecting programming status, the last page of the program sequence must use the PAGE PROGRAM (10h) command instead of the CACHE PROGRAM (15h) command. If the CACHE PROGRAM (15h) command is used every time, including the last page programming, Status Register's Bit 5 (I/O5) must be used to determine when programming is complete.

Status Register's Pass/Fail, Bit 1 (I/O1) returns the pass/fail status for the previous page when Status Register's Bit 6 (I/O6) equals a "1" (ready state). The pass/fail status of the current PROGRAM operation is returned with Status Register's Bit 0 (I/O0) when Bit 5 (I/O5) of the Status Register equals a "1" (ready state) as shown in Figure 5-15 and 5-16.

The CACHE PROGRAM command cannot be used on blocks 0-3 if used as boot blocks.

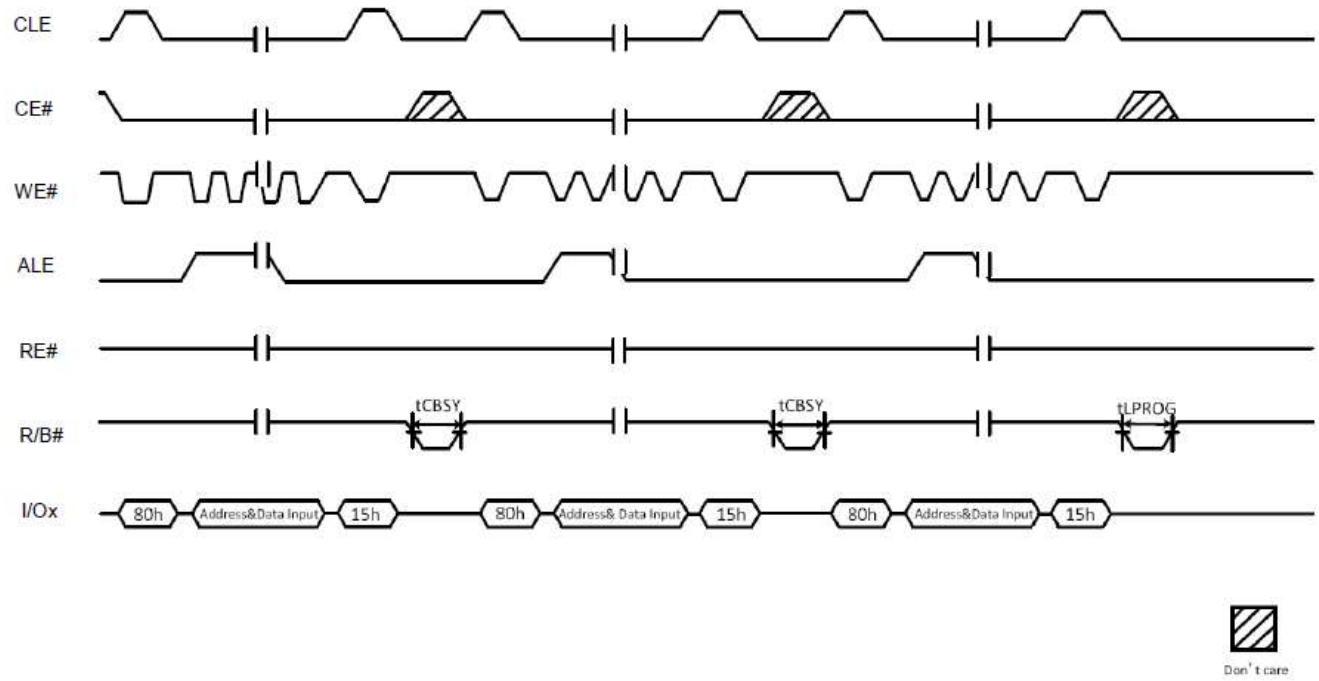


Figure 5-15 Cache Program Start

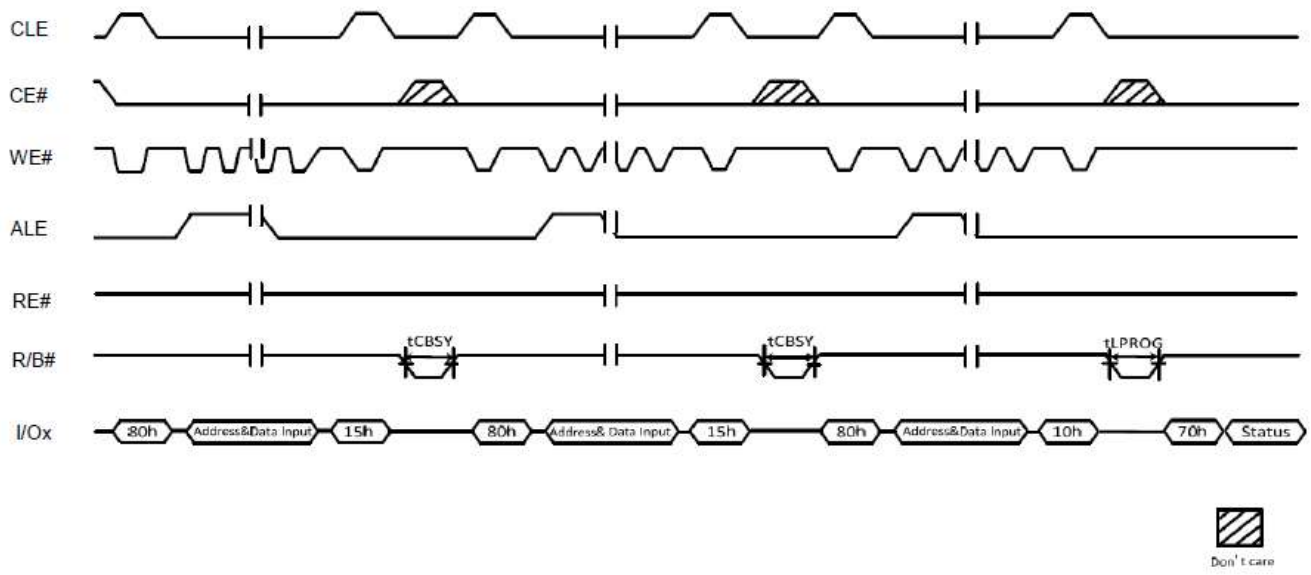


Figure 5-16 Cache Program End

TWO PLANE PAGE PROGRAM

TWO PLANE PAGE PROGRAM command make it possible for host to input data to the addressed plane's cache register and queue the cache register to be moved to the NAND FLASH array. This command can be issued several times. Each time a new plane address is specified that plane is also queued for data transfer. To input data for the final plane and to begin the program operation for all previously queued planes, either the PAGE PROGRAM command or the CACHE PROGRAM command have to be issued. All of the queued planes will move the data to the NAND FLASH array. When it is ready (SR bit 6 = 1), this command is accepted.

At the block and page address is specified, input a page to the cache register and queue it to be moved to the NAND FLASH array, the 80h is issued to the command register. Unless this command has been preceded by a TWO PLANE PAGE PROGRAM command, issuing the 80h to the command register clears all of the cache registers' contents on the selected target. Write five address cycles containing the column address and row address; data input cycles follow. Serial data is input beginning at the column address specified. At any time, while the data input cycle, the RANDOM DATA INPUT (85h) command can be issued. When data input is complete, write 11h to the command register. The device will go busy (SR bit 6 = 0, SR bit 5 = 0) for tDBSY.

To ascertain the progress of tDBSY, the host can monitor the target's R/B# signal or, the status operations (70h, 78h) can be used alternatively, When the device status shows that it is ready (SR bit 6 = 1), additional TWO PLANE PAGE PROGRAM commands can be issued to queue additional planes for data transfer, then, the PAGE PROGRAM or CACHE PROGRAM commands can be issued.

When the PAGE PROGRAM command is used as the final command of a two plane program operation, data is transferred from the cache registers to the NAND FLASH array for all of the addressed planes during tPROG. When the device is ready (SR bit 6 = 1, SR bit 5 = 1), the host should check the status of the SR bit 0 for each of the planes to verify that programming completed successfully.

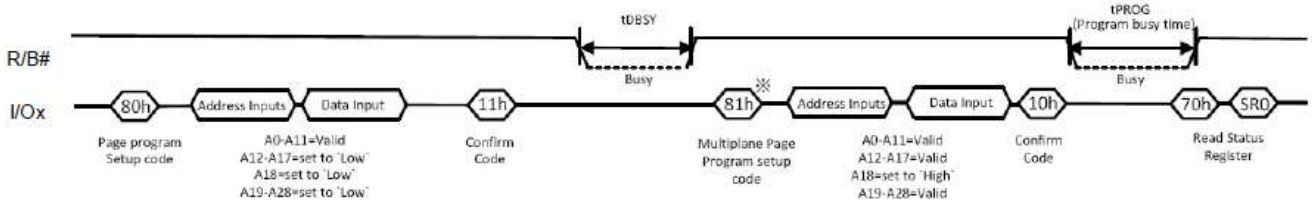
When the CACHE PROGRAM command is used as the final command of a program cache two plane operation, data is transferred from the cache registers to the data registers after the previous array operations completed. Then, the data is moved from the data registers to the NAND FLASH array for all of the addressed planes. This occurs while tCBSY. After tCBSY, the host should check the status of the SR bit 1 for each of the planes from the previous program cache operation, if any, to verify that programming completed successfully.

When system issues TWO PLANE PAGE PROGRAM, PAGE PROGRAM, and CACHE PROGRAM commands, READ STATUS (70h) command can confirm whether the operation(s) passed or failed. If the status after READ STATUS (70h) command indicates an error (SR bit 0 = 1 and/or SR bit 1 = 1), READ STATUS ENHANCED (78h) command can be determined which plane is failed.

TWO PLANE PROGRAM commands require five-cycle addresses, one address indicates the operational plane. These addresses are subject to the following requirements:

- The column address bits must be valid address for each plane
- The plane select bit, A18, must be set to “L” for 1st address input, and set to “H” for 2nd address input.
- The page address (A17-A12) and block address (A28-A19) of first input are don’t care. It follows secondary inputted page address and block address.

Two plane operations must be same type operation across the planes; for example, it is not possible to perform a PROGRAM operation on one plane with an ERASE operation on another.



1. The same row address, except for A18, is applied to the two blocks.
2. Any command between 11h and 81h is prohibited except 70h, 78h, and FFh

※81h: Traditional Protocol 80h: ONFI Protocol

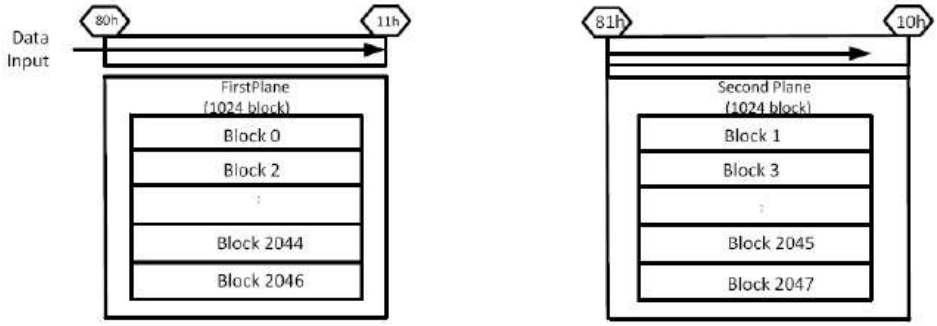
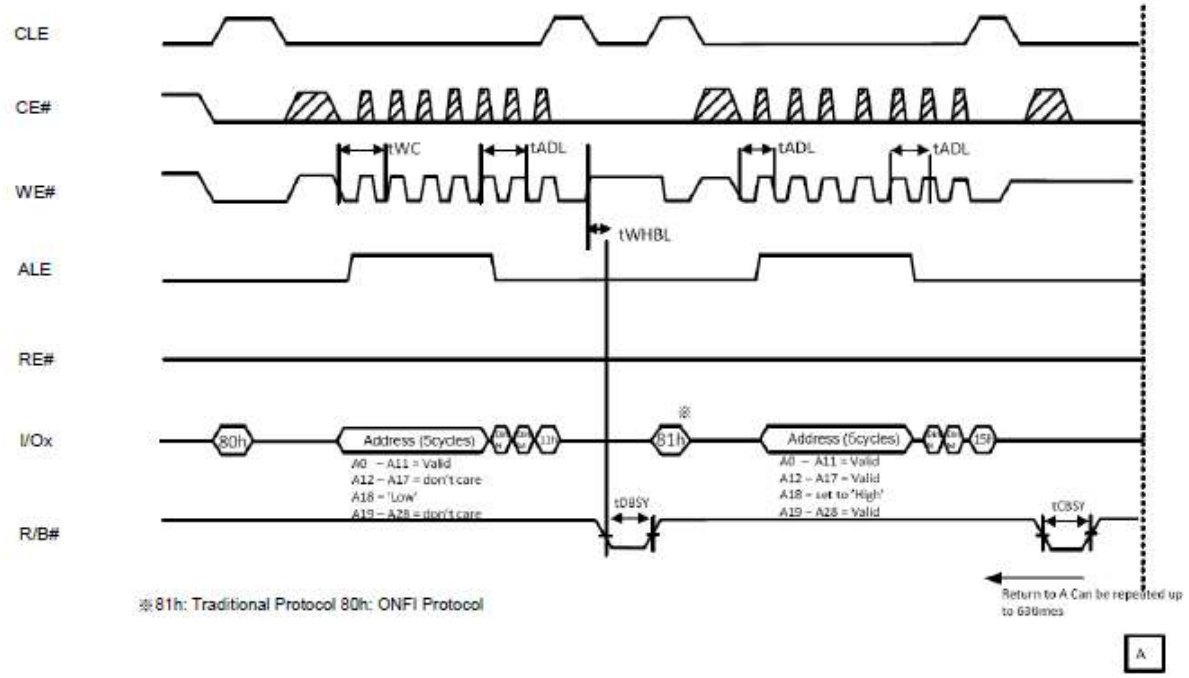
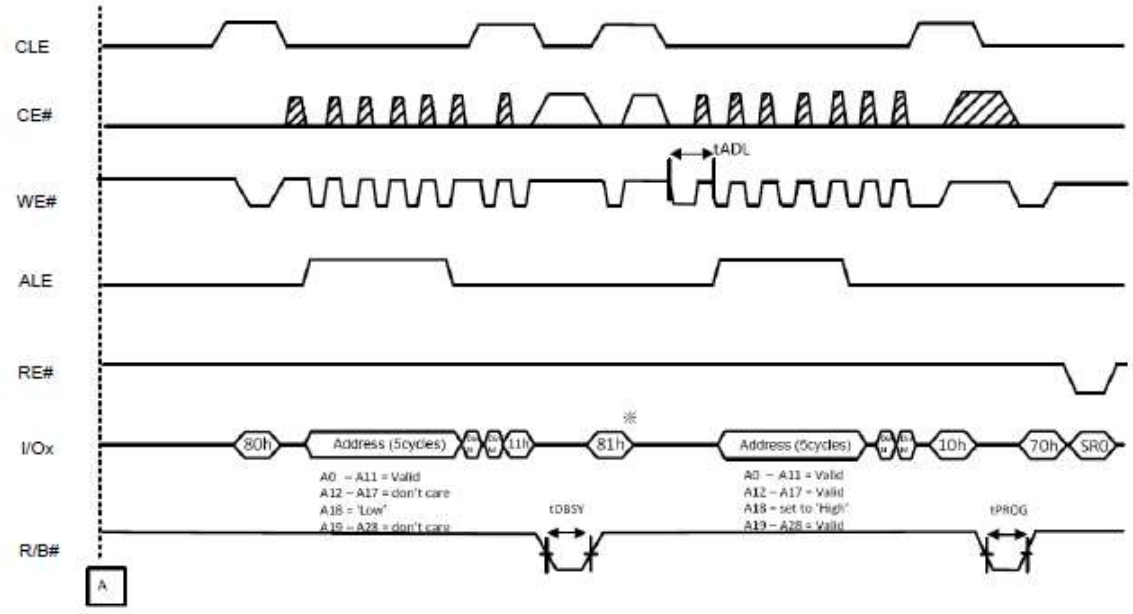


Figure 5-17 Two Plane Page Program





1. In this figure the Read Status Register (70h) is used, but the Read Status Enhanced

Figure 5-18 Two Plane Cache Program

COPY BACK Operation

Copy Back operations require two command sets. Issue a READ for COPY BACK (00h-35h) command first, then the PROGRAM for COPY BACK (85h-10h) command. Copy back operations are only supported within a same plane.

READ for COPY BACK (00h-35h)

The READ for COPY BACK command is used together with the PROGRAM for COPY BACK (85h- 10h) command. To start execution, READ for COPY BACK (00h) command is written to the Command Register, followed by the five cycles of the source page address. To start the transfer of the selected page data from the memory array to the Cache Register, write the 35h command to the Command Register.

After execution of the READ for COPY BACK command sequence and R/B# returns to HIGH marking the completion of the operation, the transferred data from the source page into the Cache Register may be read out by toggling RE#. Data is output sequentially from the column address that was originally specified with the READ for COPY BACK command. RANDOM DATA OUTPUT (05h- E0h) commands can be issued multiple times without any limitation after READ for COPY BACK command has been executed (see Figures 5-19 and 5-20).

At this point the device is in ready state to accept the PROGRAM for COPY BACK command.

PROGRAM for COPY BACK (85h-10h)

After the READ for COPY BACK command operation has been completed and R/B# goes HIGH, the PROGRAM for COPY BACK command can be written to the Command Register. The command results in the transfer of data from the Cache Register to the Data Register, then internal operations start programming of the new destination page. The sequence would be, write 85h to the Command Register, followed by the five cycle destination page address to the NAND array. Next write the 10h command to the Command Register; this will signal the internal controller to automatically start to program the data to new destination page. During this programming time, R/B# will LOW. The READ STATUS command can be used instead of the R/B# signal to determine when the program is complete. When SR bit 6 (I/O6) equals to “1”, SR bit 0 (I/O0) will indicate if the operation was successful or not.

The RANDOM DATA INPUT (85h) command can be used during the PROGRAM for COPY BACK command for modifying the original data. Once the data is copied into the Cache Register using the READ for COPY BACK (00h-35h) command, follow by writing the RANDOM DATA INPUT (85h) command, along with the address of the data to be changed. The data to be changed is placed on the external data pins. This operation copies the data into the Cache Register. Once the 10h command is written to the Command Register, the original data and the modified data are transferred to the Data Register, and programming of the new page commences. The RANDOM DATA INPUT command can be issued numerous times without limitation, as necessary before starting the programming sequence with 10h command.

Since COPY BACK operations do not use external memory and the data of source page might include a bit errors, a competent ECC scheme should be developed to check the data before programming data to a new destination page.

TWO PLANE READ for COPY BACK

To improve read through rate, TWO PLANE READ for COPY BACK operation is copied data concurrently from one or two plane to the specified cache registers.

TWO PLANE PROGRAM for COPY BACK command can move the data in two pages from the cache registers to different pages. This operation improves system performance than PROGRAM for COPY BACK operation.

TWO PLANE PROGRAM for COPY BACK

Function of TWO PLANE PROGRAM for COPY BACK command is equal to TWO-PLANE PAGE PROGRAM command, except that when 85h is written to the command register, then cache register contents are not cleared. Refer to TWO-PLANE PAGE PROGRAM for more details features.

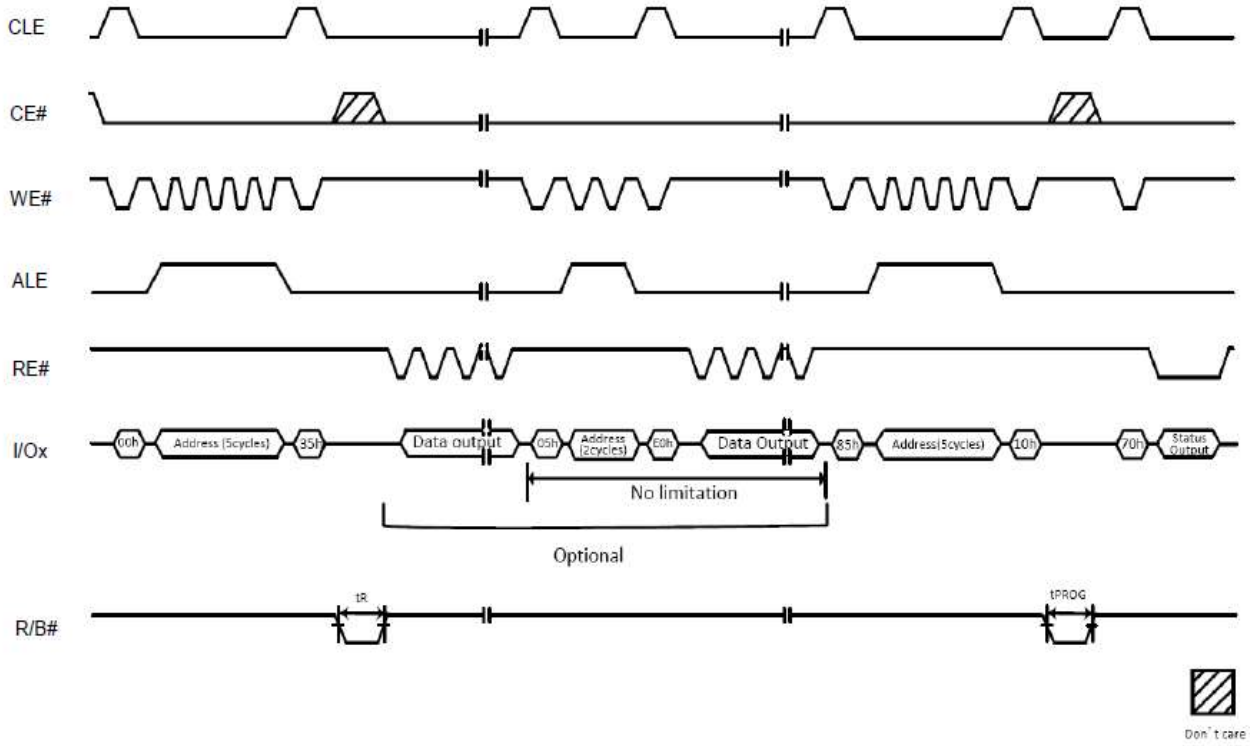


Figure 5-19 Program for copy back Operation

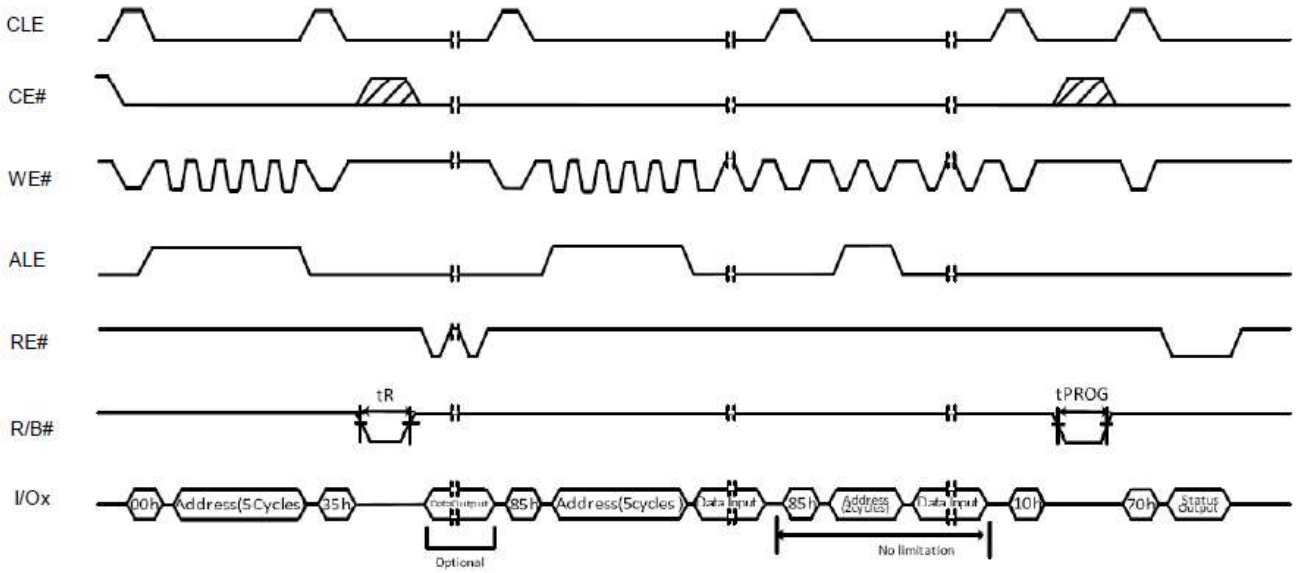


Figure 5-20 Copy Back Operation with Random Data Input

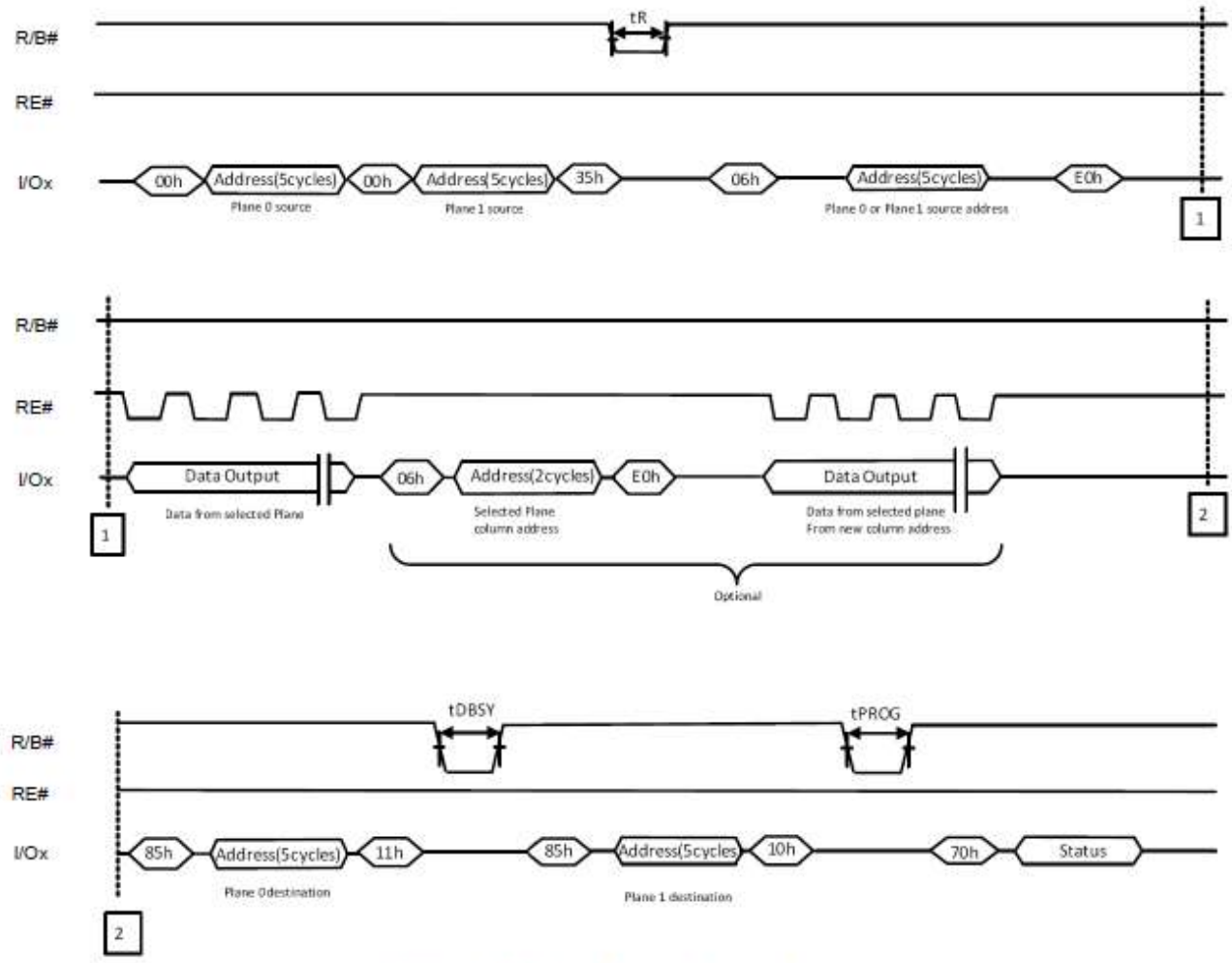


Figure 5-21 Two Plane Copy Back

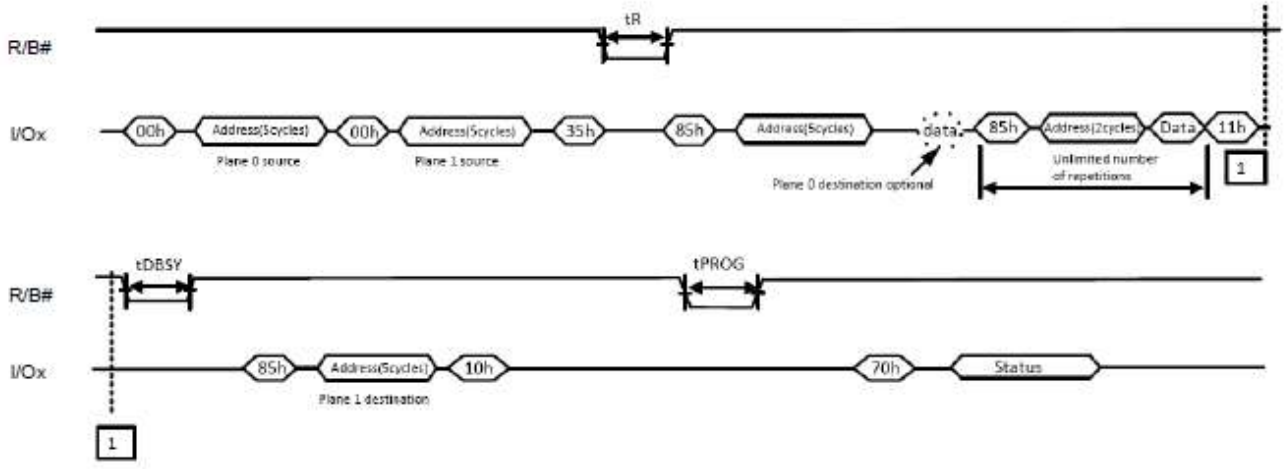


Figure 5-22 Two Plane Copy Back with Random Data Input

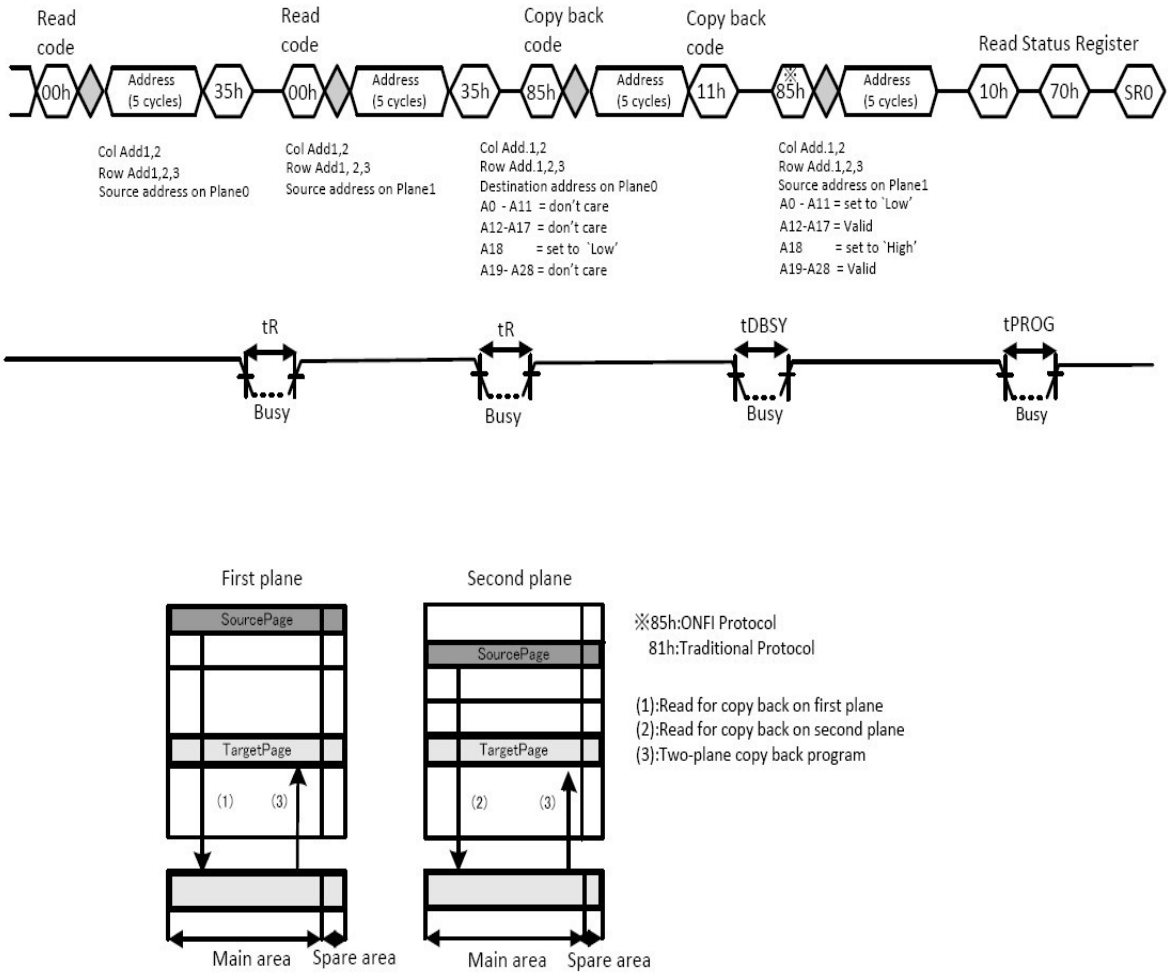


Figure 5-23 Two Plane Program for copy back

BLOCK ERASE Operation

BLOCK ERASE (60h-D0h)

Erase operations happen at the architectural block unit. This XC3D31BAH-DINA has 2048 erase blocks. Each block is organized into 64 pages (2112 bytes/page), 132K bytes (128K + 4K bytes)/block. The BLOCK ERASE command operates on a block by block basis.

Erase Setup command (60h) is written to the Command Register. Next, the three cycle block address is written to the device. The page address bits are loaded during address block address cycle, but are ignored. The Erase Confirm command (D0h) is written to the Command Register at the rising edge of WE#, R/B# goes LOW and the internal controller automatically handles the block erase sequence of operation. R/B# goes LOW during Block Erase internal operations for a period of $_{t}$BERS,

The READ STATUS (70h) command can be used for confirm block erase status. When SR bit 6 (I/O6) becomes to
“1”, block erase operation is finished. SR bit 0 (I/O0) will indicate a pass/fail condition (see Figure 5-24).

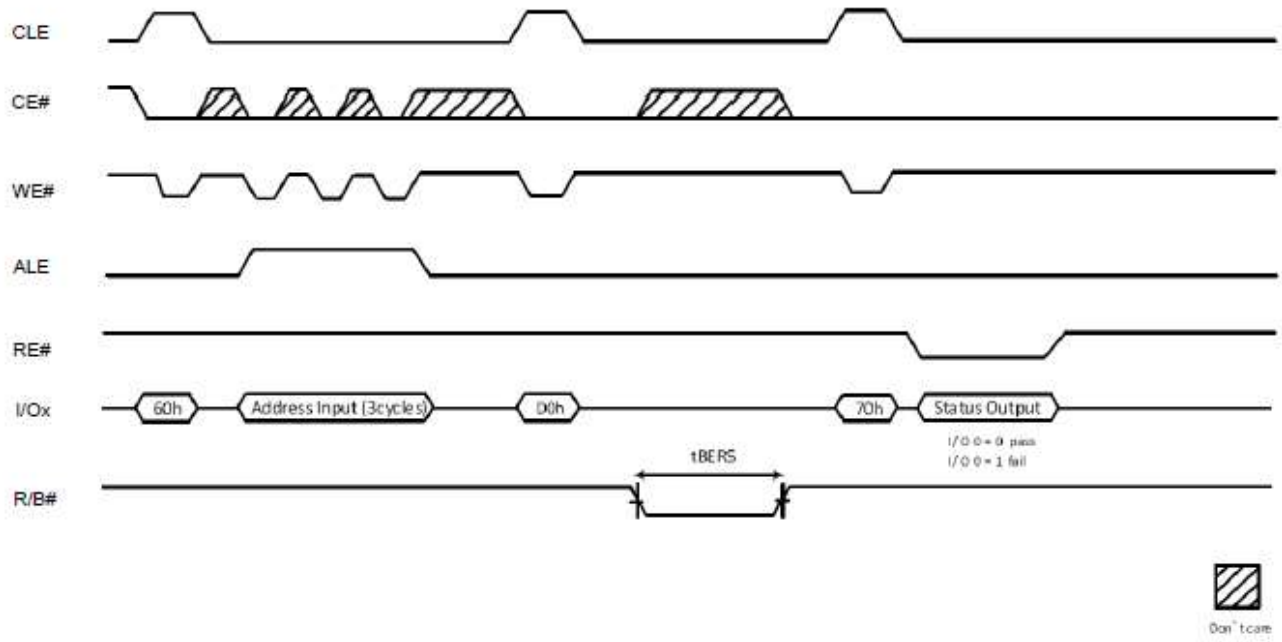


Figure 5-24 Block Erase Operation

TWO PLANE BLOCK ERASE

TWO PLANE BLOCK ERASE (60h-D1h) command indicates two blocks in the specified plane that is to be erased. To start ERASE operation for indicated blocks in the specified plane, write the BLOCK ERASE (60h-D0h) command.

To indicate a block to be erased, writing 60h to the command register, then, write three address cycles containing the row address, the page address is ignored. By writing D1h command to command register, the device will go busy (SR bit 6 = 0, SR bit 5 = 0) for $_{t}$DBSY.

To confirm busy status during $_{t}$DBSY, the host can monitor R/B# signal. Instead, system can use READ STATUS (70h) or READ STATUS ENHANCED (78h) commands. When the status shows ready (SR bit 6 = 1, SR bit 5 = 1), additional TWO PLANE BLOCK ERASE commands can be issued for erasing two blocks in a specified plane.

When system issues TWO PLANE BLOCK ERASE (60h-D1h), and BLOCK ERASE (60h-D0h) commands, READ STATUS (70h) command can confirm whether the operation(s) passed or failed. If the status after READ STATUS (70h) command indicates an error (SR bit 0 = 1), READ STATUS ENHANCED (78h) command can be determined which plane is failed.

TWO PLANE BLOCK ERASE commands require three cycles of row addresses; one address indicates the operational plane. These addresses are subject to the following requirements:

• The plane select bit, A18, must be different for each issued address.

• Block address (A28-A19) of first input is don't care. It follows secondary inputted block address.

Two plane operations must be same type operation across the planes; for example, it is not possible to perform a PROGRAM operation on one plane with an ERASE operation on another.

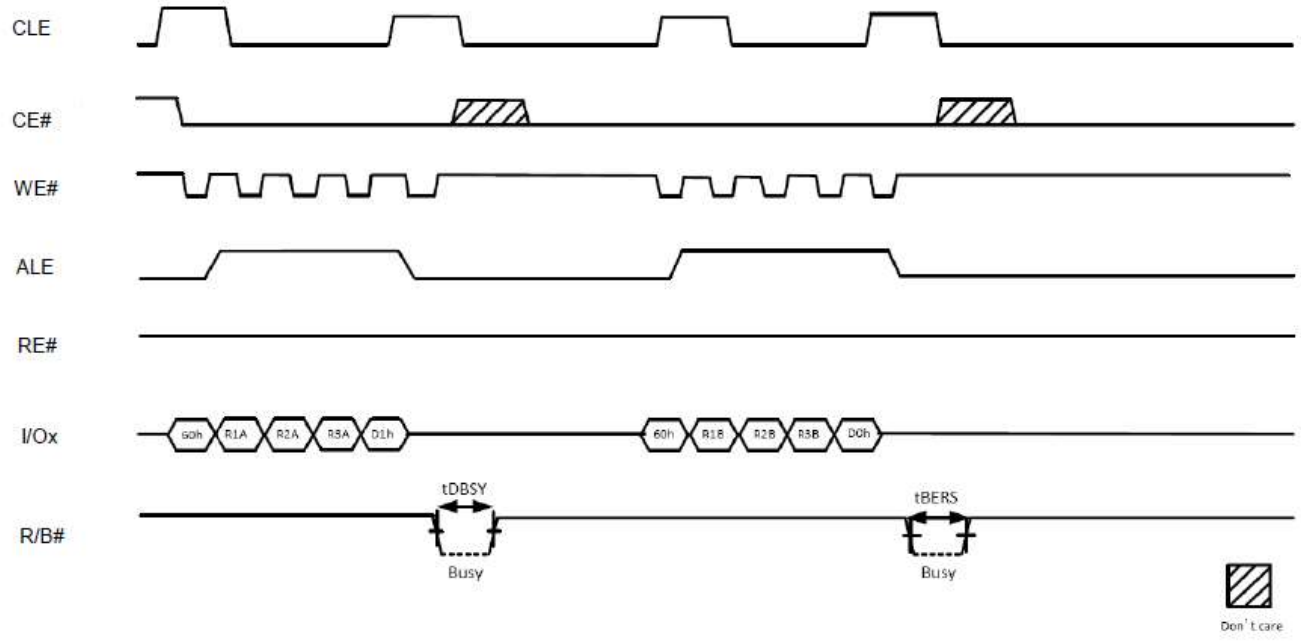


Figure 5-25 Two Plane Block Erase Operation

RESET Operation

RESET (FFh)

READ, PROGRAM, and ERASE commands can be aborted by the RESET (FFh) command during the time the XC3D31BAH-DINA is in the busy state. The Reset operation puts the device into known status.

The data that is processed in either the programming or erasing operations are no longer valid. This means the data can be partially programmed or erased and therefore data is invalid. The Command Register is cleared and is ready to accept next command. The Data Register and Cache Register contents are marked invalid.

The Status Register indicates a value of E0h when WP# is HIGH; otherwise a value of 60h is written when WP# is LOW. After RESET command is written to the command register, R/B# goes LOW for a period of $_{t}$RST (see Figure 5-26).

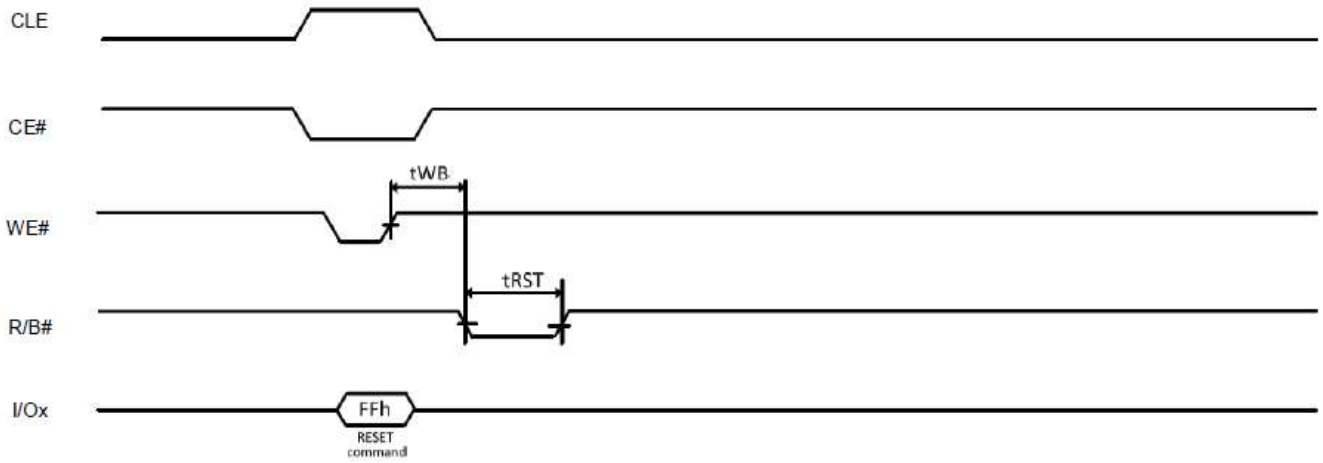


Figure 5-26 Reset Operation

FEATURE Operation

The GET FEATURES (EEh) and SET FEATURES (EFh) commands are used to change the NAND FLASH device behavior from the default power on settings. These commands use a one-byte feature address to determine which feature is to be read or modified. A range of 0 to 255 defines all features; each is described in the features table (see Table 5-8 thru 5-10). The GET FEATURES (EEh) command reads 4-Byte parameter in the features table (See GET FEATURES function). The SET FEATURES (EFh) command places the 4-Byte parameter in the features table (See SET FEATURES function).

When a feature is set, meaning it remains active by default until the device is powered off. The set feature remains the set even if a RESET (FFh) command is issued.

Table 5-8 Features

Feature address	Description
00h	N.A
02h-7Fh	Reserved
80h	Vendor specific parameter : Programmable I/O drive strength
81h	Vendor specific parameter : Programmable R/B# pull-down strength
82h-FFh	Reserved

Feature Address 80h: Programmable I/O Drive Strength

Table 5-9 Feature Address 80h

Sub feature parameter	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value	Notes
P1											
I/O drive strength	Full (default)	Reserved (0)						0	0	00h	1
	Three-quarters	Reserved (0)						0	1	01h	
	One-half	Reserved (0)						1	0	02h	
	One-quarter	Reserved (0)						1	1	03h	
P2											
		Reserved (0)								00h	
P3											
		Reserved (0)								00h	
P4											
		Reserved (0)								00h	

Note:

1. The default drive strength setting is Full strength. The Programmable I/O Drive Strength mode is used to change from the default I/O drive strength. Drive strength should be selected based on expected loading of the memory bus. This table shows the four supported output drive-strength settings. The device returns to the default drive strength mode when a power cycle has occurred. AC timing parameters may need to be relaxed if I/O drive strength is not set to full.

Feature Address 81h: Programmable R/B# Pull-down Strength

Table 5-10 Feature Address 81h

Sub feature	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value	Notes
P1											
R/B# pull-down	Full (default)	Reserved (0)						0	0	00h	1
	Three-quarters	Reserved (0)						0	1	01h	
	One-half	Reserved (0)						1	0	02h	
	One-quarter	Reserved (0)						1	1	03h	
P2											
		Reserved (0)								00h	
P3											
		Reserved (0)								00h	
P4											
		Reserved (0)								00h	

Note:

1. The default programmable R/B# pull-down strength is set to Full strength. The pull-down strength is used to change the R/B# pull-down strength. R/B# pull-down strength should be selected based on expected loading of R/B#. The four supported pull-down strength settings are shown. The device returns to the default pull-down strength when a power cycle has occurred.

GET FEATURES (EEh)

The GET FEATURES command returns the device feature settings including those previously set by the SET FEATURES command. To use the Get Feature mode write the command (EEh) to the Command Register followed by the single cycle byte Feature Address. R/B# will goes LOW for the period of $_{t}$FEAT. If Read Status (70h) command is issued for monitoring the process completion status, Read Command (00h) has to be executed to re-establish data output mode. Once, R/B# goes HIGH, the device feature settings can be read by toggling RE#. The device remains in Feature Mode until another valid command is issued to Command Register. See Figure 5-27.

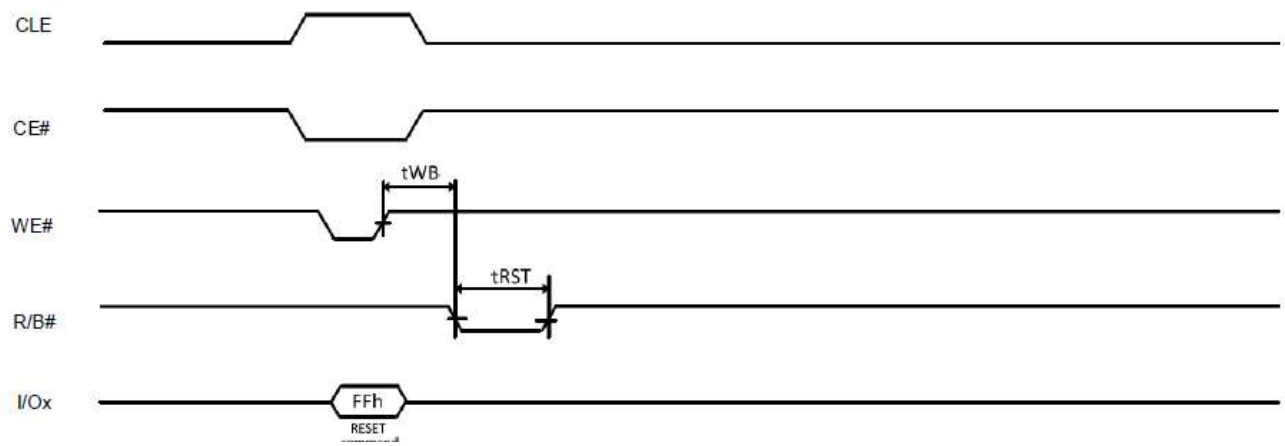


Figure 5-27 Get Feature Operation

SET FEATURES (EFh)

The SET FEATURES command sets the behavior parameters by selecting a specified feature address. To change device behavioral parameters, execute Set Feature command by writing EFh to the Command Register, followed by the single cycle feature address. Each feature parameter (P1- P4) is latched at the rising edge of each WE#. The R/B# signal will go LOW during the period of $_{t}$FEAT while the four feature parameters are stored. The Read Status (70h) command can be issued for monitoring the progress status of this operation. The parameters are stored in device until the device goes through a power on cycle. The device remains in feature mode until another valid command is issued to Command Register.

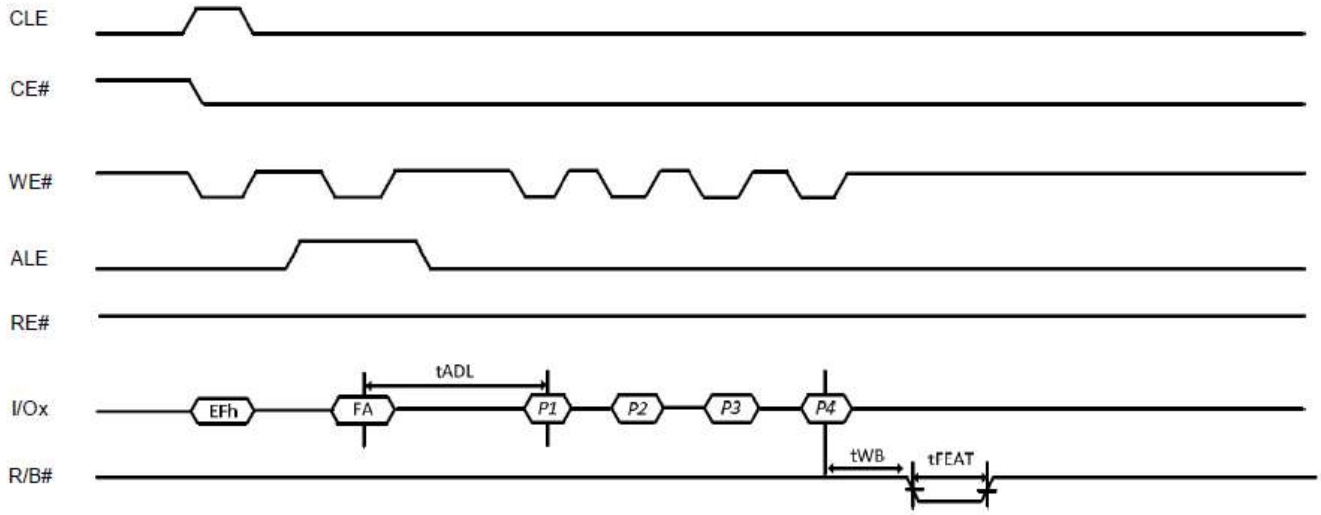


Figure 5-28 Set Feature Operation

ONE TIME PROGRAMMABLE (OTP) area

The device has One-Time Programmable (OTP) memory area comprised of a number of pages (2112 bytes/page) (1056words/page). This entire range of pages is functionally guaranteed. Only the OTP commands can access the OTP area. When the device ships from CHIPSIP, the OTP area is in an erase state (all bits equal “1”). The OTP area cannot be erased, therefore protecting the area only prevent further programming.

WRITE PROTECT

WP# pin can enable or disable program and erase commands preventing or allowing program and erase operations. Figure 5-29 to 5-34 shows the enabling or disabling timing with WP# setup time (tWW) that is from rising or falling edge of WP# to latch the first commands. After first command is latched, WP# pin must not toggle until the command operation is complete and the device is in the ready state. (SR bit 5 (I/O5) equal 1).

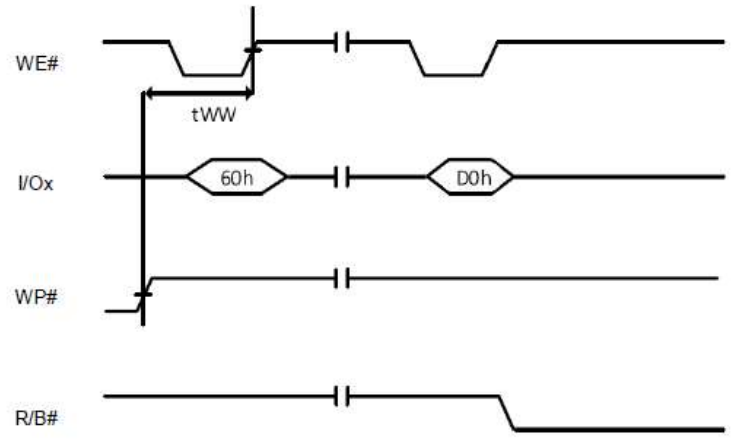


Figure 5-29 Erase Enable

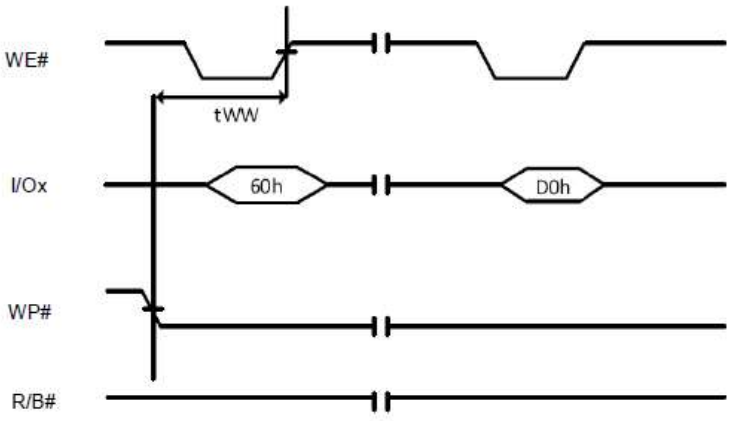


Figure 5-30 Erase Disable

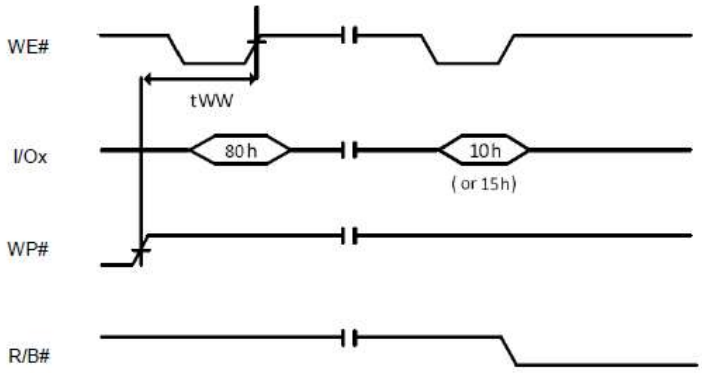


Figure 5-31 Program Enable

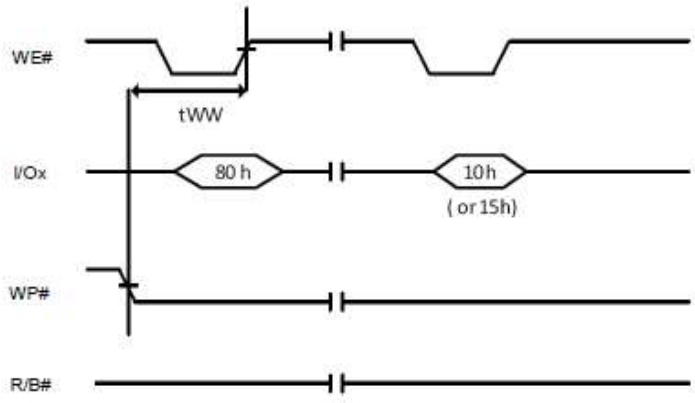


Figure 5-32 Program Disable

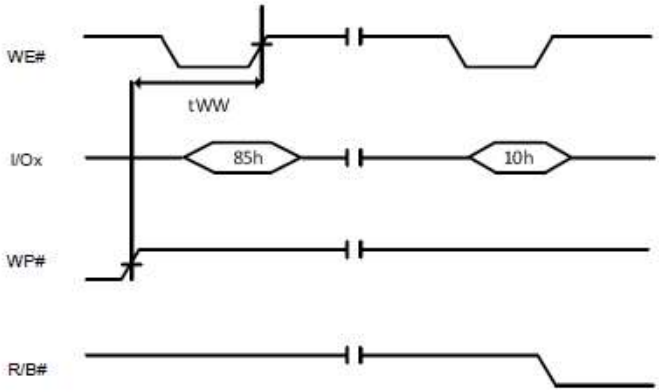


Figure 5-33 Program for Copy Back Enable

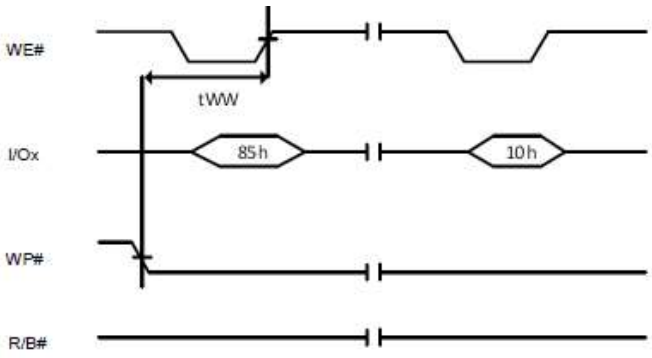


Figure 5-34 Program for Copy Back Disable

Electrical Characteristics

Table 5-11 Absolute Maximum Ratings

PARAMETERS	SYMBOL	CONDITIONS	RANGE	UNIT
Supply Voltage	V_{CC}		–0.6 to +4.6	V
Voltage Applied to Any Pin	V_{IN}	Relative to Ground	–0.6 to +4.6	V
Short circuit output current, I/Os			5	mA

Note:

1. This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.

Device power-up timing

The device is designed to avoid unexpected program/erase operations during power transitions. When the device is powered on, an internal voltage detector disables all functions whenever V_{CC} is below about 2V at 3V device. Write Protect (WP#) pin provides hardware protection and is recommended to be kept at V_{IL} during power up and power down. A recovery time of minimum 1ms is required before internal circuit gets ready for any command sequences.

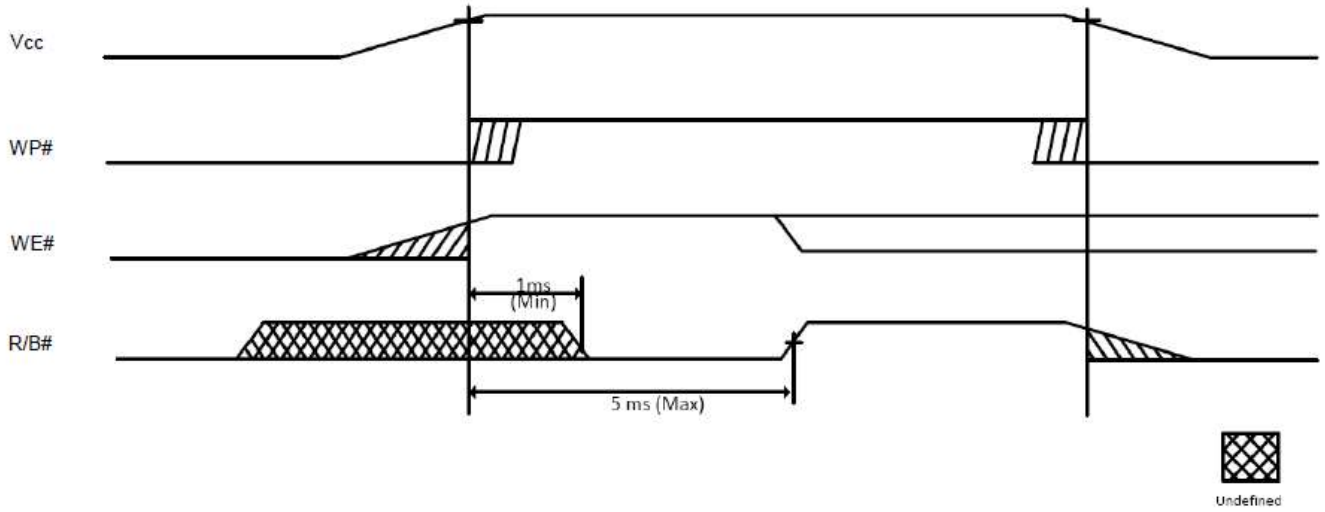


Figure 5-35 Power ON/OFF sequence

DC Electrical Characteristics

Table 5-12 DC Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	
Sequential Read current	I_{CC1}	$_tRC = _tRC$ MIN CE# = V_{IL}	-	25	35	mA
Program current	I_{CC2}	-	-	25	35	mA
Erase current	I_{CC3}	-	-	25	35	mA
Standby current (TTL)	I_{SB1}	CE# = V_{IH} WP# = 0V/V_{CC}	-	-	1	mA
Standby current (CMOS)	I_{SB2}	CE# = V_{CC} – 0.2V WP# = 0V/V_{CC}	-	10	50	uA
Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CC}	-	-	±10	uA
Output leakage current	I_{LO}	V_{OUT} =0V to V_{CC}	-	-	±10	uA
Input high voltage	V_{IH}	I/O7~0, CE#,WE#,RE#, WP#,CLE,ALE	0.8 x V_{CC}	-	V_{CC} + 0.3	V
Input low voltage	V_{IL}	-	-0.3	-	0.2 x V_{CC}	V
Output high voltage(1)	V_{OH}	I_{OH} = -400uA	2.4	-	-	V
Output low voltage(1)	V_{OL}	I_{OL} = 2.1mA	-	-	0.4	V
Output low current	$I_{OL(R/B\#)}$	V_{OL} = 0.4V	8	10	-	mA

Notes:

1. V_{OH} and V_{OL} may need to be relaxed if I/O drive strength is not set to full.

2. $I_{OL\ (R/B\#)}$ may need to be relaxed if R/B# pull-down strength is not set to full

AC Measurement Conditions

Table 5-13 AC Measurement Conditions

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
Input Capacitance(1), (2)	C_{IN}	-	10	pF
Input / Output Capacitance(1), (2)	C_{IO}	-	10	pF
Input Rise and Fall Times	TR/TF	-	5	ns
Input Pulse Voltages	-	0 to V_{CC}		V
Input / Output timing Voltage	-	$V_{CC}/2$		V
Output load (1)	CL	1TTL GATE and CL=30pF		-

Notes:

1. Verified on device characterization, not 100% tested

2. Test conditions T_A=25℃, f=1MHz, V_{IN}=0V

AC timing characteristics for Command, Address and Data Input

Table 5-14 AC timing characteristics for Command, Address and Data Input

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
ALE to Data Loading Time	$_tADL$	70	-	ns
ALE Hold Time	$_tALH$	5	-	ns
ALE setup Time	$_tALS$	10	-	ns
CE# Hold Time	$_tCH$	5	-	ns
CLE Hold Time	$_tCLH$	5	-	ns
CLE setup Time	$_tCLS$	10	-	ns
CE# setup Time	$_tCS$	15	-	ns
Data Hold Time	$_tDH$	5	-	ns
Data setup Time	$_tDS$	10	-	ns
Write Cycle Time	$_tWC$	25	-	ns
WE# High Hold Time	$_tWH$	10	-	ns
WE# Pulse Width	$_tWP$	12	-	ns
WP# setup Time	$_tWW$	100	-	ns

Note:

1. $_tADL$ is the time from the WE# rising edge of final address cycle to the WE# rising edge of first data cycle.

AC timing characteristics for Operation

Table 5-15 AC timing characteristics for Operation

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
ALE to RE# Delay	tAR	10	-	ns
CE# Access Time	tCEA	-	25	ns
CE# HIGH to Output High-Z(1)	tCHZ	-	30	ns
CLE to RE# Delay	tCLR	10	-	ns
CE# HIGH to Output Hold	tCOH	15	-	ns
Cache Busy in Cache Read mode	tRCBSY	-	25	us
Output High-Z to RE# LOW	tIR	0	-	ns
Data Transfer from Cell to Data Register	tR	-	25	us
READ Cycle Time	tRC	25	-	ns
RE# Access Time	tREA	-	20	ns
RE# HIGH Hold Time	tREH	10	-	ns
RE# HIGH to Output Hold	tRHOH	15	-	ns
RE# HIGH to WE# LOW	tRHW	100	-	ns
RE# HIGH to Output High-Z(1)	tRHZ	-	100	ns
RE# LOW to output hold	tRLOH	5	-	ns
RE# Pulse Width	tRP	12	-	ns
Ready to RE# LOW	tRR	20	-	ns
Reset Time (READ/PROGRAM/ERASE)(2)	tRST	-	5/10/500	us
WE# HIGH to Busy(3)	tWB	-	100	ns
WE# HIGH to RE# LOW	tWHR	60	-	ns

Notes:

1. AC characteristics may need to be relaxed if I/O drive strength is not set to “full.”

2. Transition is measured ±200mV from steady-state voltage with load. This parameter is sampled and not 100 % tested.

3. Do not issue new command during tWB, even if R/B# is ready.

Program and Erase Characteristics

Table 5-16 Program and Erase Characteristics

PARAMETER	SYMBOL	SPEC		UNIT
		TYP	MAX	
Number of partial page programs	NoP	-	4	cycles
Page Program time	tPROG	250	700	us
Busy Time for Cache program (1)	tCBSY	3	700	us
Busy Time for SET FEATURES /GET FEATURES	tFEAT	-	1	us
Busy Time for program/erase at locked block	tLBSY	-	3	us
Busy Time for OTP program when OTP is protected	tOBSY	-	30	us
Block Erase Time	tBERS	2	10	ms
Last Page Program time (2)	tLPROG	-	-	-
Busy Time for Two Plane page program and Two Plane Block Erase	tDBSY	0.5	1	us

Notes:

1. tCBSY maximum time depends on timing between internal program complete and data-in.

2. tLPROG = Last Page program time (tPROG) + Last -1 Page program time (tPROG) – Last page Address, Command and Data load time.

5.3 Timing Diagrams

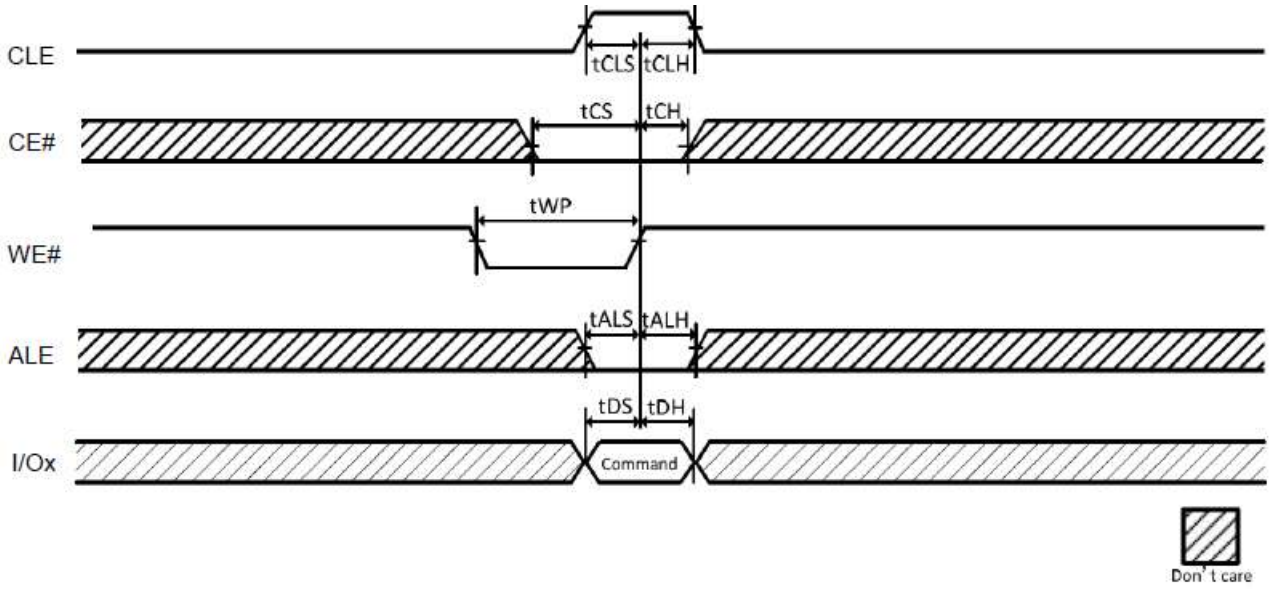


Figure 5-36 Command Latch Cycle

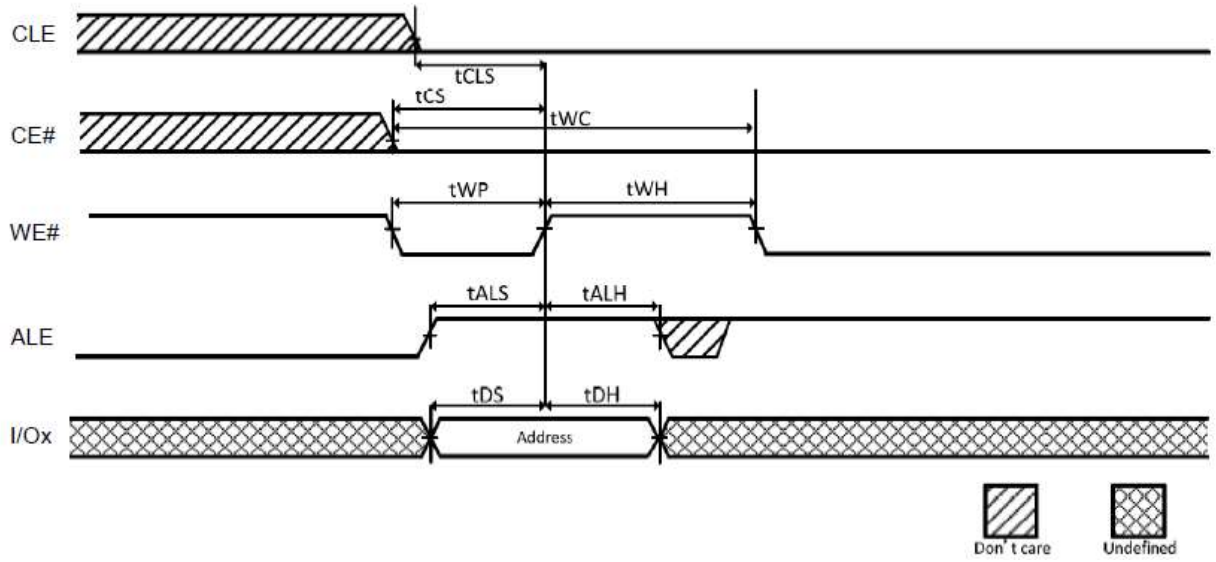


Figure 5-37 Address Latch Cycle

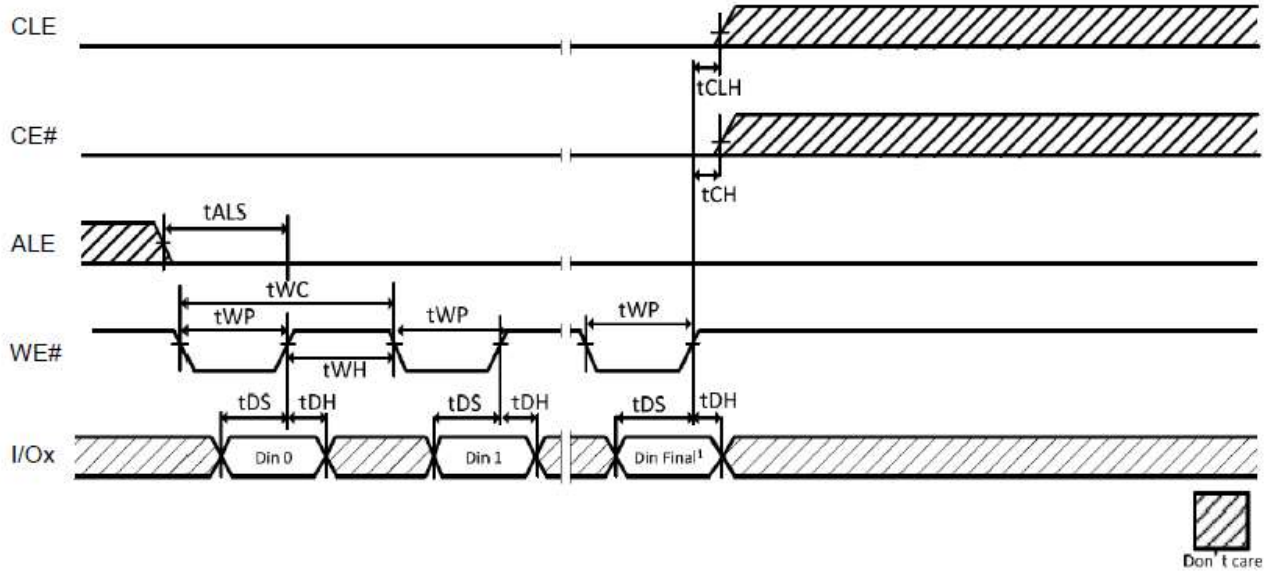


Figure 5-38 Data Latch Cycle

Note:

1. Din Final = 2,111

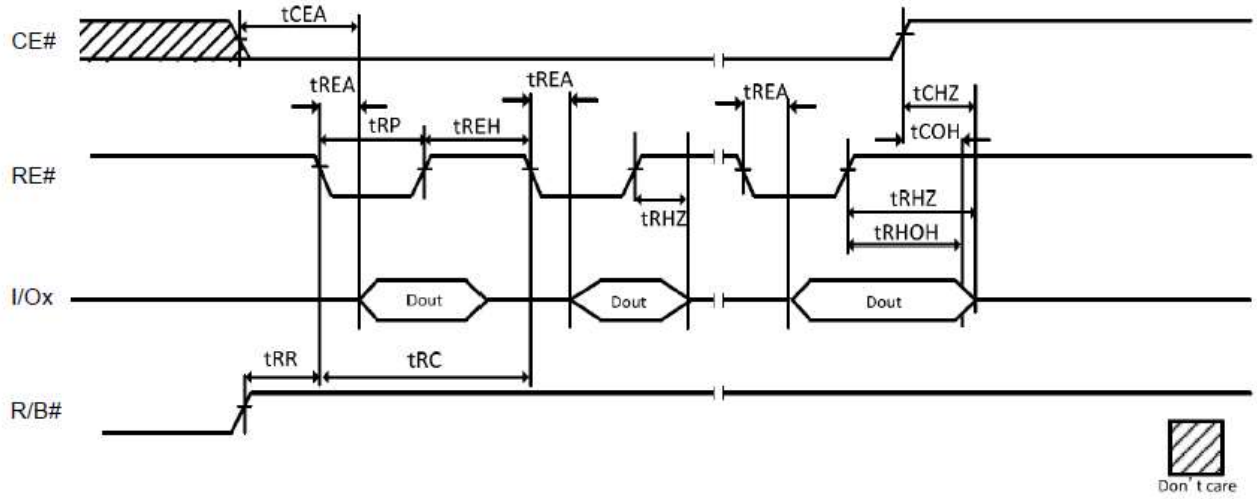


Figure 5-39 Serial Access Cycle after Read

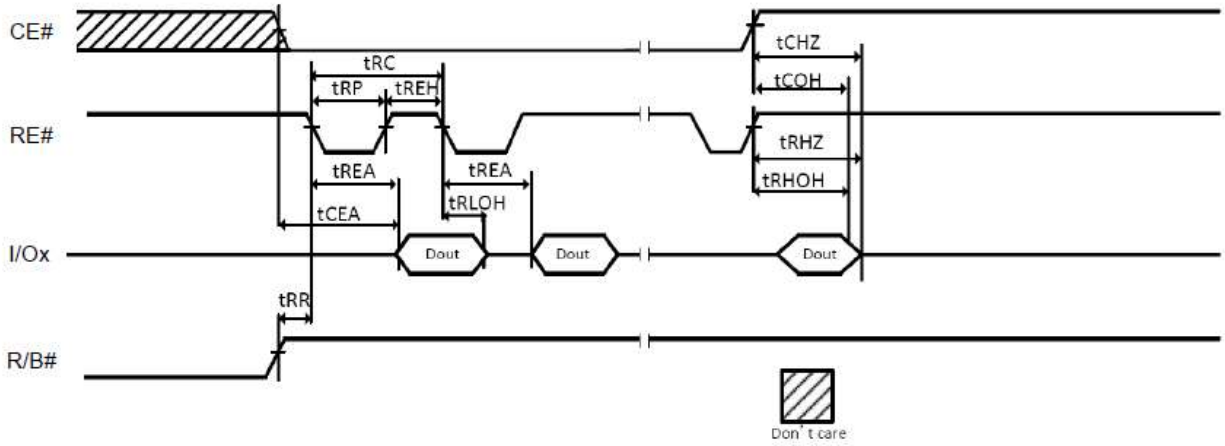


Figure 5-40 Serial Access Cycle after Read (EDO)

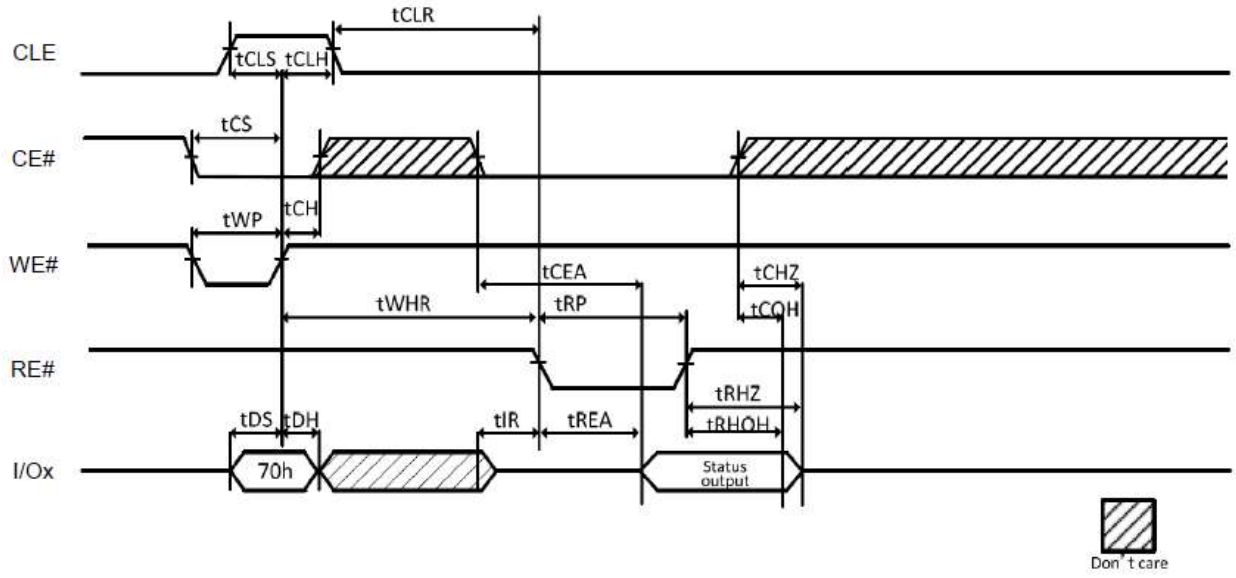


Figure 5-41 Read Status Operation

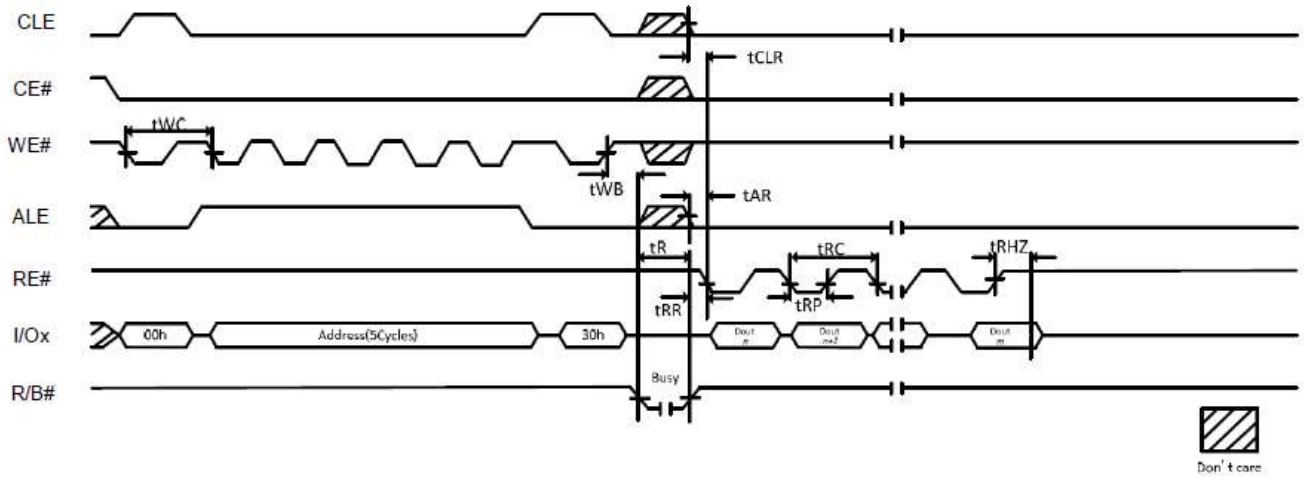


Figure 5-42 Page Read Operation

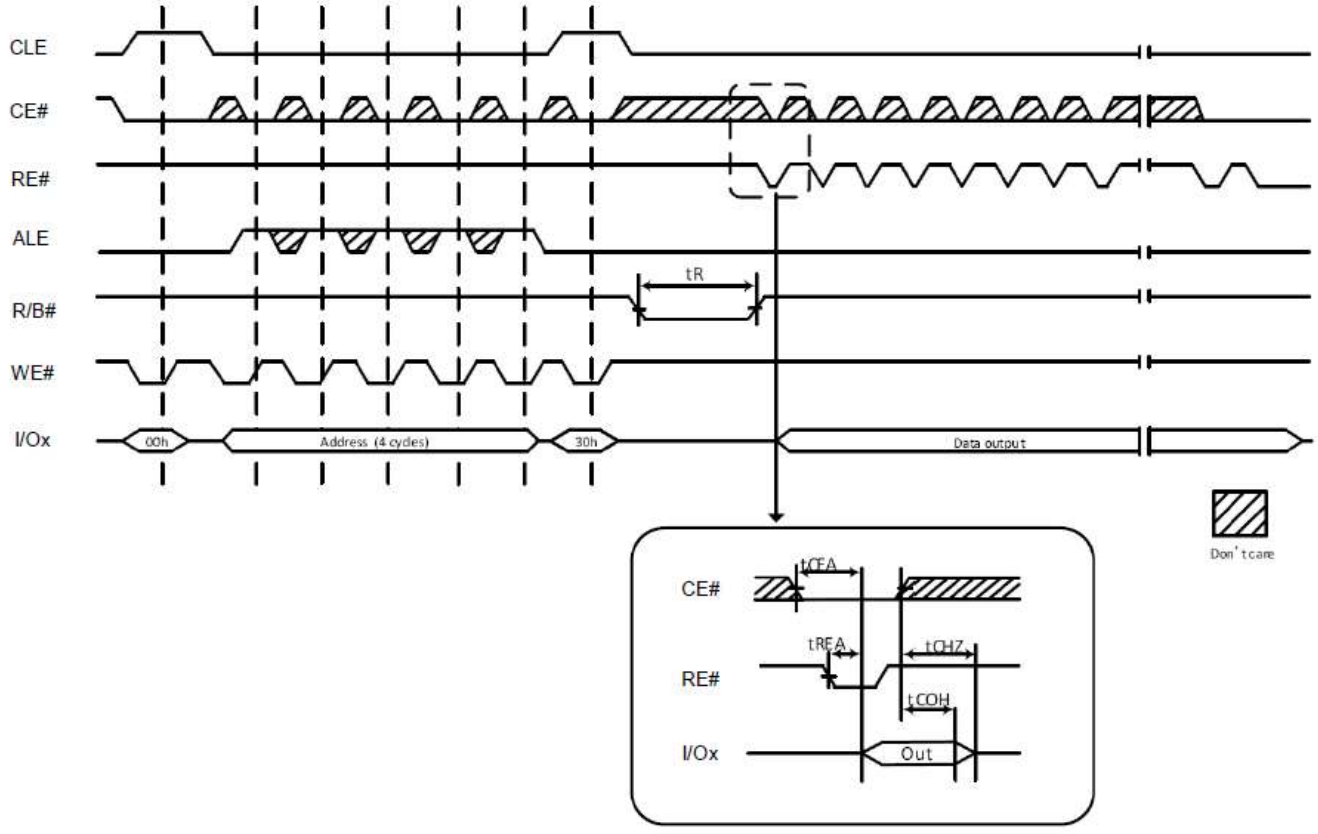


Figure 5-43 CE# Don't Care Read Operation

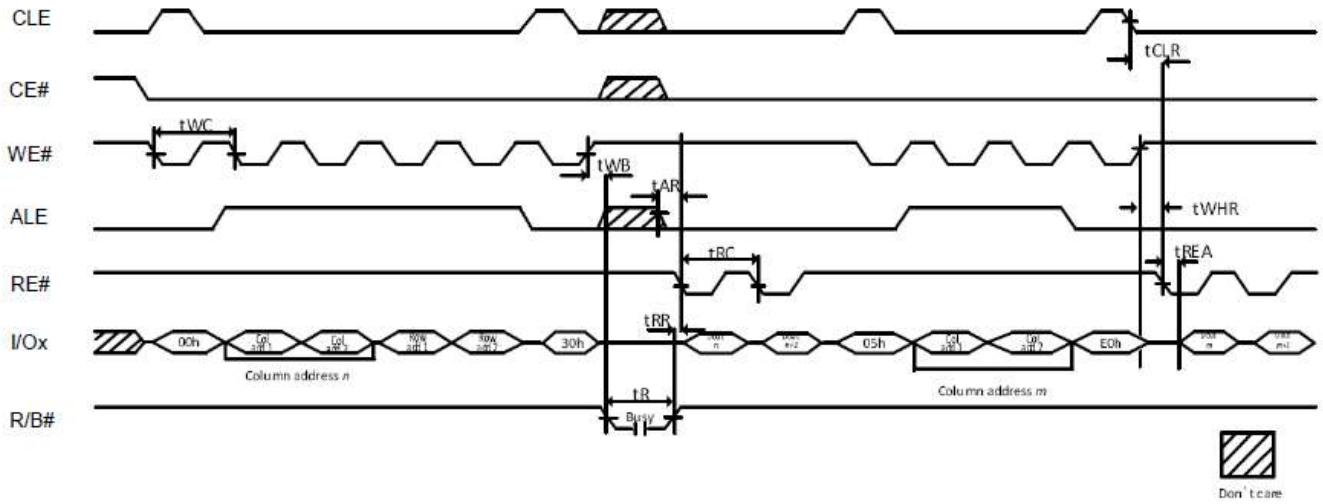


Figure 5-44 Random Data Output Operation

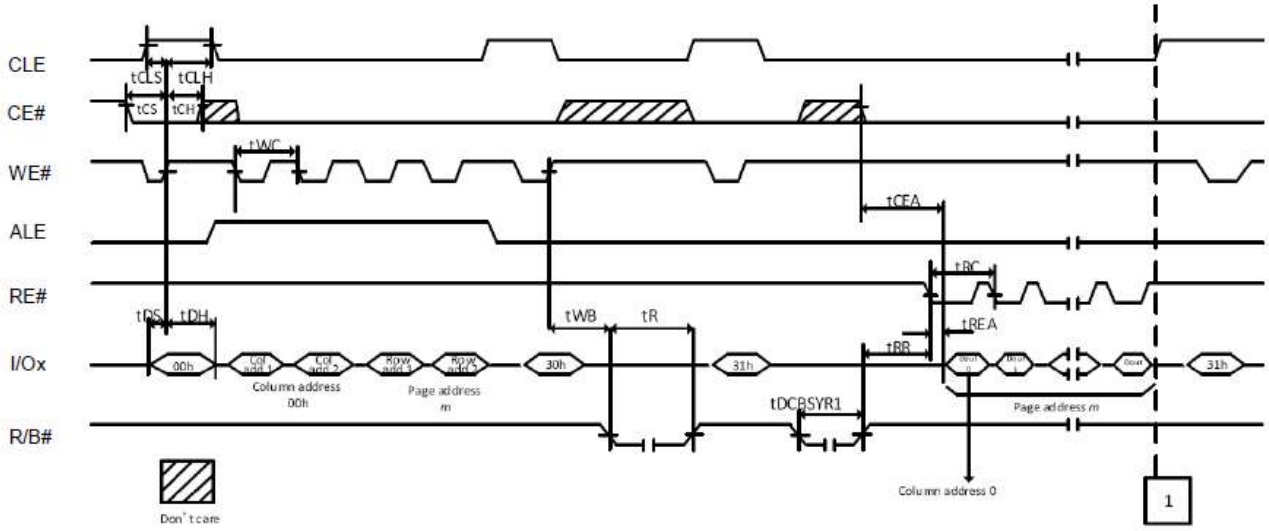


Figure 5-45 Cache Read Operation (1/2)

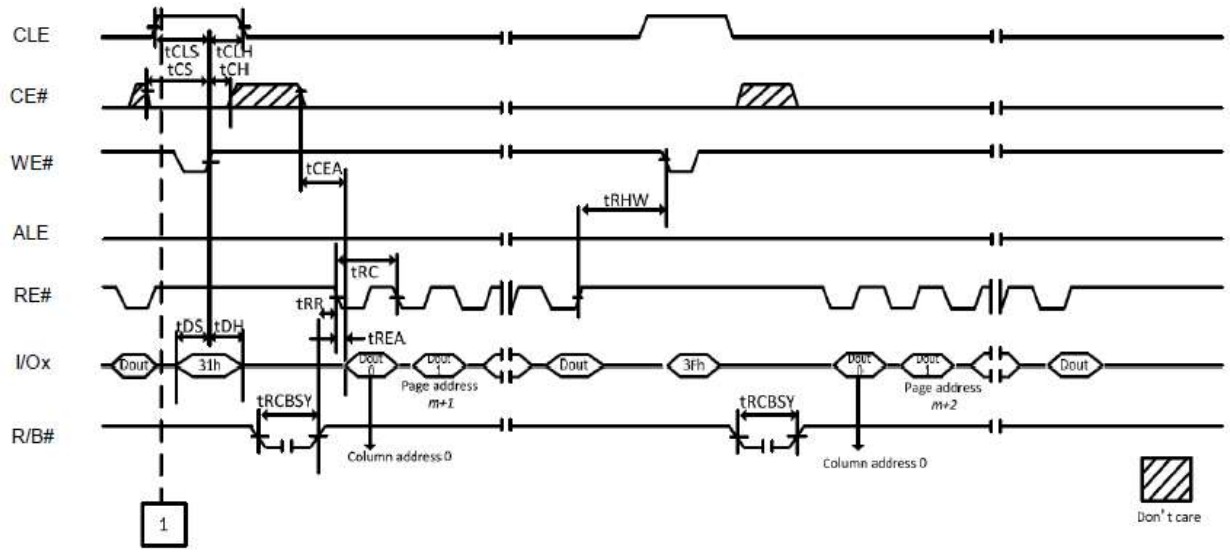


Figure 5-46 Cache Read Operation (2/2)

Note:

1. See Table 5-4 for actual value.

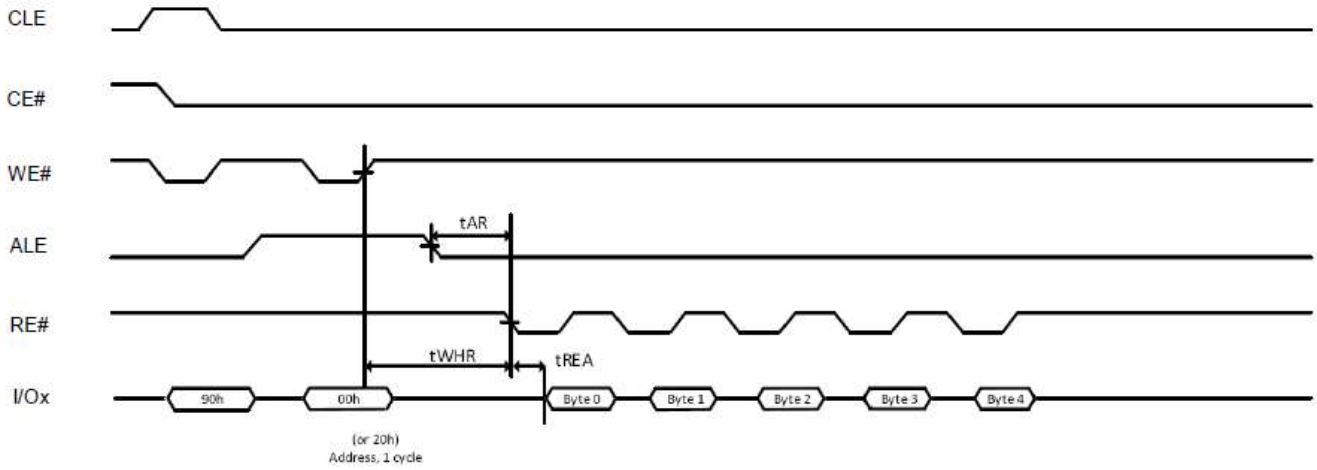


Figure 5-47 Read ID

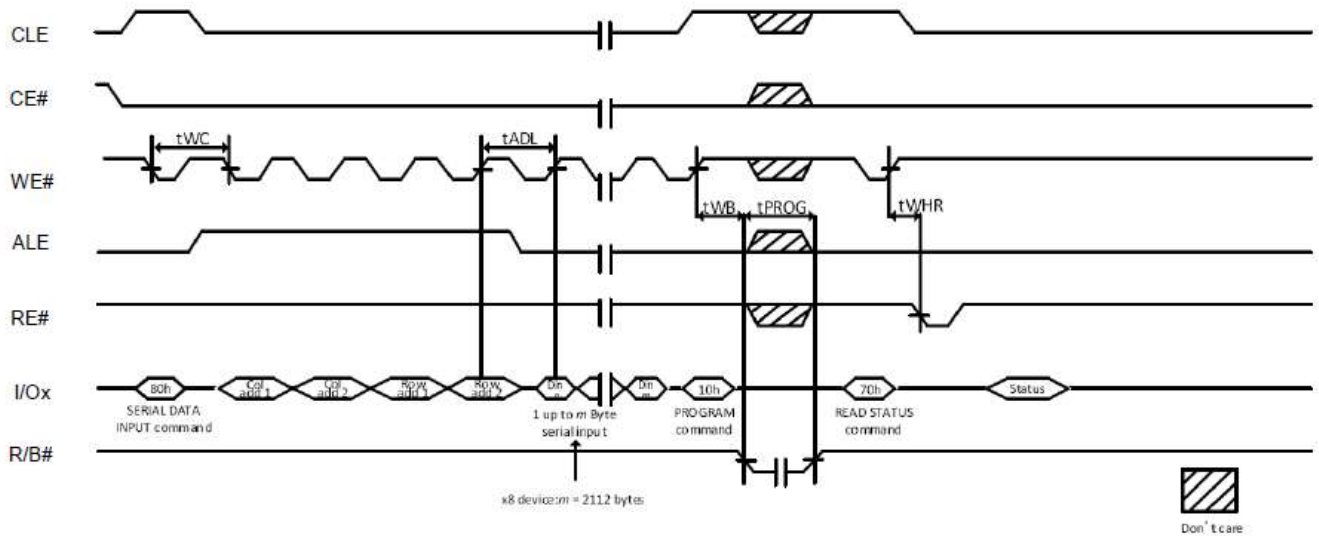


Figure 5-48 Page Program

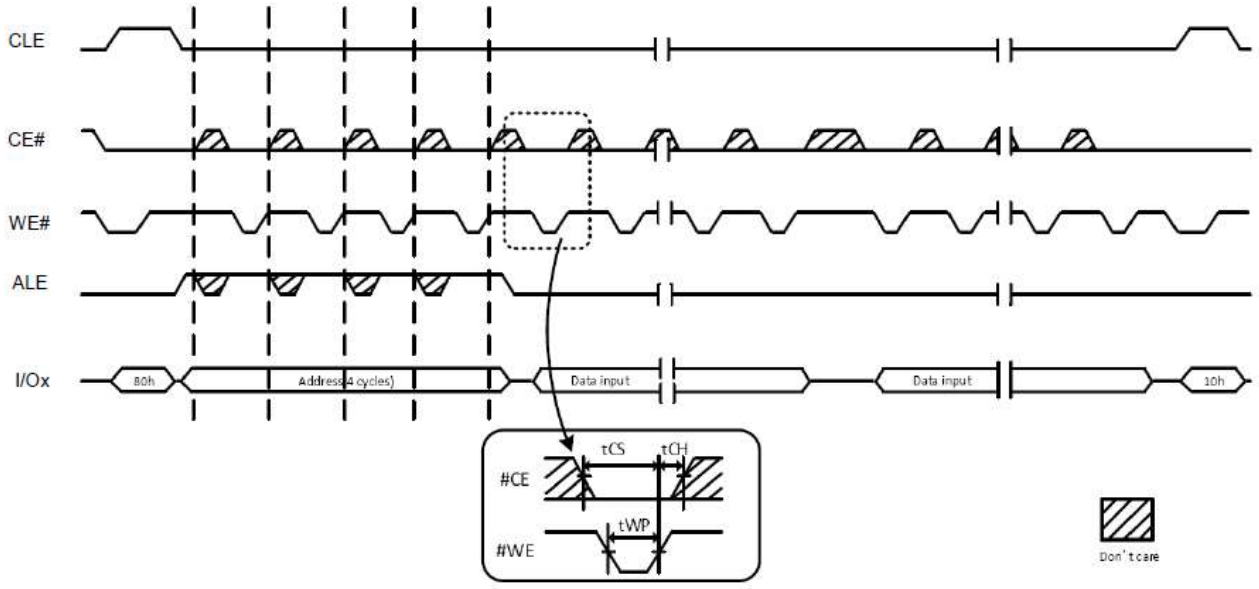


Figure 5-49 CE# Don't Care Page Program Operation

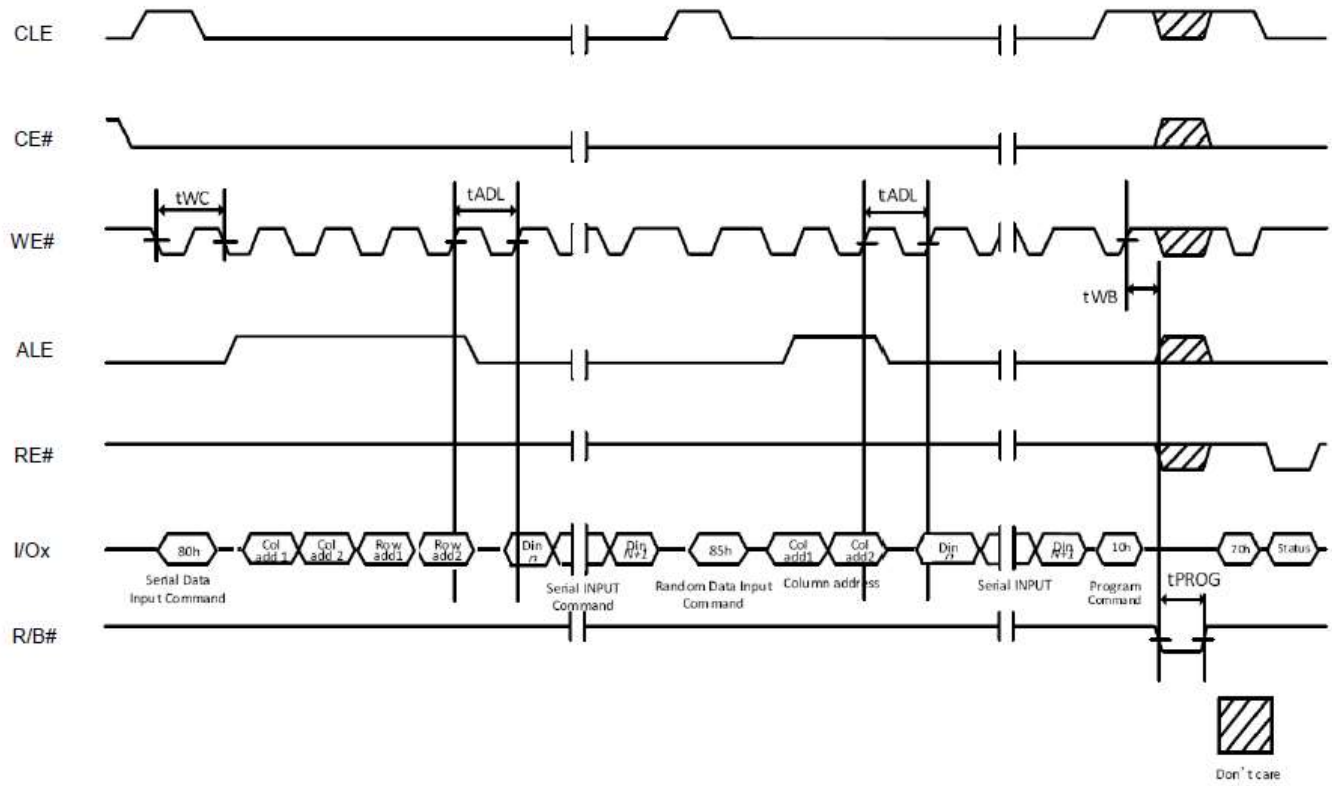


Figure 5-50 Page Program with Random Data Input

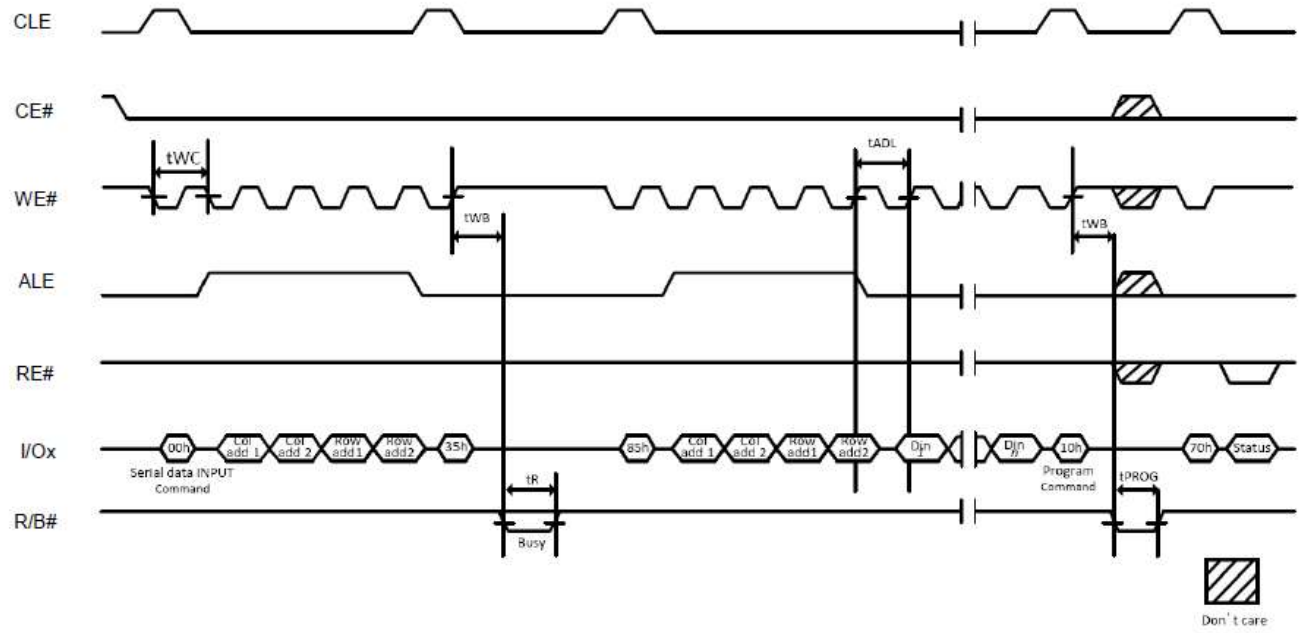


Figure 5-51 Copy Back

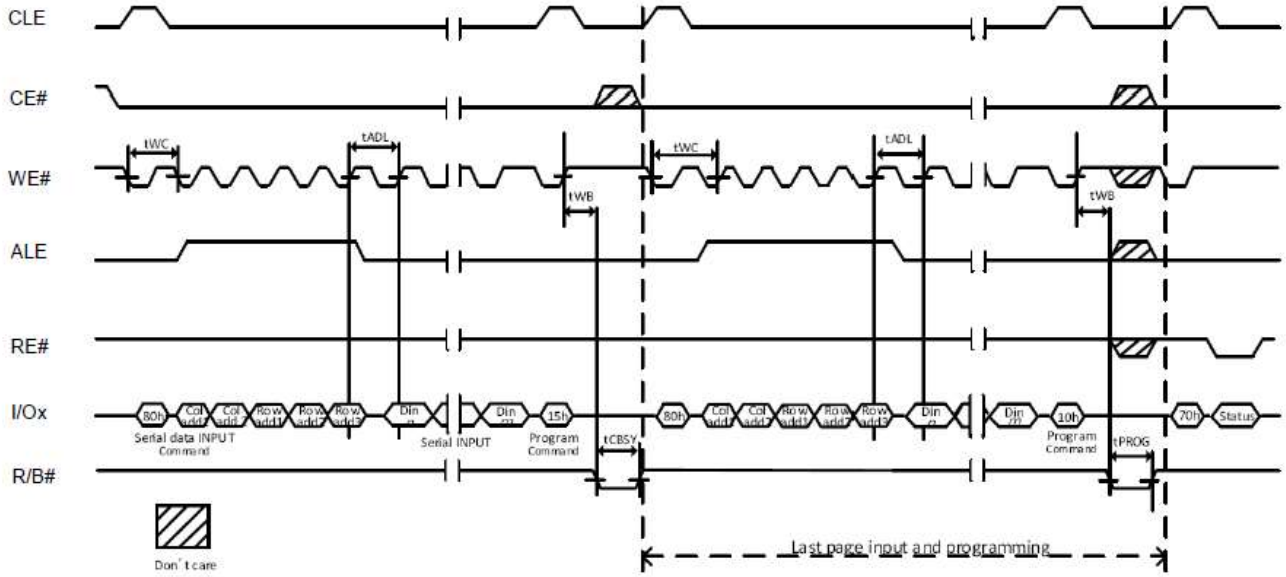


Figure 5-52 Cache Program

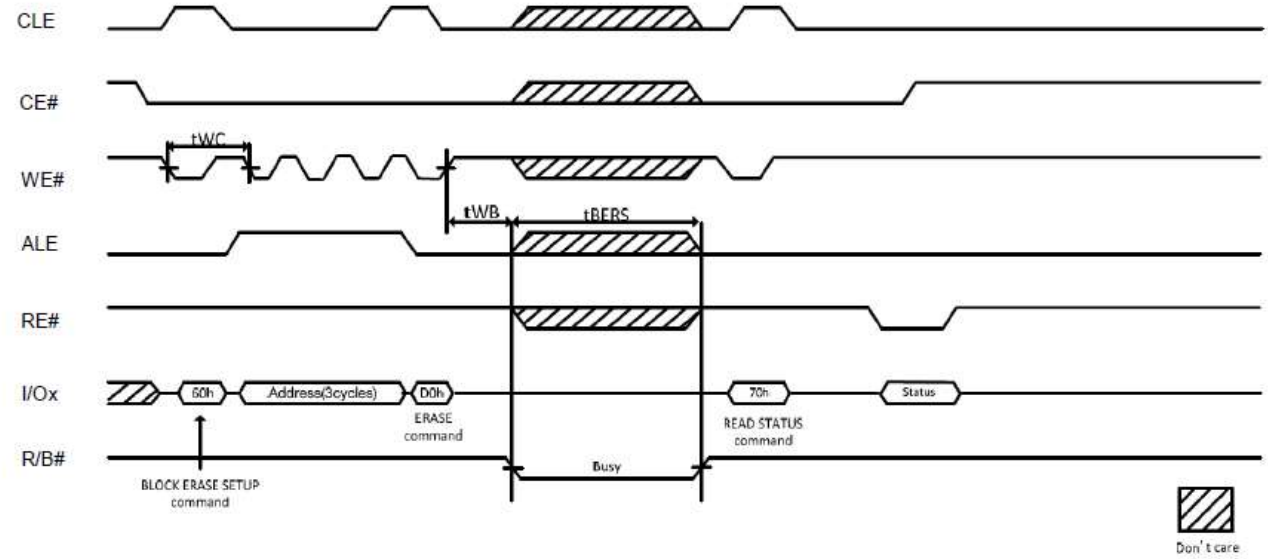


Figure 5-53 Block Erase

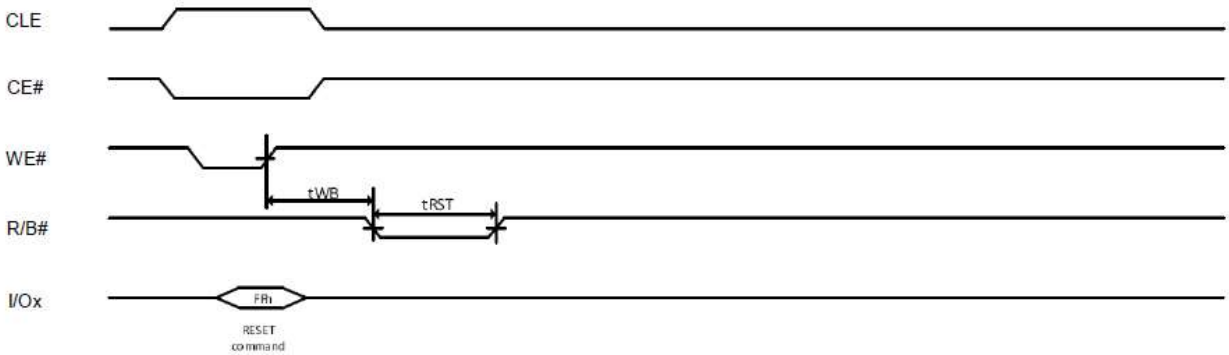


Figure 5-54 Reset

Invalid Block Management

Invalid blocks

The XC3D31BAH-DINA may have initial invalid blocks when it ships from factory. Also, additional invalid blocks may develop during the use of the device. Nvb represents the minimum number of valid blocks in the total number of available blocks (See Table 5-17). An invalid block is defined as blocks that contain one or more bad bits. Block0, blocks address 00h is guaranteed to be a valid block at the time of shipment.

Table 5-17 Valid Block Number

Parameter	Symbol	Min	Max	Unit
Valid block number	Nvb	2008	2048	blocks

Initial invalid blocks

Initial invalid blocks are defined as blocks that contain one or more invalid bits when shipped from factory.

Although the device contains initial invalid blocks, a valid block of the device is of the same quality and reliability as all valid blocks in the device with reference to AC and DC specifications. The XC3D31BAH-DINA has internal circuits to isolate each block from other blocks and therefore, the invalid blocks will not affect the performance of the entire device.

Before the device is shipped from the factory, it will be erased and invalid blocks are marked. All initial invalid blocks are marked with non-FFh at the first byte of spare area on the 1st or 2nd page. The initial invalid block information cannot be recovered if inadvertently erased. Therefore, software should be created to initially check for invalid blocks by reading the marked locations before performing any program or erase operation, and create a table of initial invalid blocks as following flow chart

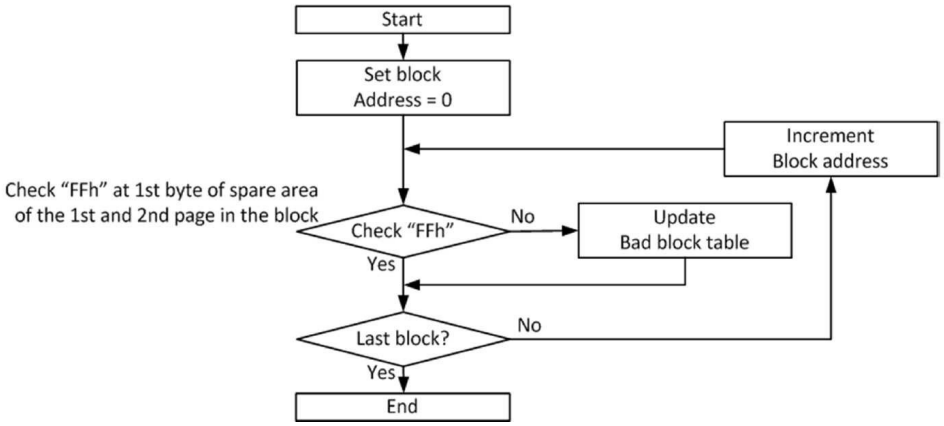


Figure 5-55 Flow chart of create initial invalid block table

Error in operation

Additional invalid blocks may develop in the device during its life cycle. Following the procedures herein is required to guarantee reliable data in the device.

After each program and erase operation, check the status read to determine if the operation failed. In case of failure, a block replacement should be done with a bad-block management algorithm. The system has to use a minimum 1-bit ECC per 528 bytes of data to ensure data recovery.

Table 5-18 Block failure

Operation	Detection and recommended procedure
Erase	Status read after erase ->Block Replacement
Program	Status read after program -> Block Replacement
Read	Verify ECC -> ECC correction

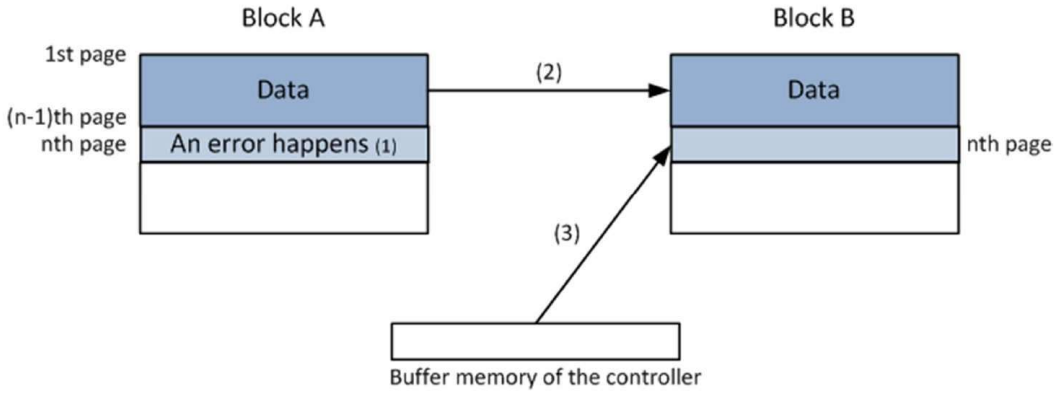


Figure 5-56 Bad block Replacement

Notes:

1. An error happens in the nth page of block A during program or erase operation.
2. Copy the data in block A to the same location of block B which is valid block.
3. Copy the nth page data of block A in the buffer memory to the nth page of block B
4. Creating or updating bad block table for preventing further program or erase to block A

Addressing in program operation

The pages within the block have to be programmed sequentially from LSB (least significant bit) page to the MSB (most significant bit) within the block. The LSB is defined as the start page to program, does not need to be page 0 in the block. Random page programming is prohibited.

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