

SD NAND Datasheet

XCSD04G-KJ

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Change History:

Rev	Changes	Date	Note
Rev1.0	Initial release	2023.05.20	

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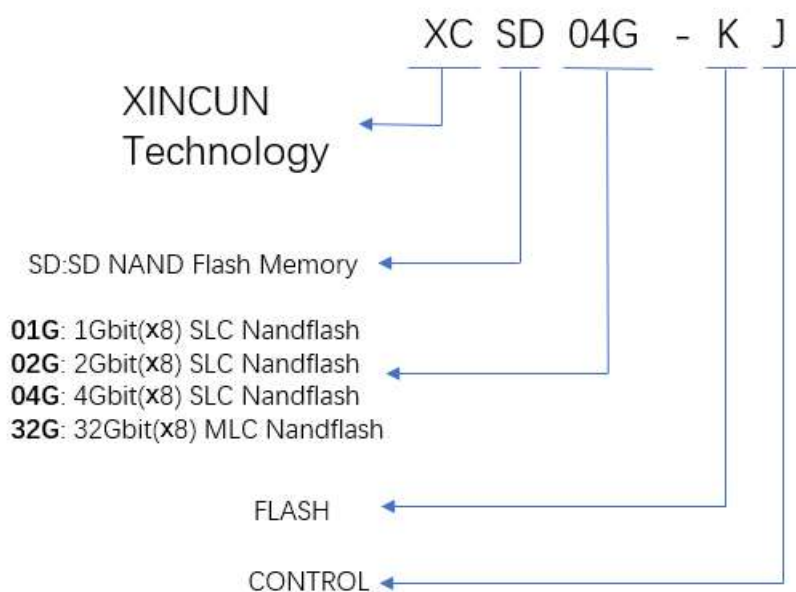
1. Introduction

Xincun SD NAND is a type of embedded storage technology which is similar to the SD card as an industry standard. The SD NAND solution provided by Xincun IC consists of the NAND flash and the high-performance controller with the LGA 8 package. 3.3V supply voltage (VCC) is required for the NAND area. The SD NAND is fully compliant with SD2.0 interface which is utilized by most of general CPU. The advantages of the SD NAND include high quality, low power consumption and cost performance.

Product models list:

Capacity	Part Number	Package	Size
1Gb	XCSD01G-KJ	LGA8	8X6mm
2Gb	XCSD02G-KJ	LGA8	8x6mm
4Gb	XCSD04G-KJ	LGA8	8x6mm
32Gb	XCSD32G-SA	LGA8	8x7.0mm

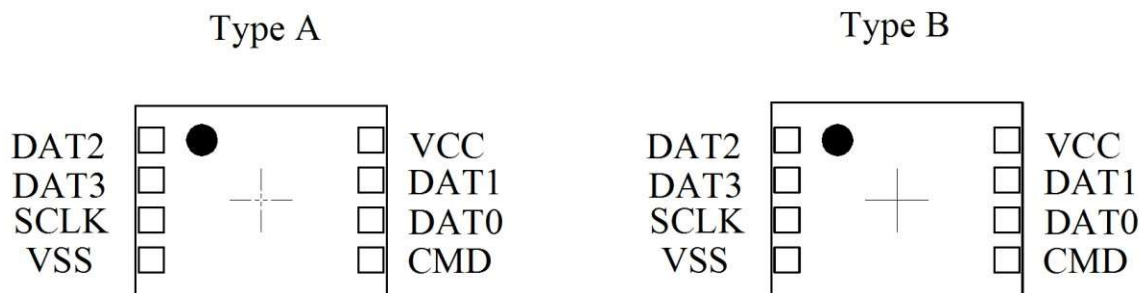
Model description:



3. Features

- 1) Support up to 50Mhz clock frequency .
- 2) Low power consumption, with the standby energy saving management mode automatically.
- 3) High Speed model, Speed class 4/class 6/class 8 supported.
- 4) SD/SPI mode supported.
- 5) Copyrights Protection Mechanism—Compling with highest security of SDMI standard.
- 6) Operating Temperature: -30°C to 85°C.
- 7) High-speed Flash Controller inside.

4. Pin Assignments (Top View)



PIN #	SD MODE			SPI MODE		
	NAME	TYPE ¹	DESCRIPTION	NAME	TYPE	DESCRIPTION
1	DAT2	I/O/PP	Data Line[Bit2]	RSV		Reserved
2	CD/DAT3 ²	I/O/PP ³	Card Detect/ Data Line[Bit3]	CS	I ³	Chip Select(Neg True)
3	SCLK	I	Clock	SCLK	I	Clock
4	VSS	S	Supply Voltage Ground	VSS	S	Supply Voltage Ground
5	CMD	PP	Command/Response	DI	I	Data In
6	DAT0	I/O/PP	Data Line[Bit0]	DO	O/PP	Data Out
7	DAT1	I/O/PP	Data Line[Bit1]	RSV		Reserved
8	VCC	S	Supply Voltage	VCC	S	Supply Voltage

Table 1: SD NAND Contact Pad Assignment

- **S**: power supply; **I**: input; **O**: output using push-pull drivers; **PP**: I/O using push-pull drivers;
- The extended **DAT** lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after **SET_BUS_WIDTH** command. The **Host** shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used. It is defined so, in order to keep compatibility to **MultiMediaCards**.
- After power up this line is input with **50KOhm** pull-up (can be used for card detection or SPI mode selection). The pull-up should be disconnected by the user, during regular data transfer, with **SET_CLR_CARD_DETECT (ACMD42)** command.

5. Product Characteristics Value

5-1.

Parameter	Range			
Capacity	1Gb	2Gb	4Gb	32Gb
	120MB	240MB	480MB	3840MB
Write Speed	4.7MB/S	4.7MB/s	4.7MB/s	10MB/s
Read Speed	12MB/S	15MB/s	15MB/s	20MB/s
Thenstandbycurrent	169 uA	169 uA	169 uA	70 uA
Work current	15mA	15 mA	15 mA	6 mA
MTBF	1,000,000hours			
R/W Cycle	SLC(100000) MLC(6000)			
Controller	AX215DA			
Controller details	AX215DA_DIE			

* Test condition :2.66G CPU, 1GB DDR, winXP OS, GL827 Card Reader, Voltage 3.3V.

5-2.

Parameter	Range	
Temperature	Work Model	-30°C ~ 85°C
Humidity	Work Model	8% to 95%, Non-condensing
	Storage Model	8% to 95%, Non-condensing

6. Physical Specifications (Top View)

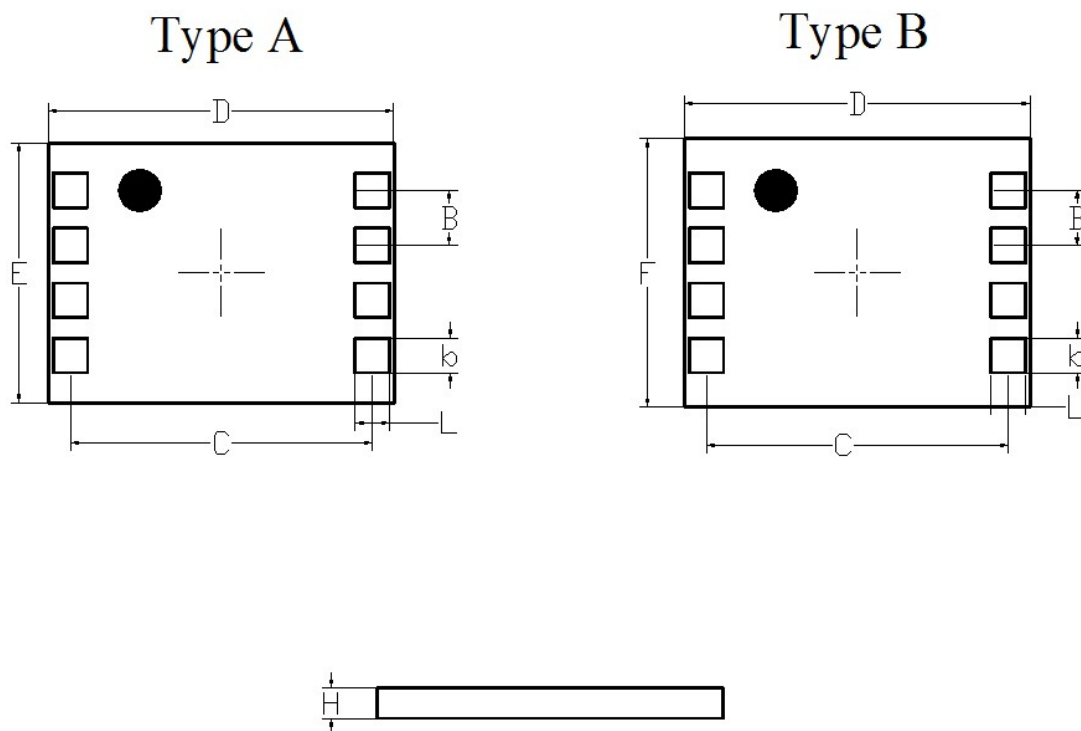


Figure F-1: Mechanical Description

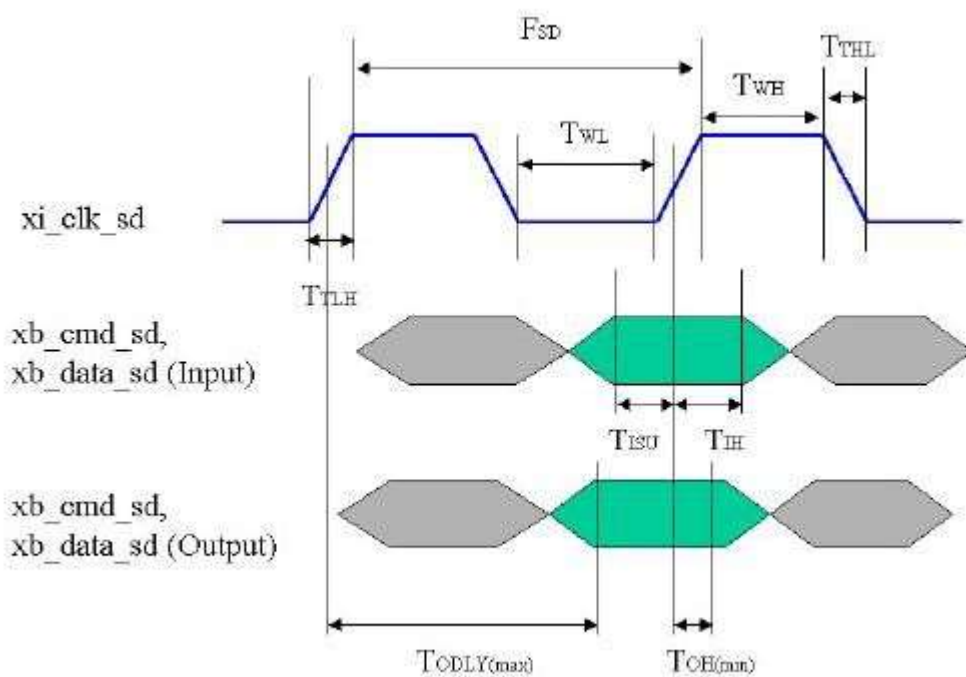
Common Dimensions				
Symbol	Min	Nom	Max	Note
b	0.65	0.70	0.75	
L	0.75	0.80	0.85	
B	-	1.27(Typ)	-	
C	6.90	7.00	7.10	
D	7.90	8.00	8.10	
E	5.90	6.00	6.10	
F	6.10	6.20	6.30	
H	0.70	0.80	0.90	

Table 2: SD NAND Package Dimensions (Units: mm)

7. DC Characteristics

Symbol	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VIL	Input low voltage		VSS-0.3		0.25VCC	V
VIH	Input high voltage		0.625VCC		VCC+0.3	V
VOL	Output low voltage	IOL=100μA @VCC_min			0.125VCC	V
VOH	Output high voltage	IOH=100μA @VCC_min	0.75VCC			V
IIN	Input leakage current	VIN=VCC or 0	-10	+/-1	10	μA
IOUT	Tri-state output leakage current		-10	+/-1	10	μA
ISTBY	Standby current	clock stop		0.16	0.2	mA
IOP	Operation current	25MHz Write		15	25	mA
		25MHz Read		15	25	mA
IOP	Operation current	50MHz Write		30	45	mA
		50MHz Read		30	45	mA

8. Bus Timing (High-speed Mode)



SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTE
F_{SD}	SD clock frequency	0	25	MHz	
t_{WL}	Clock low time	10		ns	
t_{WH}	Clock high time	10		ns	
t_{TLH}	Clock rise time		10	ns	
t_{THL}	Clock fall time		10	ns	
t_{ISU}	Input setup time	5		ns	
t_{IH}	Input hold time	5		ns	
t_{ODLY}	Output delay time	0	14	ns	
t_{oH}	Output hold time	2.5		ns	



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