

Nand Flash Datasheet

XC2EAAQP-NTH

NAND FLASH 2Gbit (256Mx8bit) 3.3V 4bit ECC FBGA63

深圳市芯存科技有限公司

Tel: 0755-29708864

Technical support: fae@szxincun.com

Website: www.szxincun.com

Product models list:

| Specifications | FLASH | VCC | Packaging |
|----------------|-------|------|------------------------|
| XC2EAAQP-NTH | 2Gb | 3.3V | FBGA63 9 x 11 x 1.00mm |

Change History:

| Rev | Changes | Date | Note |
|--------|-----------------|------------|------|
| Rev1.0 | Initial release | 2022.11.15 | |
| Rev1.1 | Update logo | 2023.05.20 | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |

NAND Flash

- HIGH DENSITY NAND FLASH MEMORIES
 - Cost effective solutions for mass storage applications
- DENSITY
 - 2Gbit
- NAND INTERFACE
 - x8 bus width.
 - Pinout compatibility for all densities
- SUPPLY VOLTAGE
 - 3.3V device : Vcc = 2.7 V~3.6 V
- PAGE SIZE
 - 2Gb :
(2 K + 128 spare) Bytes
- BLOCK SIZE
 - x8
2 GB: (128 K + 8 K spare) Bytes
- PLANE SIZE
 - 2Gbit : 1024 Blocks per Plane
- DEVICE SIZE
 - 2Gbit : 2 plane per device or 256M byte
- PAGE READ / PROGRAM
 - Random access (tR): 2Gb 30 us (max.)
 - Sequential access :3.3V : 25 ns (min.)
 - Page program time :3.3V : 300 us (Typ)
- FAST BLOCK ERASE
 - 2Gbit : Block erase time: 3.5 ms (Typ)
- COPY BACK PROGRAM
 - Fast Data Copy without external buffering
- CACHE READ
 - Internal buffer to improve the read throughput
- CHIP ENABLE DON'T CARE
 - Simple interface with microcontroller
- STATUS REGISTER
 - Normal Status Register (Read/Program/Erase)
- HARDWARE DATA PROTECTION
 - Program/Erase locked during Power transitions.
- DATA RETENTION
 - 50,000 Program/Erase cycles
(With 4-bit ECC per 528 bytes (x8))
 - 10 years Data Retention
- ONFI 1.0 COMPLIANT COMMAND SET
- ELECTRONIC SIGNATURE
 - 1st cycle : Manufacturer Code
 - 2nd cycle : Device Code
 - 3rd cycle: Internal chip number, Cell Type, Number of Simultaneously Programmed Pages.
 - 4th cycle : Page size, Block size, Organization, Spare size
 - 5th cycle: ECC, Multi-plane information
- PACKAGE
 - : 63-Ball FBGA (9.0 x 11 x 1.0 mm)
- Operating Temperature
 - : 0°C ~70°C

1. SUMMARY DESCRIPTION

XC2EAAQP-NTH NAND Series is offered in 3.3 V Vcc Power Supply, and with x8 I/O interface. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased.

The device contains 2048 blocks in SLC NAND Device.

Data in the page can be read out at 45ns(3.3V) cycle time per byte. The I/O pins serve as the ports for address and data input/ output as well as command input. This interface allows a reduced pin count and easy migration towards different densities, without any rearrangement of footprint.

Commands, Data and Addresses are synchronously introduced using CE, WE, RE, ALE and CLE input pin.

The on-chip Program/Erase Controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. The modify operations can be locked using the WP input.

The chip supports CE don't care function. This function allows the direct download of the code from the NAND Flash memory device by a microcontroller, since the CE transitions do not stop the read operation.

In addition, device supports ONFI 1.0 specification.

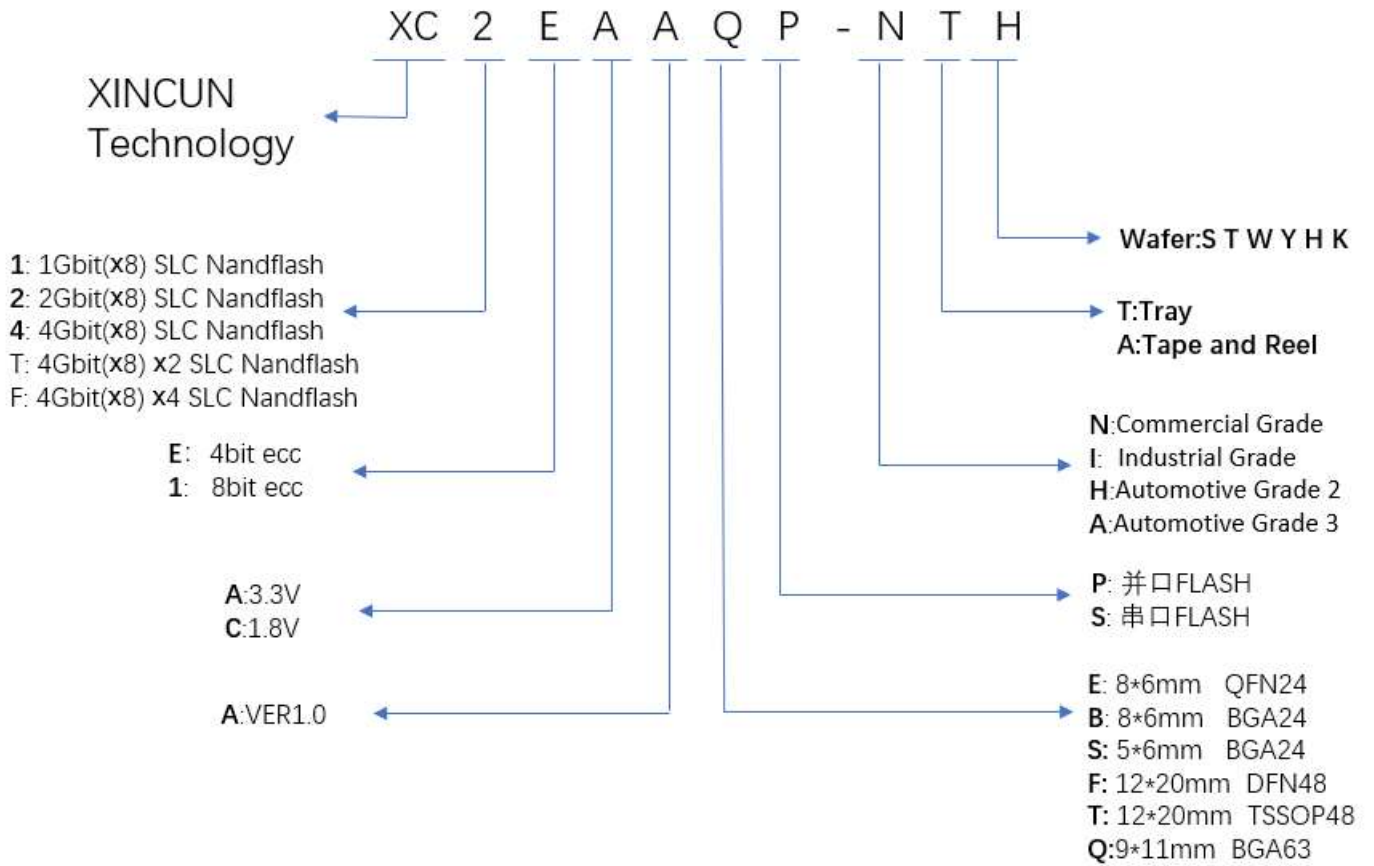
The output pin R/B (open drain buffer) signals the status of the device during each operation. In a system with multiple memories the R/B pins can be connected all together to provide a global status signal.

Even the write-intensive systems can take advantage of the XC2EAAQP-NTH NAND Series extended reliability of 100 K program/ erase cycles by providing ECC (Error Correcting Code) with real time mapping-out algorithm.

The copy back function allows the optimization of defective blocks management: when a page program operation fails the data can be directly programmed in another page inside the same array section without the time-consuming serial data insertion phase. Data read out after copy back read is allowed.

This device includes also extra features like OTP/Unique ID area, Read ID2 extension.

1.1 Xincun component Part Numbering Guide



1.2 Product Ordering Information

Figure 1-1 2Gb Logic Diagram

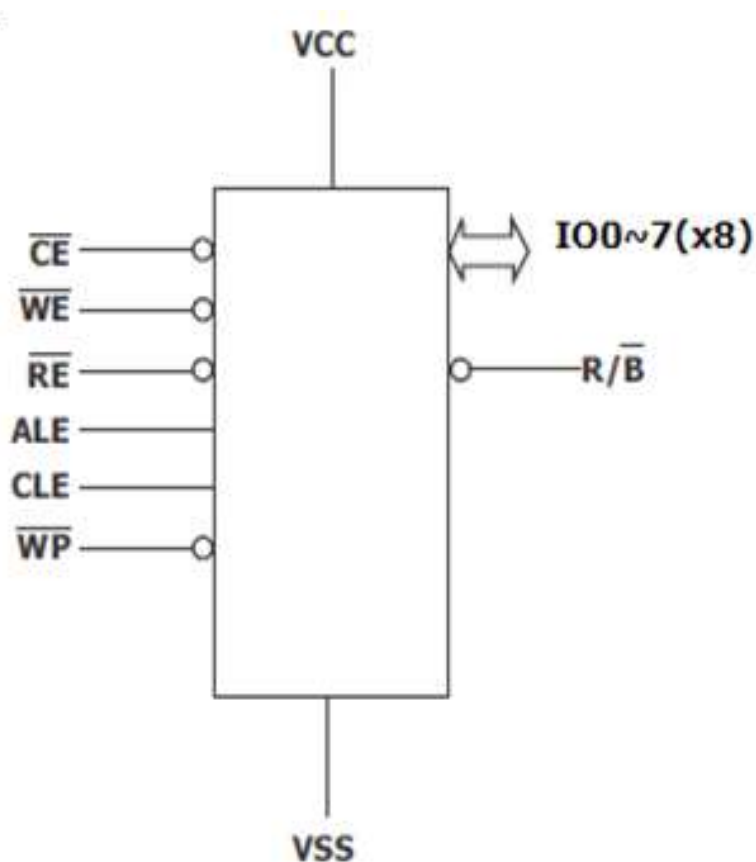


Table 1 Signal Names

| | |
|--------------|----------------------|
| IO0~IO7 (x8) | Data Input/Outputs |
| CLE | Command Latch Enable |
| ALE | Address Latch Enable |
| CE# | Chip Enable |
| RE# | Read Enable |
| WE# | Write Enable |
| WP# | Write Protect |
| R/B# | Read/Busy |
| VCC | Power Supply |
| VSS | Ground |
| NC | Not Connected |

Figure 1-2 2Gb Block diagram

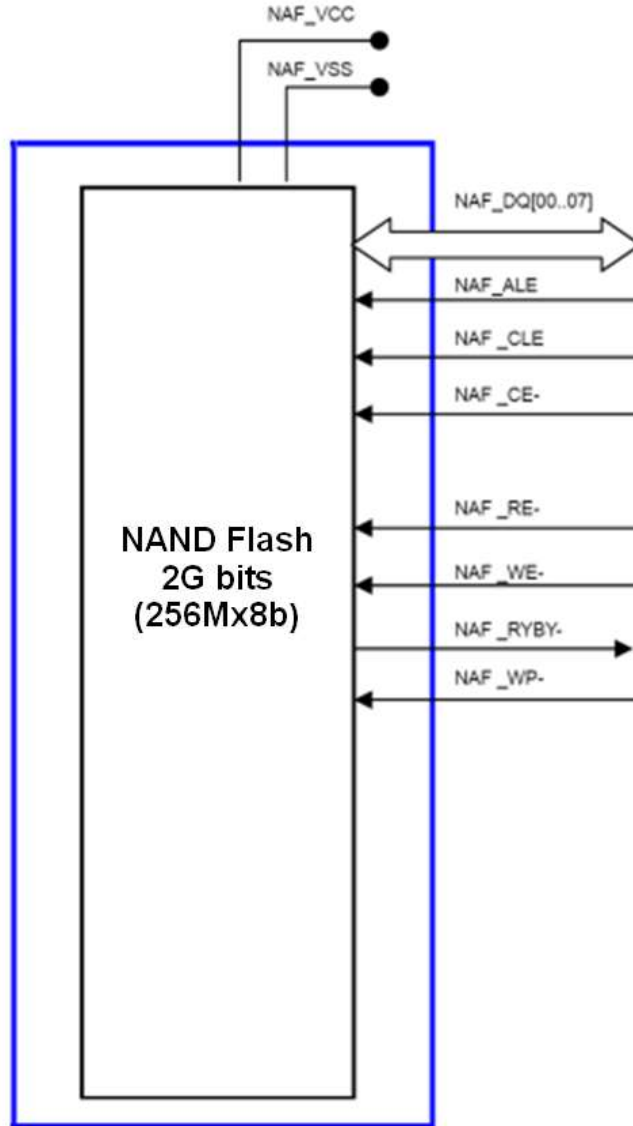


Figure 2-1 63-FBGA Contact, x8 Device, 9mm x 11mm

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
|---|-----|-----|---------|----------|----------|----------|----------|-----------|-----|-----|
| A | DNU | DNU | | | | | | | DNU | DNU |
| B | DNU | | | | | | | | DNU | DNU |
| C | | | NAF_WP- | NAF_ALE | NAF_VSS | NAF_CE- | NAF_WE- | NAF_BYBY- | | |
| D | | | NAF_VCC | NAF_RE- | NAF_CLE | NC | NC | NC | | |
| E | | | NC | NC | NC | NC | NC | NC | | |
| F | | | NC | NC | NC | NC | NAF_VSS | NC | | |
| G | | | DNU | NAF_VCC | NC | NC | NC | DNU | | |
| H | | | NC | NAF_DQ00 | NC | NC | NC | NAF_VCC | | |
| J | | | NC | NAF_DQ01 | NC | NAF_VCC | NAF_DQ05 | NAF_DQ07 | | |
| K | | | NAF_VSS | NAF_DQ02 | NAF_DQ03 | NAF_DQ04 | NAF_DQ06 | NAF_VSS | | |
| L | DNU | DNU | | | | | | | DNU | DNU |
| M | DNU | DNU | | | | | | | DNU | DNU |

1.3 PIN DESCRIPTION

Table 2 Pin Description

| Pin Name | Function | Description |
|---------------|----------------------|---|
| (x8)IO0 ~ IO7 | DATA INPUTS/OUTPUTS | The IO pins allow to input command, address and data and to output data during read / program operations. The inputs are latched on the rising edge of Write Enable (WE). The I/O buffer float to High-Z when the device is deselected or the outputs are disabled. |
| CLE | COMMAND LATCH ENABLE | This input activates the latching of the IO inputs inside the Command Register on the Rising edge of Write Enable (WE). |
| ALE | ADDRESS LATCH ENABLE | This input activates the latching of the IO inputs inside the Address Register on the Rising edge of Write Enable (WE). |
| CE | CHIP ENABLE | This input controls the selection of the device. |
| WE | WRITE ENABLE | This input acts as clock to latch Command, Address and Data. The IO inputs are latched on the rise edge of WE. |
| RE | READ ENABLE | The RE input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of RE which also increments the internal column address counter by one. |
| WP | WRITE PROTECT | The WP pin, when Low, provides an Hardware protection against undesired modify (program / erase) operations. |
| R/B | READY BUSY | The Ready/Busy output is an Open Drain pin that signals the state of the memory. |
| Vcc | SUPPLY VOLTAGE | The Vcc supplies the power for all the operations (Read, Write, Erase). |
| Vss | GROUND | GROUND |
| NC | NO CONNECTION | NO CONNECTION |

Note:

1. A 0.1uF capacitor should be connected between the Vcc Supply Voltage pin and the Vss Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.

Figure3-1 2Gb Array Organization (x8)

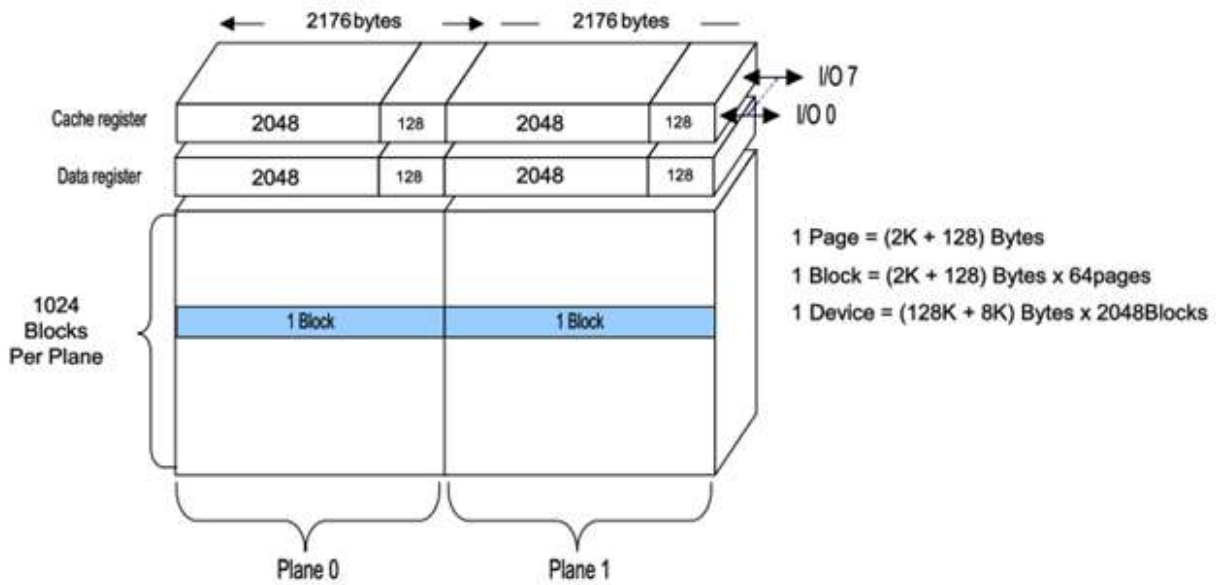


Table 3 2Gb Address Cycle Map

| | IO[15:8] | IO0 | IO1 | IO2 | IO3 | IO4 | IO5 | IO6 | IO7 |
|-----------------------|----------|-----|-----|-----|-----|-----|-----|-----|-----|
| | x8 | | | | | | | | |
| 1 st Cycle | - | A0 | A1 | A2 | A3 | A4 | A5 | A6 | A7 |
| 2 nd Cycle | - | A8 | A9 | A10 | A11 | Low | Low | Low | Low |
| 3 rd Cycle | - | A12 | A13 | A14 | A15 | A16 | A17 | A18 | A19 |
| 4 th Cycle | - | A20 | A21 | A22 | A23 | A24 | A25 | A26 | A27 |
| 5 th Cycle | - | A28 | Low | Low | Low | Low | Low | Low | Low |

Notes:

1. Low must be set to Low.
2. 1st & 2nd cycle are Column Address.
3. 3rd to 5th cycle are Row Address.

For the x8 address bits, the following rules apply:

- A0 - A11: column address in the page
- A12 - A17: page address in the block
- A18: plane address (for multiplane operations) / block address (for normal operations)
- A19 - A28: block address

1.4 Command Set

Table 4 2Gb Command Set

| Function | 1 st Cycle | 2 nd Cycle | 3 rd Cycle | 4 th Cycle | Acceptable Command During Busy |
|---|-----------------------|-----------------------|-----------------------|-----------------------|--------------------------------|
| PAGE READ | 00h | 30h | - | - | No |
| READ FOR COPY-BACK | 00h | 35h | | | No |
| SPECIAL READ FOR COPY BACK | 00h | 36h | | | No |
| READ ID | 90h | | | | No |
| READ ID2 | 30h-65h-00h | 30h | | | |
| RESET | FFh | | | | Yes |
| PAGE PROGRAM(Start) CACHE PROGRAM(End) | 80h | 10h | | | No |
| CACHE PROGRAM(Start) | 80h | 15h | | | No |
| PAGE RE-PROGRAM | 8Bh | 10h | | | No |
| COPY BACK PROGRAM | 85h | 10h | | | No |
| (Traditional) MULTI PLANE PROGRAM | 80h | 11h | 81h | 10h | No |
| ONFI MULTIPLANE PROGRAM | 80h | 11h | 80h | 10h | No |
| MULTIPLANE PAGE RE-PROGRAM | 8Bh | 11h | 8Bh | 10h | No |
| (Traditional) MULTI PLANE CACHE PGM(start/cont) | 80h | 11h | 81h | 15h | No |
| ONFI MULTI PLANE CACHE PGM(start/cont) | 80h | 11h | 80h | 15h | No |
| (Traditional) MULTI PLANE CACHE PGM(end) | 80h | 11h | 81h | 10h | No |
| ONFI MULTIPLANE CACHE PGM(end) | 80h | 11h | 80h | 10h | No |
| (Traditional) MULTI PLANE COPY BACK PROGRAM | 85h | 11h | 81h | 10h | No |
| ONFI MULTI PLANE COPY BACK PROGRAM | 85h | 11h | 85h | 10h | No |
| BLOCK ERASE | 60h | D0h | | | No |
| (Traditional) MULTI PLANE BLOCK ERASE | 60h | 60h | D0h | | No |
| ONFI MULTIPLANE BLOCK ERASE | 60h | D1h | 60h | D0h | No |
| READ STATUS REGISTER | 70h | | | | Yes |
| READ STATUS ENHANCED | 78h | | | | Yes |
| RANDOM DATA INPUT | 85h | | | | No |
| RANDOM DATA OUTPUT | 05h | E0h | | | No |
| CACHE READ (SEQUENTIAL) | 31h | | | | No |
| CACHE READ ENHANCED (RANDOM) | 00h | 31h | | | No |
| CACHE READ(End) | 3Fh | | | | No |
| READ PARAMETER PAGE | ECh | | | | No |

1.5 Mode Selection

Table 5 Mode Selection

| Mode | | CLE | ALE | CE# | WE# | RE# | WP# |
|---------------------------------|--------------------------|------|-------------------|------|-------------------|-------------------|-----------------------|
| Read Mode | Command Input | High | Low | Low | Rising | High | X |
| | Address Input (4 cycles) | Low | High | Low | Rising | High | X |
| Program | Command Input | High | Low | Low | Rising | High | High |
| | Address Input (4 cycles) | Low | High ¹ | Low | Rising | High | High |
| Data Input | | Low | Low | Low | Rising | High | High |
| Sequential Read and Data Output | | Low | Low ¹ | Low | High | Falling | X |
| Busy Time in Read | | Low | Low | Low | High ³ | High ³ | X |
| Busy Time in Program | | X | X ¹ | X | X | X | High |
| Busy Time in Erase | | X | X | X | X | X | High |
| Write Protect | | X | X | X | X | X | Low |
| Stand By | | X | X | High | X | X | 0V / Vcc ² |

Notes:

1. 0X can be VIL or VIH. H = Logic level HIGH. L = Logic level LOW.
2. WP# should be biased to CMOS high or CMOS low for stand-by mode.
3. WE# and RE# during Read Busy must be keep on high to prevent unplanned command/address/data input or to avert unintended data out. In this time, only Reset, Read Status, and Multi Plane Read Status can be input to the device.

2 BUS OPERATION

There are six standard bus operations that control the device. These are Command Input, Address Input, Data Input, Data Output, Write Protect, and Standby.

Typically glitches less than 5 ns on Chip Enable, Write Enable and Read Enable are ignored by the memory and do not affect bus operations.

2.1 Command Input

Command Input bus operation is used to give a command to the memory device. Command are accepted with Chip Enable low, Command Latch Enable High, Address Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation (write/erase) the Write Protect pin must be high. See Figure 5 and Table 12 for details of the timings requirements.

2.2 Address Input

The Address Input bus operation allows the insertion of the memory address. For the 2Gb and 4Gb devices, five write cycles are needed to input the addresses. For the 1Gb, four write cycles are needed to input the addresses. If necessary, a 5th dummy address cycle can be issued to 1Gb, which will be ignored by the NAND device without causing problems. Addresses are accepted with Chip Enable low, Address Latch Enable high, Command Latch Enable low, and Read Enable high and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation (write/erase) the Write Protect pin must be high. See Figure 6 and Table 12 for details of the timings requirements.

2.3 Data Input

Data Input bus operation allows to feed to the device the data to be programmed. The data insertion is serially and timed by the Write Enable cycles. Data are accepted only with Chip Enable low, Address Latch Enable low, Command Latch Enable low, Read Enable High, and Write Protect High and latched on the rising edge of Write Enable. See Figure 7 and Table 12 for details of the timings requirements.

2.4 Data Output

Data Output bus operation allows to read data from the memory array and to check the status register content, the lock status and the ID data. Data can be serially shifted out toggling the Read Enable pin with Chip Enable low, Write Enable High, Address Latch Enable low, and Command Latch Enable low. See Figure 8, 9, 10 and Table 12 for details of the timings requirements.

2.5 Write Protect

Hardware Write Protection is activated when the Write Protect pin is low. In this condition modify operation do not start and the content of the memory is not altered. Write Protect pin is not latched by Write Enable to ensure the protection even during the power up.

2.6 Standby

In Standby the device is deselected, outputs are disabled and Power Consumption reduced.

3 DEVICE OPERATION

3.1 Page Read

Upon initial device power up, the device defaults to Read mode. This operation is also initiated by writing 00h and 30h to the command register along with four address cycles. In two consecutive read operations, the second one does not need 00h command, which four address cycles and 30h command initiates that operation. Second read operation always requires setup command if first read operation was executed using also random data out command.

Two types of operations are available: random read, serial page read. The random read mode is enabled when the page address is changed. The 2112 bytes of data within the selected page are transferred to the data registers in less than 25 us(tR). The system controller may detect the completion of this data transfer (tR) by analyzing the output of R/B pin. Once the data in a page is loaded into the data registers, they may be read out in 25 ns cycle time by sequentially pulsing RE. The repetitive high to low transitions of the RE clock make the device output the data starting from the selected column address up to the last column address.

The device may output random data in a page instead of the consecutive sequential data by writing random data output command.

The column address of next data, which is going to be out, may be changed to the address which follows random data output command.

Random data output can be operated multiple times regardless of how many times it is done in a page.

After power up, device is in read mode so 00h command cycle is not necessary to start a read operation.

Any operation other than read or random data output causes device to exit read mode. Check Figure 11, Figure 12, and Figure 13 as references.

3.2 Page Program

The device is programmed basically by page, but it does allow multiple partial page programming of a word or consecutive bytes up to 2112, in a single page program cycle. The number of consecutive partial page programming operation within the same page without an intervening erase operation must not exceed 8; for example, 4 times for main array (1time/512byte) and 4 times for spare array (1time/16byte).

A page program cycle consists of a serial data loading period in which up to 2112 bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell.

The serial data loading period begins by inputting the Serial Data Input command (80h), followed by the four cycle address inputs and then serial data. The words other than those to be programmed do not need to be loaded. The device supports random data input in a page. The column address of next data, which will be entered, may be changed to the address which follows random data input command (85h). Random data input may be operated multiple times regardless of how many times it is done in a page.

The Page Program confirm command (10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write state controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/B output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit (I/O 0) may be checked. The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register. Figure 14 and Figure 15 detail the sequence.

3.3 Block Erase

The Erase operation is done on a block basis. Block address loading is accomplished in two cycles initiated by an Erase Setup command (60h). Only address A18 to A27 is valid while A12 to A17 are ignored. The Erase Confirm command (D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.

At the rising edge of WE after the erase confirm command input, the internal write controller handles erase and erase verify. Once the erase process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of an erase by monitoring the R/B output, or the Status bit (I/O 6) of the Status Register.

Only the Read Status command and Reset command are valid while erasing is in progress. When the erase operation is completed, the Write Status Bit (I/O 0) may be checked.

Figure 18 details the sequence.

3.4 Copy-Back Program

The copy-back program is configured to quickly and efficiently rewrite data stored in one page without utilizing an external memory. Since the time-consuming cycles of serial access and re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block is also needed to be copied to the newly assigned free block. The operation for performing a copy-back program is a sequential execution of page-read without serial access and copying-program with the address of destination page. A read operation with "35h" command and the address of the source page moves the whole 2112byte data into the internal data buffer. As soon as the device returns to Ready state, optional data read-out is allowed by toggling RE, or Copy Back command (85h) with the address cycles of destination page may be written. The Program Confirm command (10h) is required to actually begin the programming operation. Data input cycle for modifying a portion or multiple distant portions of the source page is allowed as shown in Figure 17.

"When there is a program-failure at Copy-Back operation, error is reported by pass/fail status. But, if Copy-Back operations are accumulated over time, bit error due to charge loss is not checked by external error detection/correction scheme.

For this reason, two bit error correction is recommended for the use of Copy-Back operation." Figure 16 and Figure 17 show the command sequence for the copy-back operation.

Please note that WP value is don't care during Read for copy back, while it must be set to Vcc when performing the program .

3.5 Read Status Register

The device contains a Status Register which may be read to find out whether read, program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of CE or RE, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/B pins are common-wired. RE or CE does not need to be toggled for updated status. Refer to Table13 for specific Status Register definitions, and Figure 10 for specific timings requirements. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the read command (00h) should be given before starting read cycles.

3.6 Reset

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value E0h when WP is high. Refer to Table 13 for device status after reset operation. If the device is already in reset state a new reset command will not be accepted by the command register. The R/B pin transitions to low for tRST after the Reset command is written (see Figure 19).

3.7 Read Cache

The Read Cache function permits a page to be read from the page register while another page is simultaneously read from the Flash array. A Read Page command, as defined in 3.1, shall be issued prior to the initial sequential or random Read Cache command in a read cache sequence.

The Read Cache function may be issued after the Read function is complete (SR[6] is set to one). The host may enter the address of the next page to be read from the Flash array. Data output always begins at column address 00h. If the host does not enter an address to retrieve, the next sequential page is read. When the Read Cache function is issued, SR[6] is cleared to zero (busy). After the operation is begun SR[6] is set to one (ready) and the host may begin to read the data from the previous Read or Read Cache function. Issuing an additional Read Cache function copies the data most recently read from the array into the page register. When no more pages are to be read, the final page is copied into the page register by issuing the 3Fh command. The host may begin to read data from the page register when SR[6] is set to one (ready). When the 31h and 3Fh commands are issued, SR[6] shall be cleared to zero (busy) until the page has finished being copied from the Flash array.

The host shall not issue a sequential Read Cache (31h) command after the last page of the device is read.

Figure 20 defines the Read Cache behavior and timings for the beginning of the cache operations subsequent to a Read command being issued. SR[6] conveys whether the next selected page can be read from the page register. Figure 20 also shows the Read Cache behavior and timings for the end of cache operation.

3.8 Read ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h.

3.9 Legacy Read ID

Four read cycles sequentially output the manufacturer code (ADh), and the device code and 00h, 4th cycle ID, respectively.

The command register remains in Read ID mode until further commands are issued to it.

Shows the operation sequence, while Table 14 to Table 17 explain the byte meaning.

3.10 Read ONFI Signature

To retrieve the ONFI signature, the command 90h together with an address of 20h shall be entered (i.e. it is not valid to enter an address of 00h and read 36 bytes to get the ONFI signature). The ONFI signature is the ASCII encoding of 'ONFI' where 'O' = 4Fh, 'N' = 4Eh, 'F' = 46h, and 'I' = 49h. Reading beyond four bytes yields indeterminate values. Figure 22 shows the operation sequence.

3.11 Read Parameter Page

The Read Parameter Page function retrieves the data structure that describes the chip's organization, features, timing and other behavioral parameters. Figure 23 defines the Read Parameter Page behavior. This data structure enables the host processor to automatically recognize the NAND Flash configuration of a device. The whole data structure is repeated at least three times.

The Random Data Read command can be issued during execution of the read parameter page to read specific portions of the parameter page. The Read Status command may be used to check the status of read parameter page during execution.

After completion of the Read Status command, 00h is issued by the host on the command line to continue with the data output flow for the Read Parameter Page command.

Read Status Enhanced shall not be used during execution of the Read Parameter Page command.

Note:

For Tech 32nm XC2EAAQP-NTH SLC NAND, for a particular condition, the Read Parameter Page command does not give the correct values. To overcome this issue, the host must issue a Reset command before the Read Parameter Page command. Issuance of Reset before the Read Parameter Page command will provide the correct values.

3.12 Parameter Page Data Structure Definition

Table 18 defines the parameter page data structure. For parameters that span multiple bytes, the least significant byte of the parameter corresponds to the first byte. Values are reported in the parameter page in units of bytes when referring to items related to the size of data access (as in an 8-bit data access device). For example, the chip will return how many data bytes are in a page. For a device that supports 16-bit data access, the host is required to convert byte values to word values for its use. Unused fields should be cleared to 0h. For more detailed information about Parameter Page Data bits, refer to ONFI Specification 1.0 section 5.4.1

Table 5.1 Parameter Page Description

| Byte | O/M | Description |
|--|-----|---|
| Revision information and features block | | |
| 0-3 | M | Parameter page signature Byte 0: 4Fh, "O" Byte 1: 4Eh, "N" Byte 2: 46h, "F" Byte 3: 49h, "I" |
| 4-5 | M | Revision number 2-15 Reserved (0) 1 1 = supports ONFI version 1.0 0 Reserved (0) |
| 6-7 | M | Features supported 5-15 Reserved (0) 4 1 = supports odd to even page copy-back 3 1 = supports interleaved operations 2 1 = supports non-sequential page programming 1 1 = supports multiple LUN operations |
| 8-9 | M | Optional commands supported 6-15 Reserved (0) 5 1 = supports Read Unique ID 4 1 = supports copy-back 3 1 = supports Read Status Enhanced 2 1 = supports Get Features and Set Features 1 1 = supports Read Cache commands 0 1 = supports Page Cache Program command |
| 10-31 | | Reserved (0) |
| Manufacturer information block | | |
| 32-43 | M | Device manufacturer (12 ASCII characters) |
| 44-63 | M | Device model (20 ASCII characters) |
| 64 | M | JEDEC manufacturer ID |
| 65-66 | O | Date code |
| 67-79 | | Reserved (0) |
| Memory organization block | | |
| 80-83 | M | Number of data bytes per page |
| 84-85 | M | Number of spare bytes per page |
| 86-89 | M | Number of data bytes per partial page |
| 90-91 | M | Number of spare bytes per partial page |
| 92-95 | M | Number of pages per block |
| 96-99 | M | Number of blocks per logical unit (LUN) |
| 100 | M | Number of logical units (LUNs) |
| 101 | M | Number of address cycles 4-7 Column address cycles 0-3 Row address cycles |
| 102 | M | Number of bits per cell |
| 103-104 | M | Bad blocks maximum per LUN |
| 105-106 | M | Block endurance |
| 107 | M | Guaranteed valid blocks at beginning of target |
| 108-109 | M | Block endurance for guaranteed valid blocks |
| 110 | M | Number of programs per page |

| Byte | O/M | Description |
|------------------------------------|-----|--|
| Memory organization block | | |
| 111 | M | Partial programming attributes 5-7 Reserved 4 1 = partial page layout is partial page data followed by partial page spare 1-3 Reserved 0 1 = partial page programming has constraints |
| 112 | M | Number of bits ECC correctability |
| 113 | M | Number of interleaved address bits 4-7 Reserved (0) 0-3 Number of interleaved address bits |
| 114 | O | Interleaved operation attributes 4-7 Reserved (0) 3 Address restrictions for program cache 2 1 = program cache supported 1 1 = no block address restrictions 0 Overlapped / concurrent interleaving support |
| 115-127 | | Reserved (0) |
| Electrical parameters block | | |
| 128 | M | I/O pin capacitance |
| 129-130 | M | Timing mode support 6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0, shall be 1 |
| 131-132 | O | Program cache timing mode support 6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0 |
| 133-134 | M | t _{PROG} Maximum page program time (μs) |
| 135-136 | M | t _{BERS} Maximum block erase time (μs) |
| 137-138 | M | t _R Maximum page read time (μs) |
| 139-140 | M | t _{CCS} Minimum change column setup time (ns) |
| 141-163 | | Reserved (0) |
| Vendor block | | |
| 164-165 | M | Vendor specific Revision number |
| 166-253 | | Vendor specific |
| 254-255 | M | Integrity CRC |
| Redundant Parameter Pages | | |
| 256-511 | M | Value of bytes 0-255 |
| 512-767 | M | Value of bytes 0-255 |
| 768+ | O | Additional redundant parameter pages |

Table 5.1 Parameter Page Description(continue)

Note:

1. "O" Stands for Optional, "M" for Mandatory.

4 OTHER FEATURES

4.1 Data Protection

The device is designed to offer protection from any involuntary program/erase during power- transitions. An internal voltage detector disables all functions whenever Vcc is below about 3.3 V version. WP pin provides hardware protection and is recommended to be kept at VIL during power-up and power-down. A recovery time of minimum 10us is required before internal circuit gets ready for any command sequences as shown in Figure 24. The two-step command sequence for program/erase provides additional software protection.

4.2 Ready/Busy

The device has a Ready/Busy output that provides method of indicating the completion of a page program, erase, copyback, cache program and random read completion. The R/B pin is normally high and goes to low when the device is busy (after a reset, read, program, erase operation). It returns to high when the internal controller has finished the operation.

The pin is an open-drain driver thereby allowing two or more R/B outputs to be Or-tied. Because pull-up resistor value is related to tr(R/B) and current drain during busy (I busy), an appropriate value can be obtained with the following reference chart (Figure 25). Its value can be determined by the following guidance.

Table 6 Number of Valid Blocks

| Density | Symbol | Min | Typ | Max | Unit |
|---------|-----------------|------|-----|------|--------|
| 2Gb | N _{VB} | 2008 | - | 2048 | Blocks |

Note:

- The 1st block is guaranteed to be a valid block at the time of shipment.

Table 7 Absolute Maximum Ratings

| Symbol | Parameter | Value | Unit |
|-------------------|--|--------------|------|
| T _A | Ambient Operation Temperature (Commercial Temperature Range) | 0 to 70 | °C |
| T _{bias} | Temperature Under Bias | -50 to +125 | °C |
| T _{stg} | Storage Temperature | -65 to +150 | °C |
| V _{io} | Input or Output Voltage | -0.6 to +4.6 | V |
| V _{cc} | Supply Voltage | -0.6 to +4.6 | V |

Notes:

- Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the XC2EAAQP-NTH SURE Program and other relevant quality documents.
- Minimum Voltage may undershoot to -2V during transition and for less than 20ns during transitions.

Figure 4 Functional Block Diagram

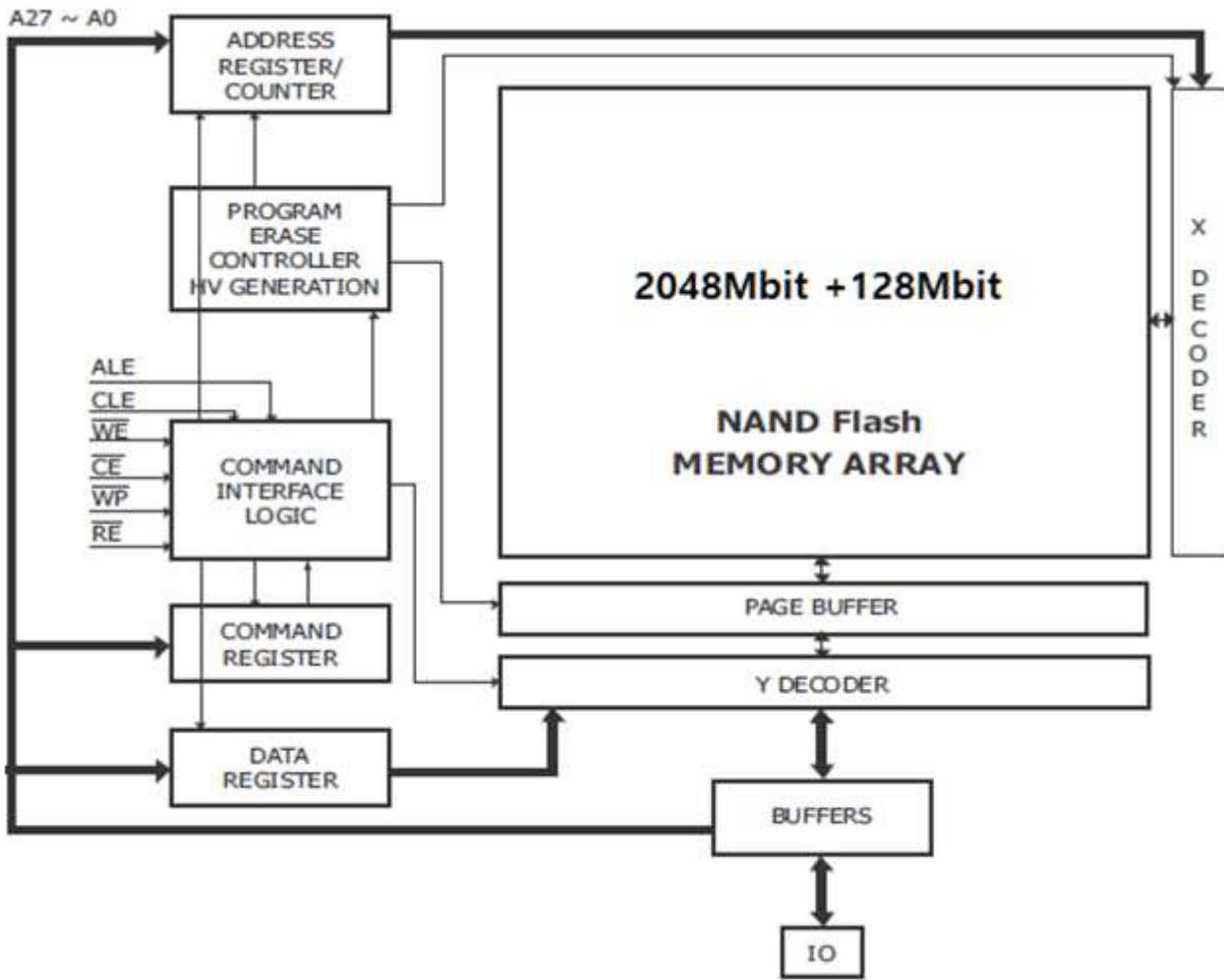


Table 8.1 (3.3V) DC and Operating Characteristics

| Parameter | Symbol | Test Conditions | 2.7V ~ 3.6V | | | Units | |
|---------------------------|-----------|----------------------------------|-------------------------------|-----|---------------|-------|----|
| | | | Min | Typ | Max | | |
| Power-On-Reset Current | ICC0 | FFh command input after power on | - | | 50 per device | mA | |
| Operating Current | Read | tRC=tRC(min) CE#=VIL,IOUT=0mA | - | 15 | 30 | mA | |
| | Program | Normal | - | - | 30 | mA | |
| | | Cache | - | - | 40 | mA | |
| Erase | ICC3 | | - | 15 | 30 | mA | |
| Standby Current,(TTL) | ICC4 | CE# = VIH WP# = 0V/VCC | - | - | 1 | mA | |
| Standby Current, (CMOS) | 2Gb | ICC5 | CE# = Vcc-0.2 WP# = 0V/VCC | - | 10 | 50 | uA |
| Input Leakage Current | ILI | VIN=0 to VCC (Max) | - | - | ± 10 | uA | |
| Output Leakage Current | ILO | VOUT=0 to VCC (Max) | - | - | ± 10 | uA | |
| Input High Voltage | VIH | - | Vccx0.8 | - | Vcc+0.3 | | |
| Input Low Voltage | VIL | - | -0.3 | - | Vccx0.2 | | |
| Output High Voltage | VOH | IOH = -400uA | 2.4 | - | - | | |
| Output Low Voltage | VOL | IOL = -100uA | | | 0.4 | | |
| Output Low Current (R/B#) | IOL(R/B#) | VOL = 0.1V | 8 | 10 | - | mA | |

Table 8.2 (3.3V) AC Test Conditions

| Parameter | Value |
|--------------------------------|--------------------------|
| | 2.7V ≤ Vcc ≤ 3.6V |
| Input Pulse Levels | 0 V to Vcc |
| Input Rise and Fall Times | 5 ns |
| Input and Output Timing Levels | Vcc /s |
| Output Load (2.7V – 3.6V) | 1 TTL GATE and CL= 50 pF |

Note:

- These parameters are verified device characterization and are not 100% tested.

Table 9 Pin Capacitance (TA = 25 °C, f = 1.0 MHz)

| Item | Symbol | Test Condition | Min | Max | Unit |
|----------------------------|--------|----------------|-----|-----|------|
| Input Capacitance | CIN | VIN = 0V | - | 10 | pF |
| Input / Output Capacitance | CIO | VIL = 0V | - | 10 | pF |

Note:

1. For the stacked devices version, the Input is 10 pF x [number of stacked chips] and the Input/Output is 10 pF x [number of stacked chips]

Table 10 Program / Erase Characteristics

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|--------|-----|-----|-------|------|
| Program Time | tPROG | - | 300 | 700 | Us |
| Dummy Busy Time for Cache Program | tCBSY | - | 3 | 700 | us |
| Dummy Busy Time for the Lock or Lock-tight Block | tLBSY | - | 5 | 10 | us |
| Read Cache busy time | tCBSYR | - | 3 | tR | us |
| Cache Program short busy time | tCBSYW | - | 5 | tPROG | us |
| Block Erase Time | tBERS | - | 3.5 | 10 | ms |

Note:

1. Typical value is measured at Vcc=3.3V, TA=25°C (3.3V Device) Not 100% tested.

Table 11 AC Timing Characteristics

| Parameter | Symbol | 3.3V | | Unit |
|--|---------------------------------|------|------------------------|------|
| | | Min | Max | |
| ALE to RE# delay | t _{AR} | 10 | | ns |
| ALE hold time | t _{ALH} | 5 | | ns |
| ALE setup time | t _{ALS} | 12 | | ns |
| Address to data loading time | t _{ADL} | 70 | | ns |
| CE# Access Time | t _{CEA} ^{*4} | | 25 | ns |
| CE# low to RE# low | t _{CR} | 10 | | ns |
| CE# hold time | t _{CH} | 5 | | ns |
| CE# high to output High-Z | t _{CHZ} | | 50 | ns |
| CLE hold time | t _{CLH} | 5 | | ns |
| CLE to RE# delay | t _{CLR} | 10 | | ns |
| CLE setup time | t _{CLS} | 12 | | ns |
| CE# high to output hold | t _{COH} ^{*3} | 15 | | ns |
| CE# high to ALE or CLE don't care | t _{CSD} | 10 | | ns |
| CE# setup time | t _{CS} | 20 | | ns |
| Data hold time | t _{DH} | 5 | | ns |
| Data setup time | t _{DS} | 12 | | ns |
| Data transfer from cell to register | t _r | | 30 | μs |
| Output High-Z to RE# low | t _{IR} | 0 | | ns |
| Read cycle time | t _{RC} | 25 | | ns |
| RE# access time | t _{REA} | | 20 | ns |
| RE# high hold time | t _{REH} | 10 | | ns |
| RE# high to output hold | t _{RHOH} ^{*3} | 15 | | ns |
| RE# high to WE# low | t _{RHW} | 100 | | ns |
| RE# high to output High-Z | t _{RHZ} | | 100 | ns |
| RE# low to output hold | t _{RLOH} | 5 | | ns |
| RE# pulse width | t _{RP} | 12 | | ns |
| Ready to RE# low | t _{RR} | 20 | | ns |
| Device resetting time (Read/Program/Erase) | t _{RST} | - | 5/10/500 ^{*2} | μs |
| WE# high to busy | t _{WB} | | 100 | ns |
| Write cycle time | t _{WC} | 25 | | ns |
| WE# high hold time | t _{WH} | 10 | | ns |
| WE# high to RE# low | t _{WHR} | 60 | | ns |
| WE# high to RE# low for Random data out | t _{WHR2} | 200 | | ns |
| WE# pulse width | t _{WP} | 12 | | ns |
| Write protect time | t _{WW} | 100 | | ns |

Notes:

1. The time to Ready depends on the value of the pull-up resistor tied to R/B# pin.
2. If Reset Command (FFh) is written at Ready state, the device goes into Busy for maximum 5μs.
3. CE# low to high or RE# low to high can be at different times and produce three cases. Depending on which signal comes high first, either t_{COH} or t_{RHOH} will be met.
4. During data output, t_{CEA} depends partly on t_{CR} (CE# low to RE# low). If t_{CR} exceeds the minimum value specified, then the maximum time for t_{CEA} may also be exceeded (t_{CEA} = t_{CR} + t_{REA}).

Table 12 Status Register Coding

| ID | Page Program | Block Erase | Read | Read Cache | Coding |
|----|---------------|---------------|---------------|----------------------|--|
| 0 | Pass / Fail | Pass / Fail | NA | NA | Pass : '0' Fail : '1' |
| 1 | NA | NA | NA | NA | - |
| 2 | NA | NA | NA | NA | - |
| 3 | NA | NA | NA | NA | - |
| 4 | NA | NA | NA | NA | - |
| 5 | Ready / Busy | Ready / Busy | Ready / Busy | P/E/R Controller Bit | Active : '0' Idle : '1' |
| 6 | Ready / Busy | Ready / Busy | Ready / Busy | Ready / Busy | Busy : '0' Ready : '1' |
| 7 | Write Protect | Write Protect | Write Protect | NA | Protected : '0' Not Protected : '1' |

Table 13 Device Identifier Coding

| Device Identifier Byte | Description |
|------------------------|---|
| 1st | Manufacturer Code |
| 2nd | Device Identifier |
| 3rd | Internal chip number, cell type, etc. |
| 4th | Page Size, Block Size, Spare Size, Organization |
| 5th | ECC, Multiplane information |

Table 14 Read ID Data Table

| Density | Org | Vcc | 1 st | 2 nd | 3 rd | 4 th | 5 th |
|---------|-----|------|-----------------|-----------------|-----------------|-----------------|-----------------|
| 2Gb | x8 | 3.3V | ADh | DAh | 90h | 95h | 46h |

Figure 5 Command Latch Cycle

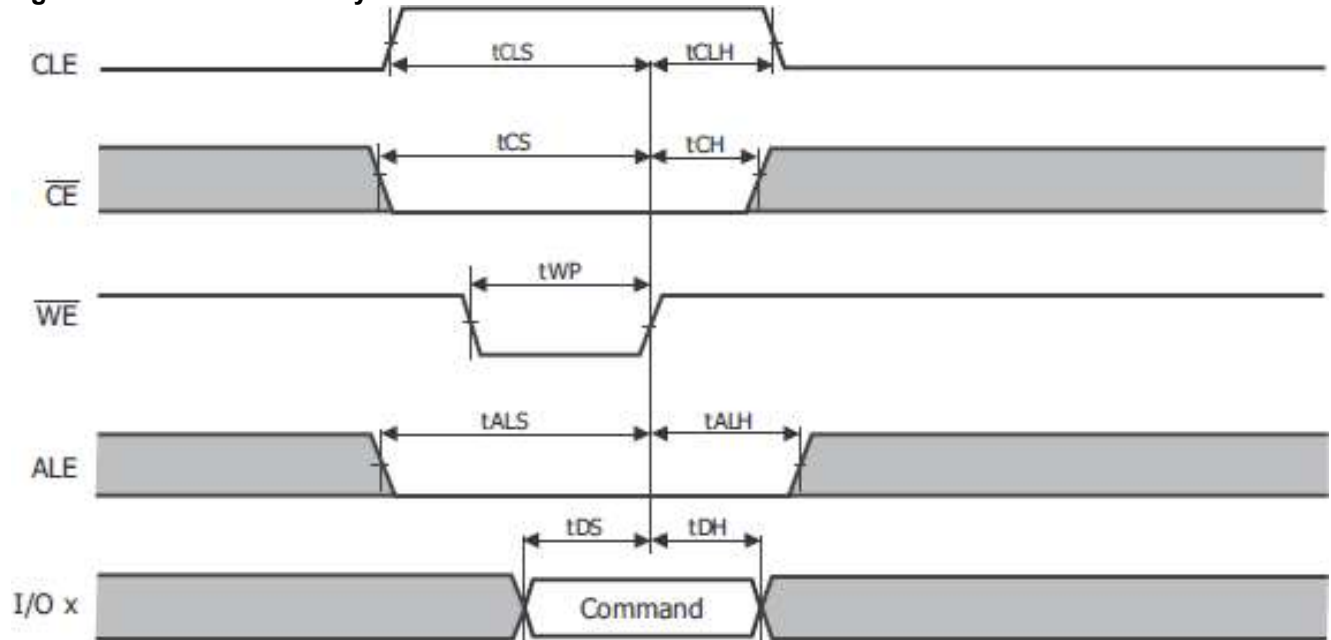


Figure 6 Address Latch Cycle

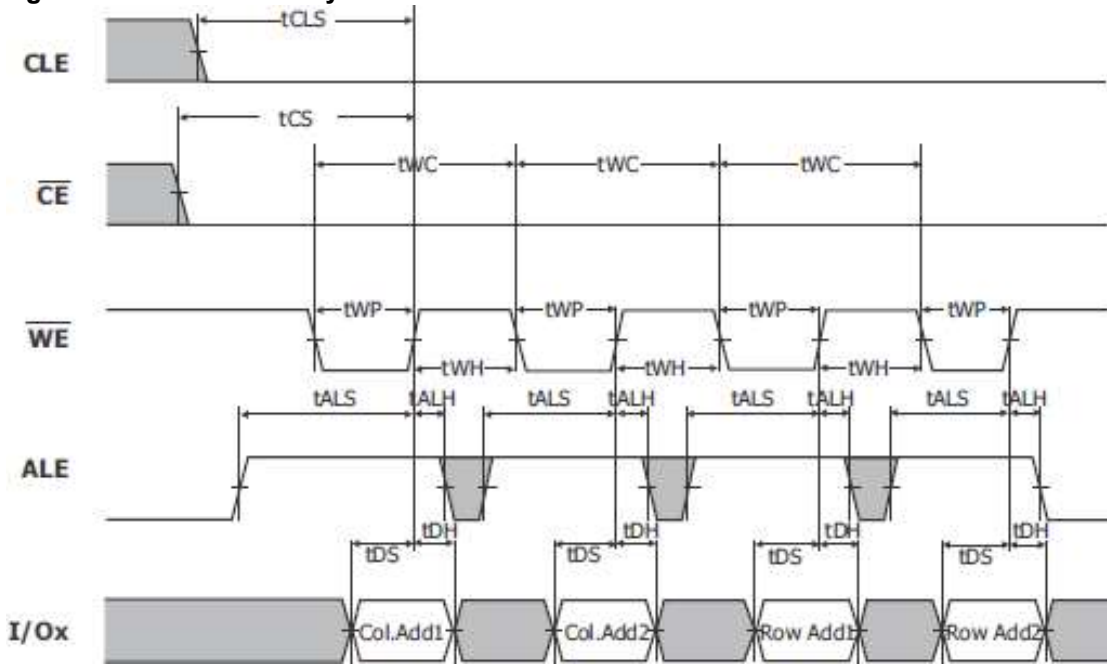


Figure 7 Input Data Latch Cycle

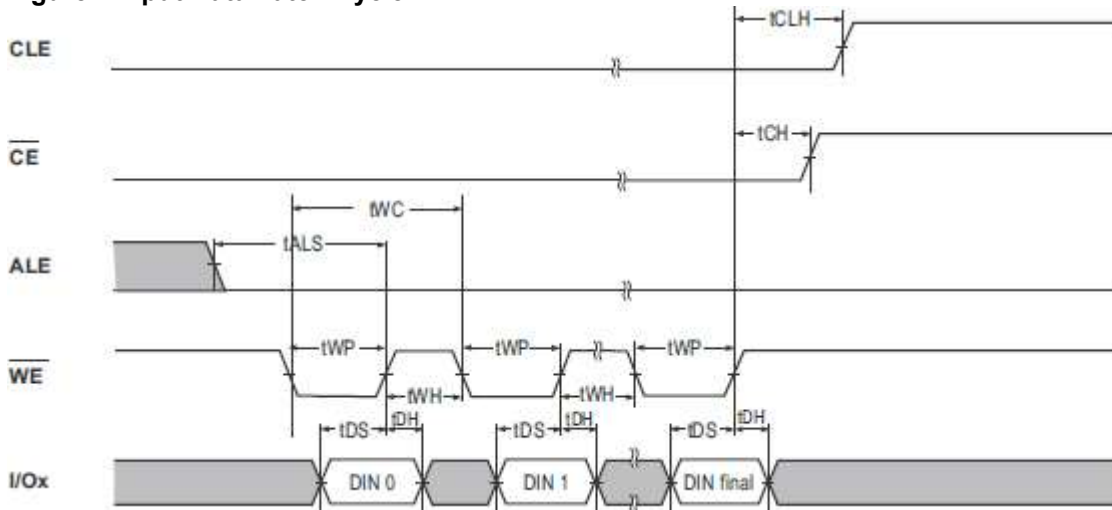
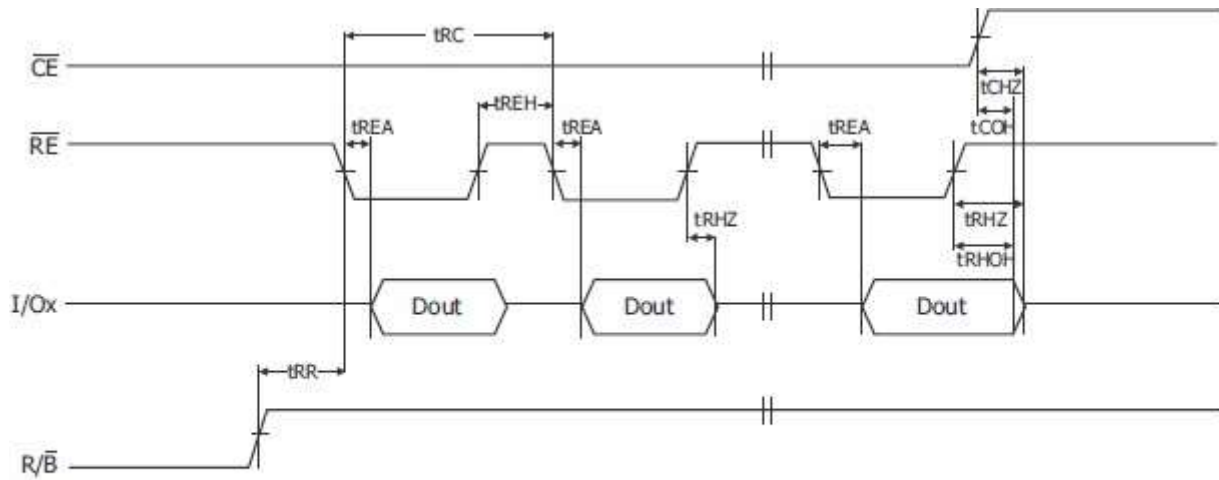
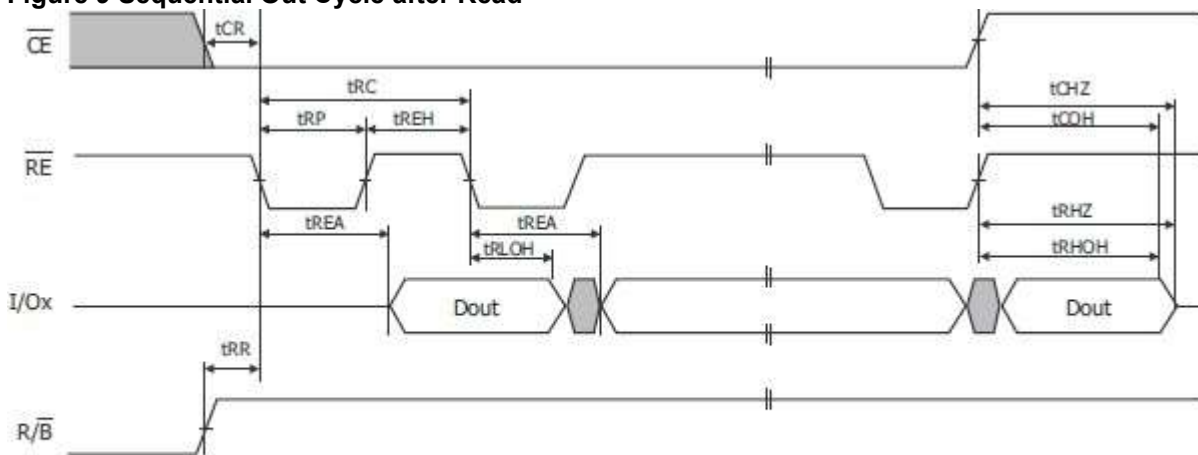


Figure 8 Sequential Out Cycle after Read (CLE=L, WE=H, ALE=L)



Notes: Transition is measured at +/-200mV from steady state voltage with load.
This parameter is sampled and not 100% tested. (t_{CHZ} , t_{RHZ})
 t_{RHOH} starts to be valid when frequency is lower than 33 MHz.
 t_{RLOH} is valid when frequency is higher than 33 MHz.

Figure 9 Sequential Out Cycle after Read



Notes: Transition is measured at +/-200mV from steady state voltage with load.
This parameter is sampled and not 100% tested. (t_{CHZ} , t_{RHZ})
 t_{RLOH} is valid when frequency is higher than 33MHz.
 t_{RHOH} starts to be valid when frequency is lower than 33MHz.

Figure 10 Status Read Cycle

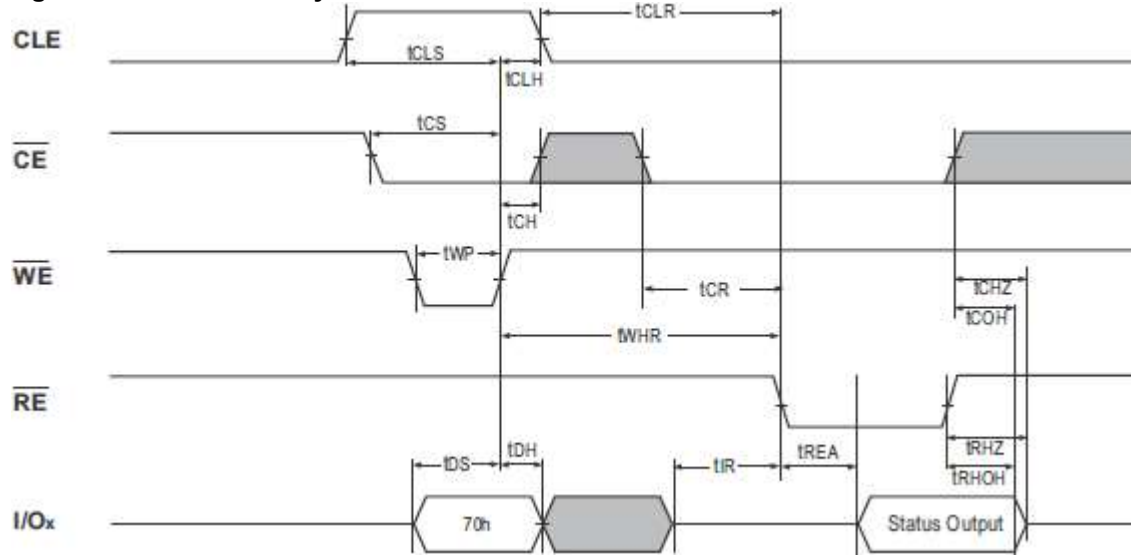


Figure 11 Read Operation (Read One Page)

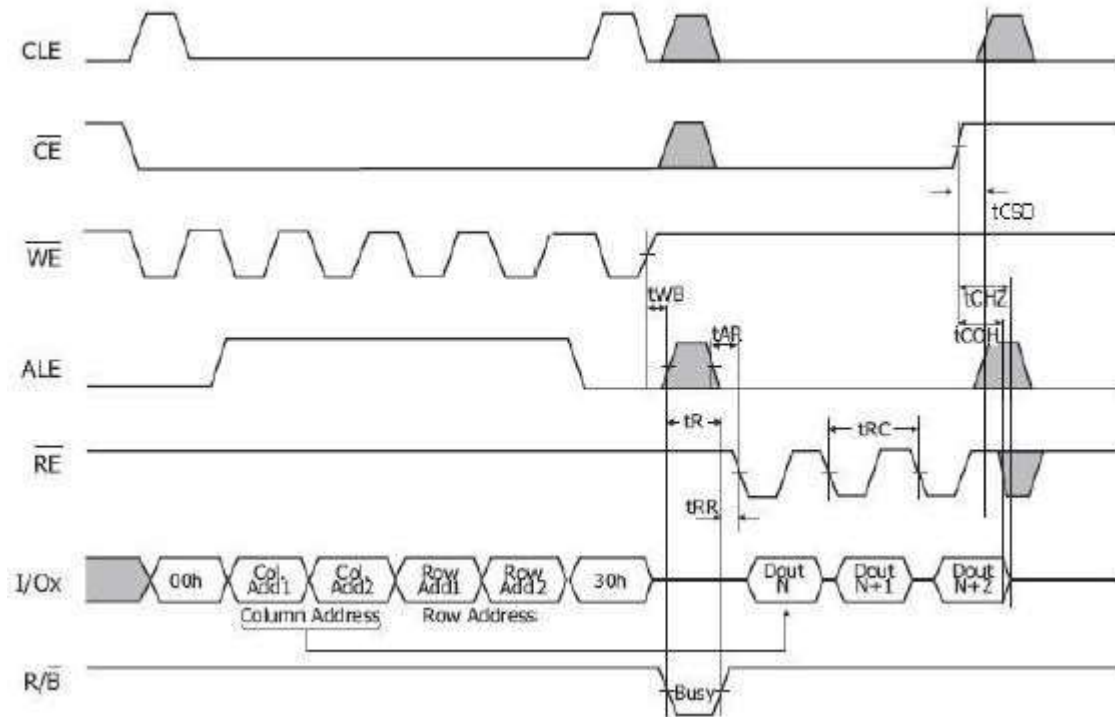


Figure 12 Read Operation (Intercepted by CE#)

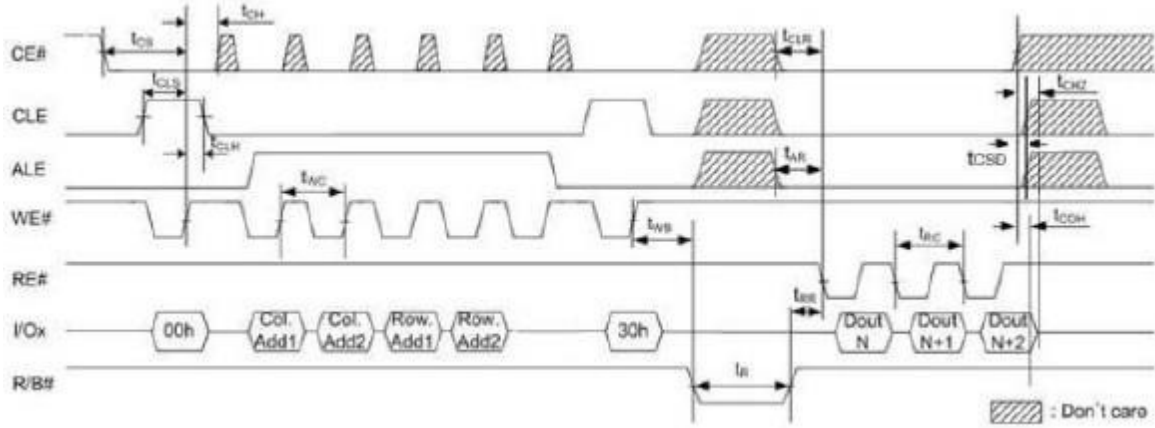


Figure 13 Random Data Output

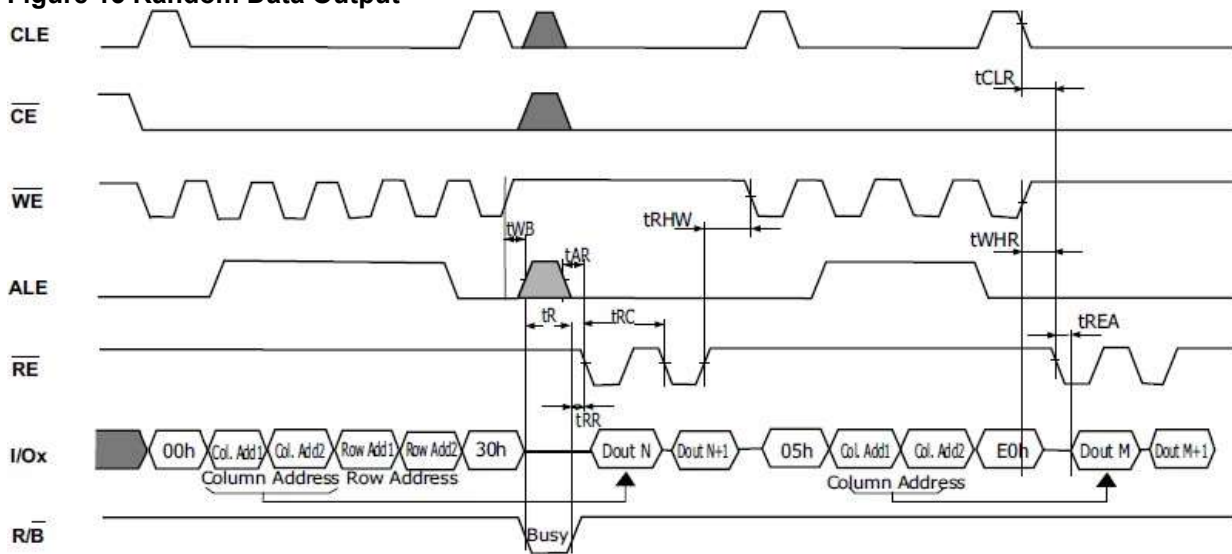


Figure 14 Page Program Operation

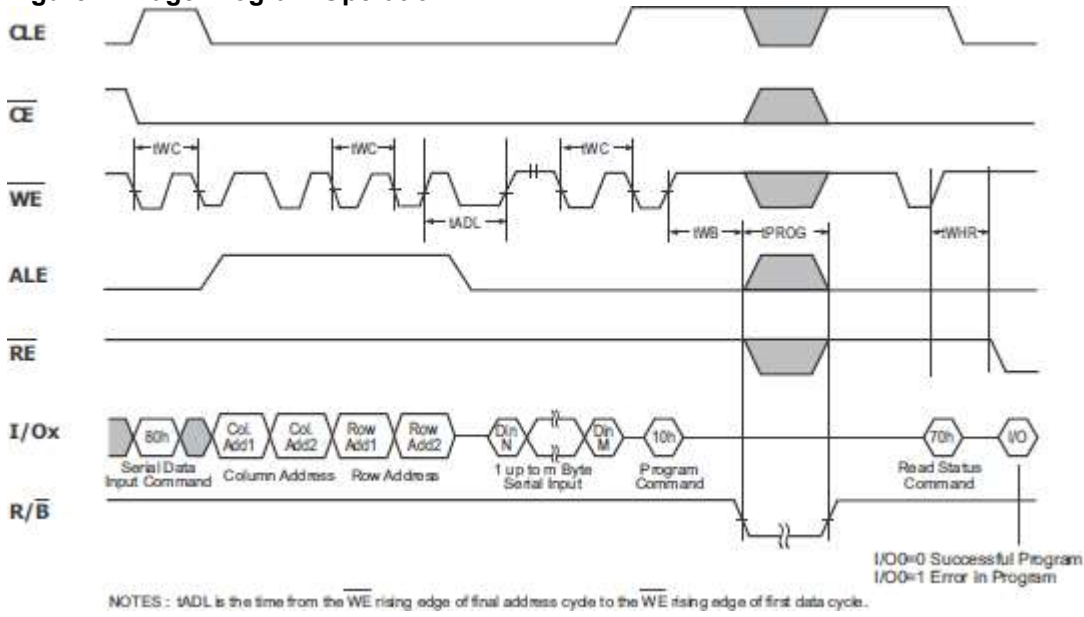


Figure 15 Random Data In

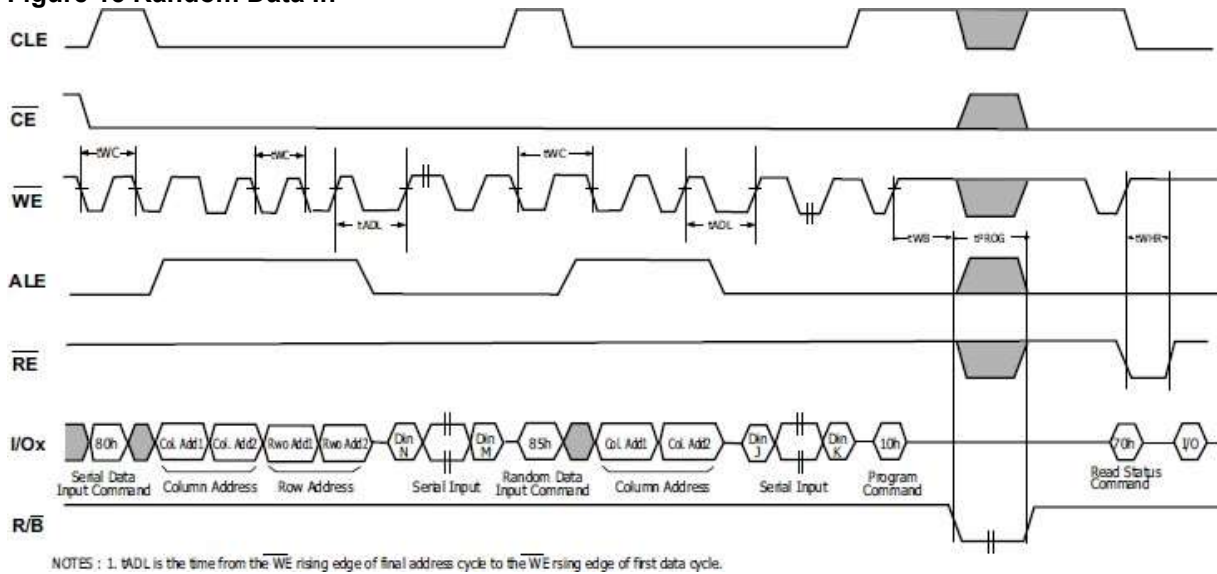


Figure 16 Copy Back Read with Optional Data Readout

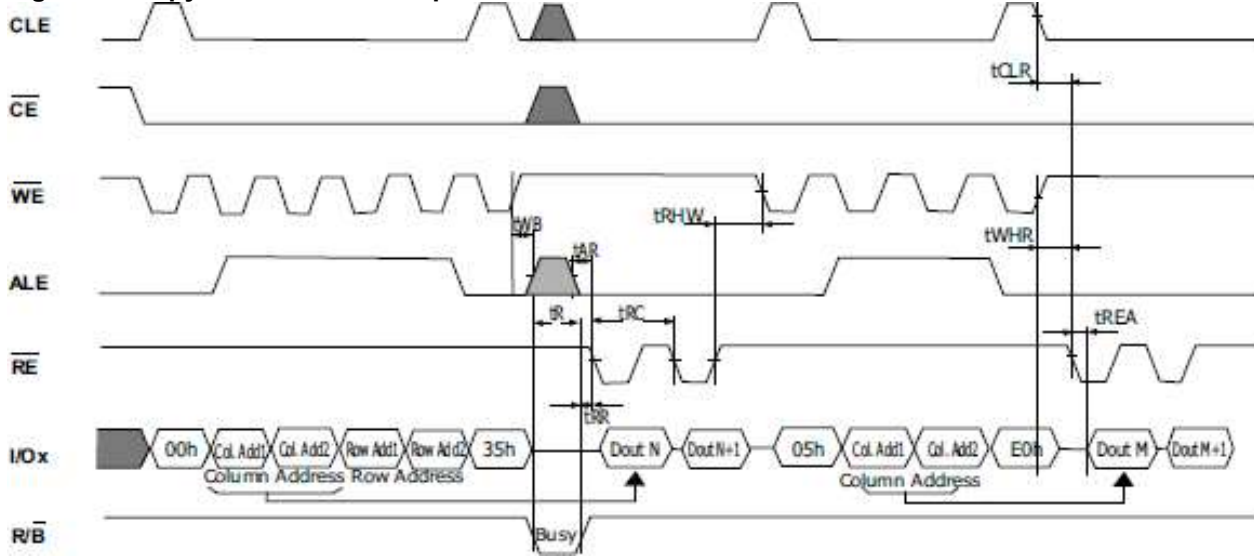
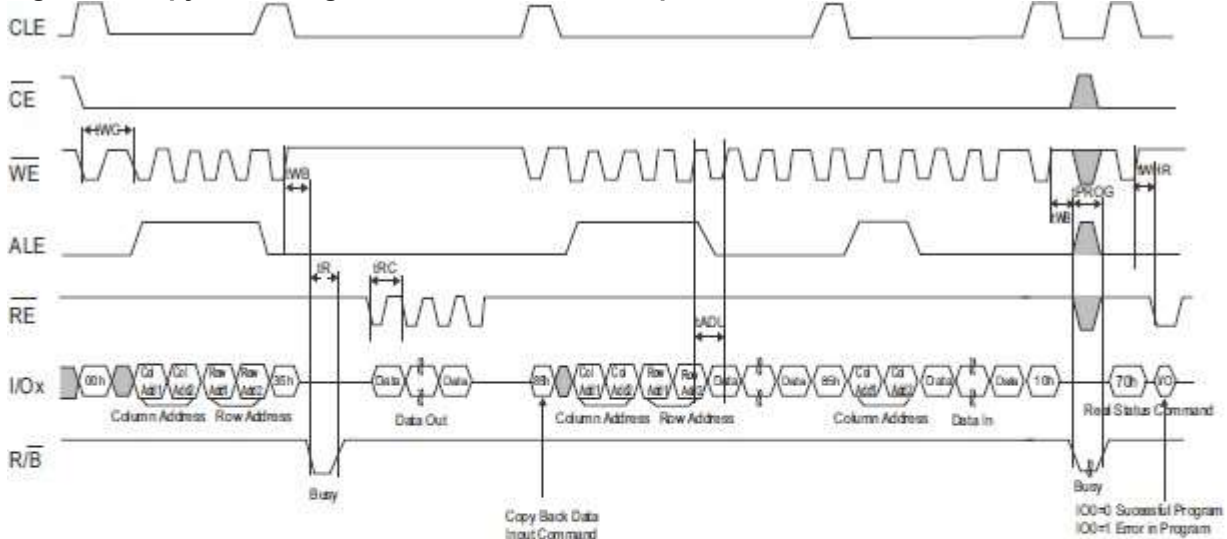


Figure 17 Copy Back Program with Random Data Input



NOTES: 1. tADL is the time from the WE rising edge of final address cycle to the WE rising edge of first data cycle.

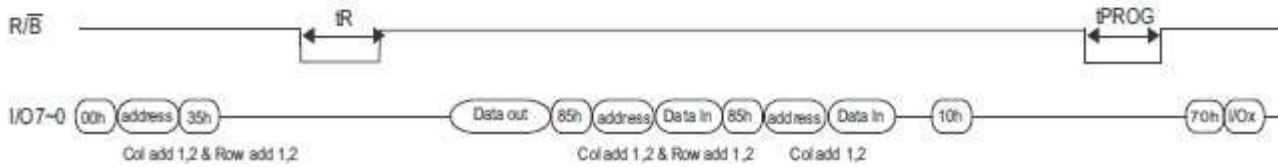


Figure 18 Block Erase Operation (Erase One Block)

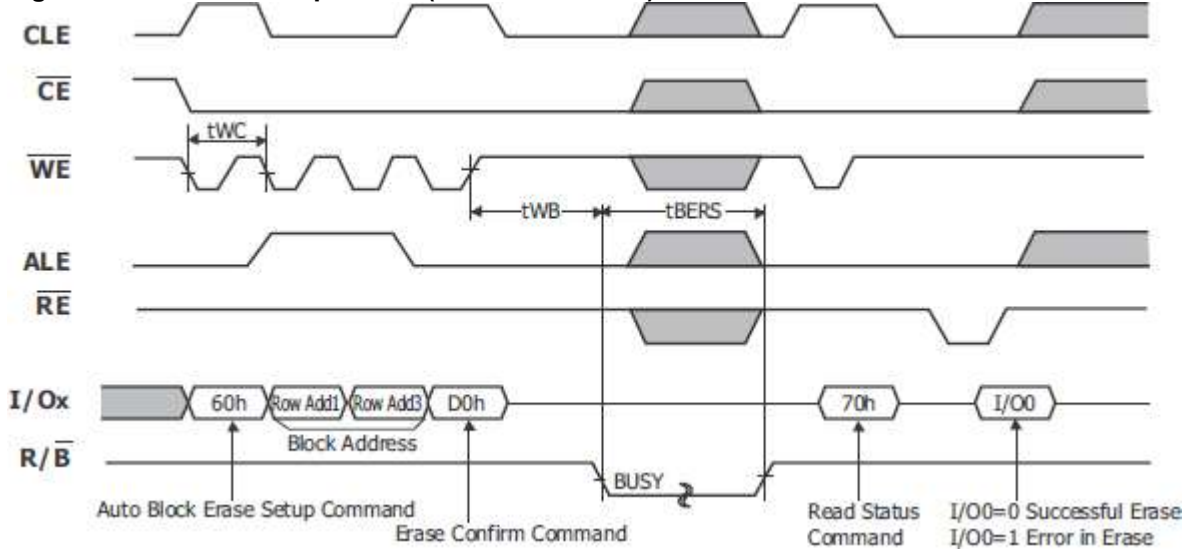


Figure 19 Reset Operation timing

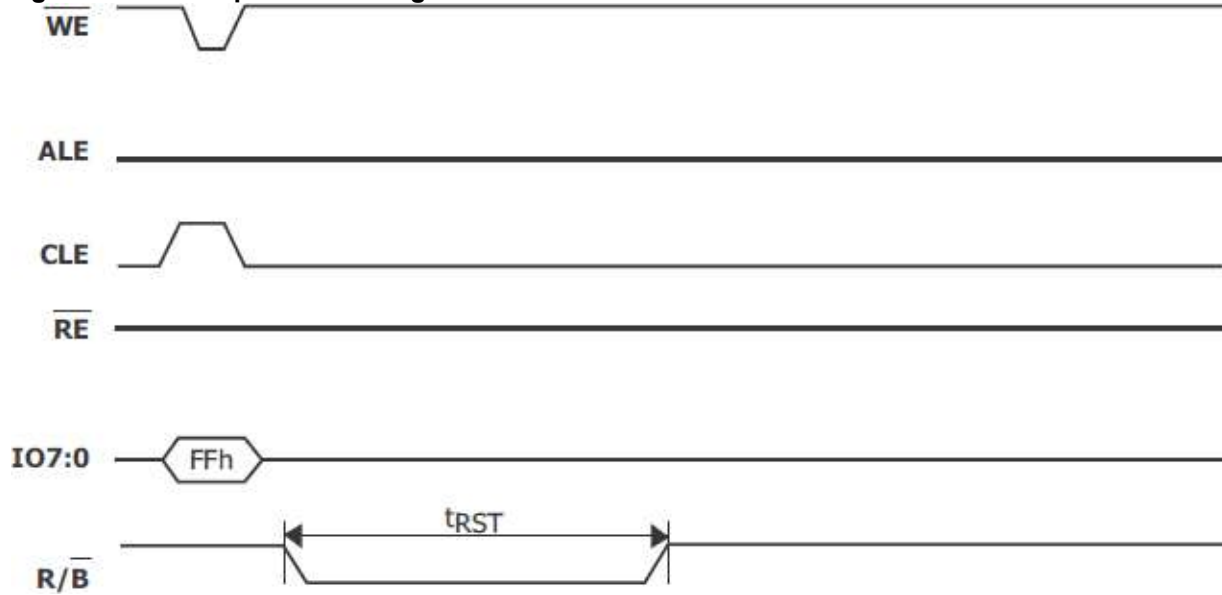


Figure 20 Read Operation with Read Cache

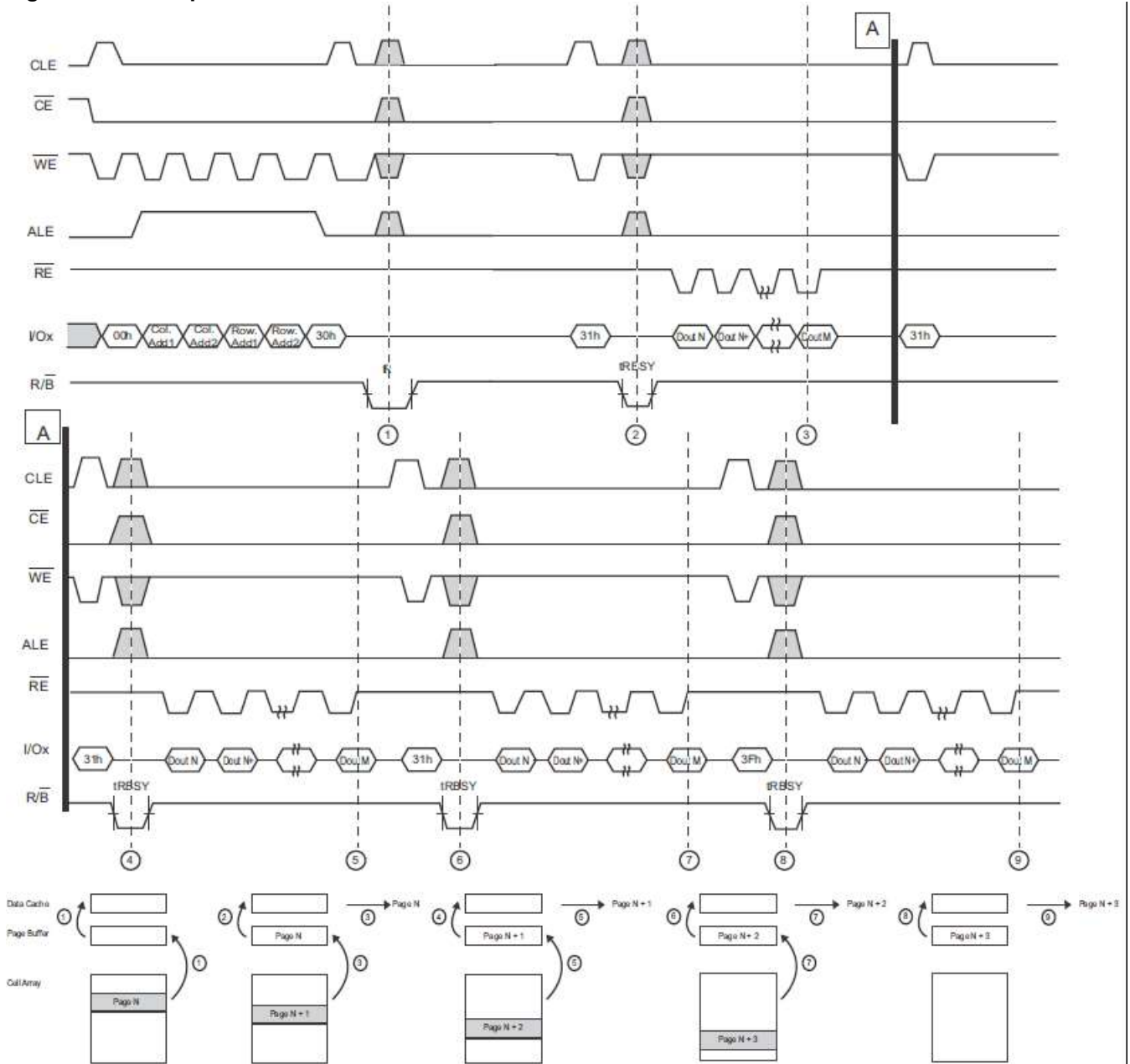


Figure 21 Read ID Operation

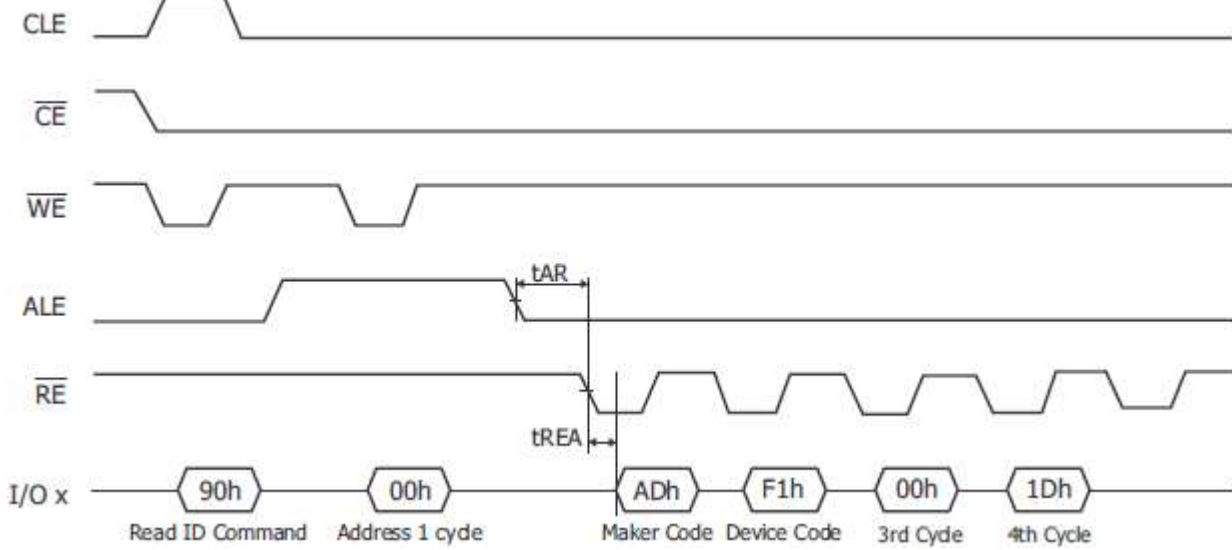


Figure 22 ONFI signature timing diagram

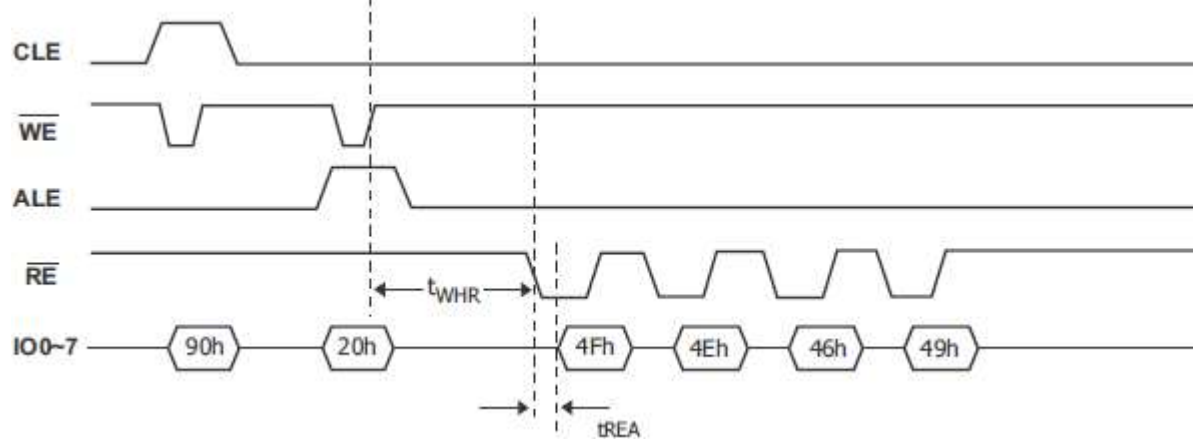


Figure 23 Read Parameter Page timings

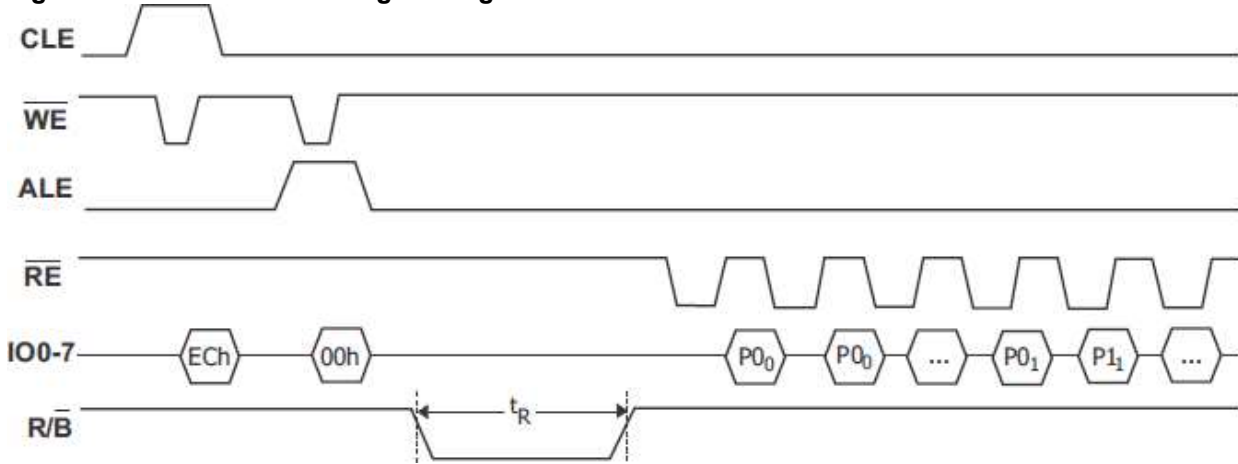


Figure 24 Power on and Data Protection timings

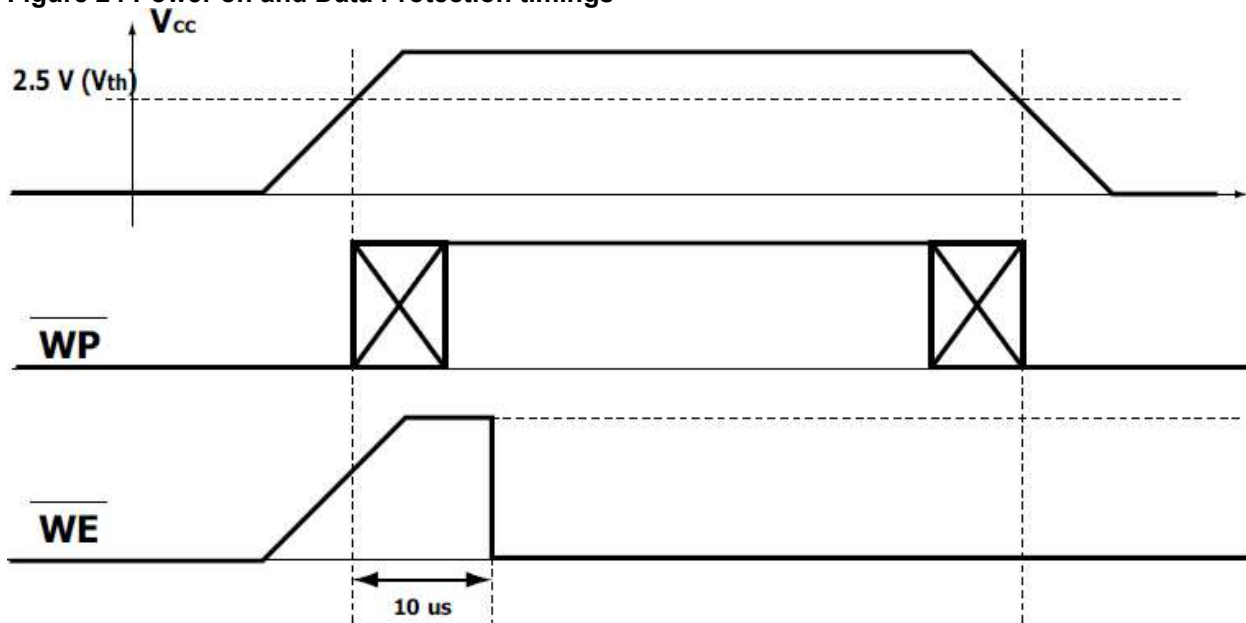


Figure 25 Ready/Busy Pin Electrical Specifications

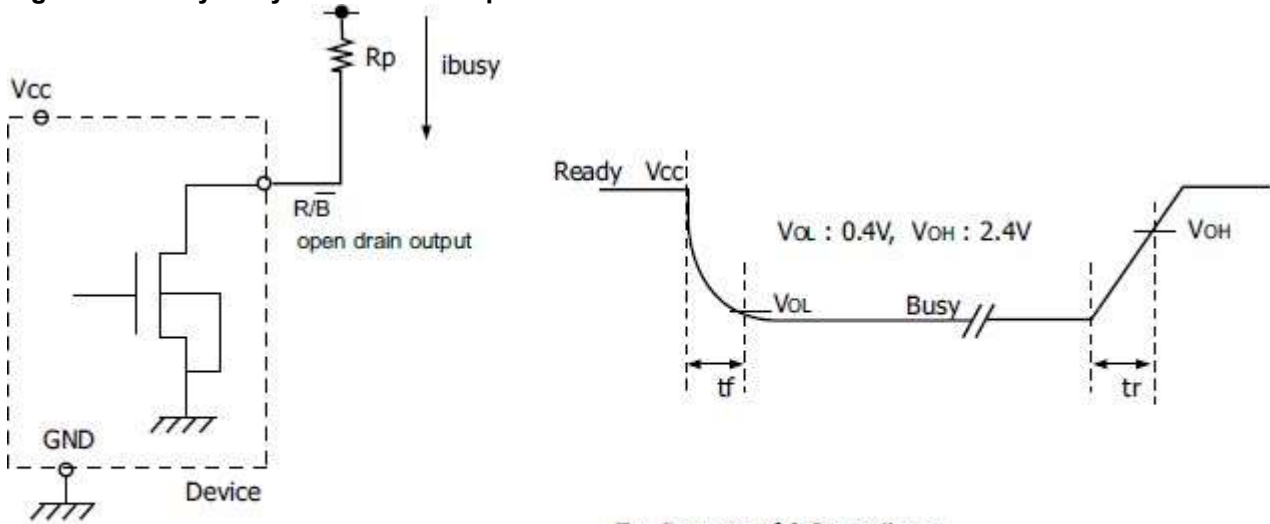
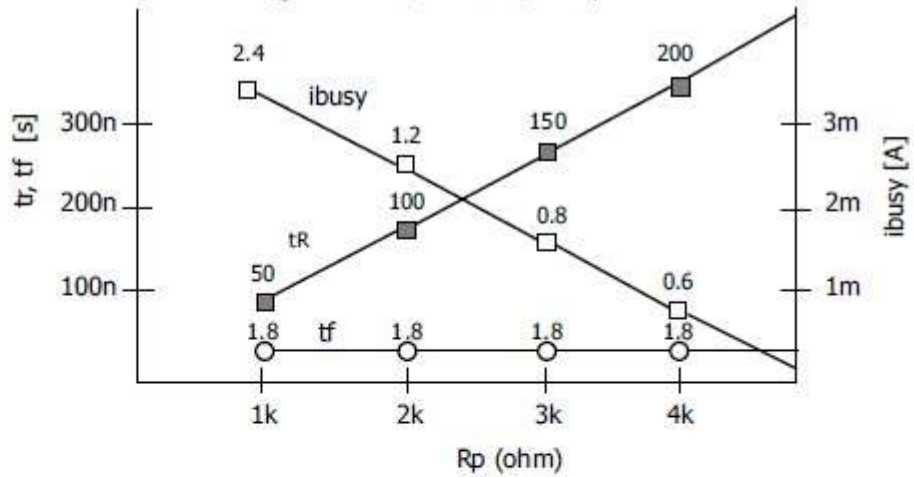


Fig. Rp vs tr, tf & Rp vs ibusy

@ Vcc = 3.3 V, Ta = 25°C, CL=50pF



Rp value guidance

$$R_p (\text{min}) = \frac{V_{cc} (\text{Max.}) - V_{oL} (\text{Max.})}{I_{oL} + \sum I_L} = \frac{3.2V}{8mA + \sum I_L}$$

where IL is the sum of the input currents of all devices tied to the R/B pin.

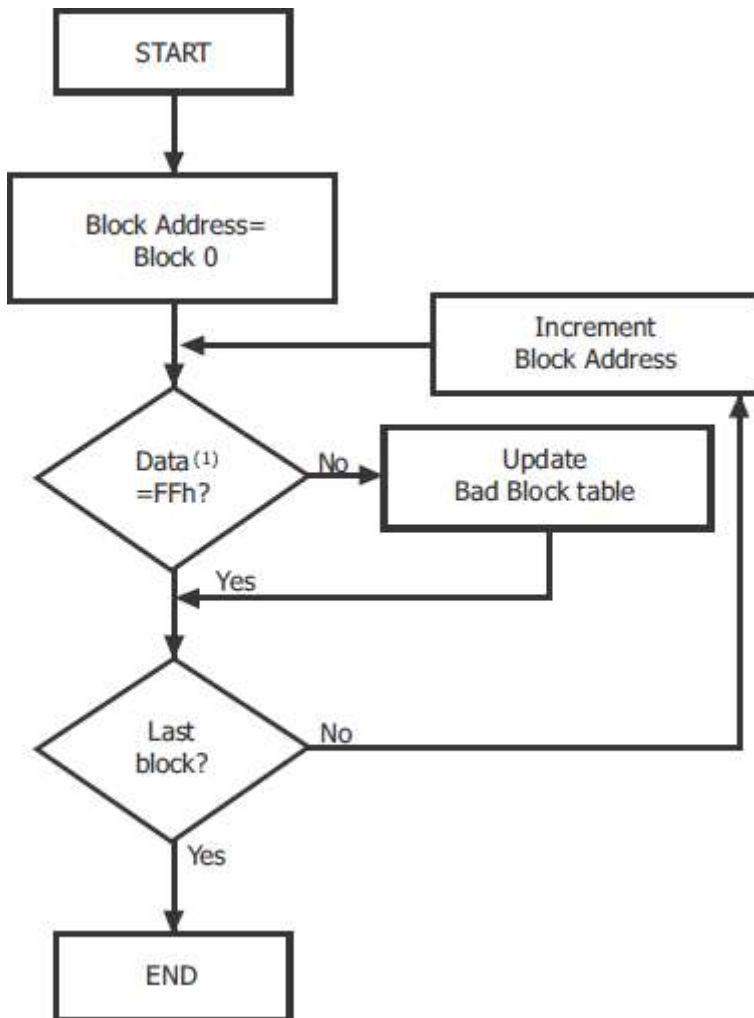
Rp(max) is determined by maximum permissible limit of tr

Bad Block Management

Devices with Bad Blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A Bad Block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor. The devices are supplied with all the locations inside valid blocks erased(FFh).

The Bad Block Information is written prior to shipping. Any block where the 1st Byte in the spare area of the 1st or 2nd th page (if the 1st page is Bad) does not contain FFh is a Bad Block. The Bad Block Information must be read before any erase is attempted as the Bad Block Information may be erased. For the system to be able to recognize the Bad Blocks based on the original information it is recommended to create a Bad Block table following the flowchart shown in Figure 26. The 1st block, which is placed on 00h block address is guaranteed to be a valid block.

Figure 26 Bad Block Management Flowchart



Note:

1. Make sure that either the 1st or 2nd page of every initial block has not FFh data at the column address of 2048.

Bad Block Replacement

Over the lifetime of the device additional Bad Blocks may develop. In this case the block has to be replaced by copying the data to a valid block. These additional Bad Blocks can be identified as attempts to program or erase them will give errors in the Status Register.

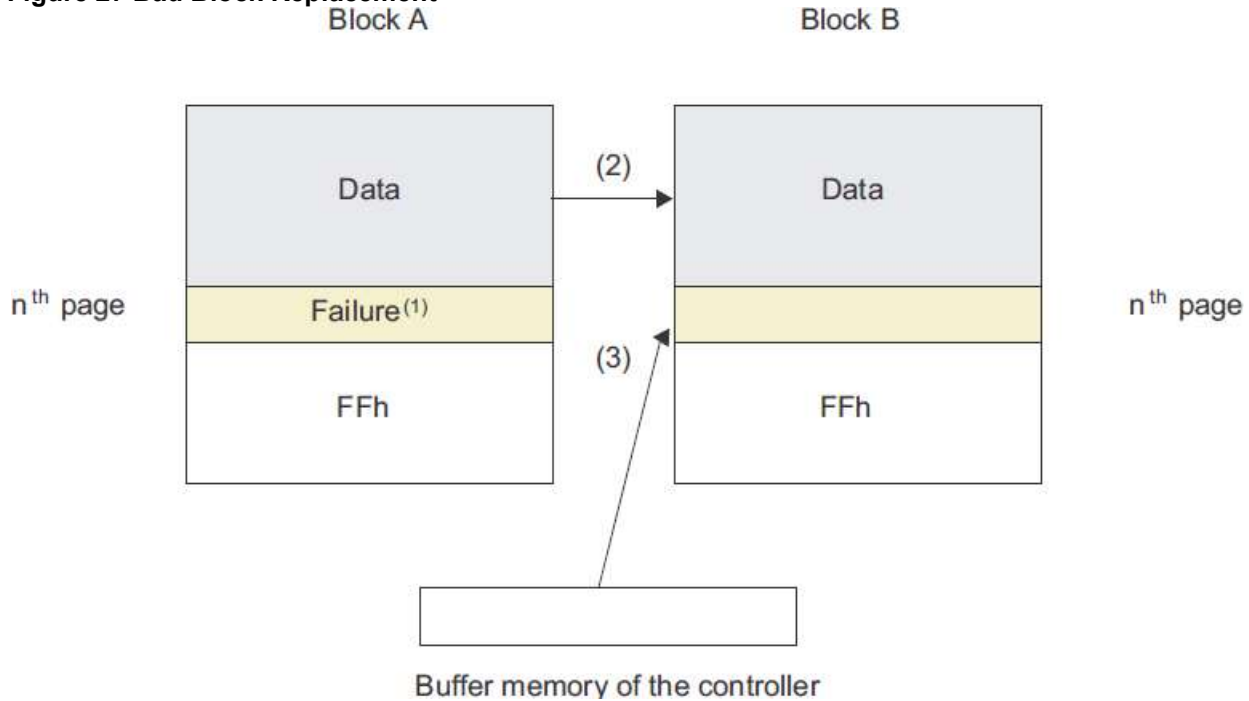
The failure of a page program operation does not affect the data in other pages in the same block, the block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block.

Refer to Table 15 and Figure 27 for the recommended procedure to follow if an error occurs during an operation.

Table 15 Block Failure

| Operation | Recommended Procedure |
|-----------|----------------------------|
| Erase | Block Replacement |
| Program | Block Replacement |
| Read | ECC (4bit / 512 + 16 byte) |

Figure 27 Bad Block Replacement



Notes:

1. An error occurs on the Block A during program or erase operation.
2. Data in Block A is copied to same location in Block B which is valid block.
3. Nth data of block A which is in controller buffer memory is copied into nth page of Block B.
4. Bad block table should be updated to prevent from erasing or programming Block A.

Write Protect Operation

The Erase and Program Operations are automatically reset when WP goes Low ($t_{WW} = 100\text{ns}$, min). The operations are enabled and disabled as follows (Figure 28~31)

Figure 28 Enable Programming

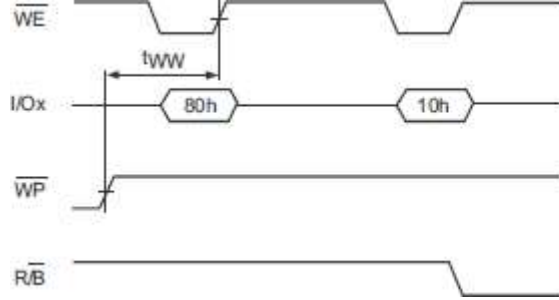


Figure 29 Disable Programming

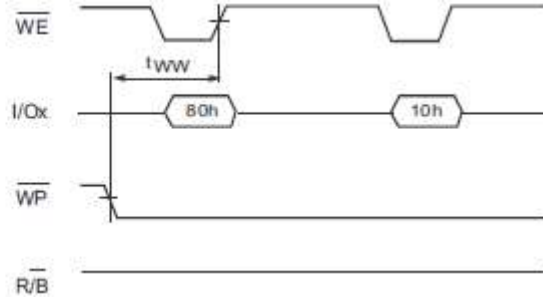


Figure 30 Enable Erasing

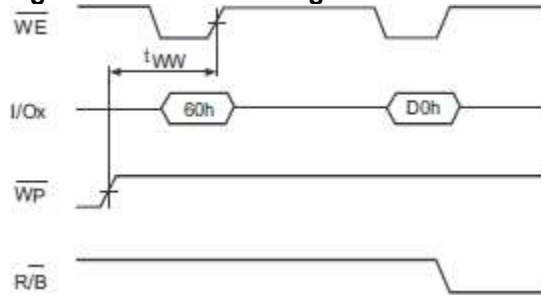
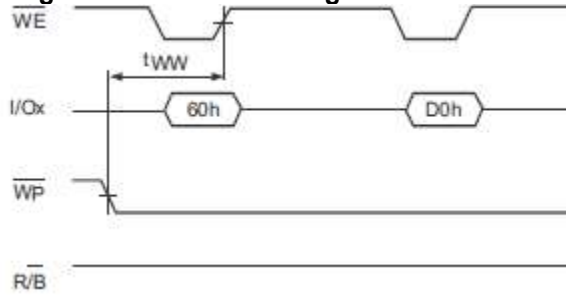
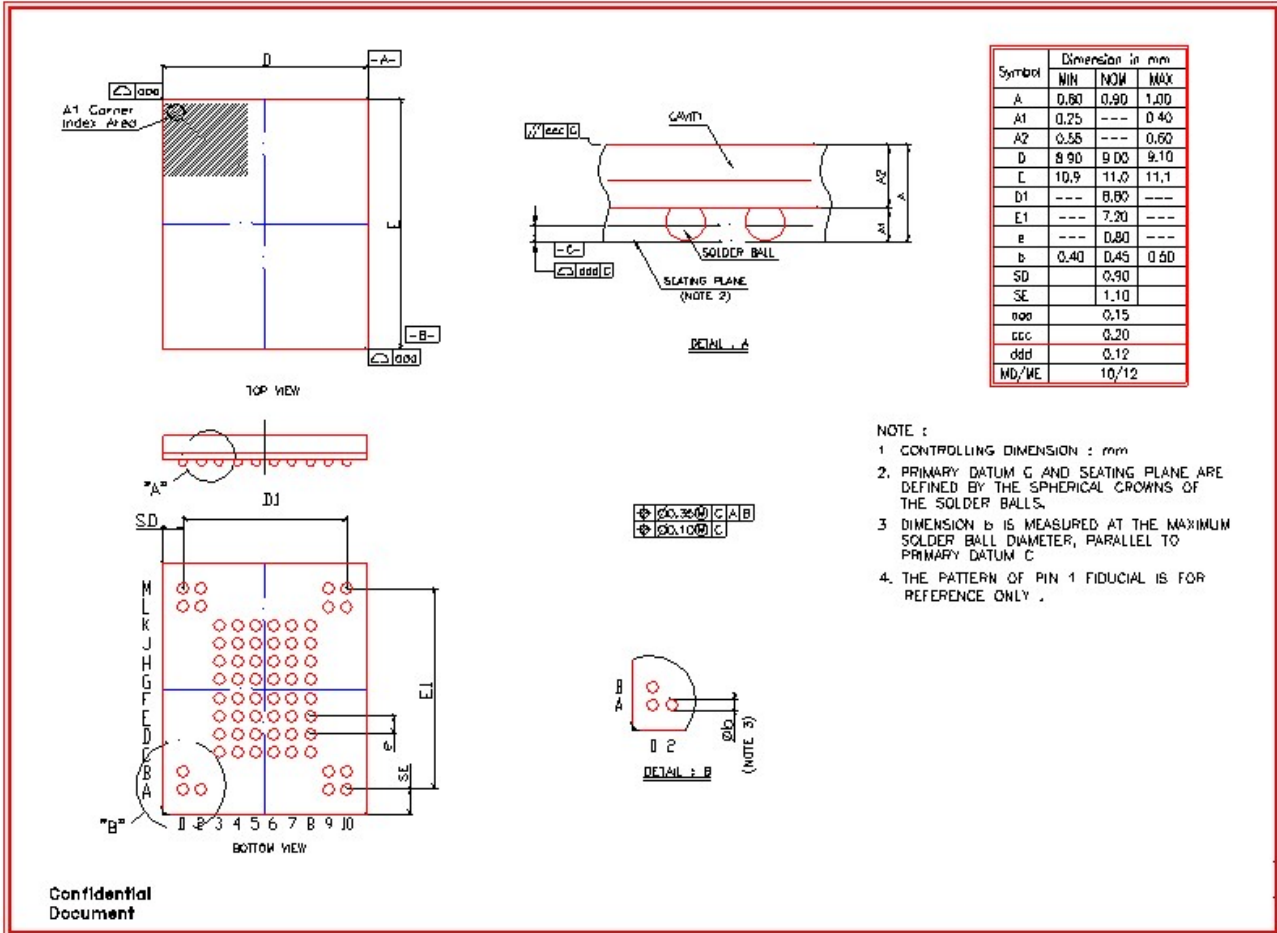


Figure 31 Disable Erasing



5 PACKAGE DIMENSION(FBGA 9 x 11 x 1.00mm, 63 Balls)



Confidential Document

XIN  CUN
[http//www.szxincun.com](http://www.szxincun.com)