DDR3L SDRAM 1Gbit Datesheet

XCCC64M16FP-EKNAB

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Using This Document

This document is intended for hardware and software engineer's general information on the XCCC64M16FP-EKNAB.Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

Revision History

Revision	Date	Description
Rev 1.0	2022/07/08	Create new document
Rev 1.1	2022/09/15	Change The temperature parameter
Rev 1.2	2023/05/20	Update logo

Document Index

1. INTRODUCTION

XCCC64M16FP-EKNAB is a 1G bits Double-Data-Rate-3L (DDR3L) DRAMs by advanced Package technology. XCCC64M16FP-EKNAB offers space saving advantage that could miniaturize your portable device, and it is conformed with Green regulations.

1.1 Application

- Compact DSC / CAR Black Box / Action Cam / 360 Cam
- Drone
- Wearable

1.2 Features

PRODUCT LIST

- XCCC64M16FP-EKNAB
  - DDR3L SDRAM: 1G bits (8Mx8-Bank x16-bit)

POWER SUPPLY

- DDR3(L) SDRAM
  - DDR3(L): 1.35V (1.283–1.45V) / Backward-compatible to DDR3: 1.5V ±0.075V

PACKAGE

- FBGA 7.5 x 13.5 x 1.2mm, 96 Balls
- Ball Pitch: 0.8mm
- Weight: TBD

Temperature

- Operating: 0 to +95°C
- Storage: -55 to +125°C

DDR3(L) SDRAM

- VDD=VDDQ=1.5V(1.425V~1.575V) VDD=VDDQ=1.35V(1.28V~1.45V), backward compatible to 1.5V applications.
- 8 banks
- 8n-bit prefetch architecture
- Fully differential clock inputs (CK,CK#) operation
- Bi-directional differential data strobe (DQS, DQS#)
- On chip DLL align DQ, DQS and DQS transition with CK transition
- DM masks write data-in at the both rising and falling edges of the data strobe
- All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock
- Programmable CAS latency 5, 6, 7, 8, 9, 10, 11, 12, 13 supported
- Programmable additive latency 0, CL-1, and CL-2 supported
- Programmable CAS Write latency (CWL) = 5, 6, 7, 8, 9, 10
- Programmable burst length 4/8 with both nibble sequential and interleave mode
- BL switch on the fly
- Average Refresh Cycle (Tcase)

  - 7.8 μs at 0°C ~ 85°C

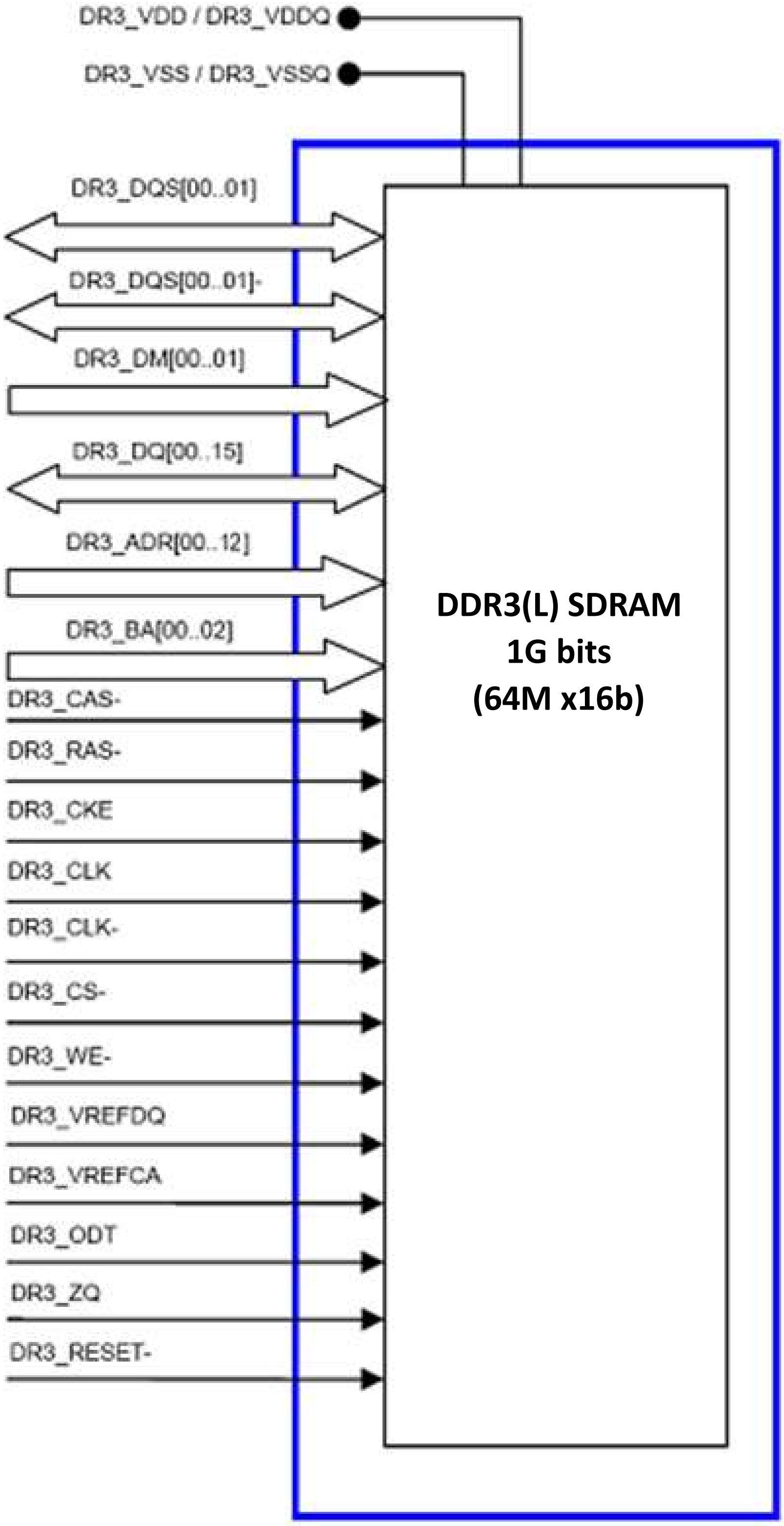
  - 3.9 μs at 85°C ~ 105°C
- Driver strength selected by MRS
- Dynamic On Die Termination
- Asynchronous RESET pin
- Internal (self) calibration: Internal self calibration through ZQ pin (RZQ: 240 ohm ± 1%)
- Write leveling
- Self refresh temperature (SRT)
- Automatic self refresh (ASR)
- Lead free & RoHS compliant
- JEDEC compliant

Speed	1066	1333	1600	1866	Unit
	7-7-7	9-9-9	11-11-11	13-13-13	
tCK(min)	1.875	1.5	1.25	1.071	ns
CAS Latency	7	9	11	13	nCK
tRCD(min)	13.125	13.5	13.75	13.91	ns
tRP(min)	13.125	13.5	13.75	13.91	ns
tRAS(min)	37.5	36	35	34	ns
tRC(min)	50.625	49.5	48.75	47.91	ns

Functionality described and the timing specifications included in this data sheet are for the DLL Enabled mode of operation.

2. FUNCTION DIAGRAM

2.1 DDR3(L)



3. PIN CONFIGURATION

3.1 Pin Assignment

	1	2	3	4	5	6	7	8	9
A	DR3_VDDQ	DR3_DQ13	DR3_DQ15				DR3_DQ12	DR3_VDDQ	DR3_VSS
B	DR3_VSSQ	DR3_VDD	DR3_VSS				DR3_DQS01-	DR3_DQ14	DR3_VSSQ
C	DR3_VDDQ	DR3_DQ11	DR3_DQ09				DR3_DQS01	DR3_DQ10	DR3_VDDQ
D	DR3_VSSQ	DR3_VDDQ	DR3_DM01				DR3_DQ08	DR3_VSSQ	DR3_VDD
E	DR3_VSS	DR3_VSSQ	DR3_DQ00				DR3_DM00	DR3_VSSQ	DR3_VDDQ
F	DR3_VDDQ	DR3_DQ02	DR3_DQS00				DR3_DQ01	DR3_DQ03	DR3_VSSQ
G	DR3_VSSQ	DR3_DQ06	DR3_DQS00-				DR3_VDD	DR3_VSS	DR3_VSSQ
H	DR3_VREFDQ	DR3_VDDQ	DR3_DQ04				DR3_DQ07	DR3_DQ05	DR3_VDDQ
J	NC	DR3_VSS	DR3_RAS-				DR3_CLK	DR3_VSS	NC
K	DR3_ODT00	DR3_VDD	DR3_CAS-				DR3_CLK-	DR3_VDD	DR3_CKE00
L	NC	DR3_CS00-	DR3_WE-				DR3_ADR10/AP	DR3_ZQ00	NC
M	DR3_VSS	DR3_BA00	DR3_BA02				NC/DR3_ADR15	DR3_VREFCA	DR3_VSS
N	DR3_VDD	DR3_ADR03	DR3_ADR00				DR3_ADR12	DR3_BA01	DR3_VDD
P	DR3_VSS	DR3_ADR05	DR3_ADR02				DR3_ADR01	DR3_ADR04	DR3_VSS
R	DR3_VDD	DR3_ADR07	DR3_ADR09				DR3_ADR11	DR3_ADR06	DR3_VDD
T	DR3_VSS	DR3_RESET-	NC/DR3_ADR13				NC/DR3_ADR14	DR3_ADR08	DR3_VSS

TOP VIEW

3.2 Pin Descriptions

Type Symbol	Description	Type Symbol	Description
I	Input	P	Power
O	Output	G	Ground
I/O	Bi-direction	X	No connect (No function, don't care)

Symbol	Type	Count	Description
DR3_ADR[00..12] (A0~A12)	I	13	**Address inputs:** Provide the row address for ACTIVATE commands, and the columnaddress and auto precharge bit (A10) for READ/WRITE commands, to select onelocation out of the memory array in the respective bank. A10 sampled during aPRECHARGE command determines whether the PRECHARGE applies to one bank (A10LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to V_{REFCA}. A12/BC#: When enabled in the mode register (MR), A12 is sampled during READand WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH = BL8 or no burst chop, LOW = BC4).
DR3_BA[00..02] (BA0~BA2 or BA[2:0])	I	3	**Bank address inputs:** BA[2:0] define the bank to which an ACTIVATE, READ, WRITE,or PRECHARGE command is being applied. BA[2:0] define which moderegister (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. BA[2:0]are referenced to V_{REFCA}.
DR3_RESET- (/ RESET、RESET# or $\overline{\text{RESET}}$)	I	1	**Reset:** RESET# is an active LOW CMOS input referenced to V_{SS}. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 × V_{DD} and DC LOW ≤ 0.2 × V_{DDQ}. RESET# assertion and deassertion are asynchronous.
DR3_DQ[00..15] (DQ0~DQ15)	I/O	16	**Data Inputs/Output:** Bi-directional data bus, Referenced to V_{REFDQ}.
DR3_RAS-, DR3_CAS-, DR3_WE- (RAS#、$\overline{\text{RAS}}$, CAS#,、$\overline{\text{CAS}}$, WE#、$\overline{\text{WE}}$)	I	3	**Command inputs:** RAS#, CAS#, and WE# (along with CS#) define the commandbeing entered and are referenced to V_{REFCA}.
DR3_CKE (CKE)	I	1	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) internalcircuitry and clocks on the DRAM. The specific circuitry that is enabled/disabled is dependent upon the DDR3(L) SDRAM configuration and operating mode. Taking CKE LOWprovides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle),oractive power-down (row active in any bank). CKE is synchronous forpower-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, RESET#, and ODT) are disabled during POWER-DOWN. Input buffers (excluding CKE and RESET#) are disabled during SELF REFRESH. CKE is referenced to V_{REFCA}.

Symbol	Type	Count	Description
DR3_CLK, DR3_CLK- (CK,CK#、CK,$\overline{CK}$)	I	2	**Clock:** CK and CK# are differential clock inputs. All control and address input signalsare sampled on the crossing of the positive edge of CK and the negative edge of CK#.Output data strobe (DQS, DQS#) is referenced to the crossings of CK and CK#.
DR3_CS- (CS#、$\overline{CS}$)	I	1	**Chip select:** CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS#provides for external rank selection on systems with multiple ranks. CS# is considered part of the command code. CS# is referenced to V_{REFCA}.
DR3_ODT (ODT)	I	1	**On-die termination:** ODT enables (registered HIGH) and disables (registered LOW)termination resistance internal to the DDR3(L) SDRAM. When enabled in normaloperation, ODT is only applied to each of the following balls: DQ[7:0], DQS, DQS#,and DM for the x8; DQ[3:0], DQS, DQS#, and DM for the x4. The ODT input isignored if disabled via the LOAD MODE command. ODT is referenced to V_{REFCA}.
DR3_DQS00 (LDQS、DQSL), DR3_DQS00- (/LDQS or DQSL# or $\overline{DQSL}$) DR3_DQS01 (UDQS or DQSU), DR3_DQS01- (/UDQS or DQSU# or $\overline{DQSU}$) (DQS,DQS#)	I/O	4	**Lower byte data strobe:** Output with read data. Edge-aligned with read data. Inputwith write data. Center-aligned to write data. **Upper byte data strobe:** Output with read data. Edge-aligned with read data. Inputwith write data. DQS is center-aligned to write data.
DR3_DM00 (LDM or DML) DR3_DM01 (UDM or DMU)	I	2	**Input data mask:** DM is an input mask signal for write data. Input data is maskedwhen DM is sampled HIGH along with the input data during a write access.Although the DM ball is input-only, the DM loading is designed to match that of theDQ and DQS balls. DM is referenced to V_{REFDQ}.
DR3_VREFCA (VREFCA)	P	1	Reference voltage for control, command, and address: VREFCA must be maintained at all times (including self refresh) for proper device operation.
DR3_VREFDQ (VREFDQ)	P	1	Reference voltage for data: VREFDQ must be maintained at all times (excluding selfrefresh) for proper device operation.
DR3_ZQ (ZQ)	P	1	External reference ball for output drive calibration: This ball is tied to external240Ω resistor RZQ, which is tied to VSSQ.
DR3_VDD (VDD)	P	9	Power Supply:1.35V (1.28V–1.45V) / Backward-compatible to 1.5V ±0.075V
DR3_VDDQ (VDDQ)	P	9	DQ Power Supply: 1.35V (1.28V–1.45V) / Backward-compatible to 1.5V ±0.075V
DR3_VSS (VSS)	G	12	Ground
DR3_VSSQ (VSSQ)	G	9	DQ Ground
NC	X	5	Not Connect Pin (Don't Care)

4. DDR3(L) SDRAM SPECIFICATION

4.1 Descriptions

The 1Gb Double-Data-Rate-3 (DDR3(L)) DRAM is a high-speed CMOS SDRAM. It is internally configured as an octal-bank DRAM.

The 1Gb chip is organized as 16Mbit x 8 I/O x 8 banks and 8Mbit x16 I/O x 8 banks. These synchronous devices achieve high speed double-data-rate transfer rates of up to 2133 Mb/sec/pin for general applications.

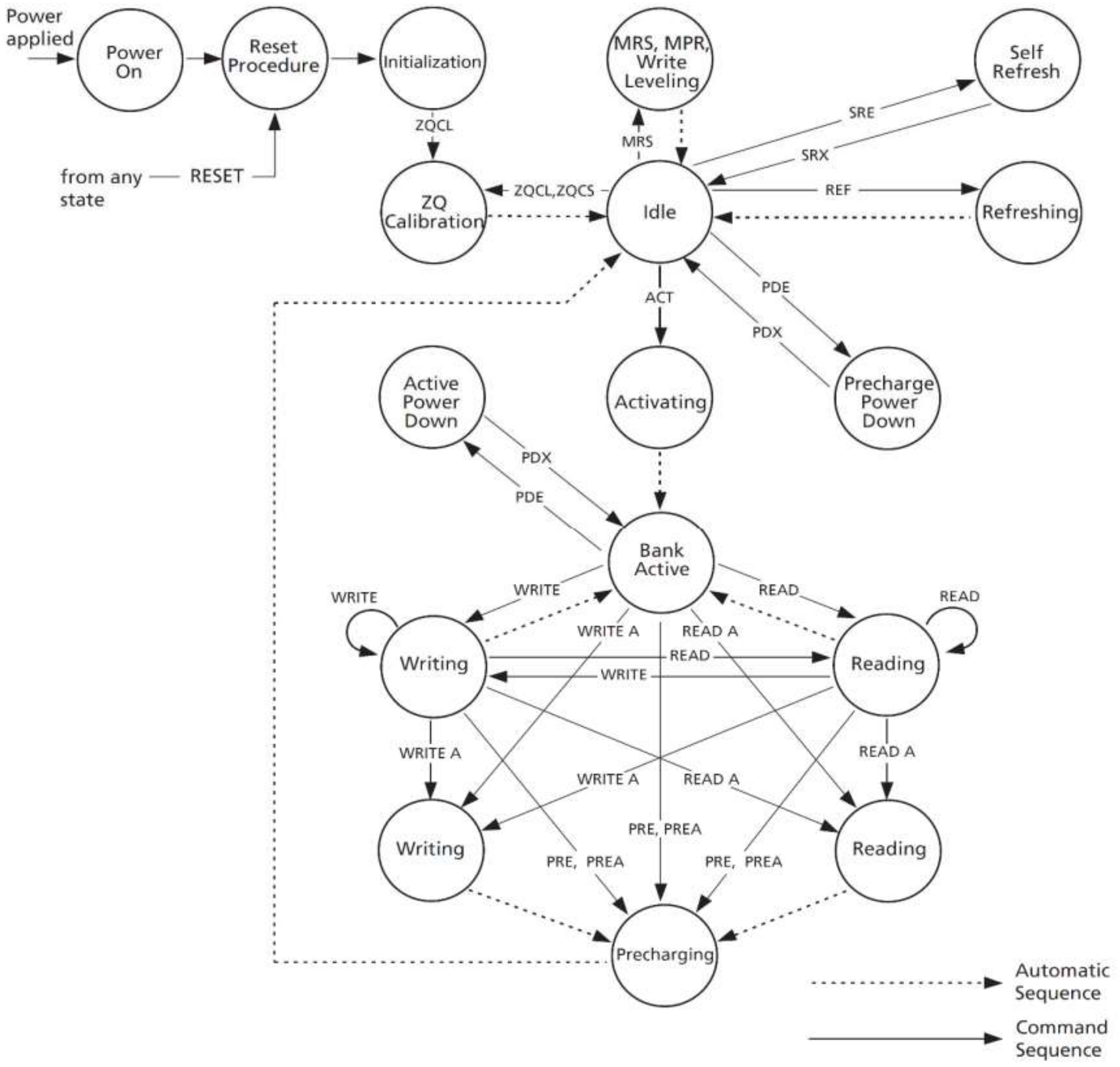
The chip is designed to comply with all key DDR3(L) DRAM key features and all of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CK rising and CK# falling). All I/Os are synchronized with a single ended DQS or differential DQS pair in a source synchronous fashion.

These devices operate with a single 1.5V ± 0.075V or 1.35V -0.067V/+0.1V power supply and are available in BGA packages.

Addressing

Configuration	64Mb x 16
Number of Bank	8
Bank address	BA0-BA2
Autoprecharge	A10/AP
Row address	A0-A12
Column address	A0-A9
BC switch on the fly	A12/BC#
Page Size	2KB
tREFI	Tc≦ 85°C:7.8µs, Tc>85°C:3.9µs
tRFC	110ns

4.2 State Diagram



State Diagram Command Definitions

Abbreviation	Function	Abbreviation	Function	Abbreviation	Function
ACT	Active	Read	RD, RDS4, RDS8	PED	Enter Power-down
PRE	Precharge	Read A	RDA, RDAS4, RDAS8	PDX	Exit Power-down
PREA	Precharge All	Write	WR, WRS4, WRS8	SRE	Self-Refresh entry
MRS	Mode Register Set	Write A	WRA, WRAS4, WRAS8	SRX	Self-Refresh exit
REF	Refresh	RESET#	Start RESET Procedure	MPR	Multi-Purpose Register
ZQCL	ZQ Calibration Long	ZQCS	ZQ Calibration Short	-	-

4.3 Basic Functionality

The DDR3(L) SDRAM is a high-speed dynamic random access memory internally configured as an eight-bank DRAM.

The DDR3(L) SDRAM uses an 8n prefetch architecture to achieve high speed operation. The 8n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR3(L) SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and two corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write operation to the DDR3(L) SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in a programmed sequence. Operation begins with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be activated. The address bit registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register.

Prior to normal operation, the DDR3(L) SDRAM must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions and device operation.

4.4 RESET and Initialization Procedure

Power-up Initialization sequence

The Following sequence is required for POWER UP and initialization

1. Apply power (RESET# is recommended to be maintained below 0.2 x VDD, all other inputs may be undefined). RESET# needs to be maintained for minimum 200µs with stable power. CKE is pulled"Low"anytime before RESET# being de-asserted (min. time 10ns). The power voltage ramp time between 300mV to VDDmin must be no greater than 200ms; and during the ramp, VDD>VDDQ and (VDD-VDDQ) <0.3 Volts.

- VDD and VDDQ are driven from a single power converter output, AND
- The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side. In addition, VTT is limited to 0.95V max once power ramp is finished, AND
- Vref tracks VDDQ/2.

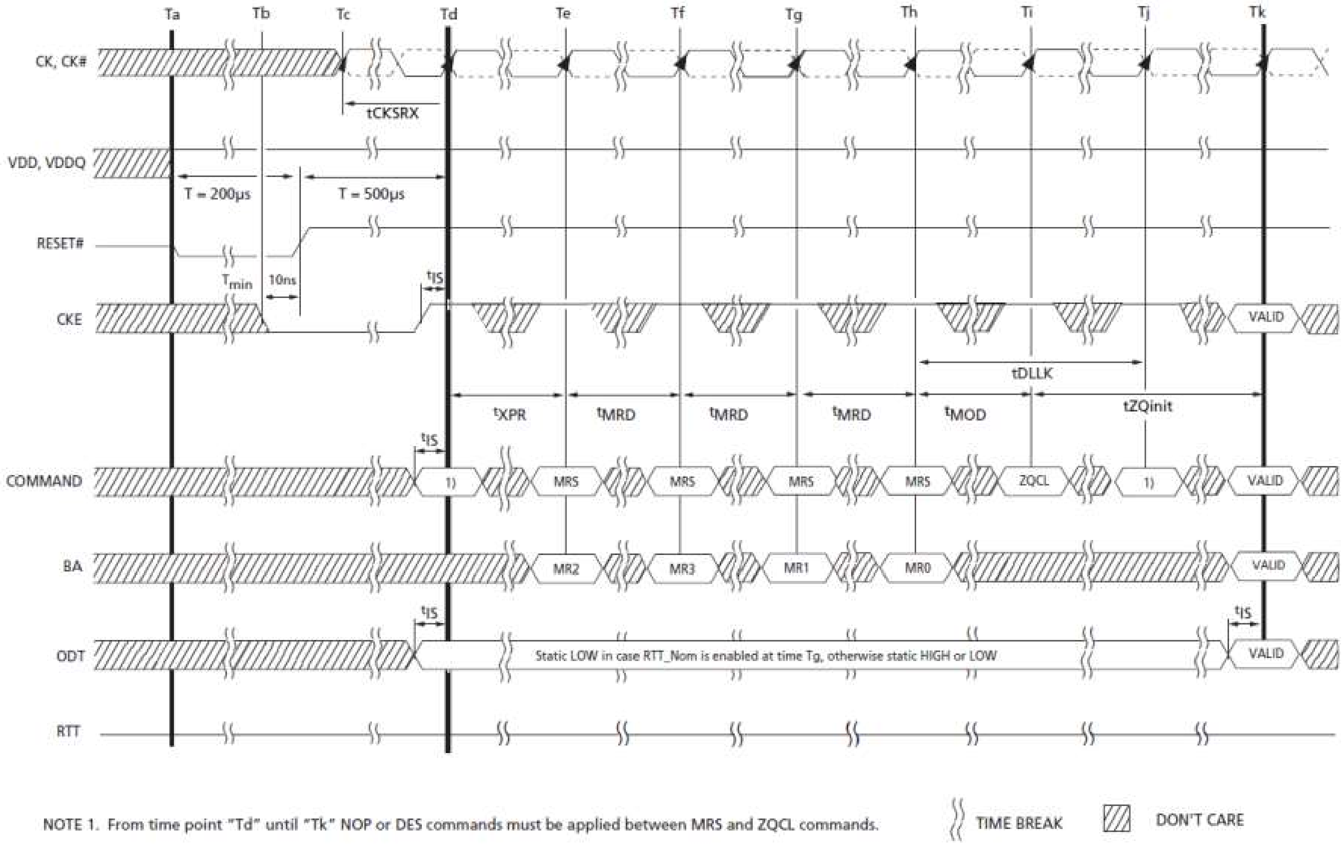
OR

- Apply VDD without any slope reversal before or at the same time as VDDQ.
- Apply VDDQ without any slope reversal before or at the same time as VTT & Vref.
- The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.

2. After RESET# is de-asserted, wait for another 500us until CKE become active. During this time, the DRAM will start internal state initialization; this will be done independently of external clocks.
3. Clock (CK, CK#) need to be started and stabilized for at least 10ns or 5tCK (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding set up time to clock (tIS) must be meeting. Also a NOP or Deselect command must be registered (with tIS set up time to clock) before CKE goes active. Once the CKE registered "High" after Reset, CKE needs to be continuously registered "High"until the initialization sequence is finished, including expiration of tDLLK and tZQinit.
4. The DDR3 DRAM will keep its on-die termination in high impedance state as long as RESET# is asserted. Further, the DRAM keeps its on-die termination in high impedance state after RESET# de-assertion until CKE is registered HIGH. The ODT input signal may be in undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT_NOM is to be enabled in MR1, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of tDLLK and tZQinit.
5. After CKE being registered high, wait minimum of Reset CKE Exit time, tXPR, before issuing the first MRS command to load mode register. [tXPR=max (tXS, 5tCK)].
6. Issue MRS command to load MR2 with all application settings. (To issue MRS command for MR2, provide "Low" to BA0 and BA2, "High" to BA1).
7. Issue MRS command to load MR3 with all application settings. (To issue MRS command for MR3, provide "Low" to BA2, "High" to BA0 and BA1).

8. Issue MRS command to load MR1 with all application settings and DLL enabled. (To issue "DLL Enable" command, provide "Low" to A0, "High" to BA0 and "Low" to BA1 and BA2).
9. Issue MRS Command to load MR0 with all application settings and "DLL reset". (To issue DLL reset command, provide "High" to A8 and "Low" to BA0-BA2).
10. Issue ZQCL command to starting ZQ calibration.
11. Wait for both tDLLK and tZQinit completed.
12. The DDR3(L) SDRAM is now ready for normal operation.

Reset and Initialization Sequence at Power- on Ramping



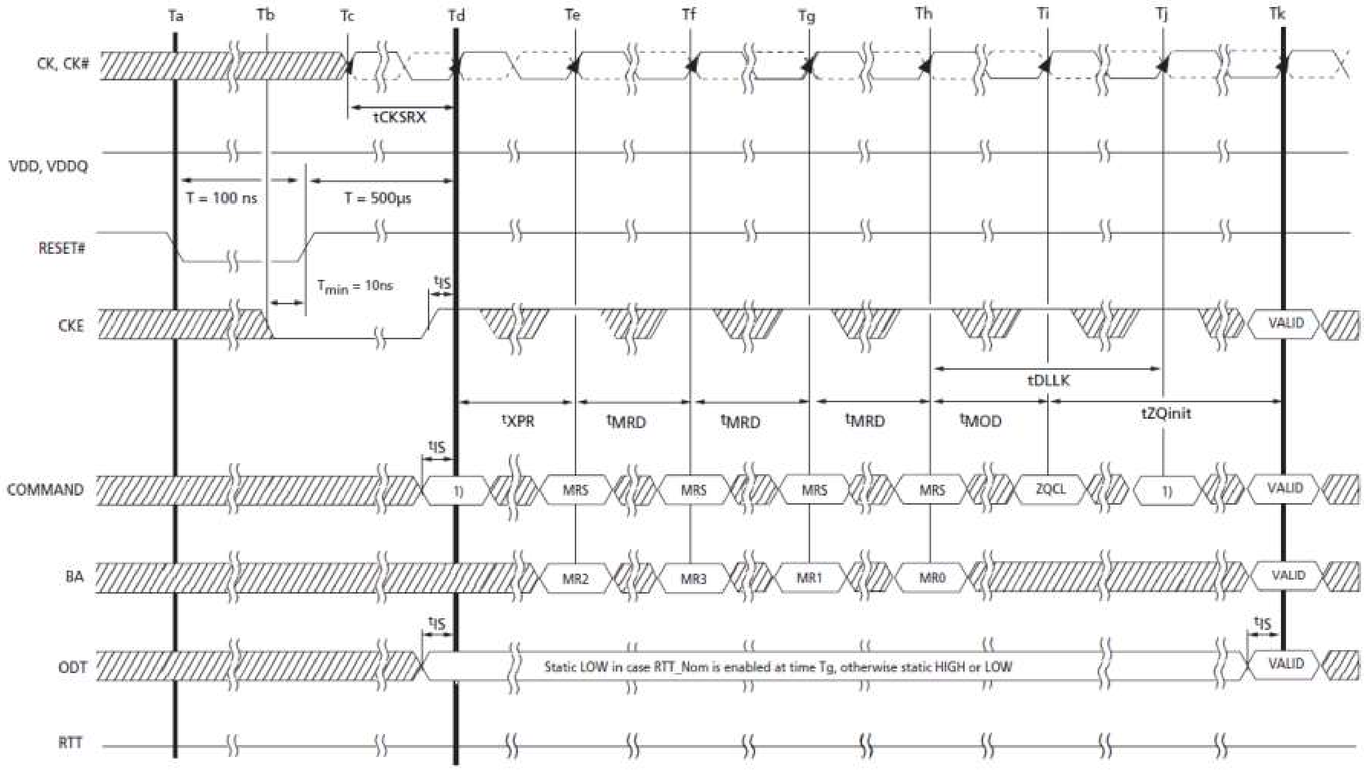
NOTE 1. From time point "Td" until "Tk" NOP or DES commands must be applied between MRS and ZQCL commands.

Reset Procedure at Stable Power

The following sequence is required for RESET at no power interruption initialization.

1. Asserted RESET below 0.2*VDD anytime when reset is needed (all other inputs may be undefined). RESET needs to be maintained for minimum 100ns. CKE is pulled “Low” before RESET being de-asserted (min. time 10ns).
2. Follow Power-up Initialization Sequence step 2 to 11.
3. The Reset sequence is now completed. DDR3 SDRAM is ready for normal operation.

Reset Procedure at Power Stable Condition

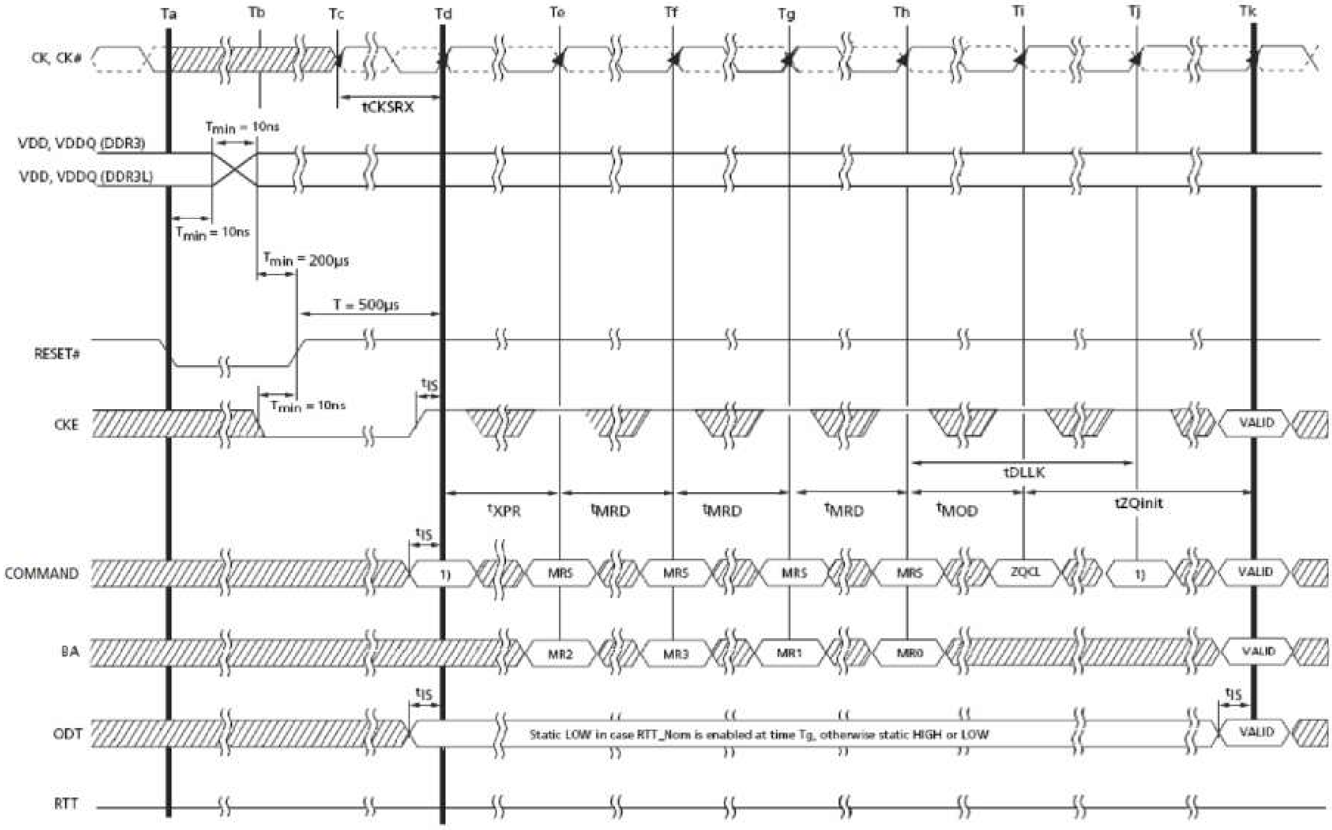


NOTE 1. From time point “Td” until “Tk” NOP or DES commands must be applied between MRS and ZQCL commands.

TIME BREAK

▨ DON'T CARE

VDDQ/VDDQ Voltage Switch Between DDR3L and DDR3



NOTE 1. From time point "Td" until "Tk" NOP or DES commands must be applied between MRS and ZQCL commands.

TIME BREAK ▨ DON'T CARE

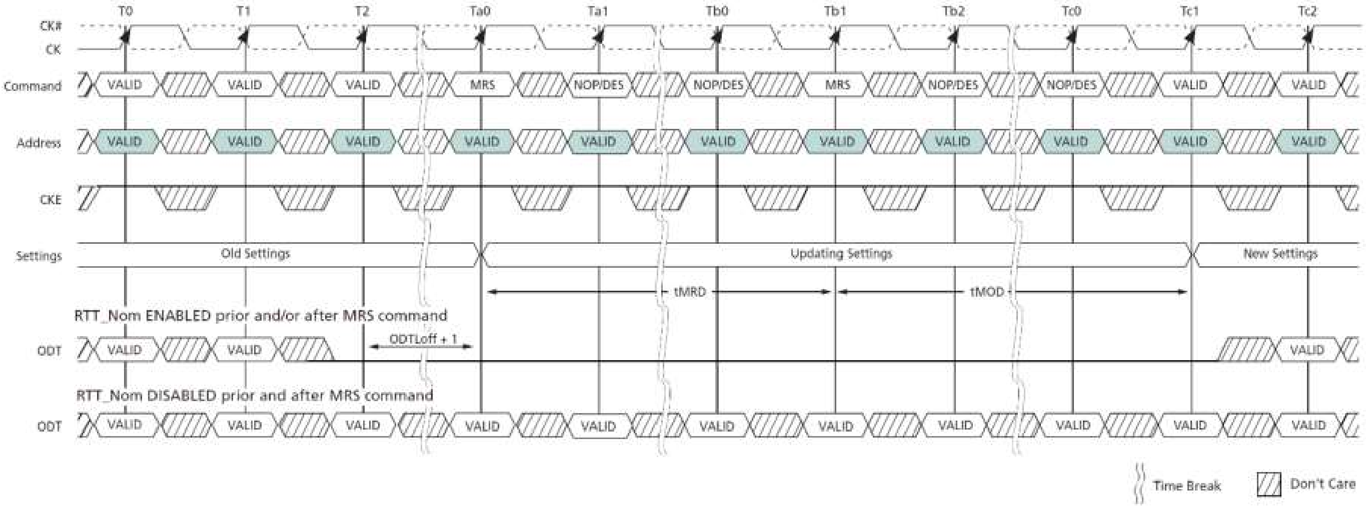
4.5 Register Definition

Programming the Mode Registers

For application flexibility, various functions, features, and modes are programmable in four Mode Registers, provided by the DDR3 SDRAM, as user defined variables and they must be programmed via a Mode Register Set (MRS) command. As the default values of the Mode Registers (/MR) are not defined, contents of Mode Registers must be fully initialized and/or re-initialized, i.e. written, after power up and/or reset for proper operation. Also the contents of the Mode Registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS command and DLL Reset do not affect array contents, which mean these commands can be executed any time after power-up without affecting the array contents.

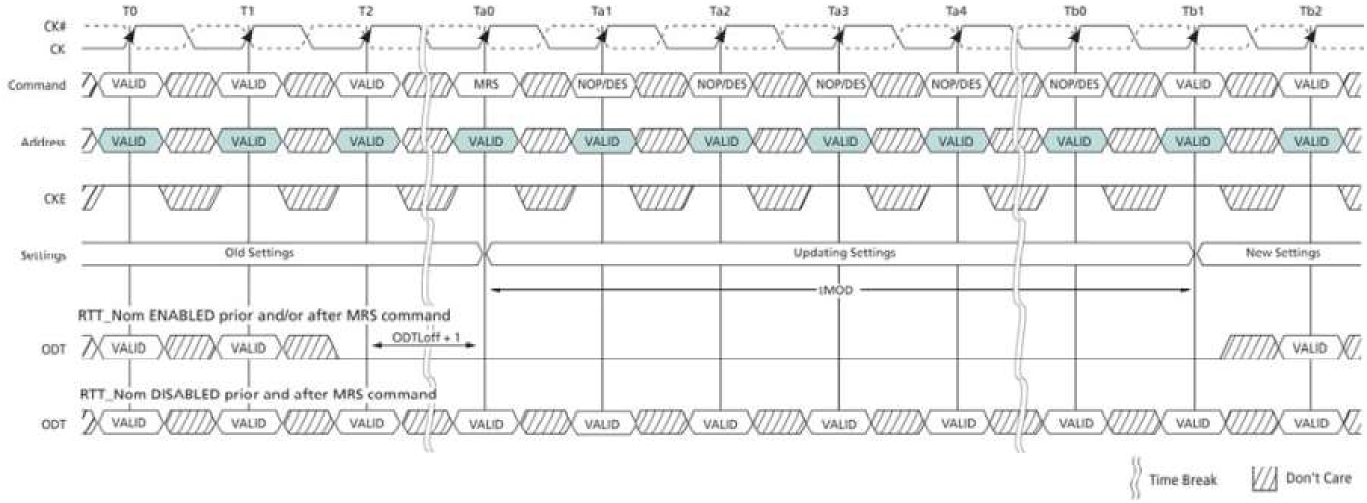
The mode register set command cycle time, tMRD is required to complete the write operation to the mode register and is the minimum time required between two MRS commands shown as below.

tMRD Timing



The MRS command to Non-MRS command delay, tMOD, is require for the DRAM to update the features except DLL reset, and is the minimum time required from an MRS command to a non-MRS command excluding NOP and DES shown as the following figure.

tMOD Timing



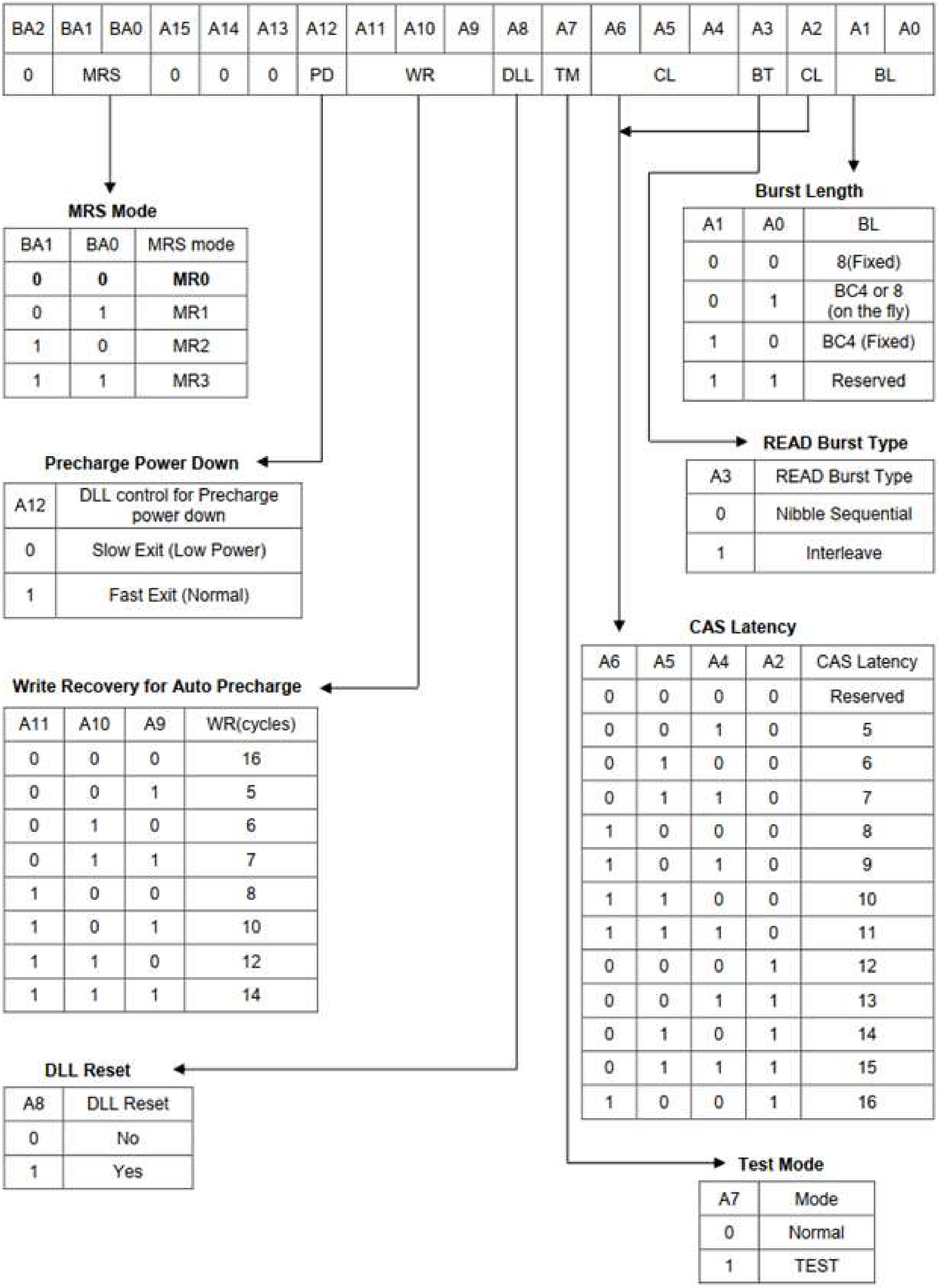
Programming the Mode Registers (Cont'd)

The mode register contents can be changed using the same command and timing requirements during normal operation as long as the DRAM is in idle state, i.e. all banks are in the precharged state with tRP satisfied, all data bursts are completed and CKE is high prior to writing into the mode register. The mode registers are divided into various fields depending on the functionality and/or modes.

Mode Register MR0

The mode-register MR0 stores data for controlling various operating modes of DDR3 SDRAM. It controls burst length, read burst type, CAS latency, test mode, DLL reset, WR, and DLL control for precharge Power-Down, which include various vendor specific options to make DDR3 SDRAM useful for various applications. The mode register is written by asserting low on CS#, RAS#, CAS#, WE#, BA0, BA1, and BA2, while controlling the states of address pins according to the following figure.

MR0 Definition



BA2	BA1	BA0	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	MRS		0	0	0	PD	WR			DLL	TM	CL			BT	CL	BL	

MRS Mode

BA1	BA0	MRS mode
0	**0**	**MR0**
0	1	MR1
1	0	MR2
1	1	MR3

Burst Length

A1	A0	BL
0	0	8(Fixed)
0	1	BC4 or 8 (on the fly)
1	0	BC4 (Fixed)
1	1	Reserved

Precharge Power Down

A12	DLL control for Precharge power down
0	Slow Exit (Low Power)
1	Fast Exit (Normal)

READ Burst Type

A3	READ Burst Type
0	Nibble Sequential
1	Interleave

CAS Latency

A6	A5	A4	A2	CAS Latency
0	0	0	0	Reserved
0	0	1	0	5
0	1	0	0	6
0	1	1	0	7
1	0	0	0	8
1	0	1	0	9
1	1	0	0	10
1	1	1	0	11
0	0	0	1	12
0	0	1	1	13
0	1	0	1	14
0	1	1	1	15
1	0	0	1	16

Write Recovery for Auto Precharge

A11	A10	A9	WR(cycles)
0	0	0	16
0	0	1	5
0	1	0	6
0	1	1	7
1	0	0	8
1	0	1	10
1	1	0	12
1	1	1	14

DLL Reset

A8	DLL Reset
0	No
1	Yes

Test Mode

A7	Mode
0	Normal
1	TEST

Note :

1. BA2 and A13~A15 are RFU and must be programmed to 0 during MRS.
2. WR (write recovery for autoprecharge)min in clock cycles is calculated by dividing tWR(in ns) by tCK(in ns) and rounding up to the next integer: WRmin[cycles] = Roundup(tWR[ns] / tCK[ns]). The WR value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with tRP to determine tDAL.
3. The table only shows the encodings for a given Cas Latency. For actual supported Cas Latency, please refer to speedbin tables for each frequency.
4. The table only shows the encodings for Write Recovery. For actual Write recovery timing, please refer to AC timing table.

Burst Length, Type, and Order

Accesses within a given burst may be programmed to sequential or interleaved order. The burst type is selected via bit A3 as shown in the MR0 Definition as above figure. The ordering of access within a burst is determined by the burst length, burst type, and the starting column address. The burst length is defined by bits A0-A1. Burst lengths options include fix BC4, fixed BL8, and on the fly which allow BC4 or BL8 to be selected coincident with the registration of a Read or Write command via A12/BC.

Burst Length	Read Write	Starting Column Address (A2, A1, A0)			Burst type: Sequential (decimal) A3 = 0	Burst type: Interleave (decimal) A3=1	Note
4 Chop	Read	0	0	0	0, 1, 2, 3, T, T, T, T	0, 1, 2, 3, T, T, T, T	1, 2, 3
		0	0	1	1, 2, 3, 0, T, T, T, T	1, 0, 3, 2, T, T, T, T	
		0	1	0	2, 3, 0, 1, T, T, T, T	2, 3, 0, 1, T, T, T, T	
		0	1	1	3, 0, 1, 2, T, T, T, T	3, 2, 1, 0, T, T, T, T	
		1	0	0	4, 5, 6, 7, T, T, T, T	4, 5, 6, 7, T, T, T, T	
		1	0	1	5, 6, 7, 4, T, T, T, T	5, 4, 7, 6, T, T, T, T	
		1	1	0	6, 7, 4, 5, T, T, T, T	6, 7, 4, 5, T, T, T, T	
		1	1	1	7, 4, 5, 6, T, T, T, T	7, 6, 5, 4, T, T, T, T	
	Write	0	V	V	0, 1, 2, 3, X, X, X, X	0, 1, 2, 3, X, X, X, X	1, 2, 4, 5
		1	V	V	4, 5, 6, 7, X, X, X, X	4, 5, 6, 7, X, X, X, X	
8	Read	0	0	0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	2
		0	0	1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6	
		0	1	0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5	
		0	1	1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4	
		1	0	0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3	
		1	0	1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2	
		1	1	0	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1	
		1	1	1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0	
	Write	V	V	V	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	2,4

Notes:

1. In case of burst length being fixed to 4 by MR0 setting, the internal write operation starts two clock cycles earlier than the BL8 mode. This means that the starting point for tWR and tWTR will be pulled in by two clocks. In case of burst length being selected on-the-fly via A12/BC, the internal write operation starts at the same point in time like a burst of 8 write operation. This means that during on-the-fly control, the starting point for tWR and tWTR will not be pulled in by two clocks.
2. 0~7 bit number is value of CA [2:0] that causes this bit to be the first read during a burst.
3. T: Output driver for data and strobes are in high impedance.
4. V: a valid logic level (0 or 1), but respective buffer input ignores level on input pins.
5. X: Do not Care

CAS Latency

The CAS Latency is defined by MR0 (bit A9~A11) as shown in the MR0 Definition figure. CAS Latency is the delay, in clock cycles, between the internal Read command and the availability of the first bit of output data. DDR3 SDRAM does not support any half clock latencies. The overall Read Latency (RL) is defined as Additive Latency (AL) + CAS Latency (CL); RL = AL + CL.

Test Mode

The normal operating mode is selected by MR0 (bit7=0) and all other bits set to the desired values shown in the MR0 definition figure. Programming bit A7 to a ‘1’ places the DDR3 SDRAM into a test mode that is only used by the DRAM manufacturer and should not be used. No operations or functionality is guaranteed if A7=1.

DLL Reset

The DLL Reset bit is self-clearing, meaning it returns back to the value of ‘0’ after the DLL reset function has been issued. Once the DLL is enabled, a subsequent DLL Reset should be applied. Anytime the DLL reset function is used, tDLLK must be met before any functions that require the DLL can be used (i.e. Read commands or ODT synchronous operations.)

Write Recovery

The programmed WR value MR0(bits A9, A10, and A11) is used for the auto precharge feature along with tRP to determine tDAL WR (write recovery for auto-precharge)min in clock cycles is calculated by dividing tWR(ns) by tCK(ns) and rounding up to the next integer: WRmin[cycles] = Roundup(tWR[ns]/tCK[ns]). The WR must be programmed to be equal or larger than tWR (min).

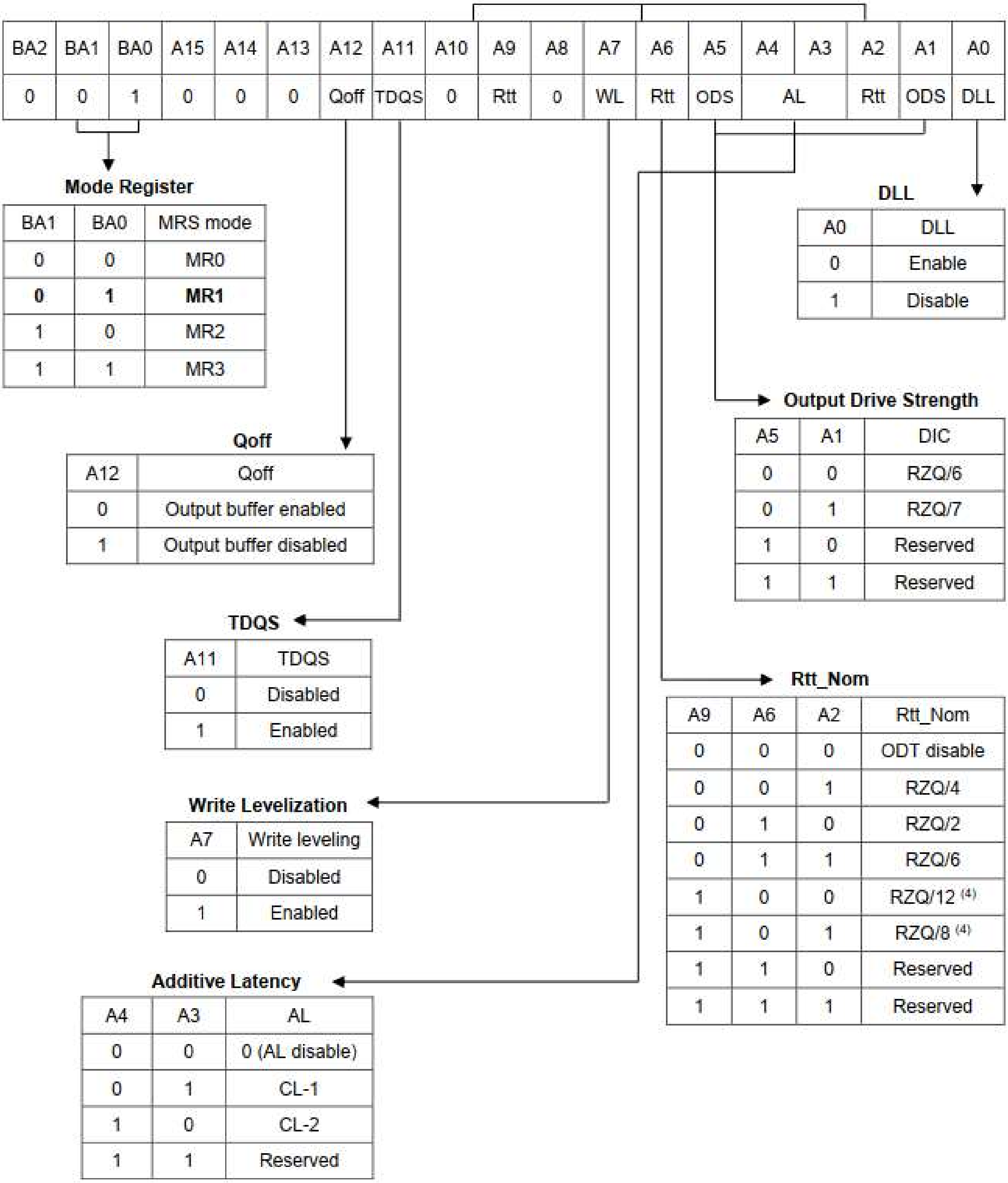
Precharge PD DLL

MR0 (bit A12) is used to select the DLL usage during precharge power-down mode. When MR0 (A12=0), or ’slow-exit’, the DLL is frozen after entering precharge power-down (for potential power savings) and upon exit requires tXPDLL to be met prior to the next valid command. When MR0 (A12=1), or ‘fast-exit’, the DLL is maintained after entering precharge power-down and upon exiting power-down requires tXP to be met prior to the next valid command.

Mode Register MR1

The Mode Register MR1 stores the data for enabling or disabling the DLL, output strength, Rtt_Nom impedance, additive latency, WRITE leveling enable and Qoff. The Mode Register 1 is written by asserting low on CS#, RAS#, CAS#, WE# high on BA0 and low on BA1 and BA2, while controlling the states of address pins according to the following figure.

MR1 Definition



BA2	BA1	BA0	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	1	0	0	0	Qoff	TDQS	0	Rtt	0	WL	Rtt	ODS	AL		Rtt	ODS	DLL

Mode Register

BA1	BA0	MRS mode
0	0	MR0
0	**1**	**MR1**
1	0	MR2
1	1	MR3

DLL

A0	DLL
0	Enable
1	Disable

Qoff

A12	Qoff
0	Output buffer enabled
1	Output buffer disabled

Output Drive Strength

A5	A1	DIC
0	0	RZQ/6
0	1	RZQ/7
1	0	Reserved
1	1	Reserved

TDQS

A11	TDQS
0	Disabled
1	Enabled

Rtt_Nom

A9	A6	A2	Rtt_Nom
0	0	0	ODT disable
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/12 (4)
1	0	1	RZQ/8 (4)
1	1	0	Reserved
1	1	1	Reserved

Write Levelization

A7	Write leveling
0	Disabled
1	Enabled

Additive Latency

A4	A3	AL
0	0	0 (AL disable)
0	1	CL-1
1	0	CL-2
1	1	Reserved

Note :

1. BA2 and A8, A10, and A13 ~ A15 are RFU and must be programmed to 0 during MRS.
2. Outputs disabled - DQs, DQSs, DQSs#.
3. RZQ = 240
4. In Write leveling Mode (MR1[bit7] = 1) with MR1[bit12]=1, all RTT_Nom settings are allowed; in Write Leveling Mode (MR1[bit7] = 1) with MR1[bit12]=0, only RTT_Nom settings of RZQ/2, RZQ/4 and RZQ/6 are allowed.
5. If RTT_Nom is used during Writes, only the values RZQ/2, RZQ/4 and RZQ/6 are allowed.

DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. During normal operation (DLL-on) with MR1 (A0=0), the DLL is automatically disabled when entering Self-Refresh operation and is automatically re-enable upon exit of Self-Refresh operation. Any time the DLL is enabled and subsequently reset, tDLLK clock cycles must occur before a Read or synchronous ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tDQSCK, tAON, or tAOF parameters. During tDLLK, CKE must continuously be registered high. DDR3 SDRAM does not require DLL for any Write operation, expect when RTT_WR is enabled and the DLL is required for proper ODT operation. For more detailed information on DLL Disable operation in DLL-off Mode.

The direct ODT feature is not supported during DLL-off mode. The on-die termination resistors must be disabled by continuously registering the ODT pin low and/or by programming the RTT_Nom bits MR1{A9,A6,A2} to {0,0,0} via a mode register set command during DLL-off mode.

The dynamic ODT feature is not supported at DLL-off mode. User must use MRS command to set Rtt_WR, MR2 {A10, A9} = {0, 0}, to disable Dynamic ODT externally.

Output Driver Impedance Control

The output driver impedance of the DDR3 SDRAM device is selected by MR1 (bit A1 and A5) as shown in MR1 definition figure.

ODT Rtt Values

DDR3 SDRAM is capable of providing two different termination values (Rtt_Nom and Rtt_WR). The nominal termination value Rtt_Nom is programmable in MR1. A separate value (Rtt_WR) may be programmable in MR2 to enable a unique Rtt value when ODT is enabled during writes. The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled.

Additive Latency (AL)

Additive Latency (AL) operation is supported to make command and data bus efficient for sustainable bandwidth in DDR3 SDRAM. In this operation, the DDR3 SDRAM allows a read or write command (either with or without auto-precharge) to be issued immediately after the active command. The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of the AL and CAS Latency (CL) register settings. Write Latency (WL) is controlled by the sum of the AL and CAS Write Latency (CWL) register settings. A summary of the AL register options are shown as the following table.

Additive Latency (AL) Setting

A4	A3	AL
0	0	0, (AL, disable)
0	1	CL-1
1	0	CL-2
1	1	Reserved

Write Leveling

For better signal integrity, DDR3 memory module adopted fly by topology for the commands, addresses, control signals, and clocks. The fly by topology has benefits from reducing number of stubs and their length but in other aspect, causes flight time skew between clock and strobe at every DRAM on DIMM. It makes difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the controller should support 'write leveling' in DDR3 SDRAM to compensate for skew.

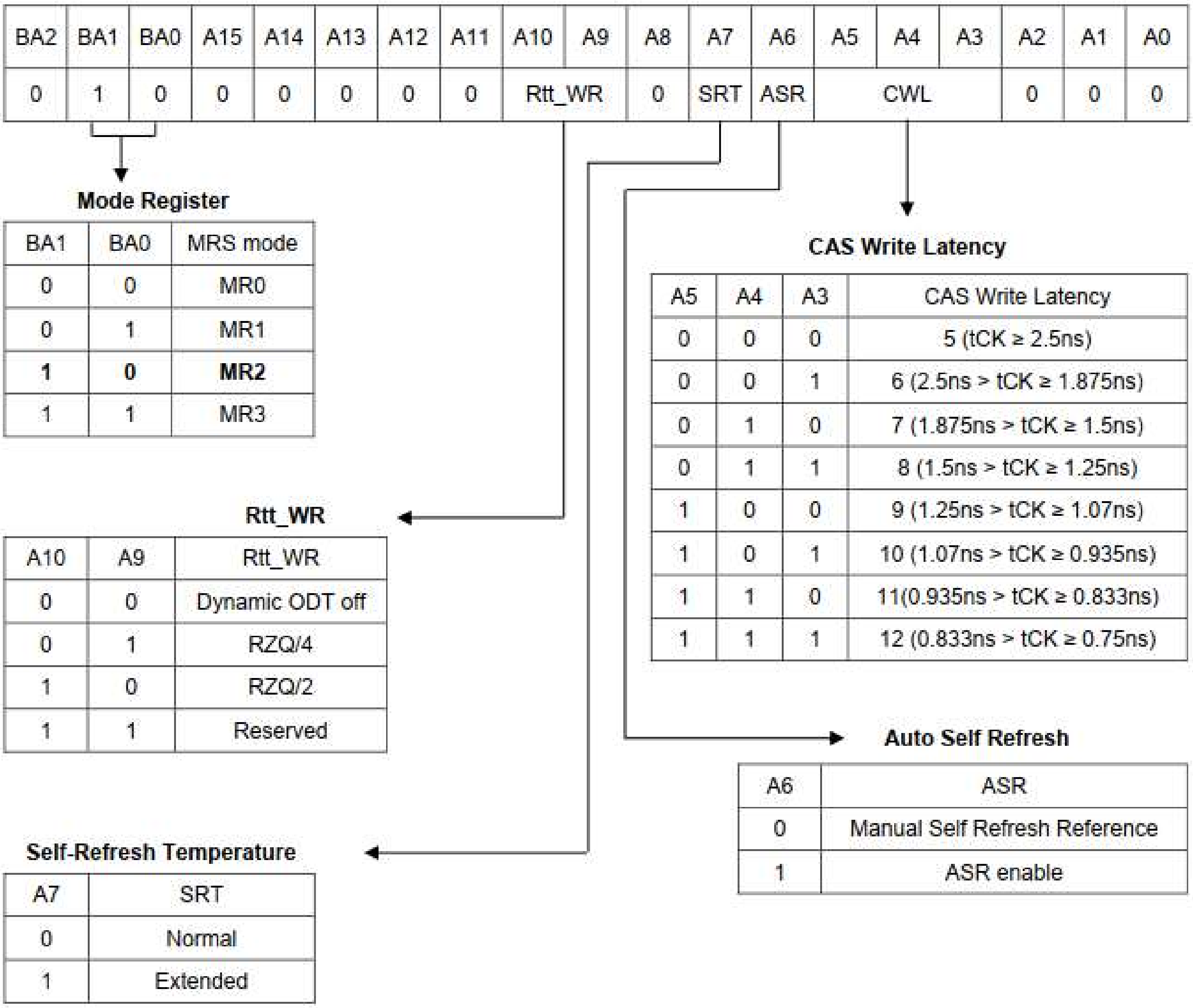
Output Disable

The DDR3 SDRAM outputs maybe enable/disabled by MR1 (bit12) as shown in MR1 definition. When this feature is enabled (A12=1) all output pins (DQs, DQS, DQS#, etc.) are disconnected from the device removing any loading of the output drivers. This feature may be useful when measuring modules power for example. For normal operation A12 should be set to ‘0’.

Mode Register MR2

The Mode Register MR2 stores the data for controlling refresh related features, Rtt_WR impedance, and CAS write latency. The Mode Register 2 is written by asserting low on CS#, RAS#, CAS#, WE# high on BA1 and low on BA0 and BA2, while controlling the states of address pins according to the table below.

MR2 Definition



BA2	BA1	BA0	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	0	0	0	0	0	0	Rtt_WR		0	SRT	ASR	CWL			0	0	0

Mode Register

BA1	BA0	MRS mode
0	0	MR0
0	1	MR1
1	**0**	**MR2**
1	1	MR3

CAS Write Latency

A5	A4	A3	CAS Write Latency
0	0	0	5 (tCK ≥ 2.5ns)
0	0	1	6 (2.5ns > tCK ≥ 1.875ns)
0	1	0	7 (1.875ns > tCK ≥ 1.5ns)
0	1	1	8 (1.5ns > tCK ≥ 1.25ns)
1	0	0	9 (1.25ns > tCK ≥ 1.07ns)
1	0	1	10 (1.07ns > tCK ≥ 0.935ns)
1	1	0	11(0.935ns > tCK ≥ 0.833ns)
1	1	1	12 (0.833ns > tCK ≥ 0.75ns)

Rtt_WR

A10	A9	Rtt_WR
0	0	Dynamic ODT off
0	1	RZQ/4
1	0	RZQ/2
1	1	Reserved

Auto Self Refresh

A6	ASR
0	Manual Self Refresh Reference
1	ASR enable

Self-Refresh Temperature

A7	SRT
0	Normal
1	Extended

1. BA2, A5, A8, A11 ~ A13 are RFU and must be programmed to 0 during MRS.
2. The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled. During write leveling, Dynamic ODT is not available.

CAS Write Latency (CWL)

The CAS Write Latency is defined by MR2 (bits A3-A5) shown in MR2. CAS Write Latency is the delay, in clock cycles, between the internal Write command and the availability of the first bit of input data. DDR3(L) DRAM does not support any half clock latencies. The overall Write Latency (WL) is defined as Additive Latency (AL) + CAS Write Latency (CWL); WL=AL+CWL.

For more information on the supported CWL and AL settings based on the operating clock frequency, refer to "Speed Bin". For detailed Write operation refer to "WRITE Operation".

Auto Self-Refresh (ASR) and Self-Refresh Temperature (SRT)

DDR3(L) SDRAM must support Self-Refresh operation at all supported temperatures. Applications requiring Self-Refresh operation in the Extended Temperature Range must use the ASR function or program the SRT bit appropriately.

Optional in DDR3(L) SDRAM: Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3(L) SDRAM devices support the following options or requirements referred to in this material. For more details refer to "Extended Temperature Usage". DDR3(L) SDRAMs must support Self-Refresh operation at all supported temperatures. Applications requiring Self-Refresh operation in the Extended Temperature Range must use the optional ASR function or program the SRT bit appropriately.

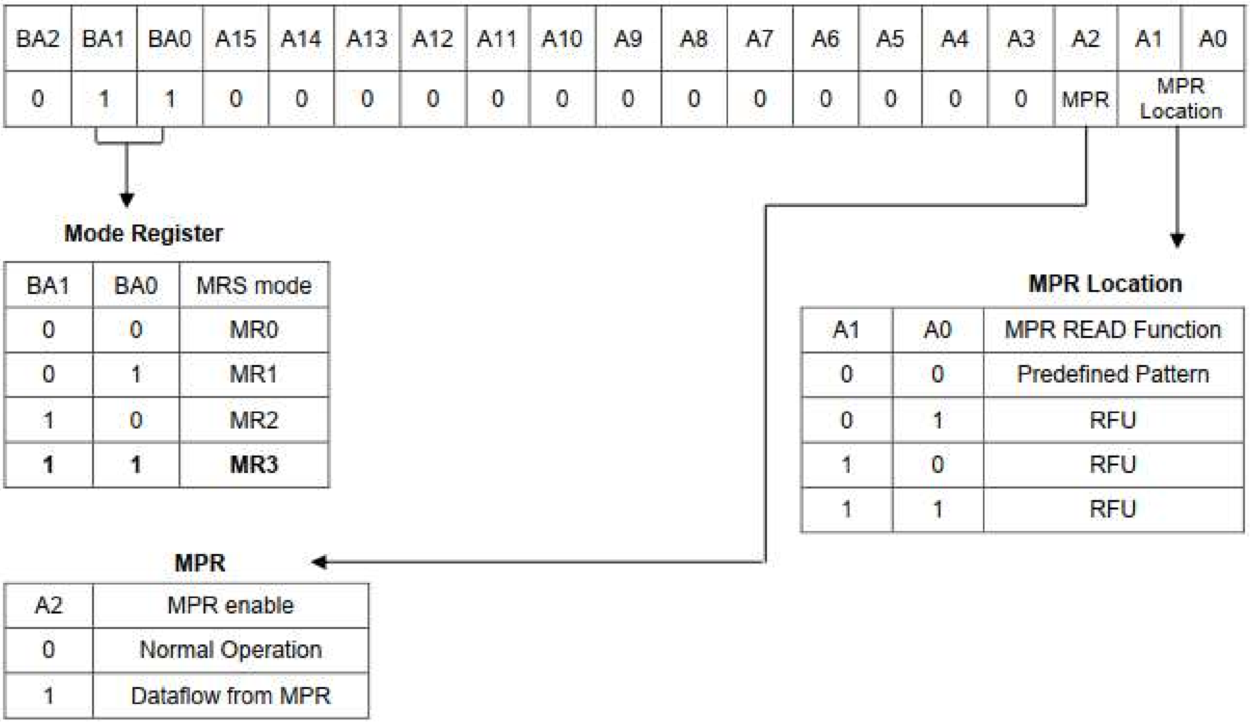
Dynamic ODT (Rtt_WR)

DDR3(L) SDRAM introduces a new feature "Dynamic ODT". In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3(L) SDRAM can be changed without issuing an MRS command. MR2 Register locations A9 and A10 configure the Dynamic ODT settings. In Write leveling mode, only RTT_Nom is available. For details on Dynamic ODT operation, refer to "Dynamic ODT".

Mode Register MR3

The Mode Register MR3 controls Multi-purpose registers. The Mode Register 3 is written by asserting low on CS#, RAS#, CAS#, WE# high on BA1 and BA0, and low on BA2 while controlling the states of address pins according to the table below.

MR3 Definition



BA2	BA1	BA0	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	MPR	MPR Location	

Mode Register

BA1	BA0	MRS mode
0	0	MR0
0	1	MR1
1	0	MR2
1	**1**	**MR3**

MPR Location

A1	A0	MPR READ Function
0	0	Predefined Pattern
0	1	RFU
1	0	RFU
1	1	RFU

MPR

A2	MPR enable
0	Normal Operation
1	Dataflow from MPR

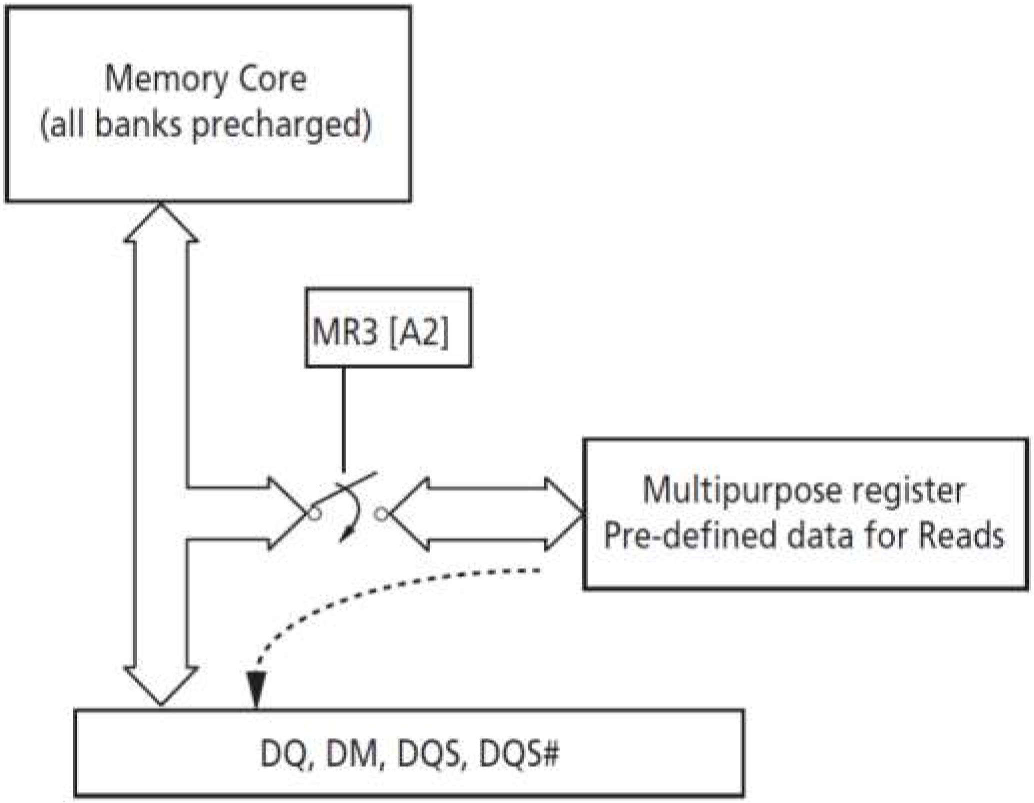
1. BA2, A3 - A15 are RFU and must be programmed to 0 during MRS.
2. The predefined pattern will be used for read synchronization.
3. When MPR control is set for normal operation (MR3 A[2] = 0) then MR3 A[1:0] will be ignored.

Multi-Purpose Register (MPR)

The Multi Purpose Register (MPR) function is used to Read out a predefined system timing calibration bit sequence. To enable the MPR, a Mode Register Set (MRS) command must be issued to MR3 register with bit A2=1. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP met). Once the MPR is enabled, any subsequent RD or RDA commands will be redirected to the Multi Purpose Register. When the MPR is enabled, only RD or RDA commands are allowed until a subsequent MRS command is issued with the MPR disabled (MR3 bit A2=0). Power down mode, Self-Refresh and any other non-RD/RDA command is not allowed during MPR enable mode. The RESET function is supported during MPR enable mode.

The Multi Purpose Register (MPR) function is used to Read out a predefined system timing calibration bit sequence.

MPR Block Diagram



To enable the MPR, a MODE Register Set (MRS) command must be issued to MR3 Register with bit A2 = 1, as following MPR MR3 Register Definition. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP met). Once the MPR is enabled, any subsequent RD or RDA commands will be redirected to the Multi Purpose Register. The resulting operation, when a RD or RDA command is issued, is defined by MR3 bits A[1:0] when the MPR is enabled. When the MPR is enabled, only RD or RDA commands are allowed until a subsequent MRS command is issued with the MPR disabled (MR3 bit A2 = 0). Note that in MPR mode RDA has the same functionality as a READ command which means the auto precharge part of RDA is ignored. Power-Down mode, Self-Refresh and any other non-RD/RDA command is not allowed during MPR enable mode. The RESET function is supported during MPR enable mode.

MPR MR3 Register Definition

MR3 A[2]	MR3 A[1:0]	Function
MPR	MPR-Loc	
0b	Don't care (0b or 1b)	Normal operation, no MPR transaction. All subsequent Reads will come from DRAM array. All subsequent Write will go to DRAM array.
1b	Enable MPR mode, subsequent RD/RDA commands defined by MR3 A[1:0].	Enable MPR mode, subsequent RD/RDA commands defined by MR3 A [1:0].

MPR Functional Description

- One bit wide logical interface via all DQ pins during READ operation.
- Register Read on x8:
- DQ [0] drives information from MPR.
- DQ [7:1] either drive the same information as DQ [0], or they drive 0b.
- Register Read on x16:
- DQL [0] and DQU [0] drive information from MPR.
- DQL [7:1] and DQU [7:1] either drive the same information as DQL [0], or they drive 0b.
- Addressing during for Multi Purpose Register reads for all MPR agents:
- BA [2:0]: don't care
- A [1:0]: A [1:0] must be equal to'00'b. Data read burst order in nibble is fixed
- A[2]: For BL=8, A[2] must be equal to 0b, burst order is fixed to [0,1,2,3,4,5,6,7]. For Burst Chop 4 cases, the burst order is switched on nibble base A [2] =0b, Burst order: 0,1,2,3. A [2] =1b, Burst order: 4,5,6,7.
- A [9:3]: don't care
- A10/AP: don't care
- A12/BC: Selects burst chop mode on-the-fly, if enabled within MR0.
- A11, A13, A14... (if available): Don't care
- Regular interface functionality during register reads:
- Support two Burst Ordering which are switched with A2 and A[1:0]=00b.
- Support of read burst chop (MRS and on-the-fly via A12/BC)
- All other address bits (remaining column address bits including A10, all bank address bits) will be ignored by the DDR3 SDRAM.
- Regular read latencies and AC timings apply.
- DLL must be locked prior to MPR Reads.

NOTE: Burst order bit 0 is assigned to LSB and burst order bit 7 is assigned to MSB of the selected MPR agent.

MPR MR3 Register Definition

MR3 A[2]	MR3 A[1:0]	Function	Burst Length	Read Address A[2:0]	Burst Order and Data Pattern
1b	00b	Read Pre-defined Pattern for System Calibration	BL8	000b	Burst order 0,1,2,3,4,5,6,7 Pre-defined Data Pattern [0,1,0,1,0,1,0,1]
			BC4	000b	Burst order 0,1,2,3 Pre-defined Data Pattern [0,1,0,1]
			BC4	100b	Burst order 4,5,6,7 Pre-defined Data Pattern [0,1,0,1]
1b	01b	RFU	BL8	000b	Burst order 0,1,2,3,4,5,6,7
			BC4	000b	Burst order 0,1,2,3
			BC4	100b	Burst order 4,5,6,7
1b	10b	RFU	BL8	000b	Burst order 0,1,2,3,4,5,6,7
			BC4	000b	Burst order 0,1,2,3
			BC4	100b	Burst order 4,5,6,7
1b	11b	RFU	BL8	000b	Burst order 0,1,2,3,4,5,6,7
			BC4	000b	Burst order 0,1,2,3
			BC4	100b	Burst order 4,5,6,7

Note:

Burst order bit 0 is assigned to LSB and the burst order bit 7 is assigned to MSB of the selected MPR agent.

4.6 DDR3 SDRAM Command Description and Operation

Command Truth Table

Function	Symbol	CKE		CS#	RAS#	CAS#	WE#	BA[2:0]	A15-A13	A12	A10/AP	A[11,9:0]	Notes
		Pre. Cycle	Next Cycle										
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code				
Refresh	REF	H	H	L	L	L	H	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	L	L	H	V	V	V	V	V	7,9,12
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	7,8,9,12
		L	H	L	H	H	H	V	V	V	V	V	
Single Bank Precharge	PRE	H	H	L	L	H	L	BA	V	V	L	V	
Precharge all Banks	PREA	H	H	L	L	H	L	V	V	V	H	V	
Bank Activate	ACT	H	H	L	L	H	H	BA	Row Address (RA)				
Write(Fixed BL8 or BC4)	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	L	L	BA	RFU	L	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	L	L	BA	RFU	H	L	CA	
Write with Auto Precharge (Fixed BL8 or BC4)	WRA	H	H	L	H	L	L	BA	RFU	V	H	CA	
Write with Auto Precharge (BC4, on the Fly)	WRAS4	H	H	L	H	L	L	BA	RFU	L	H	CA	
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	L	L	BA	RFU	H	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	
Read (BC4, on the Fly	RDS4	H	H	L	H	L	H	BA	RFU	L	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	L	H	BA	RFU	H	L	CA	
Read with Auto Precharge (Fixed BL8 or BC4)	RDA	H	H	L	H	L	H	BA	RFU	V	H	CA	
Read with Auto Precharge (BC4, on the Fly)	RDAS4	H	H	L	H	L	H	BA	RFU	L	H	CA	
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	L	H	BA	RFU	H	H	CA	
No Operation	NOP	H	H	L	H	H	H	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	11

Command Truth Table(continue)

Function	Symbol	CKE		CS#	RAS#	CAS#	WE#	BA[2:0]	A15-A13	A12	A10/AP	A[11,9:0]	Notes
		Pre. Cycle	Next Cycle										
Power Down Entry	PDE	H	L	L	H	H	H	V	V	V	V	V	6,12
		H	L	H	X	X	X	X	X	X	X	X	
Power Down Exit	PDX	L	H	L	H	H	H	V	V	V	V	V	6,12
		L	H	H	X	X	X	X	X	X	X	X	
ZQ Calibration Long	ZQCL	H	H	L	H	H	L	X	X	X	H	X	
ZQ Calibration Short	ZQCS	H	H	L	H	H	L	X	X	X	L	X	

Notes:

1. All DDR3 SDRAM commands are defined by states of CS#, RAS#, CAS#, WE# and CKE at the rising edge of the clock. The MSB of BA, RA and CA are device density and configuration dependant.
2. RESET# is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.
3. Bank addresses (BA) determine which bank is to be operated upon. For (E) MRS BA selects an (Extended) Mode Register.
4. “V” means “H or L (but a defined logic level)” and “X” means either “defined or undefined (like floating) logic level”.
5. Burst reads or writes cannot be terminated or interrupted and Fixed/on-the-Fly BL will be defined by MRS.
6. The Power-Down Mode does not perform any refresh operation.
7. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
8. Self Refresh Exit is asynchronous.
9. VREF (Both VrefDQ and VrefCA) must be maintained during Self Refresh operation.
10. The No Operation command should be used in cases when the DDR3 SDRAM is in an idle or wait state. The purpose of the No Operation command (NOP) is to prevent the DDR3 SDRAM from registering any unwanted commands between operations. A No Operation command will not terminate a pervious operation that is still executing, such as a burst read or write cycle.
11. The Deselect command performs the same function as No Operation command.
12. Refer to the CKE Truth Table for more detail with CKE transition.

CKE Truth Table

Current State	CKE		Command (N) RAS#,CAS#,WE#,CS#	Action (N)	Notes
	Prev. Cycle (N-1)	Current Cycle (N)			
Power-Down	L	L	X	Maintain Power-Down	14,15
	L	H	DESELECT or NOP	Power-Down Exit	11,14
Self-Refresh	L	L	X	Maintain Self-Refresh	15,16
	L	H	DESELECT or NOP	Self-Refresh Exit	8,12,16
Bank(s) Active	H	L	DESELECT or NOP	Active Power-Down Entry	11,13,14
Reading	H	L	DESELECT or NOP	Power-Down Entry	11,13,14,17
Writing	H	L	DESELECT or NOP	Power-Down Entry	11,13,14,17
Precharging	H	L	DESELECT or NOP	Power-Down Entry	11,13,14,17
Refreshing	H	L	DESELECT or NOP	Precharge Power-Down Entry	11
All Banks Idle	H	L	DESELECT or NOP	Precharge Power-Down Entry	11,13,14,18
	H	L	REFRESH	Self-Refresh	9,13,18

Notes:

1. CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.
2. Current state is defined as the state of the DDR3 SDRAM immediately prior to clock edge N.
3. COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N), ODT is not included here.
4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
5. The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.
6. CKE must be registered with the same value on tCKEmin consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the tCKEmin clocks of registrations. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of tIS + tCKEmin + tIH.
7. DESELECT and NOP are defined in the Command Truth Table.
8. On Self-Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the tXS period. Read or ODT commands may be issued only after tXSDLL is satisfied.
9. Self-Refresh modes can only be entered from the All Banks Idle state.
10. Must be a legal command as defined in the Command Truth Table.
11. Valid commands for Power-Down Entry and Exit are NOP and DESELECT only.
12. Valid commands for Self-Refresh Exit are NOP and DESELECT only.
13. Self-Refresh cannot be entered during Read or Write operations.
14. The Power-Down does not perform any refresh operations.
15. “X” means “don’t care“(including floating around VREF) in Self-Refresh and Power-Down. It also applies to Address pins.
16. VREF (Both Vref_DQ and Vref_CA) must be maintained during Self-Refresh operation.
17. If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power-Down is entered, otherwise Active Power-Down is entered.
18. ‘Idle state’ is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, tZQCS, etc.) as well as all Self-Refresh exit and Power-Down Exit parameters are satisfied (tXS, tXP, tXPDLL, etc).

No Operation (NOP) Command

The No operation (NOP) command is used to instruct the selected DDR3L SDRAM to perform a NOP (CS# low and RAS#, CAS# and WE# high). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

Deselect Command

The Deselect function (CS HIGH) prevents new commands from being executed by the DDR3 SDRAM. The DDR3 SDRAM is effectively deselected. Operations already in progress are not affected.

DLL- Off Mode

DDR3 DLL-off mode is entered by setting MR1 bit A0 to “1”; this will disable the DLL for subsequent operations until A0 bit set back to “0”. The MR1 A0 bit for DLL control can be switched either during initialization or later. The DLL-off Mode operations listed below are an optional feature for DDR3. The maximum clock frequency for DLL-off Mode is specified by the parameter tCKDLL_OFF. There is no minimum frequency limit besides the need to satisfy the refresh interval, tREFI.

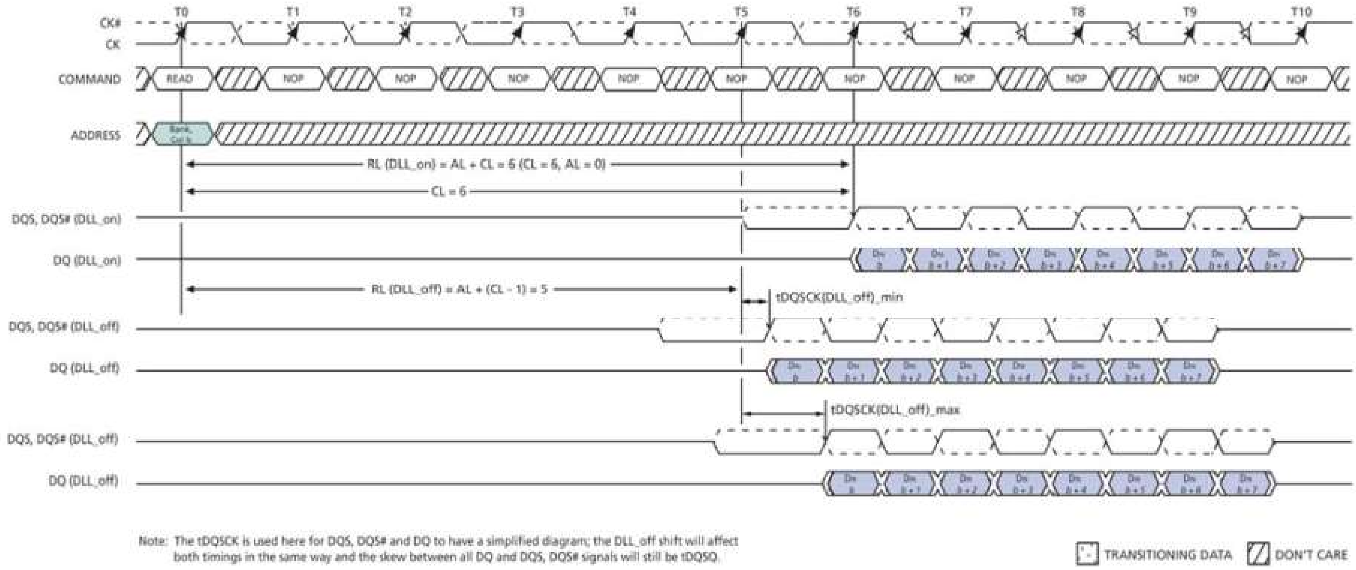
Due to latency counter and timing restrictions, only one value of CAS Latency (CL) in MR0 and CAS Write Latency (CWL) in MR2 are supported. The DLL-off mode is only required to support setting of both CL=6 and CWL=6.

DLL-off mode will affect the Read data Clock to Data Strobe relationship (tDQSCK) but not the data Strobe to Data relationship (tDQSQ, tQH). Special attention is needed to line up Read data to controller time domain.

Comparing with DLL-on mode, where tDQSCK starts from the rising clock edge (AL+CL) cycles after the Read command, the DLL-off mode tDQSCK starts (AL+CL-1) cycles after the read command. Another difference is that tDQSCK may not be small compared to tCK (it might even be larger than tCK) and the difference between tDQSCKmin and tDQSCKmax is significantly larger than in DLL-on mode.

The timing relations on DLL-off mode READ operation have shown at the following Timing Diagram (CL=6, BL=8).

DLL-off mode READ Timing Operation



Note: The tDQSCK is used here for DQS, DQS# and DQ to have a simplified diagram; the DLL_off shift will affect both timings in the same way and the skew between all DQ and DQS, DQS# signals will still be tDQSQ.

DLL on/off Switching Procedure

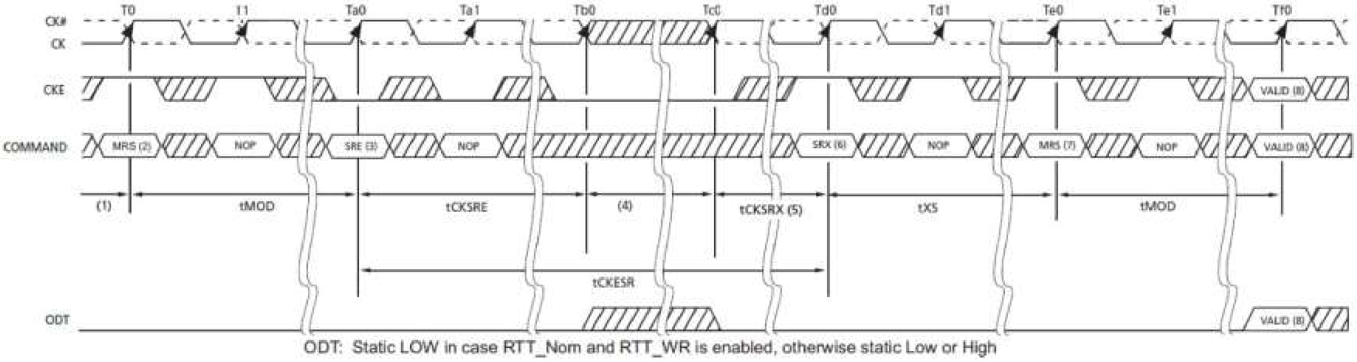
DDR3 DLL-off mode is entered by setting MR1 bit A0 to “1”; this will disable the DLL for subsequent operation until A0 bit set back to “0”.

DLL “on” to DLL “off” Procedure

To switch from DLL “on” to DLL “off” requires the frequency to be changed during Self-Refresh outlined in the following procedure:

1. Starting from Idle state (all banks pre-charged, all timing fulfilled, and DRAMs On-die Termination resistors, RTT, must be in high impedance state before MRS to MR1 to disable the DLL).
2. Set MR1 Bit A0 to “1” to disable the DLL.
3. Wait tMOD.
4. Enter Self Refresh Mode; wait until (tCKSRE) satisfied.
5. Change frequency, in guidance with “Input Clock Frequency Change” section.
6. Wait until a stable clock is available for at least (tCKSRX) at DRAM inputs.
7. Starting with the Self Refresh Exit command, CKE must continuously be registered HIGH until all tMOD timings from any MRS command are satisfied. In addition, if any ODT features were enabled in the mode registers when Self Refresh mode was entered, the ODT signal must continuously be registered LOW until all tMOD timings from any MRS command are satisfied. If both ODT features were disabled in the mode registers when Self Refresh mode was entered, ODT signal can be registered LOW or HIGH.
8. Wait tXS, and then set Mode Registers with appropriate values (especially an update of CL, CWL, and WR may be necessary. A ZQCL command may also be issued after tXS).
9. Wait for tMOD, and then DRAM is ready for next command.

DLL Switch Sequence from DLL-on to DLL-off



NOTES:
1. Starting with Idle State, RTT in Hi-Z state
2. Disable DLL by setting MR1 Bit A0 to 1
3. Enter SR
4. Change Frequency
5. Clock must be stable tCKSRX
6. Exit SR
7. Update Mode registers with DLL off parameters setting
8. Any valid command

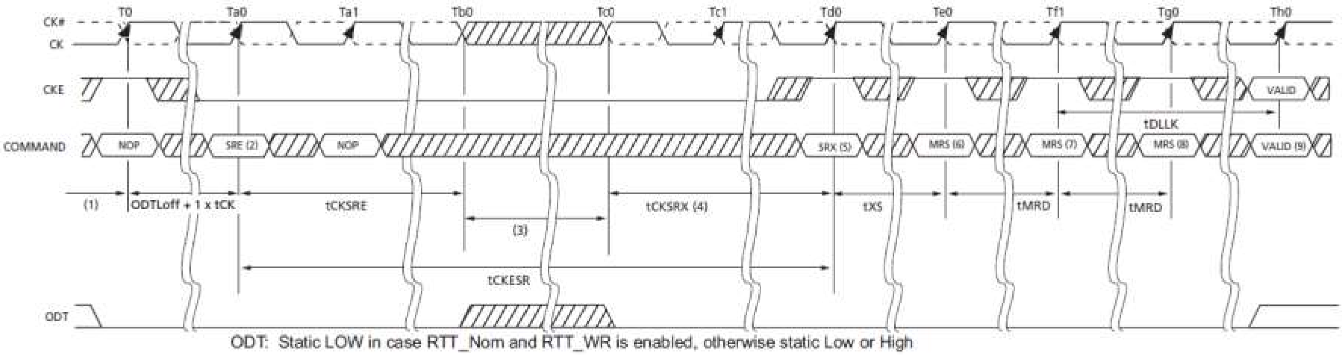
TIME BREAK ▨ DON'T CARE

DLL “off” to DLL “on” Procedure

To switch from DLL “off” to DLL “on” (with requires frequency change) during Self-Refresh:

1. Starting from Idle state (all banks pre-charged, all timings fulfilled and DRAMs On-die Termination resistors (RTT) must be in high impedance state before Self-Refresh mode is entered).
2. Enter Self Refresh Mode, wait until tCKSRE satisfied.
3. Change frequency, in guidance with “Input clock frequency change” section.
4. Wait until a stable is available for at least (tCKSRX) at DRAM inputs.
5. Starting with the Self Refresh Exit command, CKE must continuously be registered HIGH until tDLLK timing from subsequent DLL Reset command is satisfied. In addition, if any ODT features were enabled in the mode registers when Self Refresh mode was entered. the ODT signal must continuously be registered LOW until tDLLK timings from subsequent DLL Reset command is satisfied. If both ODT features are disabled in the mode registers when Self Refresh mode was entered, ODT signal can be registered LOW or HIGH.
6. Wait tXS, then set MR1 Bit A0 to “0” to enable the DLL.
7. Wait tMRD, then set MR0 Bit A8 to “1” to start DLL Reset.
8. Wait tMRD, then set Mode registers with appropriate values (especially an update of CL, CWL, and WR may be necessary. After tMOD satisfied from any proceeding MRS command, a ZQCL command may also be issued during or after tDLLK).
9. Wait for tMOD, then DRAM is ready for next command (remember to wait tDLLK after DLL Reset before applying command requiring a locked DLL!). In addition, wait also for tZQoper in case a ZQCL command was issued.

DLL Switch Sequence from DLL-off to DLL-on



ODT: Static LOW in case RTT_Nom and RTT_WR is enabled, otherwise static Low or High

NOTES:
1. Starting with Idle State
2. Enter SR
3. Change Frequency
4. Clock must be stable tCKSRX
5. Exit SR
6. Set DLL on by MR1 A0=0
7. Update Mode registers
8. Any valid command

⸾ TIME BREAK ▨ DON'T CARE

Input Clock frequency change

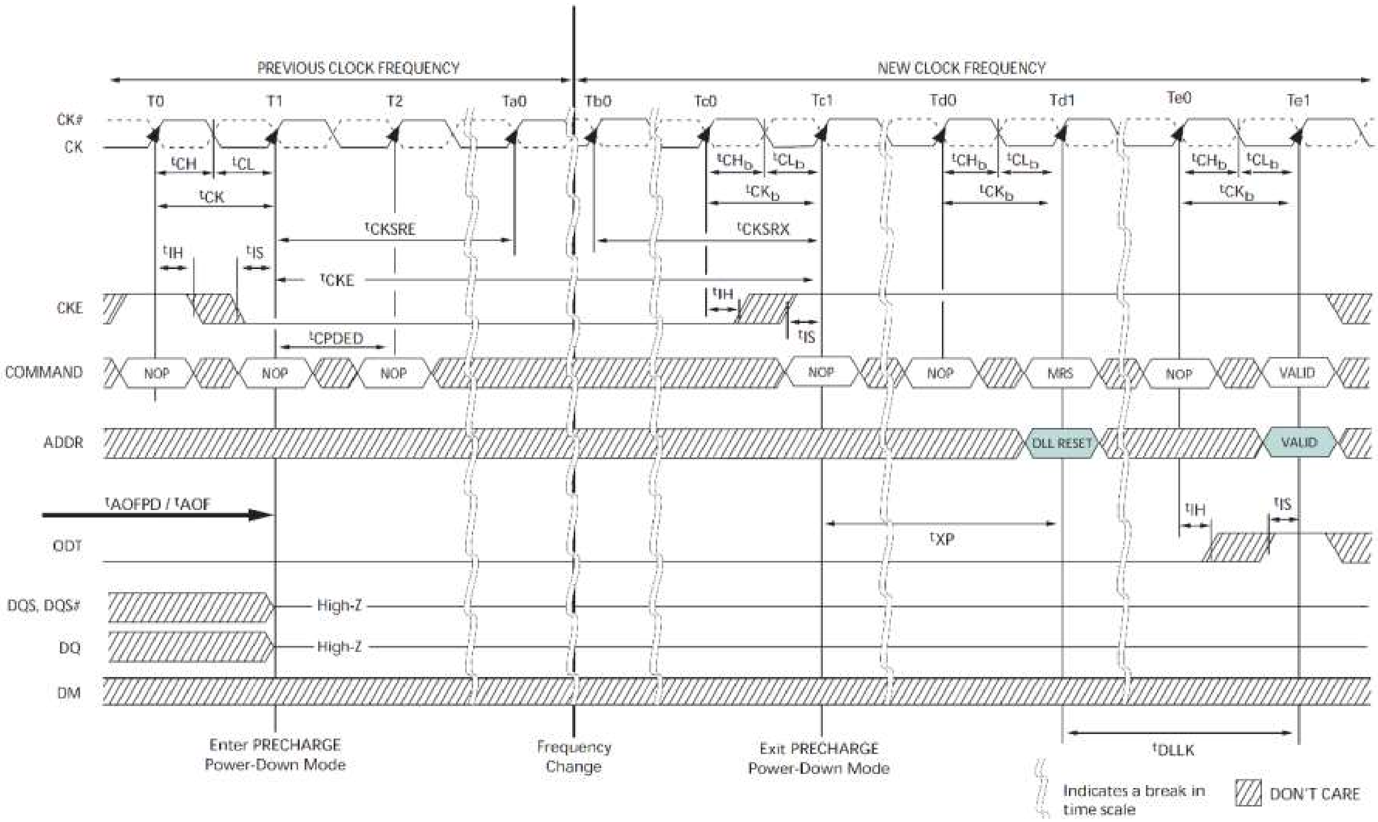
Once the DDR3 SDRAM is initialized, the DDR3 SDRAM requires the clock to be “stable” during almost all states of normal operation. This means once the clock frequency has been set and is to be in the “stable state”, the clock period is not allowed to deviate except for what is allowed for by the clock jitter and SSC (spread spectrum clocking) specification.

The input clock frequency can be changed from one stable clock rate to another stable clock rate under two conditions: (1) Self-Refresh mode and (2) Precharge Power-Down mode. Outside of these two modes, it is illegal to change the clock frequency.

For the first condition, once the DDR3 SDRAM has been successfully placed in to Self-Refresh mode and tCKSRE has been satisfied, the state of the clock becomes a don’t care. Once a don’t care, changing the clock frequency is permissible, provided the new clock frequency is stable prior to tCKSRX. When entering and exiting Self-Refresh mode of the sole purpose of changing the clock frequency. The DDR3 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade.

The second condition is when the DDR3 SDRAM is in Precharge Power-Down mode (either fast exit mode or slow exit mode). If the RTT_Nom feature was enabled in the mode register prior to entering Precharge power down mode, the ODT signal must continuously be registered LOW ensuring RTT is in an off state. If the RTT_Nom feature was disabled in the mode register prior to entering Precharge power down mode, RTT will remain in the off state. The ODT signal can be registered either LOW or HIGH in this case. A minimum of tCKSRE must occur after CKE goes LOW before the clock frequency may change. The DDR3 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade. During the input clock frequency change, ODT and CKE must be held at stable LOW levels. Once the input clock frequency is changed, stable new clocks must be provided to the DRAM tCKSRX before precharge Power Down may be exited; after Precharge Power Down is exited and tXP has expired, the DLL must be RESET via MRS. Depending on the new clock frequency additional MRS commands may need to be issued to appropriately set the WR, CL, and CWL with CKE continuously registered high. During DLL re-lock period, ODT must remain LOW and CKE must remain HIGH. After the DLL lock time, the DRAM is ready to operate with new clock frequency.

Change Frequency during Precharge Power-down



Notes:

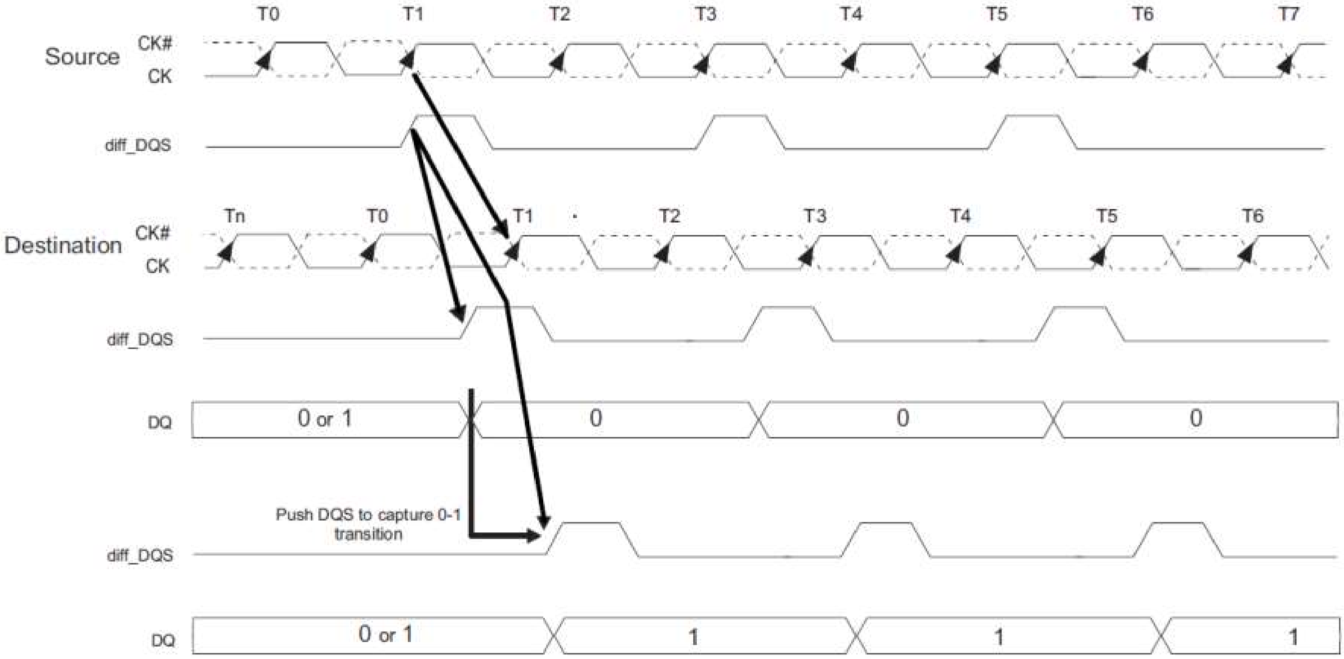
1. Applicable for both SLOW EXIT and FAST EXIT Precharge Power-down.
2. tAOFPD and tAOF must be statisfied and outputs High-Z prior to T1; refer to ODT timing section for exact requirements.
3. If the RTT_NOM feature was enabled in the mode register prior to entering Precharge power down mode, the ODT signal must continuously be registered LOW ensuring RTT is in an off state. If the RTT_NOM feature was disabled in the mode register prior to entering Precharge power down mode, RTT will remain in the off state. The ODT signal can be registered either LOW or HIGH in this case.

Write Leveling

For better signal integrity, DDR3 memory adopted fly by topology for the commands, addresses, control signals, and clocks. The fly by topology has benefits from reducing number of stubs and their length but in other aspect, causes flight time skew between clock and strobe at every DRAM on DIMM. It makes it difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the controller should support "write leveling" in DDR3 SDRAM to compensate the skew.

The memory controller can use the "write leveling" feature and feedback from the DDR3 SDRAM to adjust the DQS – DQS# to CK - CK# relationship. The memory controller involved in the leveling must have adjustable delay setting on DQS – DQS# to align the rising edge of DQS - DQS# with that of the clock at the DRAM pin. DRAM asynchronously feeds back CK – CK#, sampled with the rising edge of DQS - DQS, through the DQ bus. The controller repeatedly delays DQS –DQS# until a transition from 0 to 1 is detected. The DQS – DQS# delay established though this exercise would ensure tDQSS specification. Besides tDQSS, tDSS, and tDSH specification also needs to be fulfilled. One way to achieve this is to combine the actual tDQSS in the application with an appropriate duty cycle and jitter on the DQS-DQS signals. Depending on the actual tDQSS in the application, the actual values for tDQSL and tDQSH may have to be better than the absolute limits provided in "AC Timing Parameters" section in order to satisfy tDSS and tDSH specification. A conceptual timing of this scheme is show as below figure.

Write Leveling Concept



DQS, DQS# driven by the controller during leveling mode must be determined by the DRAM based on ranks populated. Similarly, the DQ bus driven by the DRAM must also be terminated at the controller.

One or more data bits should carry the leveling feedback to the controller across the DRAM configurations x8. Therefore, a separate feedback mechanism should be able for each byte lane. The upper data bits should provide the feedback of the upper diff_DQS (diff_UDQS) to clock relationship whereas the lower data bits would indicate the lower diff_DQS (diff_LDQS) to clock relationship.

DRAM setting for write leveling and DRAM termination unction in that mode

DRAM enters into Write leveling mode if A7 in MR1 set "High" and after finishing leveling, DRAM exits from write leveling mode if A7 in MR1 set "Low". Note that in write leveling mode, only DQS DQS# terminations are activated and deactivated via ODT pin not like normal operation.

MR setting involved in the leveling procedure

Function	MR1	Enable	Disable
Write leveling enable	A7	1	0
Output buffer mode (Qoff)	A12	0	1

DRAM termination function in the leveling mode

ODT pin at DRAM	DQS, DQS# termination	DQs termination
De-asserted	off	off
Asserted	on	off

Note:

In write leveling mode with its output buffer disabled (MR1[bit7]=1 with MR1[bit12]=1) all RTT_Nom settings are allowed; in Write Leveling Mode with its output buffer enabled (MR1[bit7]=1 with MR1[bit12]=0) only RTT_Nom settings of RZQ/2, RZQ/4, and RZQ/6 are allowed.

Procedure Description

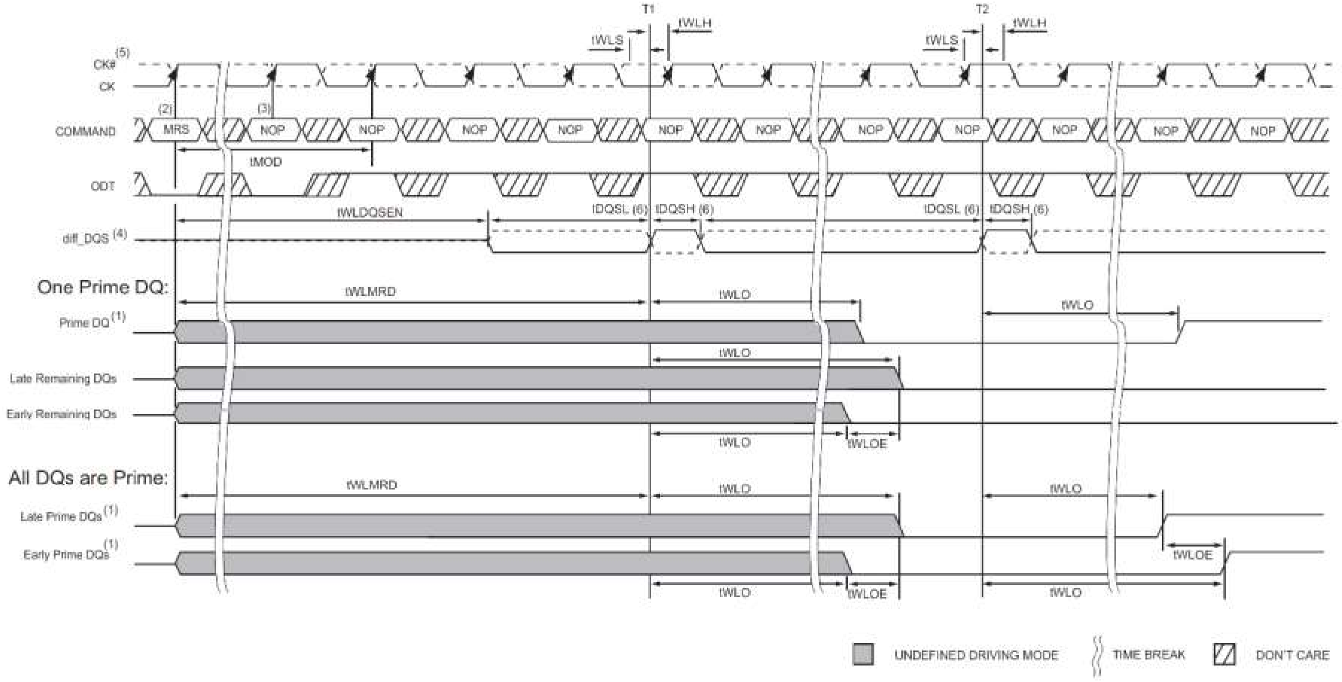
Memory controller initiates Leveling mode of all DRAMs by setting bit 7 of MR1 to 1. With entering write leveling mode, the DQ pins are in undefined driving mode. During write leveling mode, only NOP or Deselect commands are allowed. As well as an MRS command to exit write leveling mode. Since the controller levels one rank at a time, the output of other rank must be disabled by setting MR1 bit A12 to 1. Controller may assert ODT after tMOD, time at which DRAM is ready to accept the ODT signal.

Controller may drive DQS low and DQS# high after a delay of tWLDQSEN, at which time DRAM has applied on-die termination on these signals. After tDQSL and tWLMRD controller provides a single DQS, DQS# edge which is used by the DRAM to sample CK – CK# driven from controller. tWLMRD(max) timing is controller dependent.

DRAM samples CK - CK# status with rising edge of DQS and provides feedback on all the DQ bits asynchronously after tWLO timing. There is a DQ output uncertainty of tWLOE defined to allow mismatch on DQ bits; there are no read strobes (DQS, DQS#) needed for these DQs. Controller samples incoming DQ and decides to increment or decrement DQS – DQS# delay setting and launches the next DQS, DQS# pulse after some time, which is controller dependent. Once a 0 to 1 transition is detected, the controller locks DQS – DQS# delay setting and write leveling is achieved for the device. The following figure describes the timing diagram and parameters for the overall Write leveling procedure.

Timing Details of Write Leveling Sequence

DQS – DQS# is capturing CK – CK# low at T1 and CK - CK# high at T2



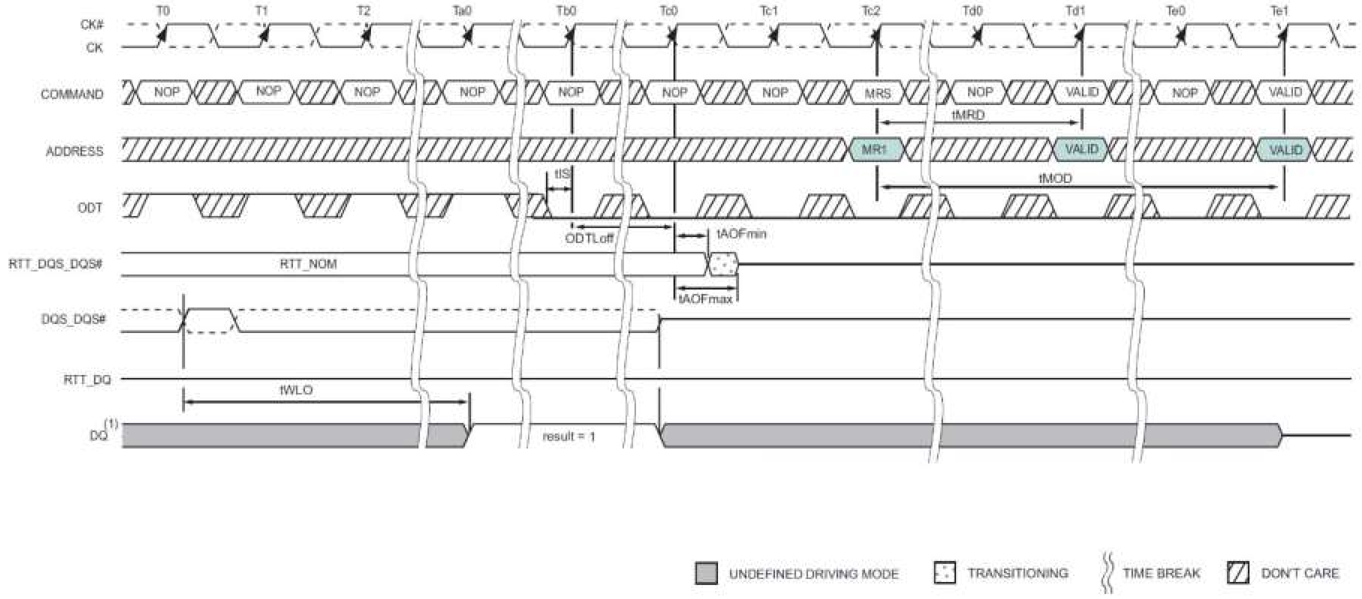
NOTES:
1. DRAM has the option to drive leveling feedback on a prime DQ or all DQs. If feedback is driven only on one DQ, the remaining DQs must be driven low, as shown in above Figure, and maintained at this state through out the leveling procedure.
2. MRS: Load MR1 to enter write leveling mode.
3. NOP: NOP or Deselect.
4. diff_DQS is the differential data strobe (DQS, DQS#). Timing reference points are the zero crossings. DQS is shown with solid line, DQS# is shown with dotted lin
5. CK, CK# : CK is shown with solid dark line, where as CK# is drawn with dotted line.
6. DQS, DQS# needs to fulfill minimum pulse width requirements tDQSH(min) and tDQSL(min) as defined for regular Writes; the max pulse width is system depende

Write Leveling Mode Exit

The following sequence describes how Write Leveling Mode should be exited:

1. After the last rising strobe edge (see ~T0), stop driving the strobe signals (see ~Tc0). Note: From now on, DQ pins are in undefined driving mode, and will remain undefined, until tMOD after the respective MR command (Te1).
2. Drive ODT pin low (tIS must be satisfied) and keep it low (see Tb0).
3. After the RTT is switched off, disable Write Level Mode via MRS command (see Tc2).
4. After tMOD is satisfied (Te1), any valid command may be registered. (MR commands may be issued after tMRD (Td1).

Timing Detail of Write Leveling Exit



Extended Temperature Usage

The DDR3 SDRAM supports the optional extended temperature range of 0°C to +95°C, TC. Thus, the SRT and ASR options must be used at a minimum. The extended temperature range DRAM must be refreshed externally at 2X (double refresh) anytime the case temperature is above +85°C (and does not exceed +95°C). The external refreshing requirement is accomplished by reducing the refresh period from 64ms to 32ms. However, self refresh mode requires either ASR or SRT to support the extended temperature. Thus either ASR or SRT must be enabled when TC is above +85°C or self refresh cannot be used until the case temperature is at or below +85°C.

Mode Register Description

Field	Bits	Description
ASR	MR2(A6)	**Auto Self-Refresh (ASR)** When enabled, DDR3 SDRAM automatically provides Self-Refresh power management functions for all supported operating temperature values. If not enabled, the SRT bit must be programmed to indicate TOPER during subsequent Self-Refresh operation. 0 = Manual SR Reference (SRT) 1 = ASR enable
SRT	MR2(A7)	**Self-Refresh Temperature (SRT) Range** If ASR = 0, the SRT bit must be programmed to indicate TOPER during subsequent Self-Refresh operation. If ASR = 1, SRT bit must be set to 0. 0 = Normal operating temperature range 1 = Extended operating temperature range 1 = Extended operating temperature range = Extended operating temperature range

Auto Self-Refresh mode - ASR mode

DDR3 SDRAM provides an Auto-Refresh mode (ASR) for application ease. ASR mode is enabled by setting MR2 bit A6=1 and MR2 bit A7=0. The DRAM will manage Self-Refresh entry in either the Normal or Extended Temperature Ranges. In this mode, the DRAM will also manage Self-Refresh power consumption when the DRAM operating temperature changes, lower at low temperatures and higher at high temperatures. If the ASR option is not supported by DRAM, MR2 bit A6 must set to 0. If the ASR option is not enabled (MR2 bit A6=0), the SRT bit (MR2 bit A7) must be manually programmed with the operating temperature range required during Self-Refresh operation. Support of the ASR option does not automatically imply support of the Extended Temperature Range.

Self-Refresh Temperature Range – SRT

SRT applies to devices supporting Extended Temperature Range only. If ASR=0, the Self-Refresh Temperature (SRT) Range bit must be programmed to guarantee proper self-refresh operation. If SRT=0, then the DRAM will set an appropriate refresh rate for Self-Refresh operation in the Normal Temperature Range. If SRT=1, then the DRAM will set an appropriate, potentially different, refresh rate to allow Self-Refresh operation in either the Normal or Extended Temperature Ranges. The value of the SRT bit can effect self-refresh power consumption, please refer to IDD table for details.

Self-Refresh Mode Summary

MR2 A[6]	MR2 A[7]	Self-Refresh operation	Allowed Operating Temperature Range for Self-Refresh mode
0	0	Self-Refresh rate appropriate for the Normal Temperature Range	Normal
0	1	Self-Refresh appropriate for either the Normal or Extended Temperature Ranges. The DRAM must support Extended Temperature Range. The value of the SRT bit can effect self-refresh power consumption, please refer to the IDD table for details.	Normal and Extended
1	0	ASR enabled (for devices supporting ASR and Normal Temperature Range). Self-Refresh power consumption is temperature dependent.	Normal
1	0	ASR enabled (for devices supporting ASR and Extended Temperature Range). Self-Refresh power consumption is temperature dependent.	Normal and Extended
1	1	Illegal	

Notes:

1. The Normal range depends on product’s grade.
   - Commercial Grade = 0˚C ~85˚C
2. The Normal and Extended range depends on product’s grade.
   - Commercial Grade = 0˚C ~95˚C

MPR MR3 Register Definition

MR3 A[2]	MR3 A[1:0]	Function
0	don't care (0 or 1)	Normal operation, no MPR transaction. All subsequent Reads will come from DRAM array. All subsequent Writes will go to DRAM array.
1	1	Enable MPR mode, subsequent RD/RDA commands defined by MR3 A[1:0].

MPR Functional Description

- One bit wide logical interface via all DQ pins during READ operation.
- Register Read on x8:
- DQ [0] drives information from MPR.
- DQ [7:1] either drive the same information as DQ [0], or they drive 0.
- Addressing during for Multi Purpose Register reads for all MPR agents:
- BA [2:0]: don't care.
- A [1:0]: A [1:0] must be equal to "00". Data read burst order in nibble is fixed.
- A[2]: For BL=8, A[2] must be equal to 0, burst order is fixed to [0,1,2,3,4,5,6,7]; For Burst chop 4 cases, the burst order is switched on nibble base, A[2]=0, burst order: 0,1,2,3, A[2]=1, burst order: 4,5,6,7. *)
- A [9:3]: don't care.
- A10/AP: don't care.
- A12/BC: Selects burst chop mode on-the-fly, if enabled within MR0
- A11, A13: don't care.
- Regular interface functionality during register reads:
- Support two Burst Ordering which are switched with A2 and A[1:0]=00.
- Support of read burst chop (MRS and on-the-fly via A12/BC).
- All other address bits (remaining column addresses bits including A10, all bank address bits) will be ignored by the DDR3 SDRAM.
- Regular read latencies and AC timings apply.
- DLL must be locked prior to MPR READs.

Note:

Burst order bit 0 is assigned to LSB and burst order bit 7 is assigned to MSB of the selected MPR agent.

MPR Register Address Definition

The following table provide an overview of the available data location, how they are addressed by MR3 A[1:0] during a MRS to MR3, and how their individual bits are mapped into the burst order bits during a Multi Purpose Register Read.

MPR MR3 Register Definition

MR3 A[2]	MR3 A[1:0]	Function	Burst Length	Read Address A[2:0]	Burst Order and Data Pattern
1	00	Read Predefined Pattern for System Calibration	BL8	000	Burst order 0,1,2,3,4,5,6,7 Pre-defined Data Pattern [0,1,0,1,0,1,0,1]
			BC4	000	Burst order 0,1,2,3 Pre-defined Data Pattern [0,1,0,1]
			BC4	100	Burst order 4,5,6,7 Pre-defined Data Pattern [0,1,0,1]
1	01	RFU	BL8	000	Burst order 0,1,2,3,4,5,6,7
			BC4	000	Burst order 0,1,2,3
			BC4	100	Burst order 4,5,6,7
1	10	RFU	BL8	000	Burst order 0,1,2,3,4,5,6,7
			BC4	000	Burst order 0,1,2,3
			BC4	100	Burst order 4,5,6,7
1	11	RFU	BL8	000	Burst order 0,1,2,3,4,5,6,7
			BC4	000	Burst order 0,1,2,3
			BC4	100	Burst order 4,5,6,7

Note:

Burst order bit 0 is assigned to LSB and the burst order bit 7 is assigned to MSB of the selected MPR agent.

ACTIVE Command

The ACTIVE command is used to open (or activate) a row in a particular bank for subsequent access. The value on the BA0-BA2 inputs selects the bank, and the addresses provided on inputs A0-A14 selects the row. These rows remain active (or open) for accesses until a precharge command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

PRECHARGE Command

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row activation a specified time (tRP) after the PRECHARGE command is issued, except in the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command is allowed if there is no open row in that bank (idle bank) or if the previously open row is already in the process of precharging. However, the precharge period will be determined by the last PRECHARGE command issued to the bank.

4.7 READ Operation

Read Burst Operation

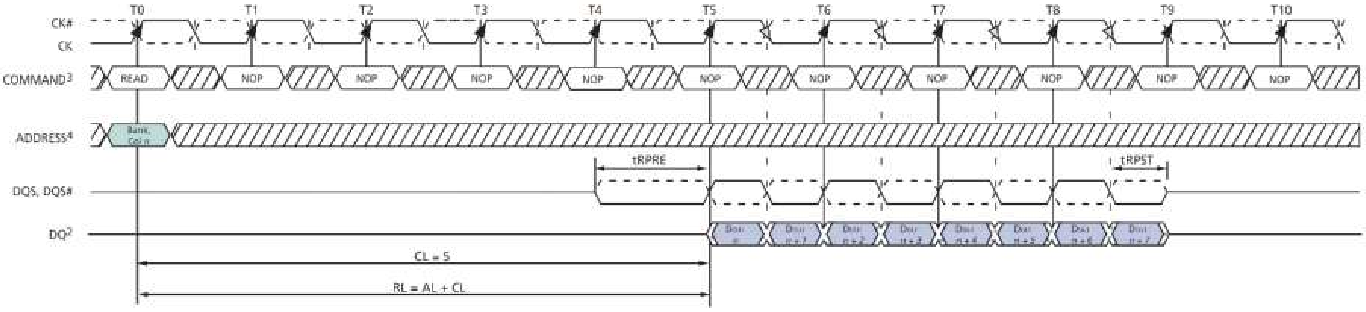
During a READ or WRITE command DDR3L will support BC4 and BL8 on the fly using address A12 during the READ or WRITE (AUTO PRECHARGE can be enabled or disabled).

A12=0, BC4 (BC4 = burst chop, tCCD=4)

A12=1, BL8

A12 will be used only for burst length control, not a column address.

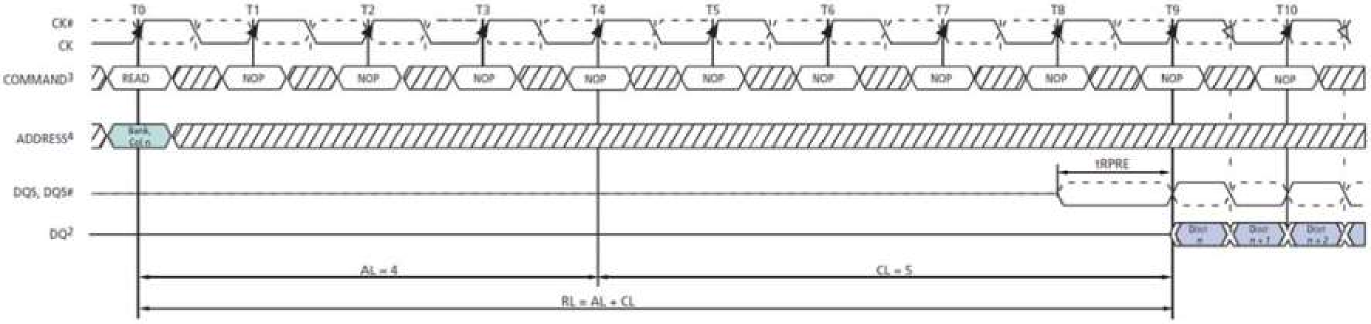
READ Burst Operation RL=5 (AL=0, CL=5, BL=8)



NOTES: 1. BL8, RL = 5, AL = 0, CL = 5.
2. Dout *n* = data-out from column *n*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T0.

⬚ TRANSITIONING DATA ▨ DON'T CARE

READ Burst Operation RL=9 (AL=4, CL=5, BL=8)



NOTES: 1. BL8, RL = 9, AL = (CL - 1), CL = 5.
2. Dout *n* = data-out from column *n*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T0.

⬚ TRANSITIONING DATA ▨ DON'T CARE

READ Timing Definitions

Read timing is shown in the following figure and is applied when the DLL is enabled and locked.

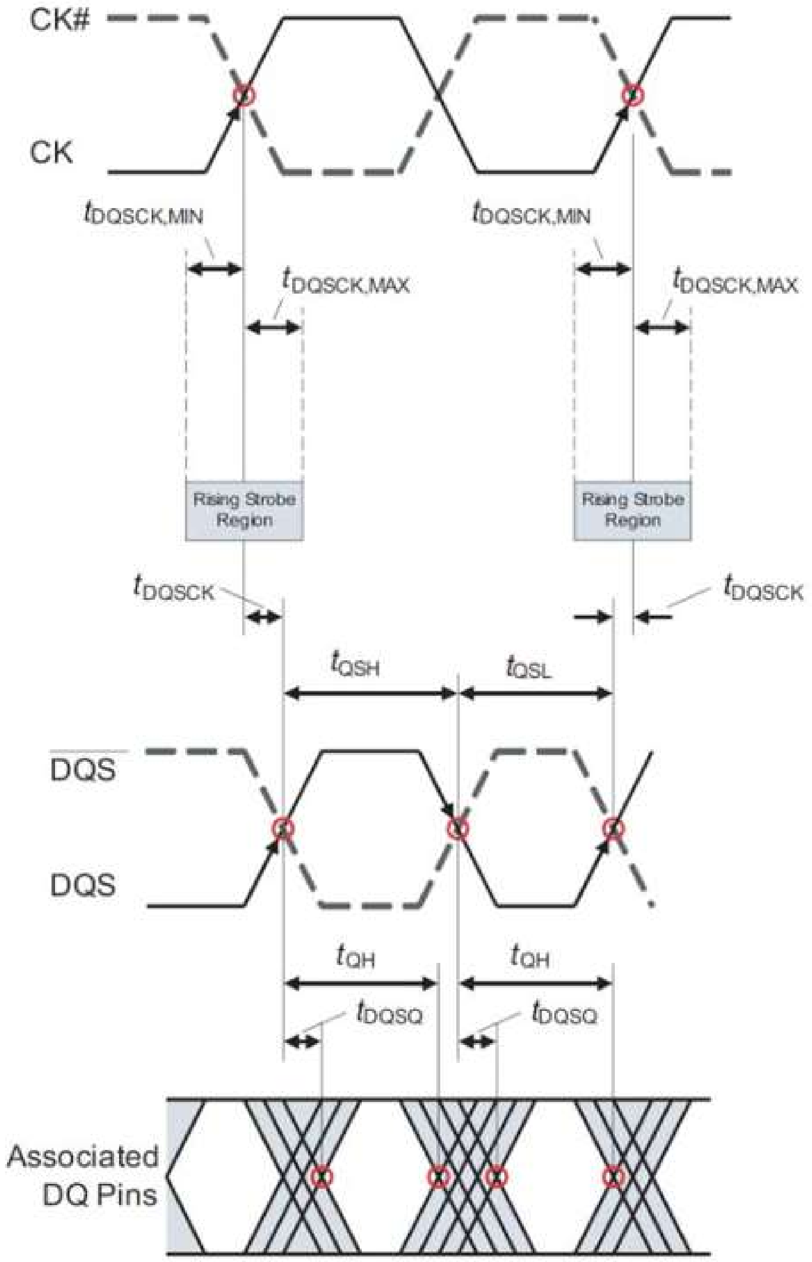
Rising data strobe edge parameters:

- tDQSCK min/max describes the allowed range for a rising data strobe edge relative to CK, CK#.
- tDQSCK is the actual position of a rising strobe edge relative to CK, CK#.
- tQSH describes the DQS, DQS# differential output high time.
- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

Falling data strobe edge parameters:

- tQSL describes the DQS, DQS# differential output low time.
- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

Reads Timing Definition



Read Timing; Clock to Data Strobe relationship

Clock to Data Strobe relationship is shown in the following figure and is applied when the DLL is enabled and locked.

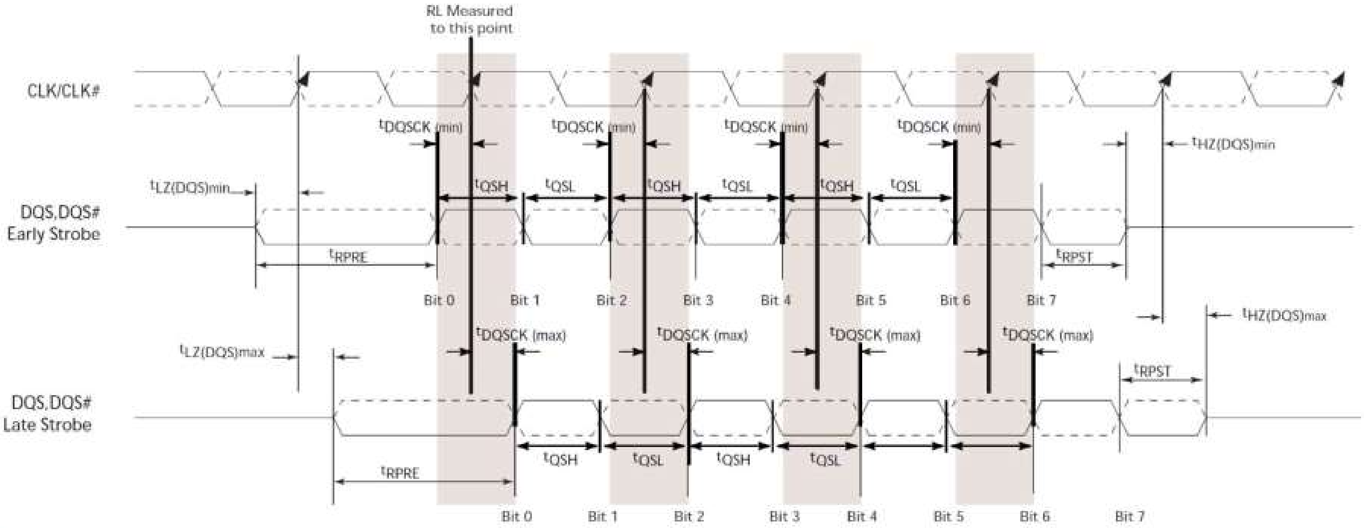
Rising data strobe edge parameters:

- tDQSCK min/max describes the allowed range for a rising data strobe edge relative to CK and CK#.
- tDQSCK is the actual position of a rising strobe edge relative to CK and CK#.
- tQSH describes the data strobe high pulse width.

Falling data strobe edge parameters:

- tQSL describes the data strobe low pulse width.

Clock to Data Strobe relationship



Notes:

1. Within a burst, rising strobe edge is not necessarily fixed to be always at tDQSCK(min) or tDQSCK(max). Instead, rising strobe edge can vary between tDQSCK(min) and tDQSCK(max).
2. The DQS, DQS# differential output high time is defined by tQSH and the DQS, DQS# differential output low time is defined by tQSL.
3. Likewise, tLZ(DQS)min and tHZ(DQS)min are not tied to tDQSCKmin (early strobe case) and tLZ(DQS)max and tHZ(DQS)max are not tied to tDQSCKmax (late strobe case).
4. The minimum pulse width of read preamble is defined by tRPRE(min).
5. The maximum read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZDSQ(max) on the right side.
6. The minimum pulse width of read postamble is defined by tRPST(min).
7. The maximum read preamble is bound by tLZDQS(min) on the left side and tDQSCK(max) on the right side

Read Timing; Data Strobe to Data Relationship

The Data Strobe to Data relationship is shown in the following figure and is applied when the DLL and enabled and locked.

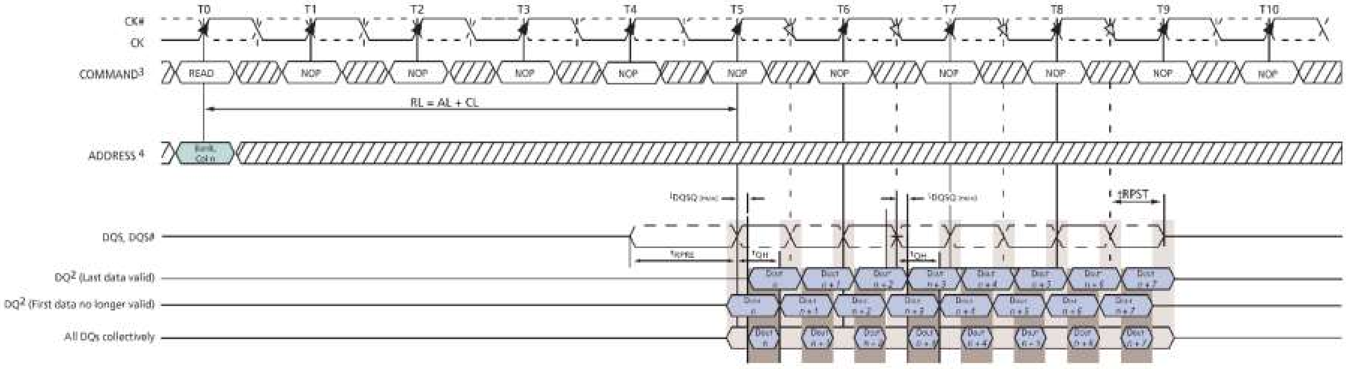
Rising data strobe edge parameters:

- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

Falling data strobe edge parameters:

- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.
- tDQSQ; both rising/falling edges of DQS, no tAC defined

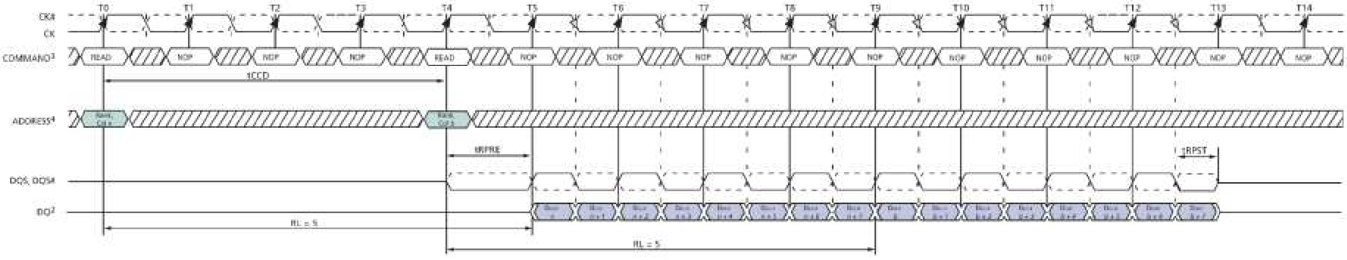
Data Strobe to Data Relationship



NOTES: 1. BL = 8, RL = 5 (AL = 0, CL = 5)
2. Dout *n* = data-out from column *n*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T0.
5. Output timings are referenced to VDDQ/2, and DLL on for locking.
6. tDQSQ defines the skew between DQS,DQS# to Data and does not define DQS,DQS# to Clock.
7. Early Data transitions may not always happen at the same DQ. Data transitions of a DQ can vary (either early or late) within a burst.

☐ TRANSITIONING DATA ▨ DON'T CARE

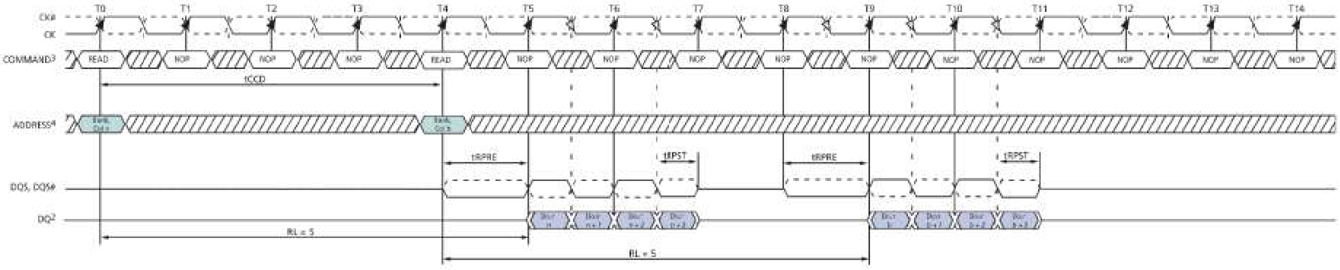
READ (BL8) to READ (BL8)



☐ TRANSITIONING DATA ▨ DON'T CARE

NOTE: 1. BL8, RL = 5 (CL = 5, AL = 0)
2. Dout *n (or b)* = data-out from column *n (or column b)*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ commands at T0 and T4.

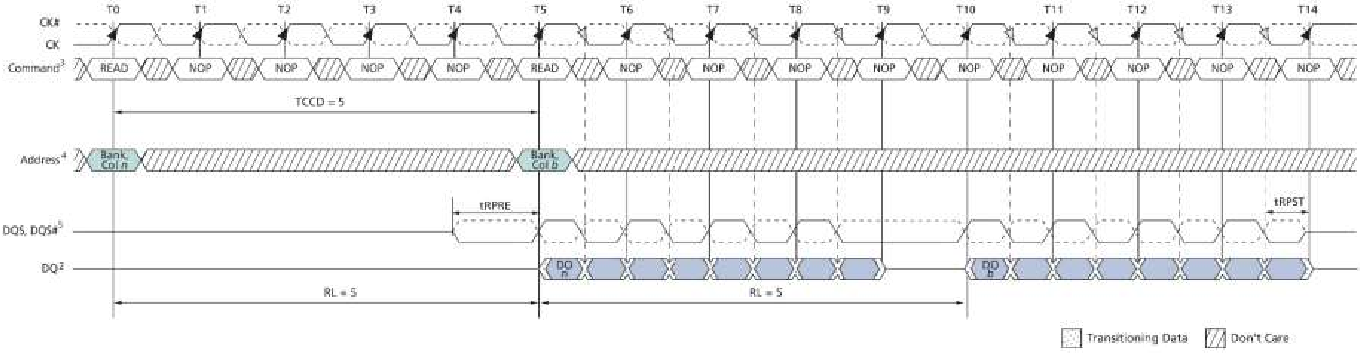
READ (BC4) to READ (BC4)



☐ TRANSITIONING DATA ▨ DON'T CARE

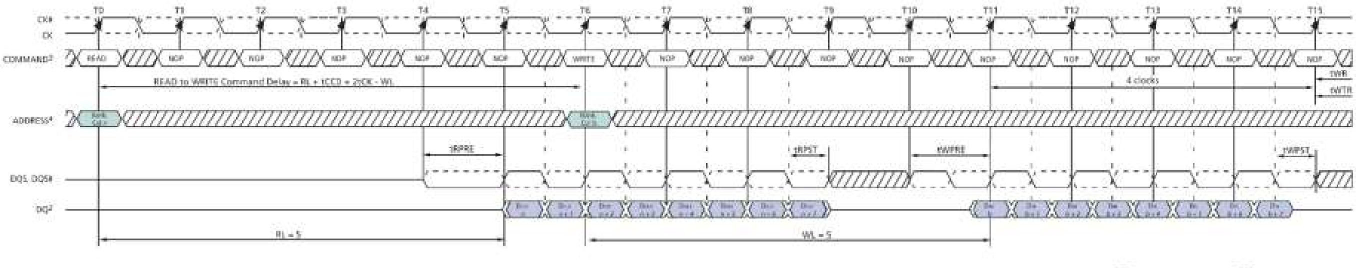
NOTE: 1. BC4, RL = 5 (CL = 5, AL = 0)
2. Dout *n (or b)* = data-out from column *n (or column b)*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by either MR0[A1:0 = 10] or MR0[A1:0 = 01] and A12 = 0 during READ commands at T0 and T4.

Nonconsecutive READ (BL8) to READ (BL8)



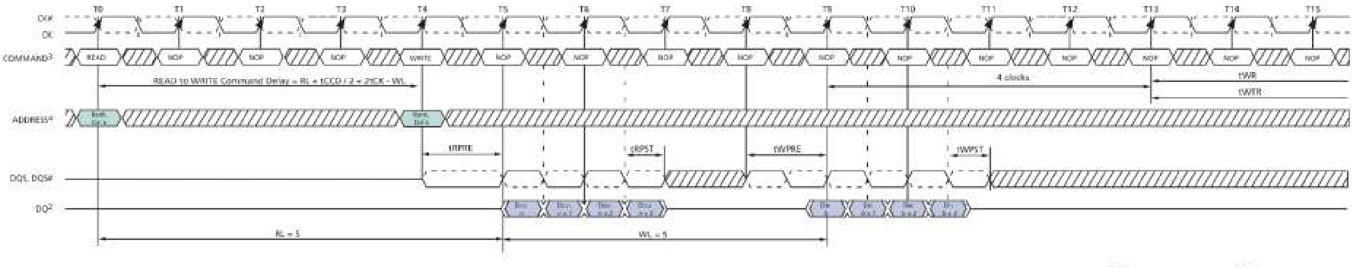
NOTE: 1. BL8, RL = 5 (CL = 5, AL = 0), tCCD=5
2. Dout n (or b) = data-out from column n (or column b).
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ commands at T0 and T4.
5. DQS-DQS# is held logic low at T9

READ (BL8) to WRITE (BL8)



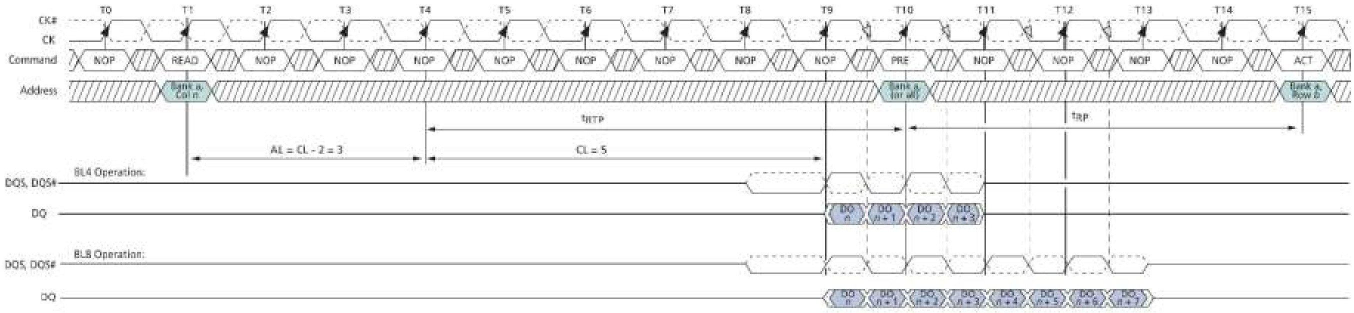
NOTE: 1. BL8, RL = 5 (CL = 5, AL = 0), WL = 5 (CWL = 5, AL = 0)
2. Dout n = data-out from column, Din b = data-in from column b.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T0 and WRITE command at T6.

READ (BC4) to WRITE (BC4) OTF



NOTE: 1. BC4, RL = 5 (CL = 5, AL = 0), WL = 5 (CWL = 5, AL = 0)
2. Dout n = data-out from column, Din b = data-in from column b.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:0 = 01] and A12 = 0 during READ command at T0 and WRITE command at T4.

READ to PRECHARGE, RL = 8, AL = CL-2, CL = 5, tRTP = 6, tRP = 5



NOTE: 1. RL = 8 (CL = 5, AL = CL - 2)
2. Dout n = data-out from column n.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. The example assumes tRAS.MIN is satisfied at Precharge command time (T10) and that tRC.MIN is satisfied at the next Active command time (T15).

4.8 Write Operation

DDR3L Burst Operatio

During a READ or WRITE command, DDR3L will support BC4 and BL8 on the fly using address A12 during the READ or WRITE (Auto Precharge can be enabled or disabled).
A12=0, BC4 (BC4 = Burst Chop, tCCD=4)
A12=1, BL8
A12 is used only for burst length control, not as a column address.

Write Timing Violations

Motivation

Generally, if timing parameters are violated, a complete reset/initialization procedure has to be initiated to make sure the DRAM works properly. However, it is desirable for certain minor violations that the DRAM is guaranteed not to “hang up” and errors be limited to that particular operation.

For the following, it will be assumed that there are no timing violations with regard to the Write command itself (including ODT, etc.) and that it does satisfy all timing requirements not mentioned below.

Data Setup and Hold Violations

Should the strobe timing requirements (tDS, tDH) be violated, for any of the strobe edges associated with a write burst, then wrong data might be written to the memory location addressed with the offending WRITE command.

Subsequent reads from that location might result in unpredictable read data, however, the DRAM will work properly otherwise.

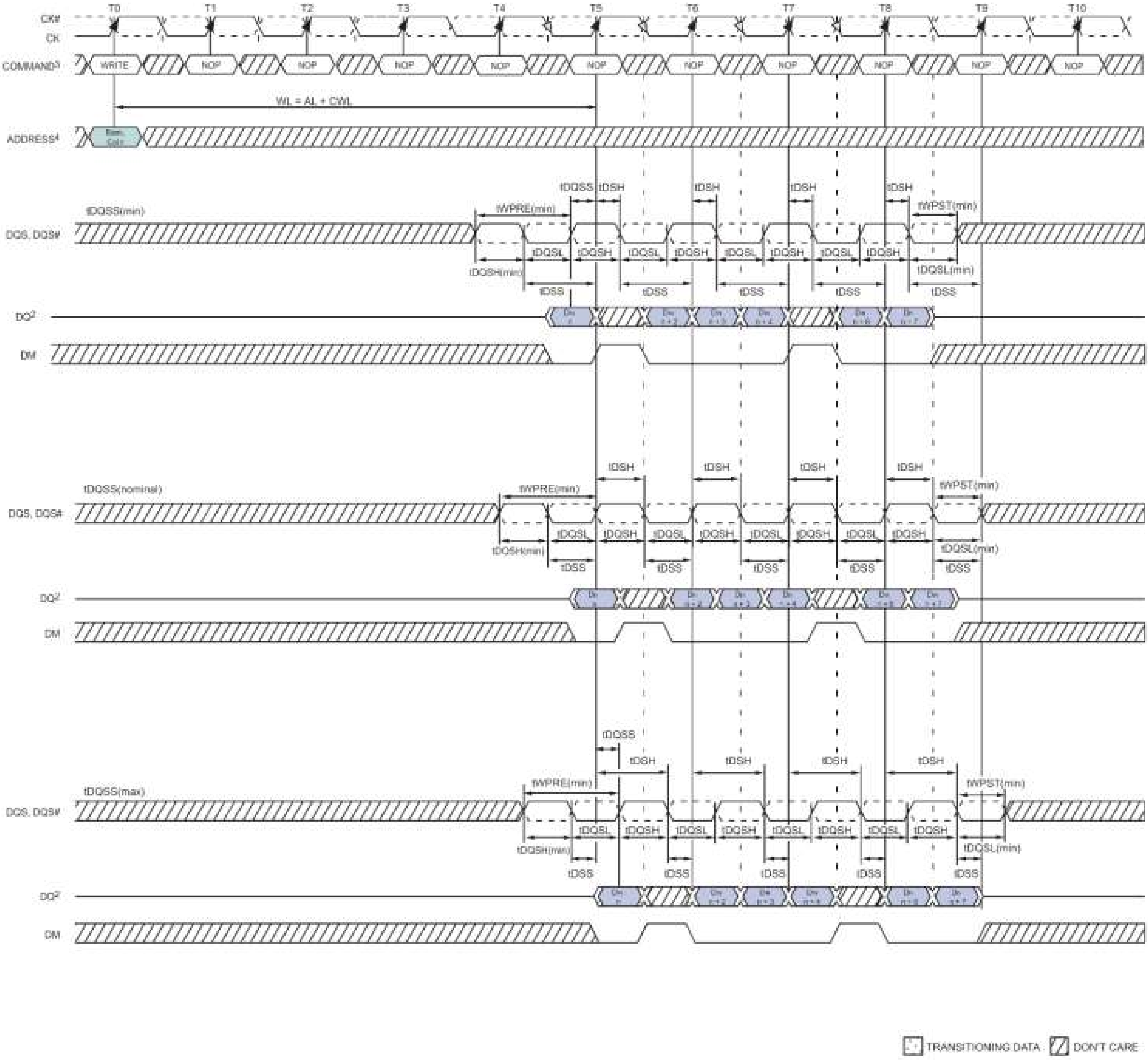
Strobe to Strobe and Strobe to Clock Violations

Should the strobe timing requirements (tDQSH, tDQSL, tWPRE, tWPST) or the strobe to clock timing requirements (tDSS, tDSH, tDQSS) be violated, for any of the strobe edges associated with a Write burst, then wrong data might be written to the memory location addressed with the offending WRITE command. Subsequent reads from that location might result in unpredictable read data, however the DRAM will work properly otherwise.

Write Timing Parameters

This drawing is for example only to enumerate the strobe edges that “belong” to a write burst. No actual timing violations are shown here. For a valid burst all timing parameters for each edge of a burst need to be satisfied (not only for one edge - as shown).

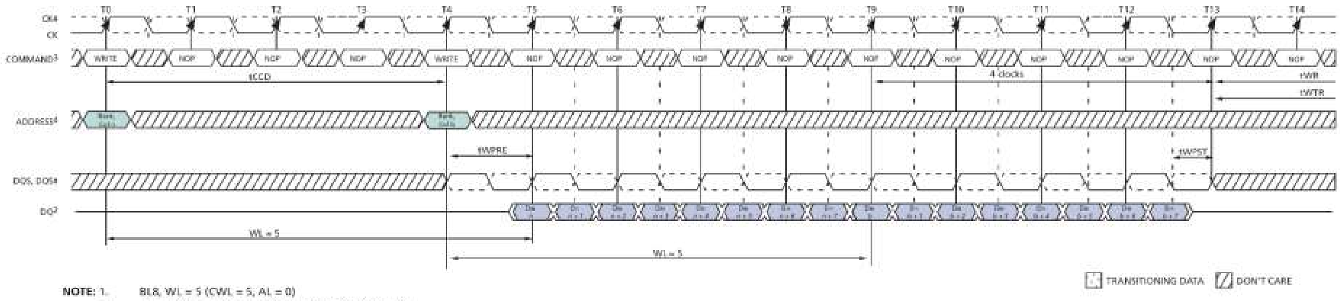
Write Timing Definition



Notes:

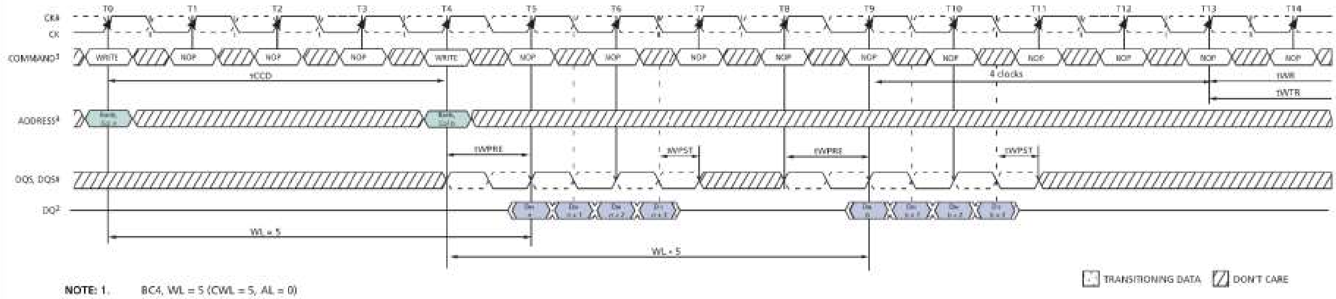
1. BL=8, WL=5 (AL=0, CWL=5).
2. Din n = data in from column n.
3. NOP commands are shown for ease of illustration; other command may be valid at these times.
4. BL8 setting activated by either MR0 [A1:0=00] or MR0 [A1:0=01] and A12 = 1 during WRITE command at T0.
5. tDQSS must be met at each rising clock edge.

WRITE (BL8) to WRITE (BL8)



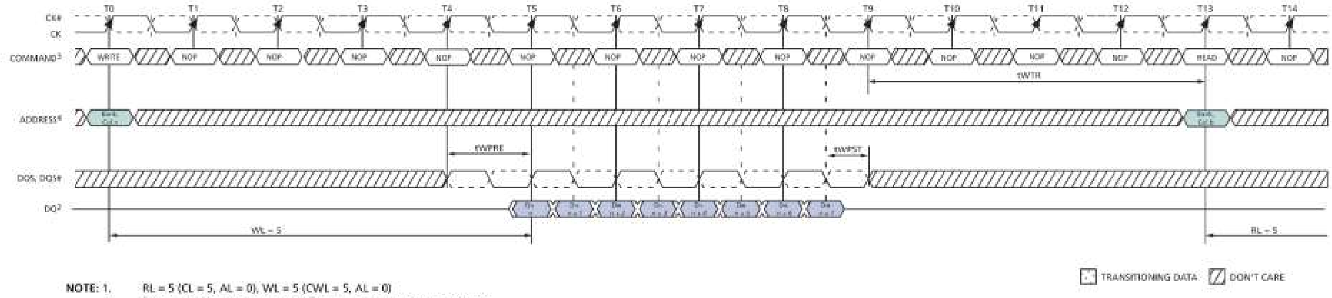
NOTE: 1. BL8, WL = 5 (CWL = 5, AL = 0)
2. D_{IN} *n (or b)* = data-in from column *n (or column b)*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during WRITE command at T0 and T4.
5. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T13.

WRITE (BC4) to WRITE (BC4) OTF



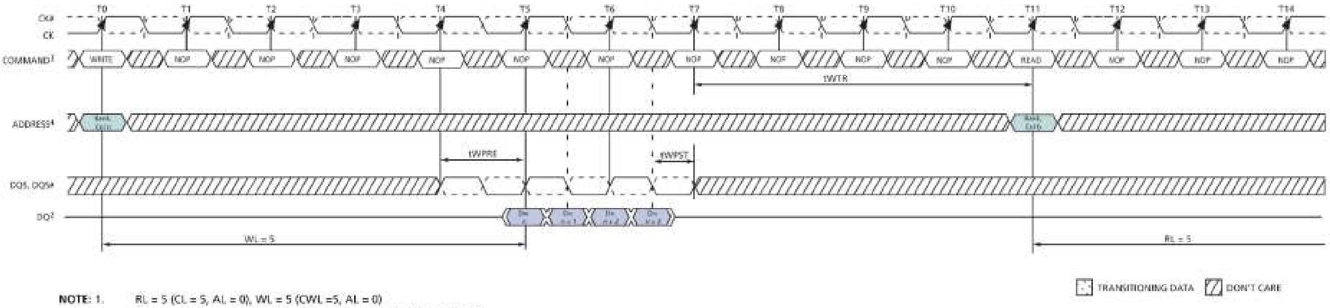
NOTE: 1. BC4, WL = 5 (CWL = 5, AL = 0)
2. D_{IN} *n (or b)* = data-in from column *n (or column b)*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:0 = 01] and A12 = 0 during WRITE command at T0 and T4.
5. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge at T13 (4 clocks from T9).

WRITE (BL8) to READ (BC4/BL8) OTF



NOTE: 1. RL = 5 (CL = 5, AL = 0), WL = 5 (CWL = 5, AL = 0)
2. D_{IN} *n* = data-in from column *n*; D_{OUT} *b* = data-out from column *b*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during WRITE command at T0. READ command at T13 can be either BC4 or BL8 depending on MR0[A1:0] and A12 status at T13.

WRITE (BC4) to READ (BC4)



NOTE: 1. RL = 5 (CL = 5, AL = 0), WL = 5 (CWL =5, AL = 0)
2. D_{IN} *n* = data-in from column *n*; D_{OUT} *b* = data-out from column *b*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:0 = 10].

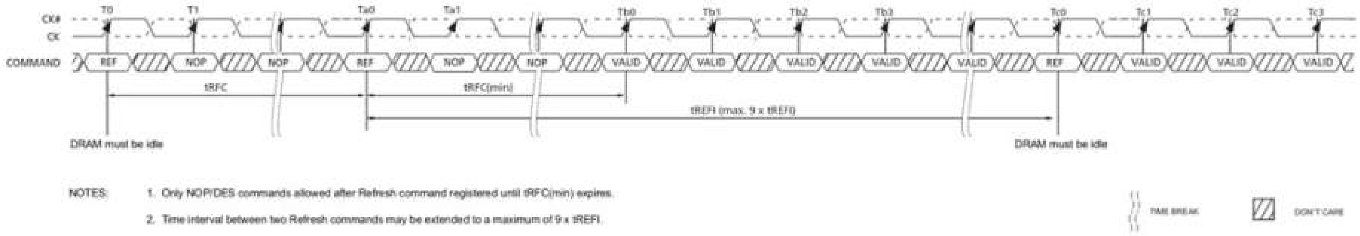
Refresh Command

The Refresh command (REF) is used during normal operation of the DDR3 SDRAMs. This command is not persistent, so it must be issued each time a refresh is required. The DDR3 SDRAM requires Refresh cycles at an average periodic interval of tREFI. When CS#, RAS#, and CAS# are held Low and WE# High at the rising edge of the clock, the chip enters a Refresh cycle. All banks of the SDRAM must be precharged and idle for a minimum of the precharge time tRP(min) before the Refresh Command can be applied. The refresh addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during a Refresh command. An internal address counter suppliers the address during the refresh cycle. No control of the external address bus is required once this cycle has started. When the refresh cycle has completed, all banks of the SDRAM will be in the precharged (idle) state. A delay between the Refresh Command and the next valid command, except NOP or DES, must be greater than or equal to the minimum Refresh cycle time tRFC(min) as shown in the following figure.

In general, a Refresh command needs to be issued to the DDR3L SDRAM regularly every tREFI interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided.

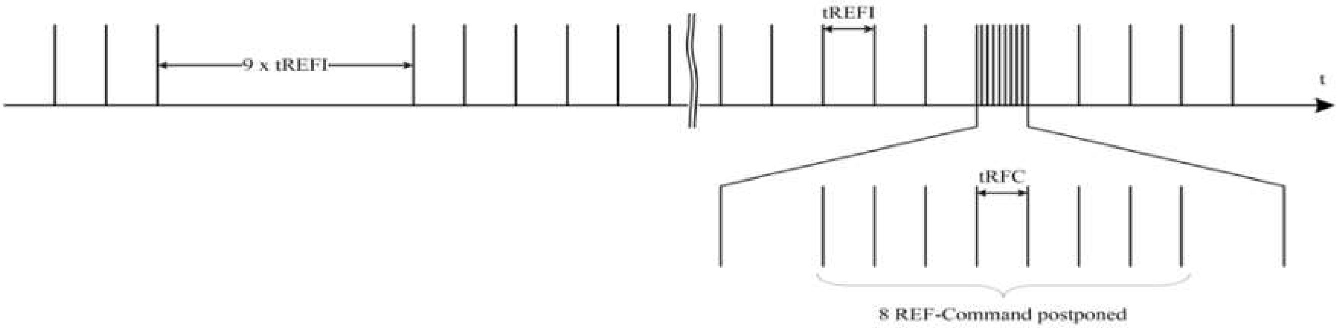
A maximum of 8 Refresh commands can be postponed during operation of the DDR3L SDRAM, meaning that at no point in time more than a total of 8 Refresh commands are allowed to be postponed. In case that 8 Refresh commands are postponed in a row, the resulting maximum interval between the surrounding Refresh commands is limited to 9 x tREFI. A maximum of 8 additional Refresh commands can be issued in advance ("pulled in"), with each one reducing the number of regular Refresh commands required later by one. Note that pulling in more than 8 Refresh commands in advance does not further reduce the number of regular Refresh commands required later, so that the resulting maximum interval between two surrounding Refresh command is limited to 9 x tREFI. Before entering Self-Refresh Mode, all postponed Refresh commands must be executed.

Self-Refresh Entry/Exit Timing

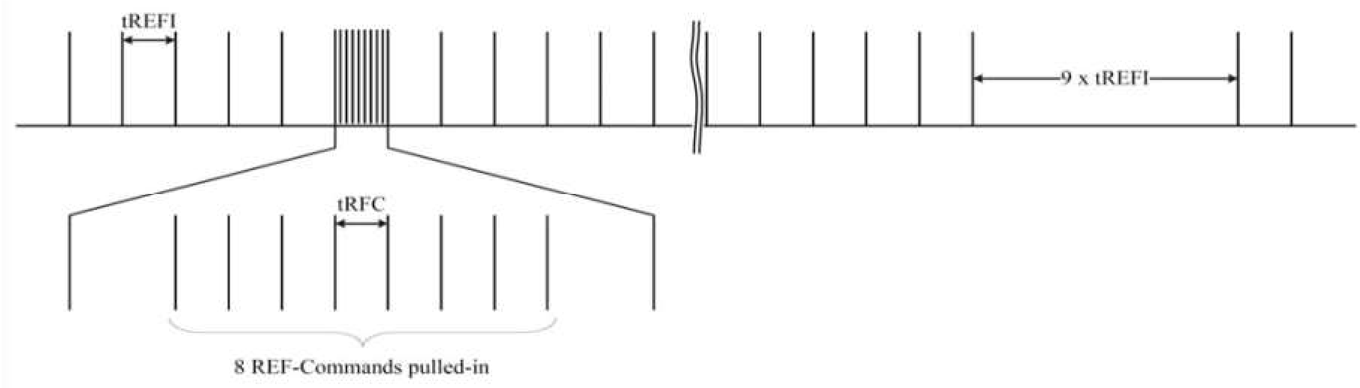


NOTES:
1. Only NOP/DES commands allowed after Refresh command registered until tRFC(min) expires.
2. Time interval between two Refresh commands may be extended to a maximum of 9 x tREFI.

Postponing Refresh Commands (Example)



Pulled-in Refresh Commands (Example)



Self-Refresh Operation

The Self-Refresh command can be used to retain data in the DDR3L SDRAM, even if the reset of the system is powered down. When in the Self-Refresh mode, the DDR3L SDRAM retains data without external clocking. The DDR3L SDRAM device has a built-in timer to accommodate Self-Refresh operation. The Self-Refresh Entry (SRE) Command is defined by having CS#, RAS#, CAS#, and CKE held low with WE# high at the rising edge of the clock.

Before issuing the Self-Refreshing-Entry command, the DDR3L SDRAM must be idle with all bank precharge state with tRP satisfied. Also, on-die termination must be turned off before issuing Self-Refresh-Entry command, by either registering ODT pin low “ODTL + 0.5tCK” prior to the Self-Refresh Entry command or using MRS to MR1 command. Once the Self-Refresh Entry command is registered, CKE must be held low to keep the device in Self-Refresh mode. During normal operation (DLL on), MR1 (A0=0), the DLL is automatically disabled upon entering Self- Refresh and is automatically enabled (including a DLL-RESET) upon exiting Self-Refresh.

When the DDR3L SDRAM has entered Self-Refresh mode, all of the external control signals, except CKE and RESET#, are “don’t care”. For proper Self-Refresh operation, all power supply and reference pins (VDD, VDDQ, VSS, VSSQ, VRefCA, and VRefDQ) must be at valid levels. The DRAM initiates a minimum of one Refresh command internally within tCKE period once it enters Self-Refresh mode.

The clock is internally disabled during Self-Refresh operation to save power. The minimum time that the DDR3L SDRAM must remain in Self-Refresh mode is tCKE. The user may change the external clock frequency or halt the external clock tCKSRE after Self-Refresh entry is registered; however, the clock must be restarted and stable tCKSRX before the device can exit Self-Refresh mode.

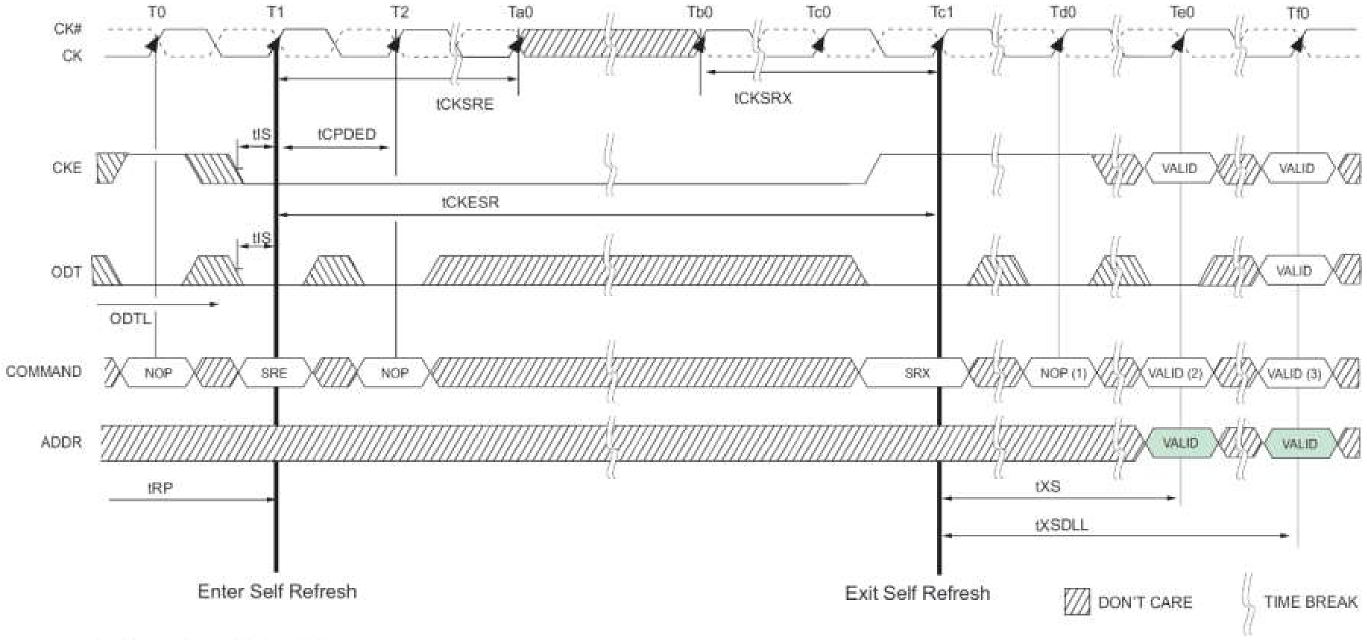
The procedure for exiting Self-Refresh requires a sequence of events. First, the clock must be stable prior to CKE going back HIGH. Once a Self-Refresh Exit Command (SRX, combination of CKE going high and either NOP or Deselect on command bus) is registered, a delay of at least tXS must be satisfied before a valid command not requiring a locked DLL can be issued to the device to allow for any internal refresh in progress. Before a command which requires a locked DLL can be applied, a delay of at least tXSDLL and applicable ZQCAL function requirements must be satisfied.

Before a command that requires a locked DLL can be applied, a delay of at least tXSDLL must be satisfied. Depending on the system environment and the amount of time spent in Self-Refresh, ZQ calibration commands may be required to compensate for the voltage and temperature drift as described in “ZQ Calibration Commands”. To issue ZQ calibration commands, applicable timing requirements must be satisfied.

CKE must remain HIGH for the entire Self-Refresh exit period tXSDLL for proper operation except for Self- Refresh re-entry. Upon exit from Self-Refresh, the DDR3(L) SDRAM can be put back into Self-Refresh mode after waiting at least tXS period and issuing one refresh command (refresh period of tRFC). NOP or deselect commands must be registered on each positive clock edge during the Self-Refresh exit interval tXS. ODT must be turned off during tXSDLL.

The use of Self-Refresh mode instructs the possibility that an internally times refresh event can be missed when CKE is raised for exit from Self-Refresh mode. Upon exit from Self-Refresh, the DDR3(L) SDRAM requires a minimum of one extra refresh command before it is put back into Self-Refresh mode.

Self-Refresh Entry/Exit Timing



NOTES:
1. Only NOP or DES command.
2. Valid commands not requiring a locked DLL.
3. Valid commands requiring a locked DLL.

4.9 Power-Down Modes

Power-Down Entry and Exit

Power-Down is synchronously entered when CKE is registered low (along with NOP or Deselect command). CKE is not allowed to go low while mode register set command, MPR operations, ZQCAL operations, DLL locking or read/write operation are in progress. CKE is allowed to go low while any of other operation such as row activation, precharge or auto precharge and refresh are in progress, but power-down IDD spec will not be applied until finishing those operation.

The DLL should be in a locked state when power-down is entered for fastest power-down exit timing. If the DLL is not locked during power-down entry, the DLL must be reset after exiting power-down mode for proper read operation and synchronous ODT operation. DRAM design provides all AC and DC timing and voltage specification as well proper DLL operation with any CKE intensive operations as long as DRAM controller complies with DRAM specifications.

During Power-Down, if all banks are closed after any in progress commands are completed, the device will be in precharge Power-Down mode; if any bank is open after in progress commands are completed, the device will be in active Power-Down mode.

Entering Power-down deactivates the input and output buffers, excluding CK, CK, ODT, CKE, and RESET#. To protect DRAM internal delay on CKE line to block the input signals, multiple NOP or Deselect commands are needed during the CKE switch off and cycle(s) after, this timing period are defined as tCPDED. CKE_low will result in deactivation of command and address receivers after tCPDED has expired.

Power-Down Entry Definitions

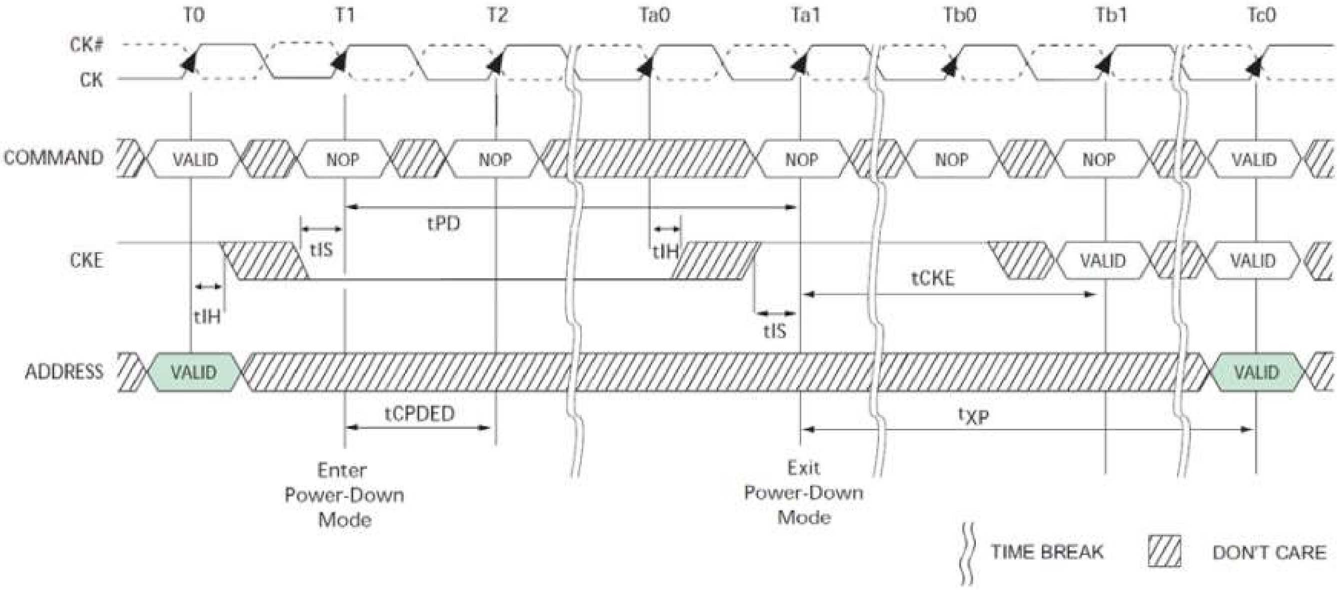
Status of DRAM	MRS bit A12	DLL	PD Exit	Relevant Parameters
Active (A Bank or more open)	Don't Care	On	Fast	tXP to any valid command.
Precharged (All Banks Precharged)	0	off	Slow	tXP to any valid command. Since it is in precharge state, commands here will be ACT, AR, MRS/EMRS, PR or PRA. tXPDLL to commands who need DLL to operate, such as RD, RDA or ODT control line.
Precharged (All Banks Precharged)	1	off	Fast	tXP to any valid command.

Also the DLL is disabled upon entering precharge power-down (Slow Exit Mode), but the DLL is kept enabled during precharge power-down (Fast Exit Mode) or active power-down. In power-down mode, CKE low, RESET# high, and a stable clock signal must be maintained at the inputs of the DD3 SDRAM, and ODT should be in a valid state but all other input signals are “Don’t care” (If RESET# goes low during Power-Down, the DRAM will be out of PD mode and into reset state).

CKE low must be maintain until tCKE has been satisfied. Power-down duration is limited by 9 times tREFI of the device.

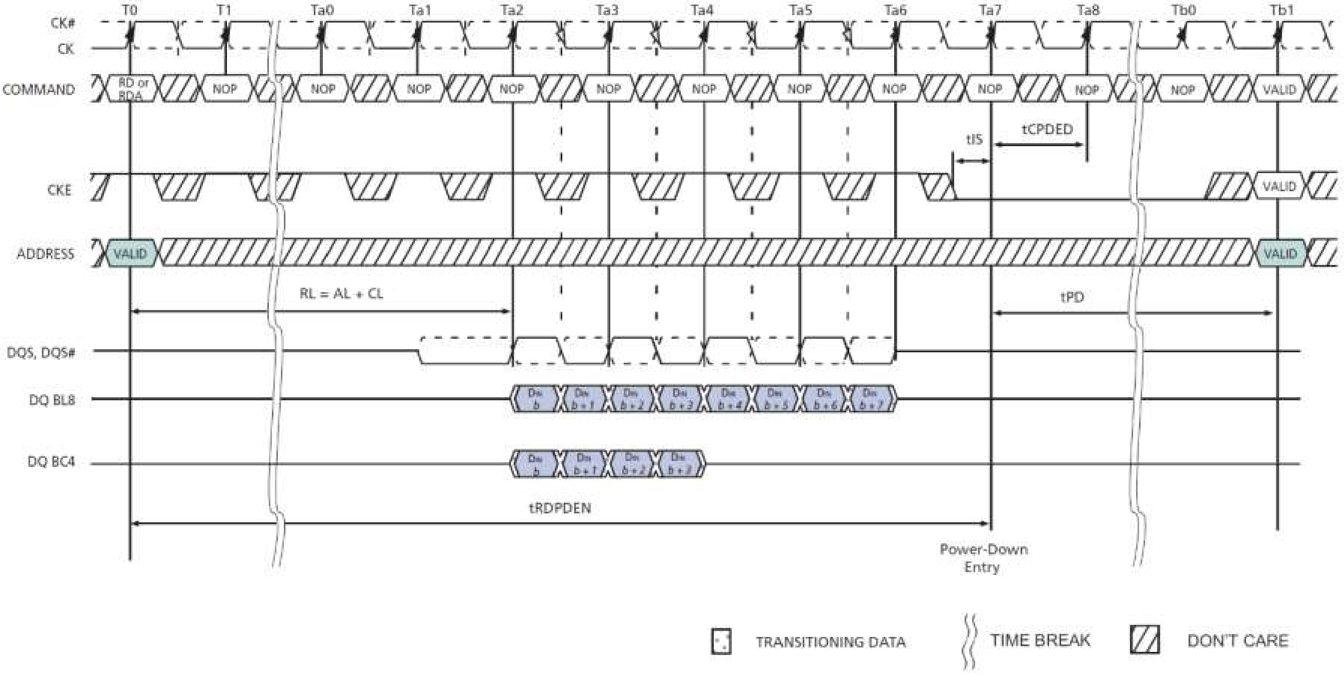
The power-down state is synchronously exited when CKE is registered high (along with a NOP or Deselect command).CKE high must be maintained until tCKE has been satisfied. A valid, executable command can be applied with power-down exit latency, tXP and/or tXPDLL after CKE goes high. Power-down exit latency is defined at AC spec table of this datasheet.

Active Power-Down Entry and Exit timing diagram

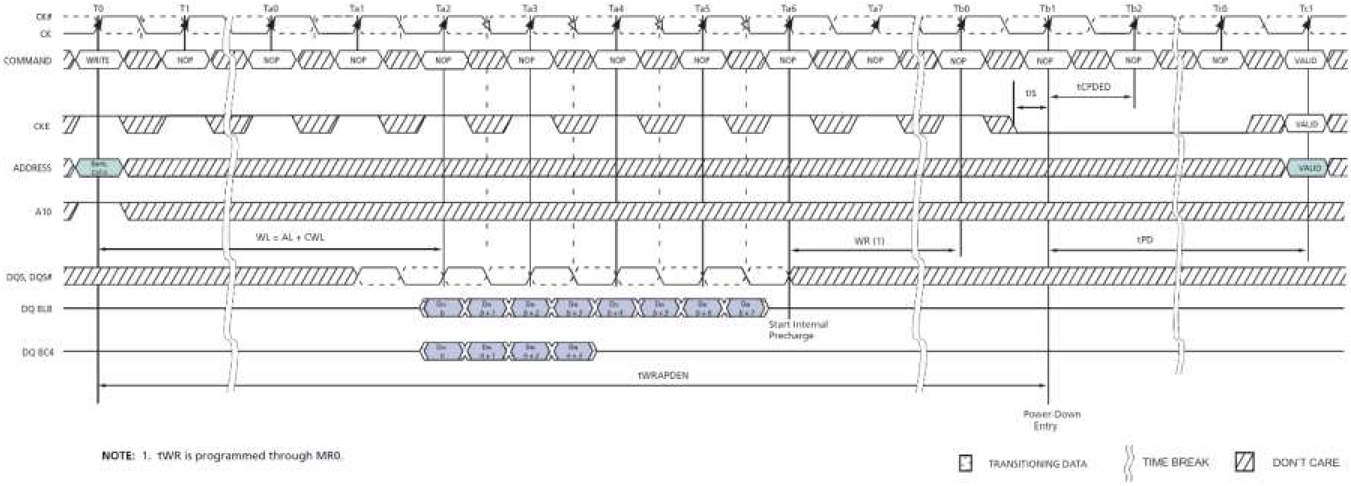


Timing Diagrams for CKE with PD Entry, PD Exit with Read, READ with Auto Precharge, Write and Write with Auto Precharge, Activate, Precharge, Refresh, MRS:

Power-Down Entry after Read and Read with Auto Precharge

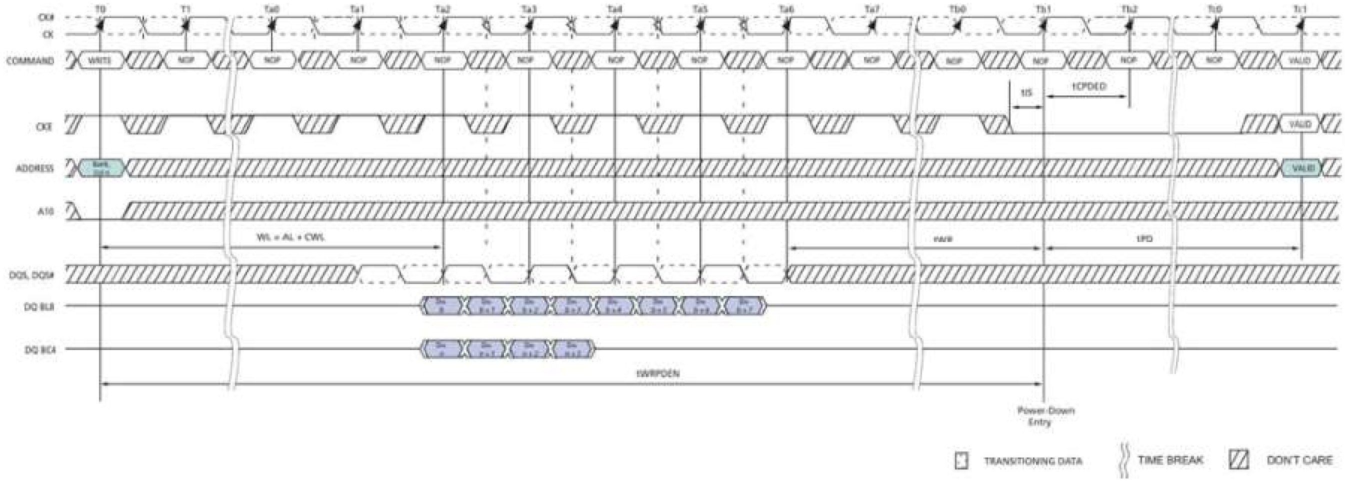


Power-Down Entry after Write with Auto Precharge

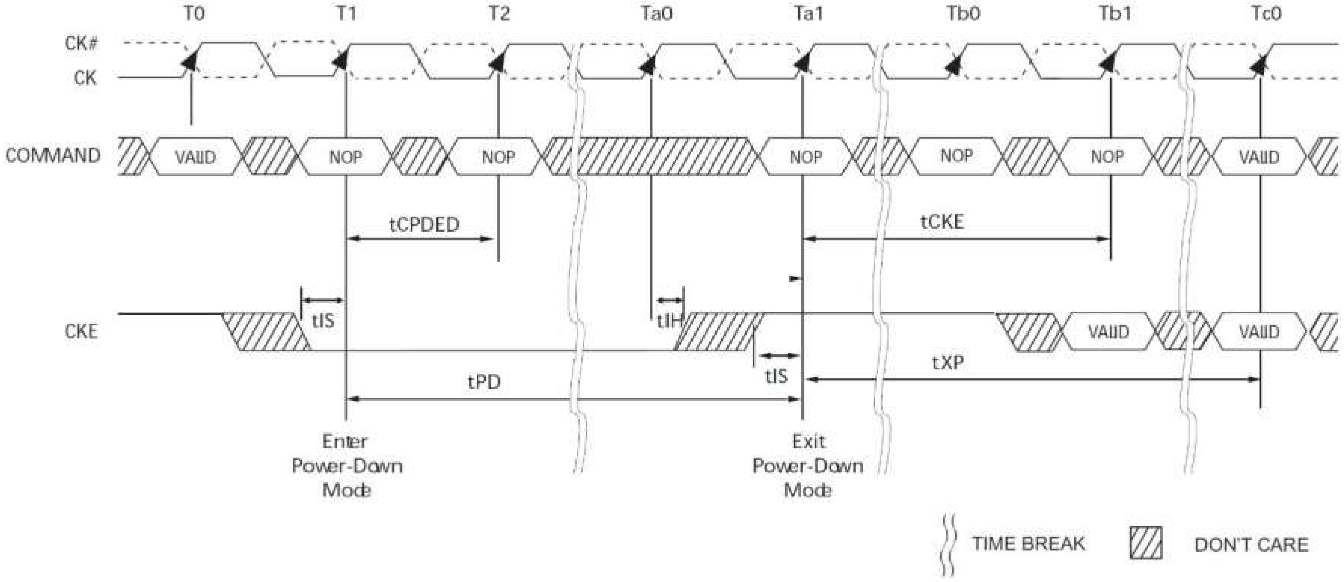


NOTE: 1. tWR is programmed through MR0.

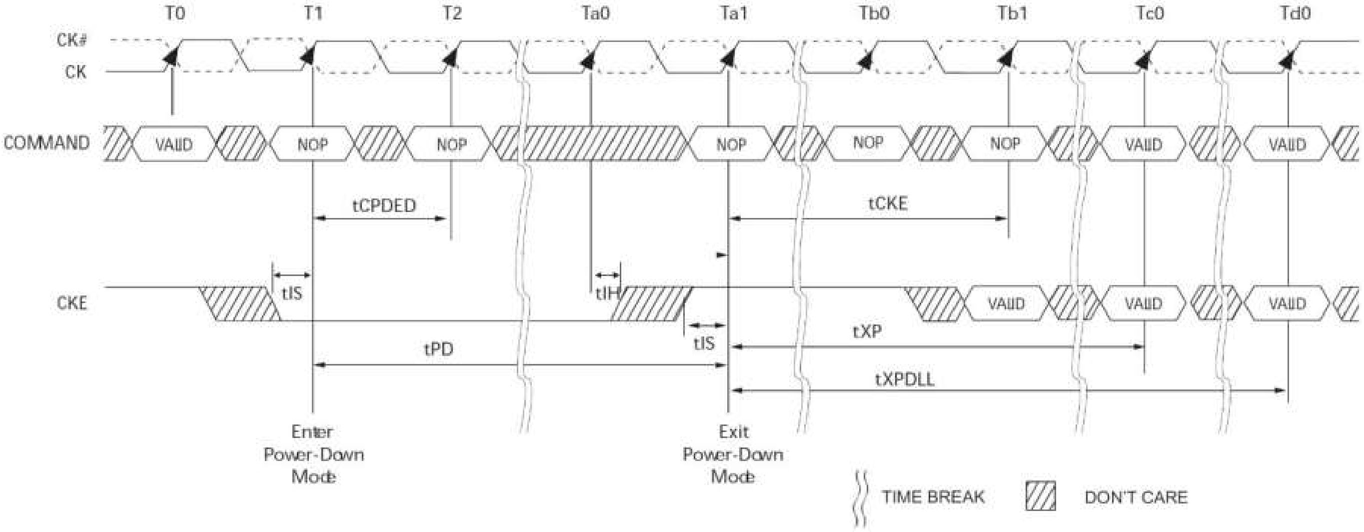
Power-Down Entry after Write



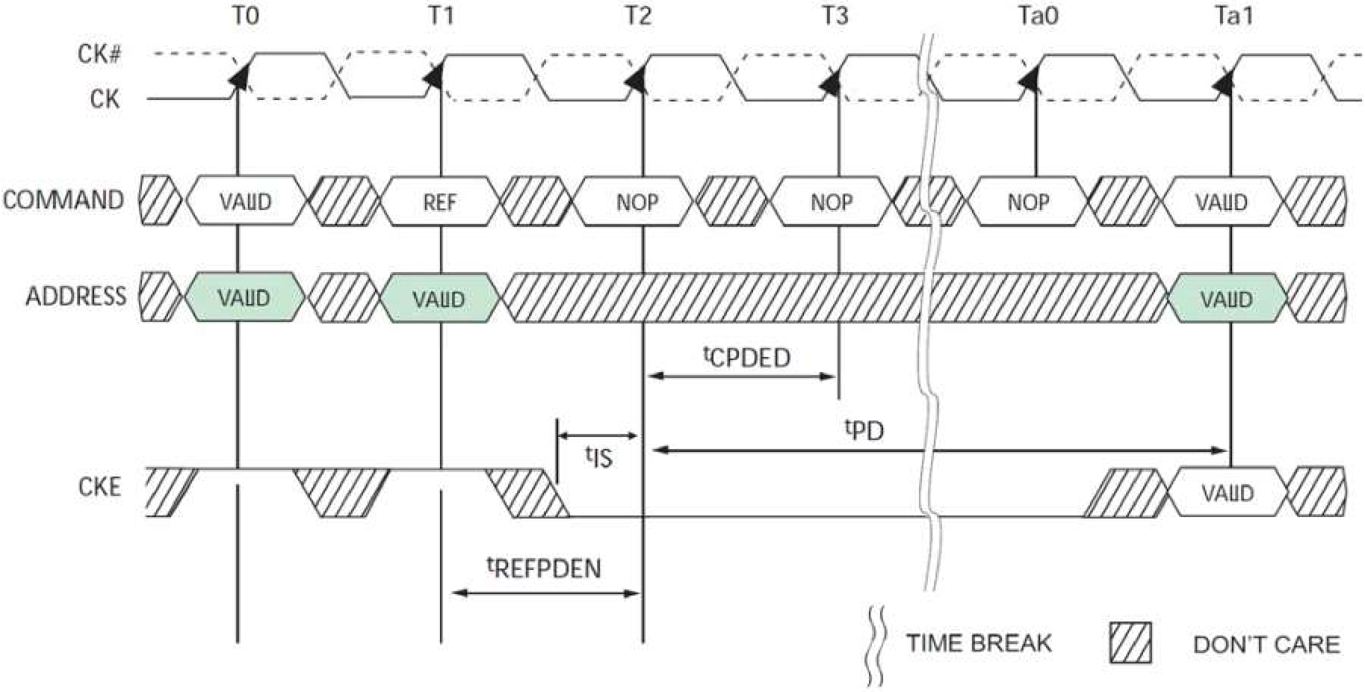
Precharge Power-Down (Fast Exit Mode) Entry and Exit



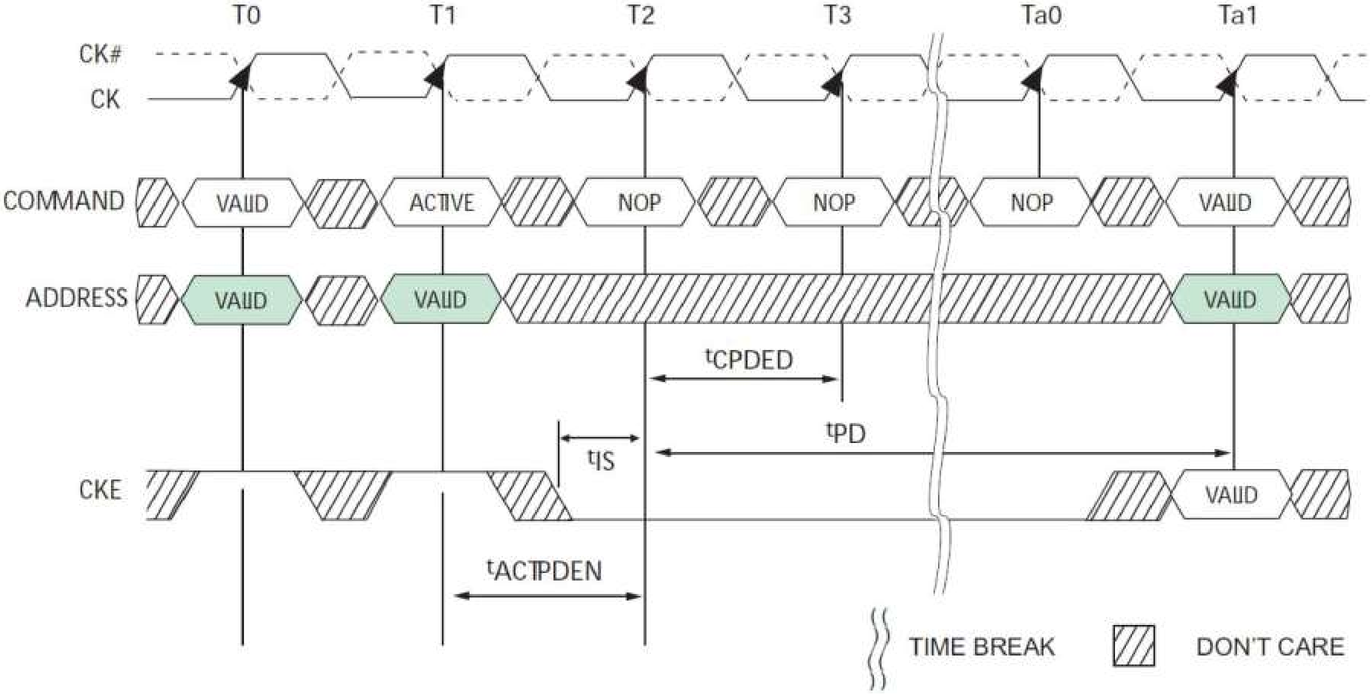
Precharge Power-Down (Slow Exit Mode) Entry and Exit



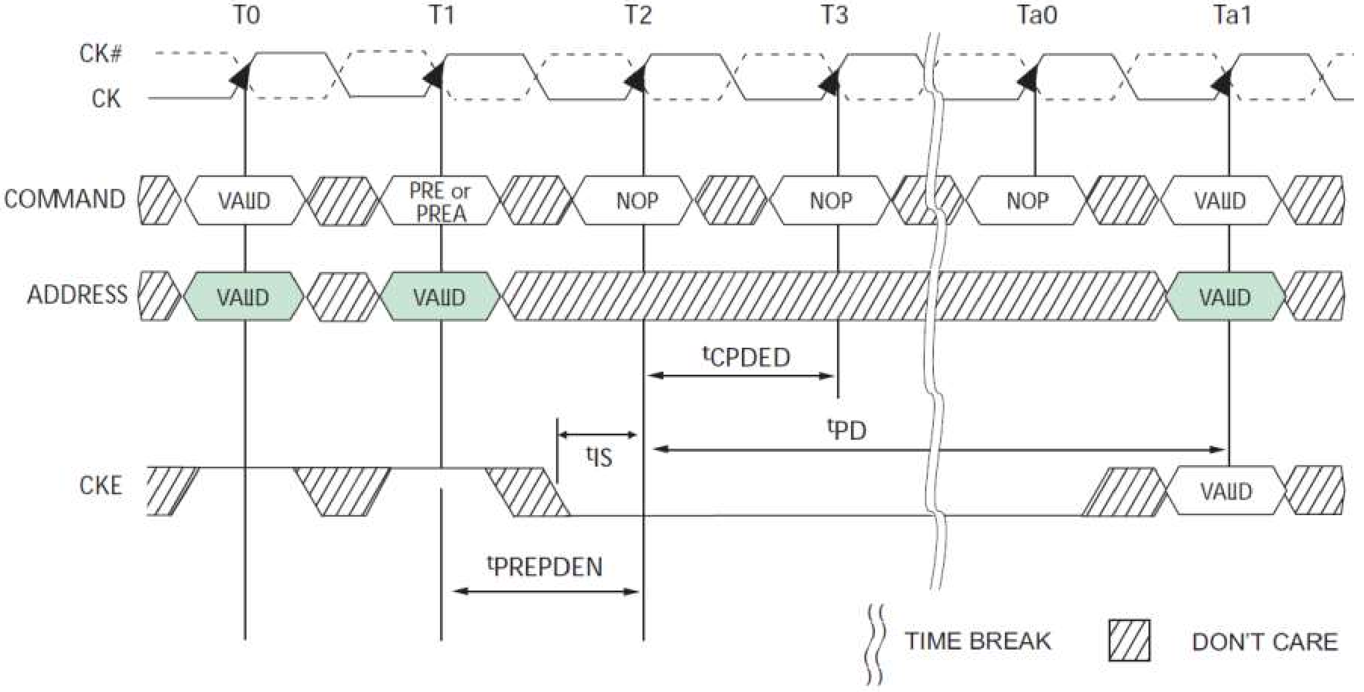
Refresh Command to Power-Down Entry



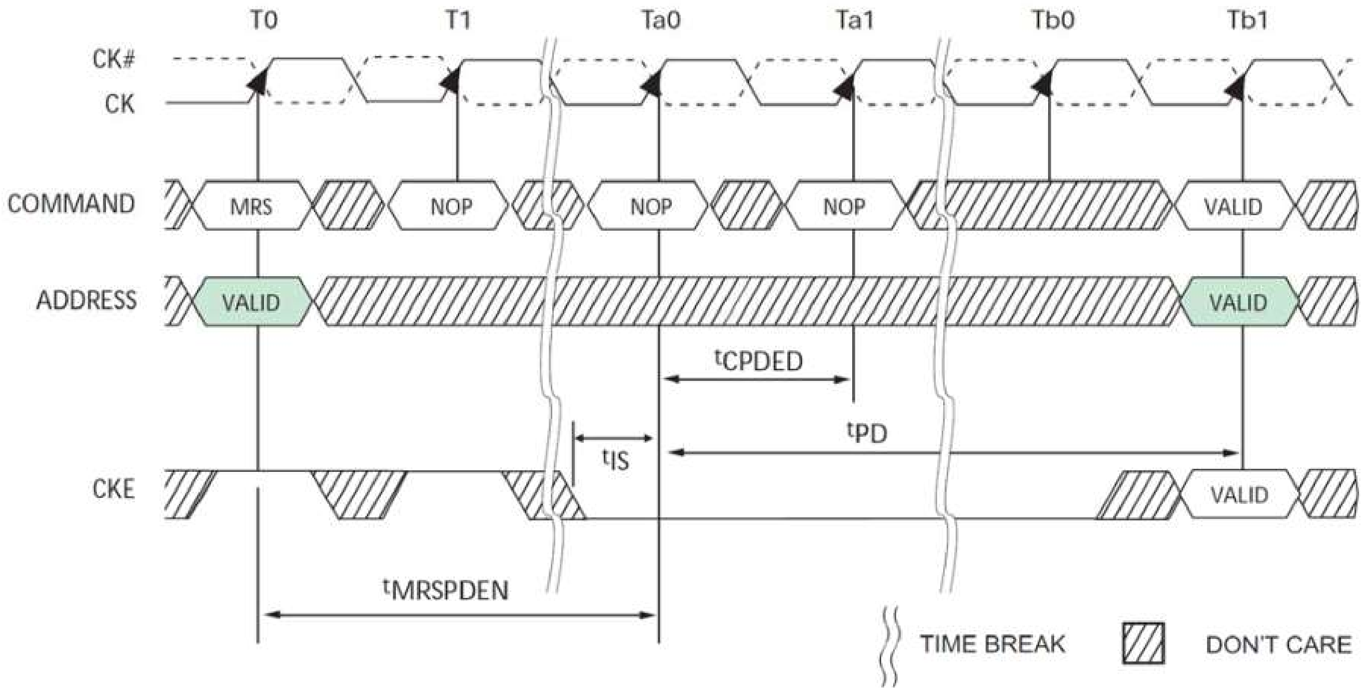
Active Command to Power-Down Entry



Precharge/Precharge all Command to Power-Down Entry



MRS Command to Power-Down Entry



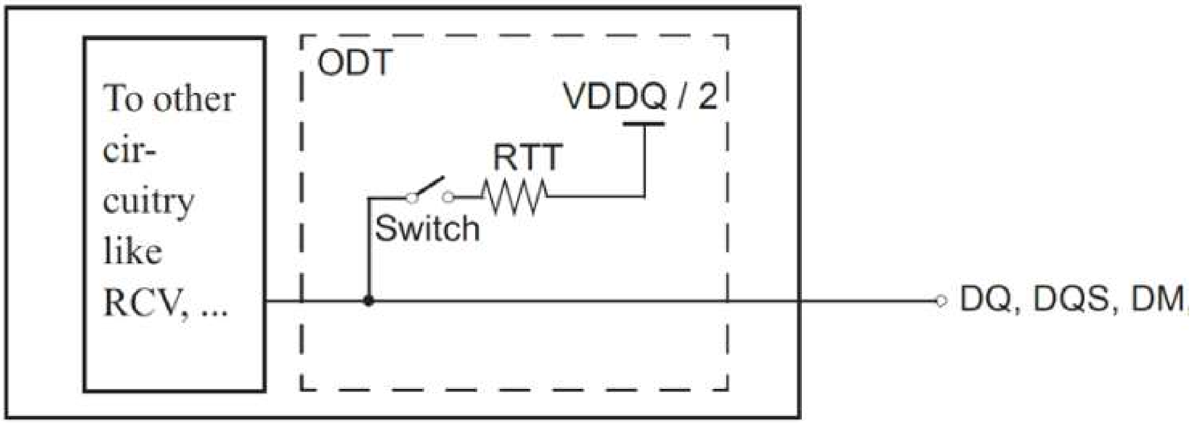
4.10 On-Die Termination (ODT)

ODT (On-Die Termination) is a feature of the DDR3L SDRAM that allows the DRAM to turn on/off termination resistance. For x16 configuration, ODT is applied to each DQU, DQL, DQSU, DQSU#, DQSL, DQSL#, DMU and DML signal via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.

The ODT feature is turned off and not supported in Self-Refresh mode.

A simple functional representation of the DRAM ODT feature is shown as below.

Functional representation of ODT



The switch is enabled by the internal ODT control logic, which uses the external ODT pin and other control information. The value of RTT is determined by the settings of Mode Register bits. The ODT pin will be ignored if the Mode Register MR1 and MR2 are programmed to disable ODT and in self-refresh mode.

ODT Mode Register and ODT Truth Table

The ODT Mode is enabled if either of MR1 {A2, A6, A9} or MR2 {A9, A10} are non-zero. In this case, the value of RTT is determined by the settings of those bits.

Application: Controller sends WR command together with ODT asserted.

One possible application: The rank that is being written to provides termination.

DRAM turns ON termination if it sees ODT asserted (except ODT is disabled by MR)
DRAM does not use any write or read command decode information.

Termination Turth Table

ODT pin	DRAM Termination State
0	OFF
1	On, (Off, if disabled by MR1 (A2, A6, A9) and MR2 (A9, A10) in gereral)

Synchronous ODT Mode

Synchronous ODT mode is selected whenever the DLL is turned on and locked. Based on the powerdown definition, these modes are:

- Any bank active with CKE high
- Refresh with CKE high
- Idle mode with CKE high
- Active power down mode (regardless of MR0 bit A12)
- Precharge power down mode if DLL is enabled during precharge power down by MR0 bit A12

The direct ODT feature is not supported during DLL-off mode. The on-die termination resistors must be disabled by continuously registering the ODT pin low and/or by programming the RTT_Nom bits MR1{A9,A6,A2} to {0,0,0} via a mode register set command during DLL-off mode.

In synchronous ODT mode, RTT will be turned on ODTLon clock cycles after ODT is sampled high by a rising clock edge and turned off ODTLoff clock cycles after ODT is registered low by a rising clock edge. The ODT latency is tied to the write latency (WL) by: ODTLon = WL - 2; ODTLoff = WL-2.

ODT Latency and Posted ODT

In synchronous ODT Mode, the Additive Latency (AL) programmed into the Mode Register (MR1) also applies to the ODT signal. The DRAM internal ODT signal is delayed for a number of clock cycles defined by the Additive Latency (AL) relative to the external ODT signal. ODTLon = CWL + AL - 2; ODTLoff = CWL + AL - 2. For details, refer to DDR3L SDRAM latency definitions.

ODT Latency

Symbol	Parameter	DDR3L-1066	DDR3L-1333	DDR3L-1600	DDR3L-1866	Unit
ODTLon	ODT turn on Latency	WL - 2 = CWL + AL - 2				tCK
ODTLoff	ODT turn off Latency	WL - 2 = CWL + AL - 2				tCK

Timing Parameters

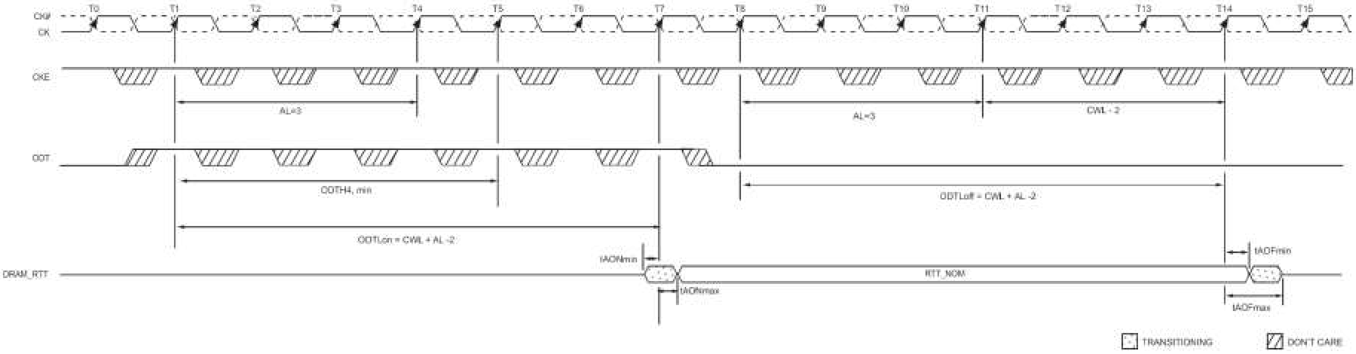
In synchronous ODT mode, the following timing parameters apply: ODTLon, ODTLoff, tAON min/max, tAOF min/max.

Minimum RTT turn-on time (tAON min) is the point in time when the device leaves high impedance and ODT resistance begins to turn on. Maximum RTT turn-on time (tAON max) is the point in time when the ODT resistance is fully on. Both are measured from ODTLon.

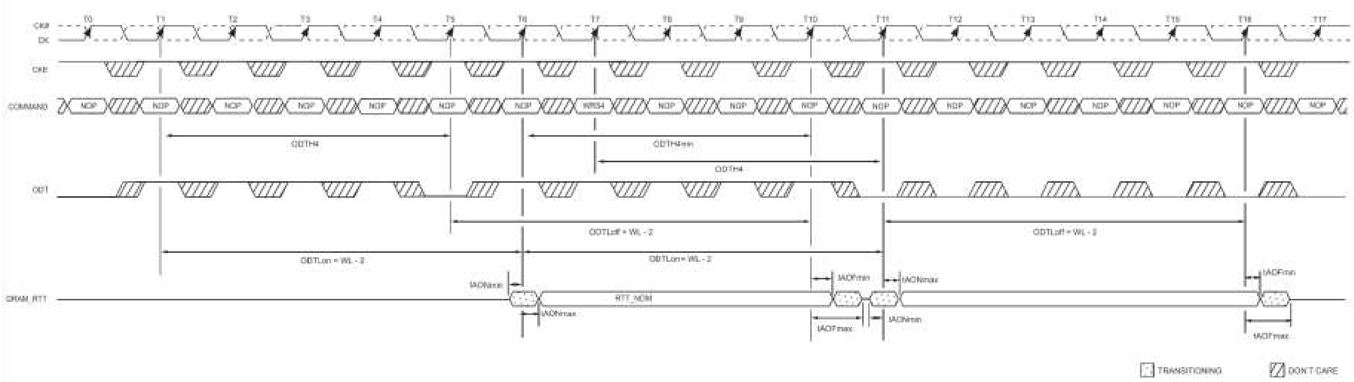
Minimum RTT turn-off time (tAOF min) is the point in time when the device starts to turn off the ODT resistance. Maximum RTT turn off time (tAOF max) is the point in time when the on-die termination has reached high impedance. Both are measured from ODTLoff.

When ODT is asserted, it must remain high until ODTH4 is satisfied. If a Write command is registered by the SDRAM with ODT high, then ODT must remain high until ODTH4 (BL=4) or ODTH8 (BL=8) after the write command. ODTH4 and ODTH8 are measured from ODT registered high to ODT registered low or from the registration of a write command until ODT is registered low.

Synchronous ODT Timing Example for AL=3; CWL=5; ODTLon=AL+CWL-2=6; ODTLoff=AL+CWL-2=6



Synchronous ODT example with BL=4, WL=7

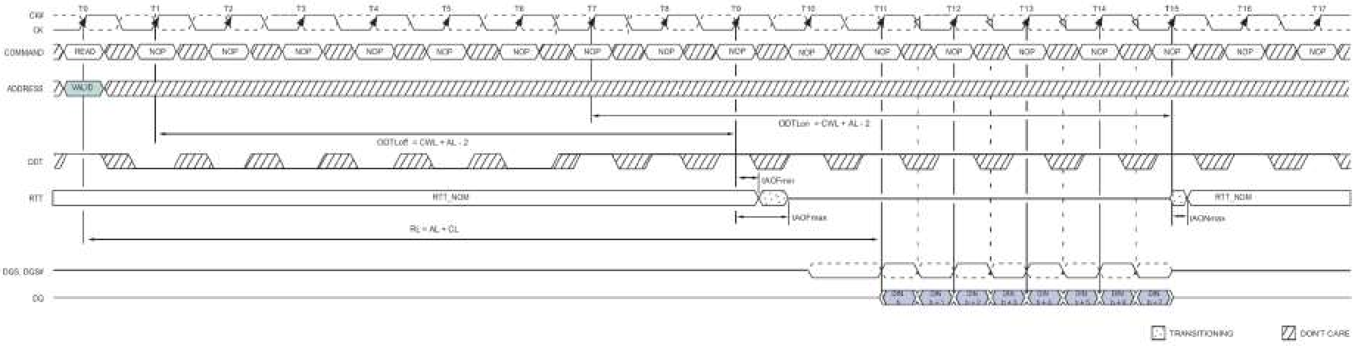


ODT must be held for at least ODTH4 after assertion (T1); ODT must be kept high ODTH4 (BL=4) or ODTH8 (BL=8) after Write command (T7). ODTH is measured from ODT first registered high to ODT first registered low, or from registration of Write command with ODT high to ODT registered low. Note that although ODTH4 is satisfied from ODT registered at T6 ODT must not go low before T11 as ODTH4 must also be satisfied from the registration of the Write command at T7.

ODT during Reads

As the DDR3 SDRAM cannot terminate and drive at the same time, RTT must be disabled at least half a clock cycle before the read preamble by driving the ODT pin low appropriately. RTT may not be enabled until the end of the post-amble as shown in the following figure. DRAM turns on the termination when it stops driving which is determined by tHZ. If DRAM stops driving early (i.e. tHZ is early), then tAONmin time may apply. If DRAM stops driving late (i.e. tHZ is late), then DRAM complies with tAONmax timing. Note that ODT may be disabled earlier before the Read and enabled later after the Read than shown in this example.

ODT must be disabled externally during Reads by driving ODT low. (Example: CL=6; AL=CL-1=5; RL=AL+CL=11; CWL=5; ODTLon=CWL+AL-2=8; ODTLoff=CWL+AL-2=8)



Dynamic ODT

In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3 SDRAM can be changed without issuing an MRS command. This requirement is supported by the “Dynamic ODT” feature as described as follows:

Functional Description

The Dynamic ODT Mode is enabled if bit (A9) or (A10) of MR2 is set to ‘1’. The function is described as follows:
Two RTT values are available: RTT_Nom and RTT_WR.

- The value for RTT_Nom is preselected via bits A [9,6,2] in MR1.
- The value for RTT_WR is preselected via bits A [10,9] in MR2.
  During operation without write commands, the termination is controlled as follows:
- Nominal termination strength RTT_Nom is selected.
- Termination on/off timing is controlled via ODT pin and latencies ODTLon and ODTLoff. When a Write command
- (WR, WRA, WRS4, WRS8, WRAS4, WRAS8) is registered, and if Dynamic ODT is enabled, the termination is controlled as follows:
- A latency ODTLcnw after the write command, termination strength RTT_WR is selected.
- A latency ODTLcwn8 (for BL8, fixed by MRS or selected OTF) or ODTLcwn4 (for BC4, fixed by MRS or selected OTF) after the write command, termination strength RTT_Nom is selected.
- Termination on/off timing is controlled via ODT pin and ODTLon, ODTLoff.

The following table shows latencies and timing parameters which are relevant for the on-die termination control in Dynamic ODT mode.

The dynamic ODT feature is not supported at DLL-off mode. User must use MRS command to set RTT_WR, MR2 [A10,A9 = [0,0], to disable Dynamic ODT externally.

When ODT is asserted, it must remain high until ODTH4 is satisfied. If a Write command is registered by the SDRAM with ODT high, then ODT must remain high until ODTH4 (BL=4) or ODTH8 (BL=8) after the Write command. ODTH4 and ODTH8 are measured from ODT registered high to ODT registered low or from the registration of Write command until ODT is register low.

Latencies and timing parameters relevant for Dynamic ODT

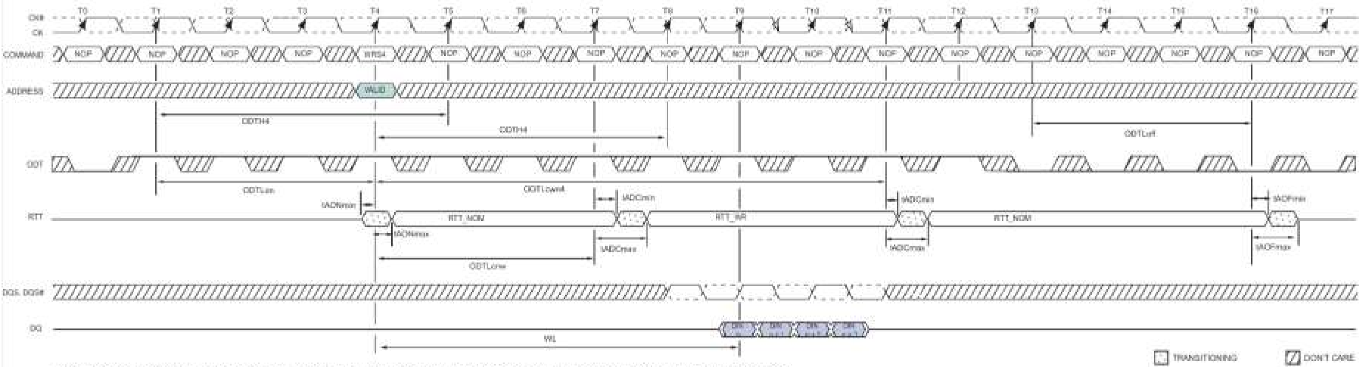
Name and Description	Symbol	Defined from	Defined to	Definition for all DDR3L speed pin	Unit
ODT turn-on Latency	ODTLon	registering external	ODT signal high turning termination on	ODTLon=WL-2	tCK
ODT turn-off Latency	ODTLoff	registering external	ODT signal low turning termination off	ODTLoff=WL-2	tCK
ODT Latency for changing from RTT_Nom to RTT_WR	ODTLcnw	registering external write command	change RTT strength from RTT_Nom to RTT_WR	ODTLcnw=WL-2	tCK
ODT Latency for change from RTT_WR to RTT_Nom (BL=4)	ODTLcwn4	registering external write command change	RTT strength from RTT_WR to RTT_Nom	ODTLcwn4=4+ODTLoff	tCK
ODT Latency for change from RTT_WR to RTT_Nom (BL=8)	ODTLcwn8	registering external write command change	RTT strength from RTT_WR to RTT_Nom	ODTLcwn8=6+ODTLoff	tCK (avg)
Minimum ODT high time after ODT assertion	ODTH4	registering ODT high	ODT registered low	ODTH4=4	tCK (avg)
Minimum ODT high time after Write (BL=4)	ODTH4	registering write with ODT high	ODT registered low	ODTH4=4	tCK (avg)
Minimum ODT high time after Write (BL=8)	ODTH8	registering write with ODT high	ODT register low	ODTH8=6	tCK (avg)
RTT change skew	tADC	ODTLcnw ODTLcwn	RTT valid	tADC(min)=0.3tCK(avg) tADC(max)=0.7tCK(avg)	tCK (avg)

Note:

1. tAOF, nom and tADC, nom are 0.5tCK (effectively adding half a clock cycle to ODTLoff, ODTcnw, and ODTLcwn)

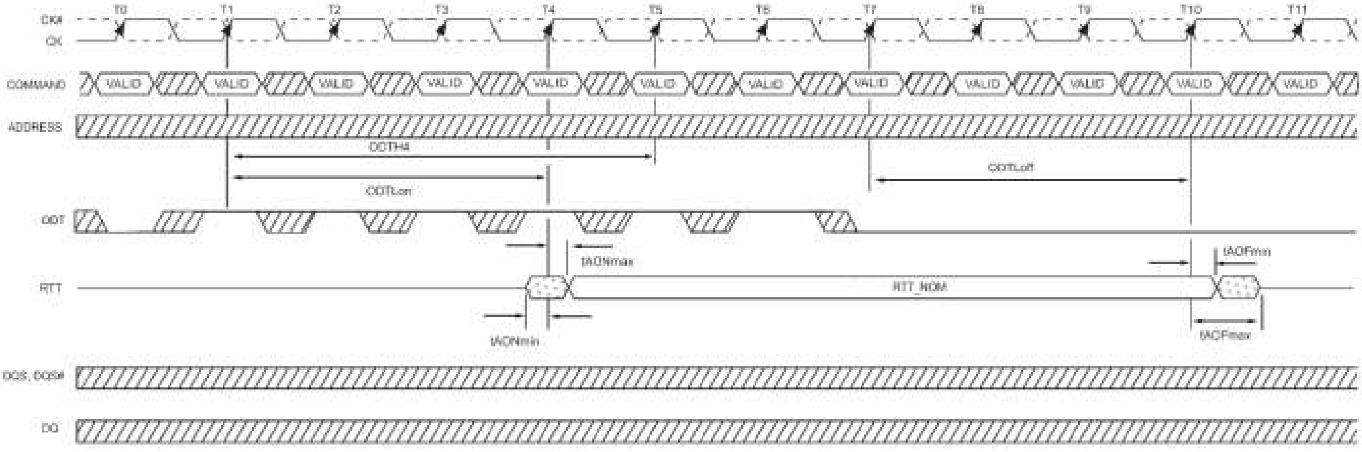
ODT Timing Diagrams

Dynamic ODT: Behavior with ODT being asserted before and after the write



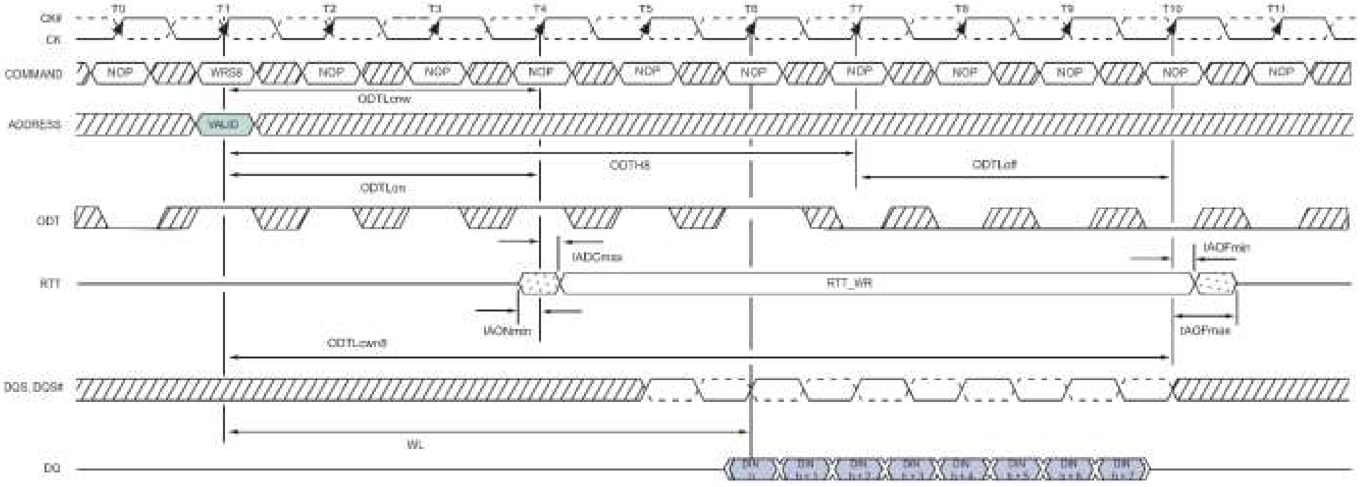
NOTE: Example for BC4 (via MRS or OTF), AL = 0, CWL = 5. ODTH4 applies to first registering ODT high and to the registration of the Write command.
In this example, ODTH4 would be satisfied if ODT went low at T8 (4 clocks after the Write command).

Dynamic ODT: Behavior without write command, AL=0, CWL=5



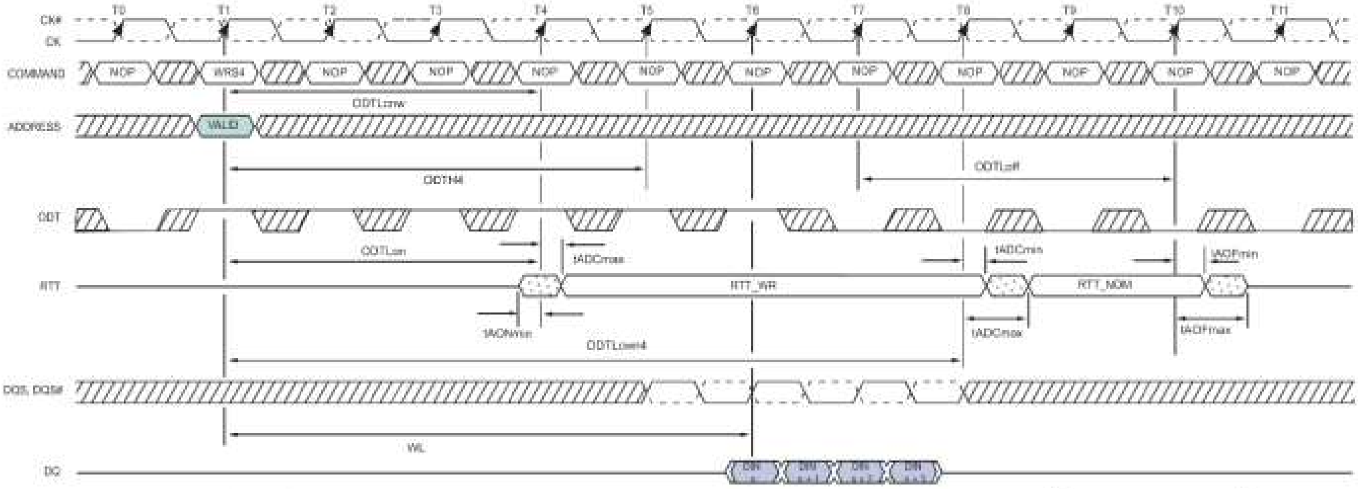
NOTE: ODTH4 is defined from ODT registered high to ODT registered low, so in this example, ODTH4 is satisfied.
ODT registered low at T5 would also be legal.

Dynam Dynamic ODT: Behavior with ODT pin being asserted together with write command for the duration of 6 clock cycles



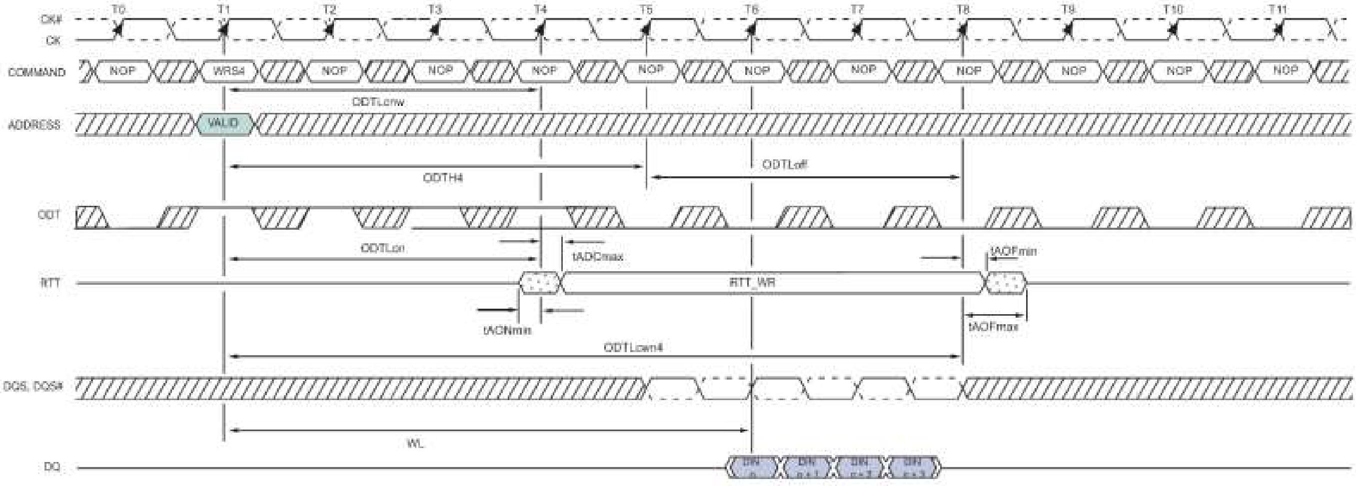
NOTE: Example for BL8 (via MRS or OTF), AL = 0, CWL = 5. In this example, ODTH8 = 6 is exactly satisfied.

Dynamic ODT: Behavior with ODT pin being asserted together with write command for a duration of 6 clock cycles, example for BC4 (via MRS or OTF), AL=0, CWL=5



NOTE: ODTH4 is defined from ODT registered high to ODT registered low, so in this example, ODTH4 is satisfied. ODT registered low at T5 would also be legal.

Dynam Dynamic ODT: Dynamic ODT: Behavior with ODT pin being asserted together with write command for the duration of 4 clock cycles



NOTE: Example for BC4 (via MRS or OTF), AL = 0, CWL = 5. In this example, ODTH4 = 4 is exactly satisfied.

Asynchronous ODT Mode

Asynchronous ODT mode is selected when DRAM runs in DLLon mode, but DLL is temporarily disabled (i.e. frozen) in precharge power-down (by MR0 bit A12). Based on the power down mode definitions, this is currently Precharge power down mode if DLL is disabled during precharge power down by MR0 bit A12.

In asynchronous ODT timing mode, internal ODT command is NOT delayed by Additive Latency (AL) relative to the external ODT command.

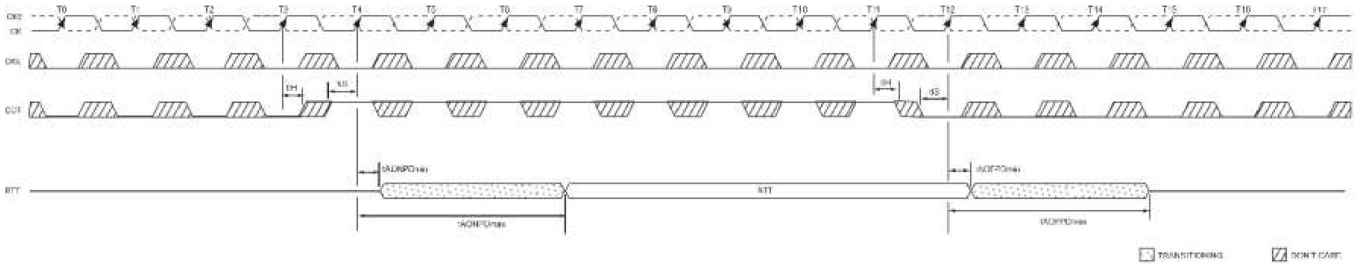
In asynchronous ODT mode, the following timing parameters apply: tAONPD min/max, tAOFPD min/max.

Minimum RTT turn-on time (tAONPD min) is the point in time when the device termination circuit leaves high impedance state and ODT resistance begins to turn on. Maximum RTT turn on time (tAONPD max) is the point in time when the ODT resistance is fully on.

tAONPDmin and tAONPDmax are measured from ODT being sampled high.

Minimum RTT turn-off time (tAOFPDmin) is the point in time when the devices termination circuit starts to turn off the ODT resistance. Maximum ODT turn off time (tAOFPDmax) is the point in time when the on-die termination has reached high impedance. tAOFPDmin and tAOFPDmax are measured from ODT being sample low.

Asynchronous ODT Timings on DDR3 SDRAM with fast ODT transition: AL is Ignored



In Precharge Power Down, ODT receiver remains active; however no Read or Write command can be issued, as the respective ADD/CMD receivers may be disabled.

Asynchronous ODT Timing Parameters for all Speed Bins

Symbol	Description	Min	Max	Unit
tAONPD	Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	2	8.5	ns
tAOFPD	Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	2	8.5	ns

ODT timing parameters for Power Down (with DLL frozen) entry and exit transition period

Description	Min	Max
ODT to RTT turn-on delay	min{ ODTLon * tCK + tAONmin; tAONPDmin } min{ (WL - 2) * tCK + tAONmin; tAONPDmin }	max{ ODTLon * tCK + tAONmax; tAONPDmax } max{ (WL - 2) * tCK + tAONmax; tAONPFmax }
ODT to RTT turn-off delay	min{ ODTLoff * tCK + tAOFmin; tAOFPDmin } min{ (WL - 2) * tCK + tAOFmin; tAOFPDmin }	max{ ODTLoff * tCK + tAOFmax; tAOFPDmax } max{ (WL - 2) * tCK + tAOFmax; tAOFPDmax }
tANPD	WL - 1	

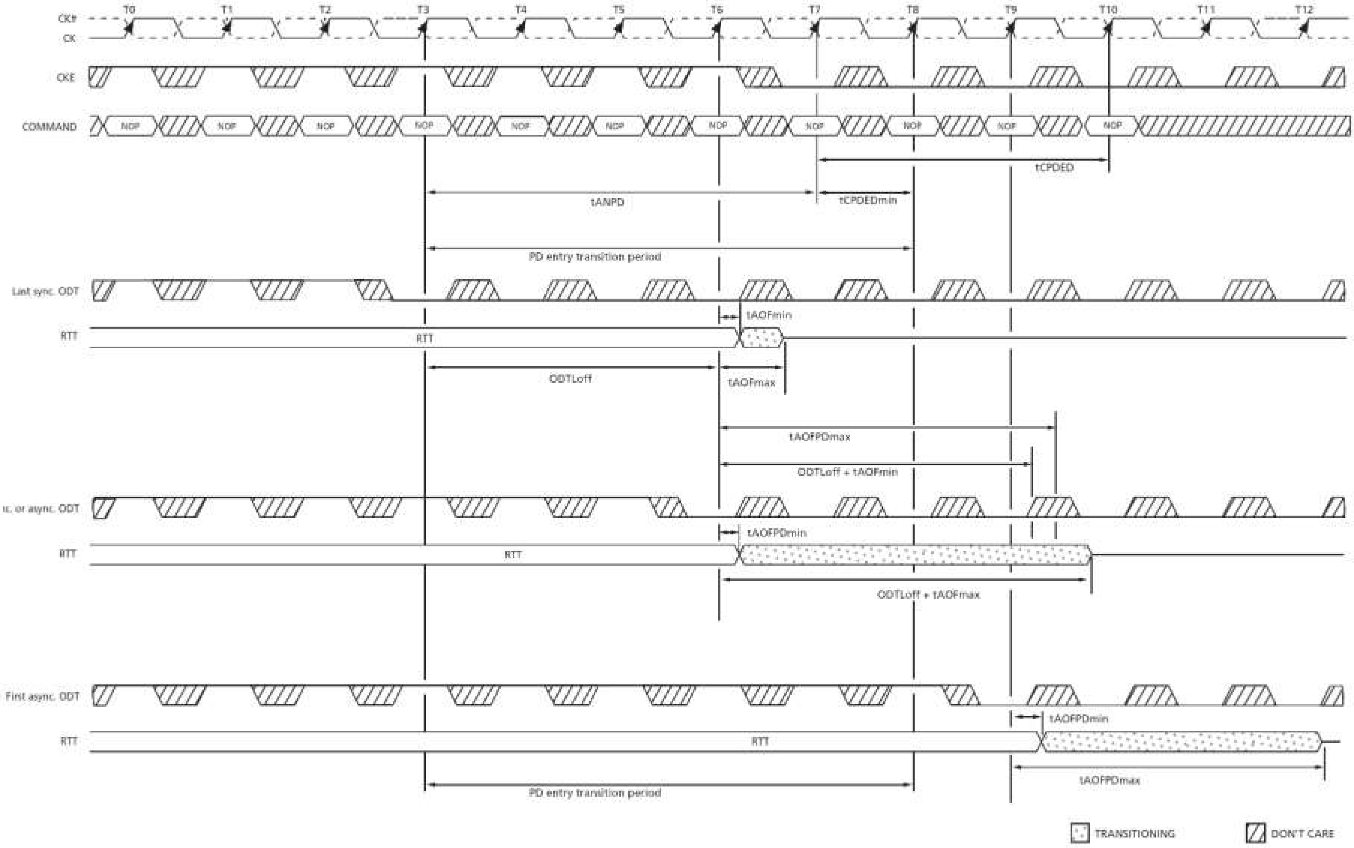
Synchronous to Asynchronous ODT Mode Transition during Power-Down Entry

If DLL is selected to be frozen in Precharge Power Down Mode by the setting of bit A12 in MR0 to “0”, there is a transition period around power down entry, where the DDR3L SDRAM may show either synchronous or asynchronous ODT behavior.

The transition period is defined by the parameters tANPD and tCPDED(min). tANPD is equal to (WL-1) and is counted backwards in time from the clock cycle where CKE is first registered low. tCPDED(min) starts with the clock cycle where CKE is first registered low. The transition period begins with the starting point of tANPD and terminates at the end point of tCPDED(min). If there is a Refresh command in progress while CKE goes low, then the transition period ends at the later one of tRFC(min) after the Refresh command and the end point of tCPDED(min). Please note that the actual starting point at tANPD is excluded from the transition period, and the actual end point at tCPDED(min) and tRFC(min, respectively, are included in the transition period.

ODT assertion during the transition period may result in an RTT changes as early as the smaller of tAONPDmin and (ODTLon*tck+tAONmin) and as late as the larger of tAONPDmax and (ODTLon*tCK+tAONmax). ODT de-assertion during the transition period may result in an RTT change as early as the smaller of tAOFPDmin and (ODTLoff*tCK+tAOFmin) and as late as the larger of tAOFPDmax and (ODTLoff*tCK+tAOFmax). Note that, if AL has a large value, the range where RTT is uncertain becomes quite large. The following figure shows the three different cases: ODT_A, synchronous behavior before tANPD; ODT_B has a state change during the transition period; ODT_C shows a state change after the transition period.

Synchronous to asynchronous transition during Precharge Power Down (with DLL frozen) entry (AL=0; CWL=5; tANPD=WL-1=4)



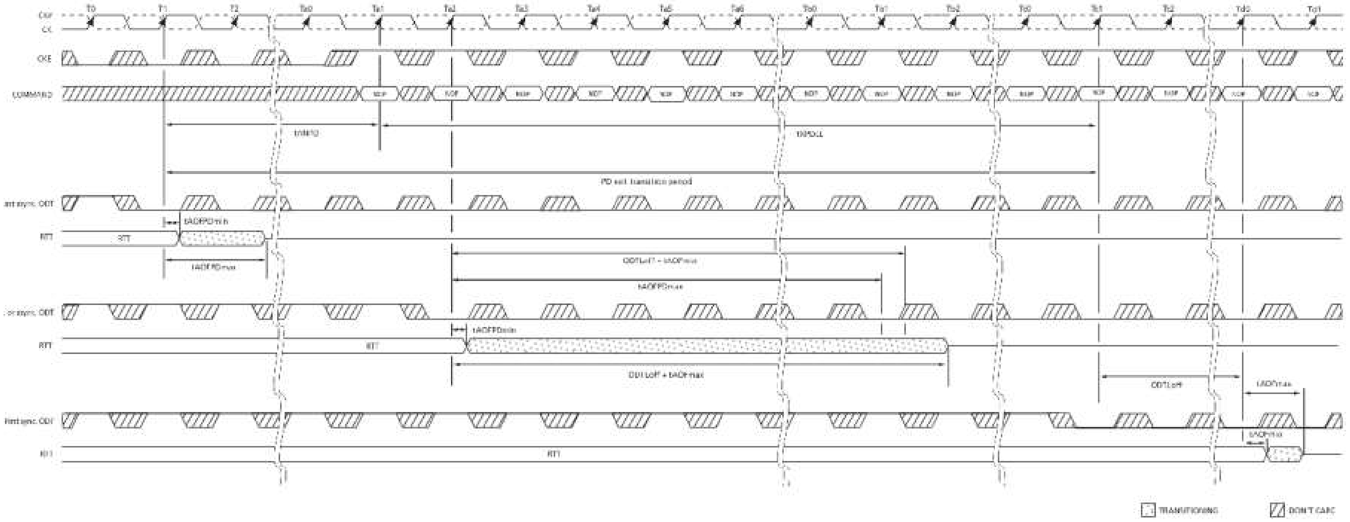
Asynchronous to Synchronous ODT Mode transition during Power-Down Exit

If DLL is selected to be frozen in Precharge Power Down Mode by the setting of bit A12 in MR0 to “0”, there is also a transition period around power down exit, where either synchronous or asynchronous response to a change in ODT must be expected from the DDR3L SDRAM.

This transition period starts tANPD before CKE is first registered high, and ends tXPDLL after CKE is first registered high. tANPD is equal to (WL -1) and is counted (backwards) from the clock cycle where CKE is first registered high.

ODT assertion during the transition period may result in an RTT change as early as the smaller of tAONPDmin and (ODTLon* tCK+tAONmin) and as late as the larger of tAONPDmax and (ODTLon*tCK+tAONmax). ODT deassertion during the transition period may result in an RTT change as early as the smaller of tAOFPDmin and (ODTLoff*tCK+tAOFmin) and as late as the larger of tAOFPDmax and (ODToff*tCK+tAOFmax). Note that if AL has a large value, the range where RTT is uncertain becomes quite large. The following figure shows the three different cases: ODT_C, asynchronous response before tANPD; ODT_B has a state change of ODT during the transition period; ODT_A shows a state change of ODT after the transition period with synchronous response.

Asynchronous to synchronous transition during Precharge Power Down (with DLL frozen) exit (CL=6; AL=CL-1; CWL=5; tANPD=WL-1=9)

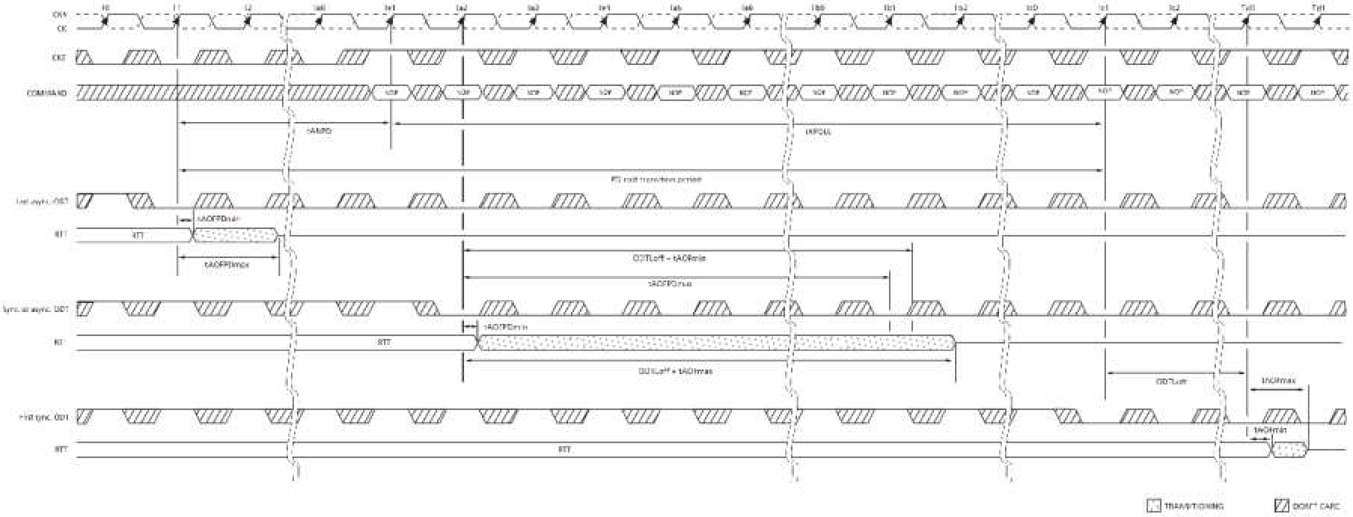


Asynchronous to Synchronous ODT Mode during short CKE high and short CKE low periods

If the total time in Precharge Power Down state or Idle state is very short, the transition periods for PD entry and PD exit may overlap. In this case, the response of the DDR3L SDRAMs RTT to a change in ODT state at the input may be synchronous or asynchronous from the state of the PD entry transition period to the end of the PD exit transition period (even if the entry ends later than the exit period).

If the total time in Idle state is very short, the transition periods for PD exit and PD entry may overlap. In this case, the response of the DDR3L SDRAMs RTT to a change in ODT state at the input may be synchronous or asynchronous from the state of the PD exit transition period to the end of the PD entry transition period. Note that in the following figure, it is assumed that there was no Refresh command in progress when Idle state was entered.

Transition period for short CKE cycles with entry and exit period overlapping (AL=0; WL=5; tANPD=WL-1=4)



4.11 ZQ Calibration Commands

ZQ Calibration Description

ZQ Calibration command is used to calibrate DRAM Ron and ODT values. DDR3L SDRAM needs longer time to calibrate output driver and on-die termination circuits at initialization and relatively smaller time to perform periodic calibrations.

ZQCL command is used to perform the initial calibration during power-up initialization sequence. This command may be issued at any time by the controller depending on the system environment. ZQCL command triggers the calibration engine inside the DRAM and once calibration is achieved the calibrated values are transferred from calibration engine to DRAM IO which gets reflected as updated output driver and on-die termination values.

The first ZQCL command issued after reset is allowed a timing period of tZQinit to perform the full calibration and the transfer of values. All other ZQCL commands except the first ZQCL command issued after RESET is allowed a timing period of tZQoper.

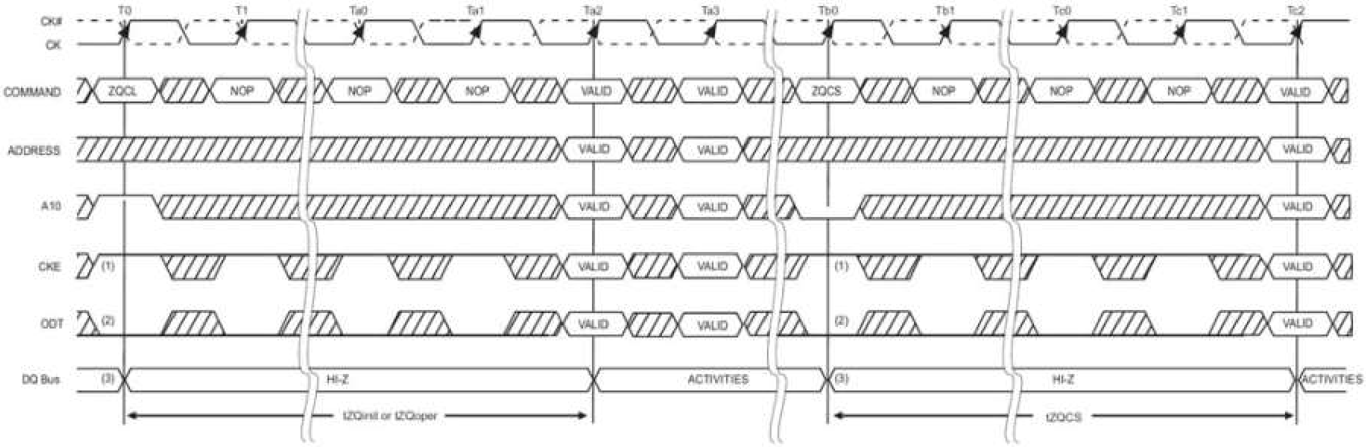
ZQCS command is used to perform periodic calibrations to account for voltage and temperature variations. A shorter timing window is provided to perform the calibration and transfer of values as defined by timing parameter tZQCS. No other activities should be performed on the DRAM channel by the controller for the duration of tZQinit, tZQoper, or tZQCS. The quiet time on the DRAM channel allows calibration of output driver and on-die termination values. Once DRAM calibration is achieved, the DRAM should disable ZQ current consumption path to reduce power.

All banks must be precharged and tRP met before ZQCL or ZQCS commands are issued by the controller.

ZQ calibration commands can also be issued in parallel to DLL lock time when coming out of self refresh. Upon selfrefresh exit, DDR3L SDRAM will not perform an IO calibration without an explicit ZQ calibration command. The earliest possible time for ZQ Calibration command (short or long) after self refresh exit is tXS.

In systems that share the ZQ resistor between devices, the controller must not allow any overlap of tZQoper, tZQinit, or tZQCS between ranks.

ZQ Calibration Timing



NOTES: 1. CKE must be continuously registered high during the calibration procedure.

2. On-die termination must be disabled via the ODT signal or MRS during the calibration procedure.

3. All devices connected to the DQ bus should be high impedance during the calibration procedure.

TIME BREAK

▨ DON'T CARE

ZQ External Resistor Value, Tolerance, and Capacitive loading

In order to use the ZQ calibration function, a 240 ohm ±1% tolerance external resistor connected between the ZQ pin and ground. The single resistor can be used for each SDRAM or one resistor can be shared between two SDRAMs if the ZQ calibration timings for each SDRAM do not overlap. The total capacitive loading on the ZQ pin must be limited.

4.12 Absolute Maximum Ratings

Absolute Maximum DC Ratings

Symbol	Parameter	Values	Unit	Note
VDD	Voltage on VDD pin relative to Vss	-0.4 ~ 1.8	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.4 ~ 1.8	V	1,3
VIN, VOUT	Voltage on any pin relative to Vss	-0.4 ~ 1.8	V	1
TSTG	Storage temperature	-55 ~ 100	°C	1,2

Notes:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM.
3. VDD and VDDQ must be within 300mV of each other at all times; and Vref must be not greater than 0.6 x VDDQ, when VDD and VDDQ are less than 500mV; Vref may be equal to or less than 300mV.

Refresh parameters by device density

Parameter	Symbol	1Gb	Unit
REF command to ACT or REF command time	tRFC	110	ns

Temperature Range

Symbol	Parameter	Rating	Unit	Note
Commercial (-C)	Normal Operating Temperature Range	0 ≤ Toper ≤ 85	°C	1
	Extended Temperature Range	85 < Toper ≤ 95	°C	1,2

Notes:

1. Operating Temperature Toper is the case surface temperature on the center/top side of the DRAM.
2. Some applications require operation of the DRAM in the Extended Temperature Range between 85°C and 95°C case temperature.

Full specifications are guaranteed in this range, but the following additional apply:

a) Refresh commands must be doubled in frequency, therefore, reducing the Refresh interval tREFI to 3.9us.

b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6=0 and MR2 A7=1) or enable the optional Auto Self-Refresh mode (MR2 A6=1 and MR2 A7=0).

4.13 AC & DC Operating Conditions

Recommended DC Operating Conditions

Symbol	Parameter		Rating			Unit	Note
			Min.	Typ.	Max.		
VDD	Supply Voltage	DDR3	1.425	1.5	1.575	V	1,2
		DDR3L	1.283	1.35	1.45		3,4,5,6
VDDQ	Supply Voltage for Output	DDR3	1.425	1.5	1.575	V	1,2
		DDR3L	1.283	1.35	1.45		3,4,5,6

Notes:

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together
3. Maximun DC value may not be great than 1.425V.The DC value is the linear average of VDD/ VDDQ(t) over a very long period of time (e.g., 1 sec).
4. If maximum limit is exceeded, input levels shall be governed by DDR3 specifications.
5. Under these supply voltages, the device operates to this DDR3L specification.
6. Once initialized for DDR3 operation, DDR3L operation may only be used if the device is in reset while VDD and VDDQ are changed for DDR3L operation.
7. VDD= VDDQ= 1.35V (1.283–1.45V) Backward compatible to VDD= VDDQ= 1.5V ±0.075V Supports DDR3L devices to be backward com-patible in 1.5V applications.

AC & DC Input Measurement Levels

DDR3 AC and DC Logic Input Levels for Command and Address

Symbol	Parameters	DDR3-1066/1333/1600		DDR3-1866		Unit	Note
		Min	Max	Min	Max		
VIH.CA(DC100)	DC input logic high	Vref + 0.100	VDD	Vref + 0.100	VDD	V	1,5
VIL.CA(DC100)	DC input logic low	VSS	Vref - 0.100	VSS	Vref - 0.100	V	1,6
VIH.CA(AC175)	AC input logic high	Vref + 0.175	Note2			V	1,2,7
VIL.CA(AC175)	AC input logic low	Note2	Vref - 0.175			V	1,2,8
VIH.CA(AC150)	AC input logic high	Vref + 0.150	Note2			V	1,2,7
VIL.CA(AC150)	AC input logic low	Note2	Vref - 0.150			V	1,2,8
VIH.CA(AC135)	AC input logic high			Vref + 0.135	Note 2	V	1,2,7
VIL.CA(AC135)	AC input logic low			Note 2	Vref - 0.135	V	1,2,8
VIH.CA(AC125)	AC input logic high			Vref + 0.125	Note 2	V	1,2,7
VIL.CA(AC125)	AC input logic low			Note 2	Vref - 0.125	V	1,2,8
VREFCA(DC)	Reference Voltage for ADD, CMD inputs	0.49 * VDD	0.51 * VDD	0.49 * VDD	0.51 * VDD	V	3,4,9

Notes:

1. For input only pins except RE ET. Vref = VrefCA(DC).
2. See “Overshoot and Undershoot Specifications” .
3. The ac peak noise on VRef may not allow VRef to deviate from VRefCA(DC) by more than +/-1% VDD (for reference: approx. +/- 15 mV).
4. For reference: approx. VDD/2 +/- 15 mV.
5. VIH(dc) is used as a simplified symbol for VIH.CA(DC100)
6. VIL(dc) is used as a simplified symbol for VIL.CA(DC100)
7. VIH(ac) is used as a simplified symbol for VIH.CA(AC135), and VIH.CA(AC125); VIH.CA(AC175) value is used when Vref + 0.175V is referenced, VIH.CA(AC135) value is used when Vref + 0.135V is referenced, and VIH.CA(AC125) value is used when Vref + 0.125V is referenced.

8. VIL(ac) is used as a simplified symbol for VIL.CA(AC135) and VIL.CA(AC125); VIL.CA(AC135) value is used when Vref - 0.135V is referenced, and VIL.CA(AC125) value is used when Vref - 0.125V is referenced.
9. VrefCA(DC) is measured relative to VDD at the same point in time on the same device.

DDR3L AC and DC Logic Input Levels for Command and Address

Symbol	Parameter	DDR3L-1066/1333/1600/1866		Unit	Note
		Min.	Max.		
VIH.DQ(DC90)	DC input logic high	Vref + 0.09	VDD	V	1
VIL.DQ(DC90)	DC input logic Low	VSS	Vref - 0.09	V	1
VIH.CA(AC160)	AC input logic high	Vref + 0.16	Note2	V	1,2
VIL.CA(AC160)	AC input logic low	Note2	Vref - 0.16	V	1,2
VIH.CA(AC135)	AC input logic high	Vref + 0.135	Note2	V	1,2
VIL.CA(AC135)	AC input logic low	Note2	Vref - 0.135	V	1,2
VREFCA(DC)	Reference Voltage for ADD, CMD inputs	0.49 x VDD	0.51 x VDD	V	3,4

Notes:

1. For input only pins except RESET.Vref=VrefCA(DC)
2. See "Overshoot and Undershoot Specifications"
3. The ac peak noise on Vref may not allow Vref to deviate from Vref(DC) by more than +/- 0.1% VDD.
4. For reference: approx. VDD/2 +/- 15mV. DDR3L is VDD/2 +/-13.5mV.

DDR3 AC and DC Logic Input Levels for DQ and DM

Symbol	Parameters	DDR3-1066/1333/1600		DDR3-1866		Unit	Note
		Min	Max	Min	Max		
VIH.DQ(DC100)	DC input logic high	Vref + 0.100	VDD	Vref + 0.100	VDD	V	1,5
VIL.DQ(DC100)	DC input logic low	VSS	Vref - 0.100	VSS	Vref - 0.100	V	1,6
VIH.DQ(AC175)	AC input logic high	Vref + 0.175	Note2	-	-	V	1,2,7
VIL.DQ(AC175)	AC input logic low	Note2	Vref - 0.175	-	-	V	1,2,8
VIH.DQ(AC150)	AC input logic high	Vref + 0.150	Note2	-	-	V	1,2,7
VIL.DQ(AC150)	AC input logic low	Note2	Vref - 0.150	-	-	V	1,2,8
VIH.DQ(AC135)	AC input logic high	-	-	Vref + 0.135	Note 2	V	1,2,7
VIL.DQ(AC135)	AC input logic low	-	-	Vref + 0.135	Note 2	V	1,2,8
VREFDQ(DC)	Reference Voltage for DQ, DM inputs	0.49 * VDD	0.51 * VDD	0.49 * VDD	0.51 * VDD	V	3,4,9

Notes:

1. Vref = VrefDQ(DC).
2. See “Overshoot and Undershoot Specifications” .
3. The ac peak noise on VRef may not allow VRef to deviate from VRefDQ(DC) by more than +/-1% VDD (for reference:approx. +/- 15 mV).
4. For reference: approx. VDD/2 +/- 15 mV.
5. VIH(dc) is used as a simplified symbol for VIH.DQ(DC100)
6. VIL(dc) is used as a simplified symbol for VIL.DQ(DC100)
7. VIH(ac) is used as a simplified symbol for VIH.DQ(AC135); VIH.DQ(AC135) value is used when Vref + 0.135V is referenced.
8. VIL(ac) is used as a simplified symbol for VIL.DQ(AC135); VIL.DQ(AC135) value is used when Vref - 0.135V is referenced.
9. VrefCA(DC) is measured relative to VDD at the same point in time on the same device.

DDR3L AC and DC Logic Input Levels for DQ and DM

Symbol	Parameter	DDR3L-1066/1333/1600/1866		Unit	Note
		Min.	Max.		
VIH.DQ(DC90)	DC input logic high	Vref + 0.09	VDD	V	1
VIL.DQ(DC90)	DC input logic Low	VSS	Vref - 0.09	V	1
VIH.CA(AC160)	AC input logic high	Vref + 0.16	Note2	V	1,2
VIL.CA(AC160)	AC input logic low	Note2	Vref - 0.16	V	1,2
VIH.CA(AC135)	AC input logic high	Vref + 0.135	Note2	V	1,2
VIL.CA(AC135)	AC input logic low	Note2	Vref - 0.135	V	1,2
VREFCA(DC)	Reference Voltage for ADD, CMD inputs	0.49 x VDD	0.51 x VDD	V	3,4

Notes:

1. For input only pins except RESET.Vref=VrefCA(DC)
2. See "Overshoot and Undershoot Specifications"
3. The ac peak noise on Vref may not allow Vref to deviate from Vref(DC) by more than +/- 0.1% VDD.
4. For reference: approx. VDD/2 +/- 15mV. DDR3L is VDD/2 +/-13.5mV.

Vref Tolerances

The dc-tolerance limits and ac-moist limits for the reference voltages VrefCA and VrefDQ are illustrated in the following figure. It shows a valid reference voltage Vref(t) as a function of time. (Vref stands for VrefCA and VrefDQ likewise).

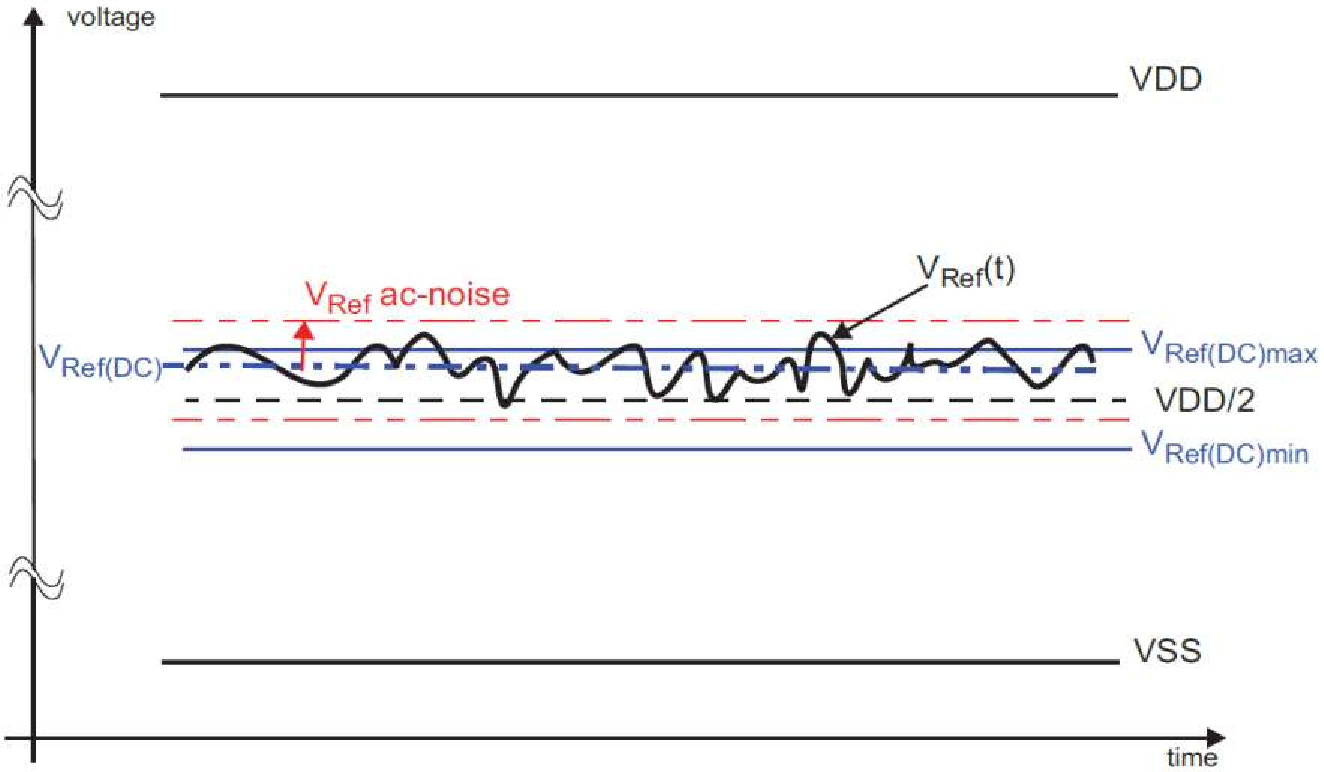
Vref(DC) is the linear average of Vref(t) over a very long period of time (e.g.,1 sec). This average has to meet the min/max requirement in previous page. Furthermore Vref(t) may temporarily deviate from Vref(DC) by no more than ±1% VDD.

The voltage levels for setup and hold time measurements VIH(AC), VIH(DC), VIL(AC), and VIL(DC) are dependent on Vref. “Vref” shall be understood as Vref(DC).

The clarifies that dc-variations of Vref affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for Vref(DC) deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and de-rating values need to include time and voltage associated with Vref ac-noise. Timing and voltage effects due to ac-noise on Vref up to the specified limit (±1% of VDD) are included in DRAM timing and their associated de-ratings.

Illustration of Vref(DC) tolerance and Vrefac-noise limits



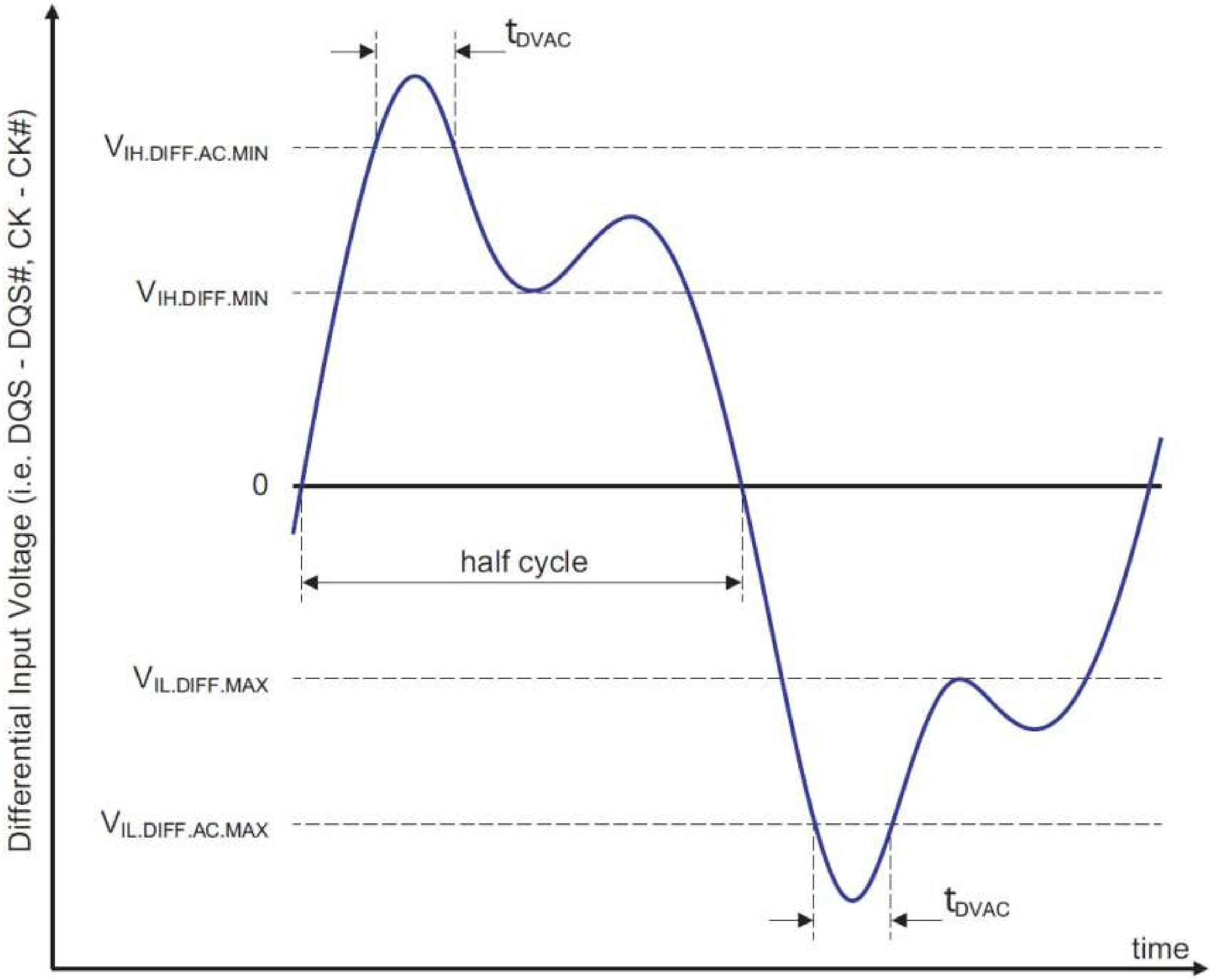
DDR3 Differential AC and DC Input Levels for clock (CK- CK#) and strobe (DQS- DQS#)

Symbol	Parameters	DDR3-1066/1333/1600/1866		Unit	Note
		Min	Max		
VIHdiff	Differential input logic high	+0.200	Note3	V	1
VILdiff	Differential input logic low	Note3	-0.200	V	1
VIHdiff(ac)	Differential input high ac	2 x (VIH(ac) – Vref)	Note3	V	2
VILdiff(ac)	Differential input low ac	Note3	2 x (Vref - VIL(ac))	V	2
DDR3L-1066,1333, 1600					
VIHdiff	Differential input logic high	+0.180	Note3	V	1
VILdiff	Differential input logic low	Note3	-0.180	V	1
VIHdiff(ac)	Differential input high ac	2 x (VIH(ac) – Vref)	Note3	V	2
VILdiff(ac)	Differential input low ac	Note3	2 x (Vref - VIL(ac))	V	2

Notes:

1. Used to define a differential signal slew-rate.
2. For CK - CK use VIH/VIL(ac) of ADD/CMD and VREFCA; for DQS - DQS#, DQSL, DQSL#, DQSU, DQSU# use VIH/VIL(ac) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also there.
3. These values are not defined, however the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits (VIH(dc)max, VIL(dc)min) for single-ended signals as well as limitations for overshoot and undershoot.

Definition of differential ac-swing and “time above ac-level”



DDR3 Allowed time before ringback (tDVAC) for CK - CK# and DQS – DQS#

Slew Rate [V/ns]	DDR3-1066 / 1333 / 1600						DDR3-1866			
	tDVAC [ps] @lVIH/Ldiff(ac)l = 350mV		tDVAC [ps] @lVIH/Ldiff(ac)l = 300mV		tDVAC [ps] @lVIH/Ldiff(ac)l = (DQS- -DQS#) only		tDVAC [ps] @lVIH/Ldiff(ac)l = 300mV		tDVAC [ps] @lVIH/Ldiff(ac)l = (CK- CK#) only	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
>4.0	75	-	175	-	214	-	134	-	139	
4.0	57	-	170	-	214	-	134	-	139	
3.0	50	-	167	-	191	-	112	-	118	
2.0	38	-	119	-	146	-	67	-	77	
1.8	34	-	102	-	131	-	52	-	63	
1.6	29	-	81	-	113	-	33	-	45	
1.4	22	-	54	-	88	-	9	-	23	
1.2	note	-	19	-	56	-	note	-	note	
1.0	Note	-	note	-	11	-	note	-	note	
<1.0	Note	-	note	-	note	-	note	-	note	

Note:

1. Rising input differential signal shall become equal to or greater than VIHdiff(ac) level and Falling input differential signal shall become equal to or less than VILdiff(ac) level.

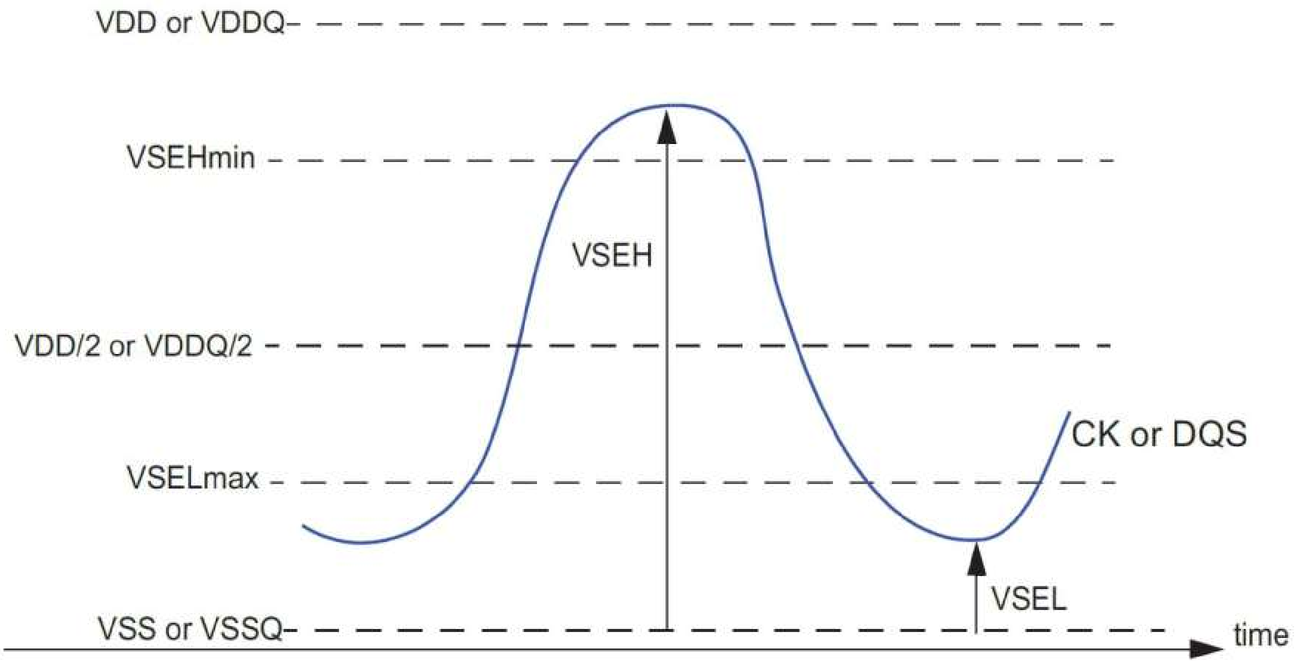
DDR3L Allowed time before ringback (tDVAC) for CK - CK# and DQS – DQS#

Slew Rate [V/ns]	DDR3L-1066 / 1333 / 1600				DDR3L-1866					
	tDVAC [ps] @lVIH/Ldiff(ac)l = 320mV		tDVAC [ps] @lVIH/Ldiff(ac)l = 270mV		tDVAC [ps] @lVIH/Ldiff(ac)l = 270mV		tDVAC [ps] @lVIH/Ldiff(ac)l = 250mV		tDVAC [ps] @lVIH/Ldiff(ac)l = 260mV	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
> 4.0	189	-	201	-	163	-	168	-	176	-
4.0	189	-	201	-	163	-	168	-	176	-
3.0	162	-	179	-	140	-	147	-	154	-
2.0	109	-	134	-	95	-	105	-	111	-
1.8	91	-	119	-	80	-	91	-	97	-
1.6	69	-	100	-	62	-	74	-	78	-
1.4	40	-	76	-	37	-	52	-	56	-
1.2	note	-	44	-	5	-	22	-	24	-
1.0	note	-	note	-	note	-	note	-	note	-
< 1.0	note	-	note	-	note	-	note	-	note	-

Note:

1. Rising input differential signal shall become equal to or greater than VIHdiff(ac) level and Falling input differential signal shall become equal to or less than VILdiff(ac) level.

Single-ended requirements for differential signals



Each individual component of a differential signal (CK, DQS, DQSL, DQSU, CK#, DQS#, DQSL#, or DQSU#) has also to comply with certain requirements for single-ended signals.

CK and CK# have to approximately reach VSEHmin / VSELmax (approximately equal to the ac-levels (VIH(ac) / VIL(ac)) for ADD/CMD signals) in every half-cycle. DQS, DQSL, DQSU, DQS#, DQSL#, or DQSU# have to reach VSEHmin / VSELmax approximately the ac-levels (VIH(ac) / VIL(ac)) for DQ signals) in every half-cycle proceeding and following a valid transition.

Note that the applicable ac-levels for ADD/CMD and DQ's might be different per speed-bin etc. E.g., if VIH150(ac)/VIL150(ac) is used for ADD/CMD signals, then these ac-levels apply also for the single ended signals CK and CK#.

Single-ended levels for CK, DQS, DQSL, DQSU, CK#, DQS#, DQSL#, or DQSU#

Symbol	Parameter	DDR3-1066/1333/1600/1866		Unit	Note
		Min.	Max.		
VSEH	Single-ended high level for strobes	(VDDQ / 2) + 0.175	Note 3	V	1,2
	Single-ended high level for CK, CK#	(VDDQ / 2) + 0.175	Note 3	V	1,2
VSEL	Single-ended low level for strobes	Note 3	(VDDQ / 2) - 0.175	V	1,2
	Single-ended low level for CK, CK#	Note 3	(VDDQ / 2) - 0.175	V	1,2

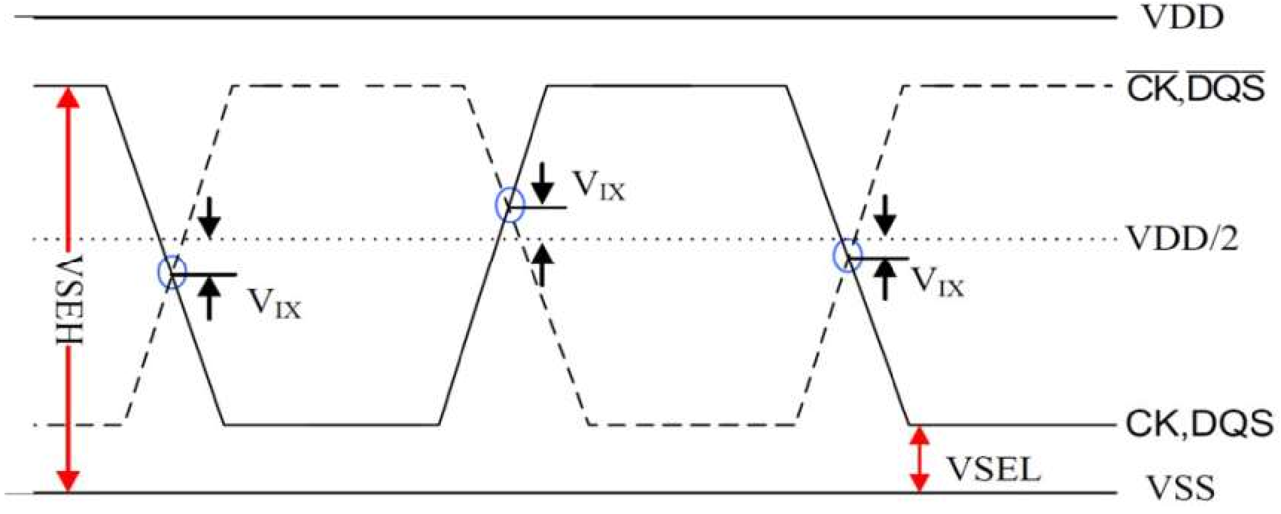
Notes:

1. For CK, CK# use VIH/VIL(ac) of ADD/CMD; for strobes (DQSL, DQSL#, DQSU, DQSU#) use VIH/VIL(ac) of DQs.
2. VIH(ac)/VIL(ac) for DQs is based on VREFDQ; VIH(ac)/VIL(ac) for ADD/CMD is based on VREFCA; if a reduced achigh or ac-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined, however the single-ended signals CK, CK#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot.

Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, CK# and DQS, DQS#) must meet the requirements in the following table. The differential input cross point voltage Vix is measured from the actual cross point of true and complete signal to the midlevel between of VDD and VSS.

VIX Definition



Cross point voltage for differential input signals (CK, DQS)

Symbol	Parameter		1066/1333/1600/1866		Unit	Note
			Min.	Max.		
VIX(CK)	Differential Input Cross Point Voltage relative to VDD/2 for CK, CK#	DDR3	-150	150	mV	1
			-175	175		
		DDR3L	-150	150		
VIX(DQS)	Differential Input Cross Point Voltage relative to VDD/2 for DQS, DQS#	DDR3	-150	150	mV	1
		DDR3L	-150	150		

Notes:

1. The relation between Vix Min/Max and VSEL/VSEH should satisfy following:
(VDD/2) + VIX (min) - VSEL >= 25 mV;
VSEH - ((VDD/2) + VIX (max)) >= 25 mV;

2. Extended range for Vix is only allowed for clock and if single-ended clock input signals CK and CK# are monotonic with a single-ended swing VSEL / VSEH of at least VDD/2 +/-250 mV, and when the differential slew rate of CK - CK# is larger than 3 V/ns

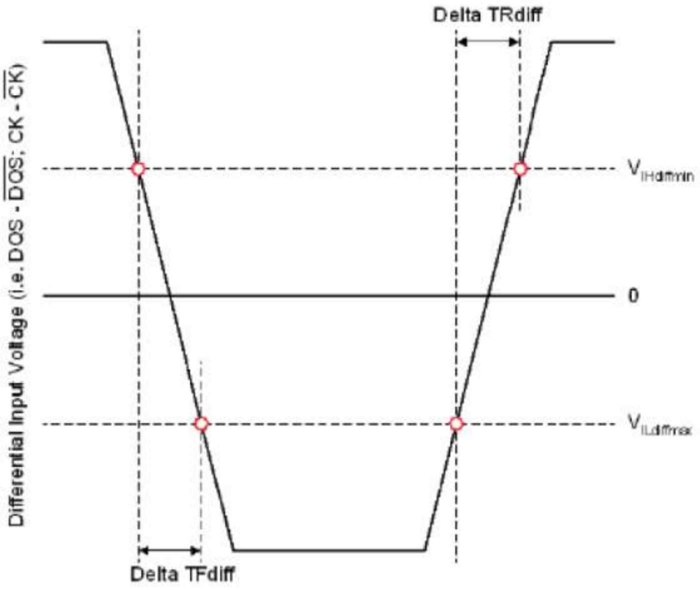
Slew Rate Definition for Differential Input Signals

Input slew rate for differential signals (CK, CK# and DQS, DQS#) are defined and measured as shown below.

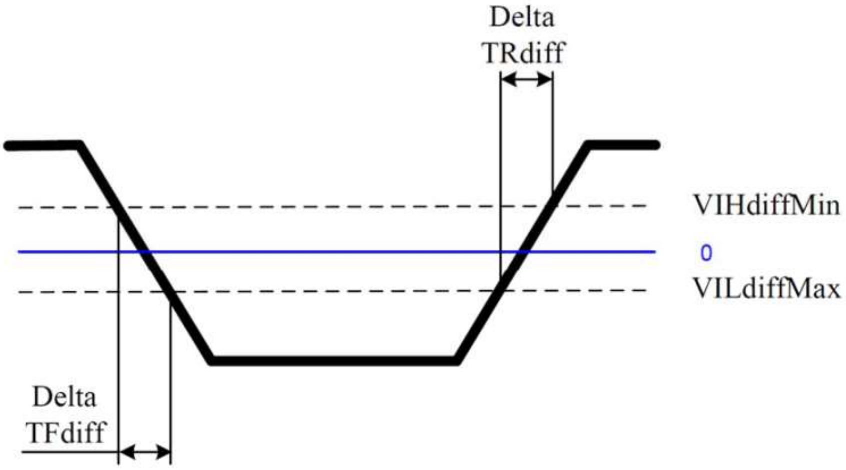
Differential Input Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential input slew rate for rising edge (CK, CK# and DQS, DQS#)	VILdiffmax	VIHdiffmin	[VIHdiffmin-VILdiffmax] / DeltaTRdiff
Differential input slew rate for falling edge (CK, CK# and DQS, DQS#)	VIHdiffmin	VILdiffmax	[VIHdiffmin-VILdiffmax] / DeltaTFdiff
The differential signal (i.e., CK- CK# & DQS- DQS#) must be linear between these thresholds			

Ended Output Slew Rate Definition



Input Nominal Slew Rate Definition for single ended signals



AC and DC Output Measurement Levels

4.14 AC and DC Output Measurement Levels

Single Ended AC and DC Output Levels

Symbol	Parameter	Values	Unit	Note
VOH(DC)	DC output high measurement level (for IV curve linearity)	0.8 x VDDQ	V	
VOM(DC)	DC output mid measurement level (for IV curve linearity)	0.5 x VDDQ	V	
VOL(DC)	DC output low measurement level (for IV curve linearity)	0.2 x VDDQ	V	
VOH(AC)	AC output high measurement level (for output SR)	VTT + 0.1 x VDDQ	V	1
VOL(AC)	AC output low measurement level (for output SR)	VTT - 0.1 x VDDQ	V	1

Note:

1. The swing of ± 0.1 × VDDQ is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to VTT = VDDQ/2.

Differential AC and DC Output Levels

Symbol	Parameter	DDR3/DDR3L	Unit	Note
VOHdiff(AC)	AC differential output high measurement level (for output SR	+0.2 x VDDQ	V	1
VOLdiff(AC)	AC differential output low measurement level (for output SR)	-0.2 x VDDQ	V	1

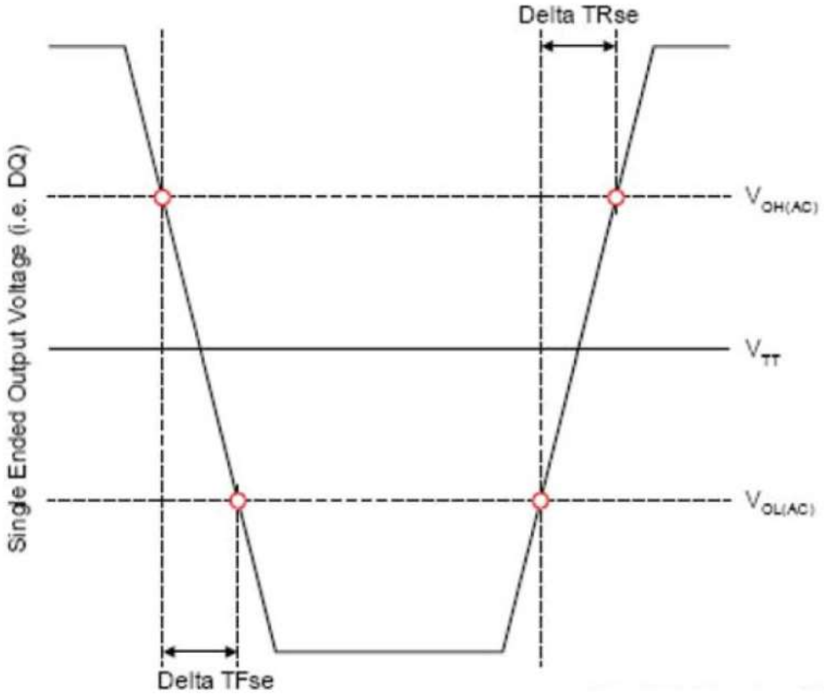
Note:

1. The swing of ± 0.2 × VDDQ is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to VTT = VDDQ/2 at each of the differential outputs.

Single Ended Output Slew Rate

Description	Measured		Defined by
	From	To	
Single-ended output slew rate for rising edge	VOL(AC)	VOH(AC)	[VOH(AC) - VOL(AC)] / DeltaTRse
Single-ended output slew rate for falling edge	VOH(AC)	VOL(AC)	[VOH(AC) - VOL(AC)] / DeltaTFse
Note: Output slew rate is verified by design and characterization, and may not be subject to production test.			

Single Ended Output Slew Rate Definition



Output Slew Rate (Single-ended)

Parameter	Symbol	Option	Min.	Max.	Unit
Single-ended Output Slew Rate	SRQse	DDR3	2.5	5	V/ns
		DDR3L	1.75	5	

Note:

SR: Slew Rate.

Q: Query Output (like in DQ, which stands for Data-in, Query -Output).

se: Single-ended signals.

For Ron = RZQ/7 setting.

Note:

1. In two cases, a maximum slew rate of 6V/ns applies for a single DQ signal within a byte lane.

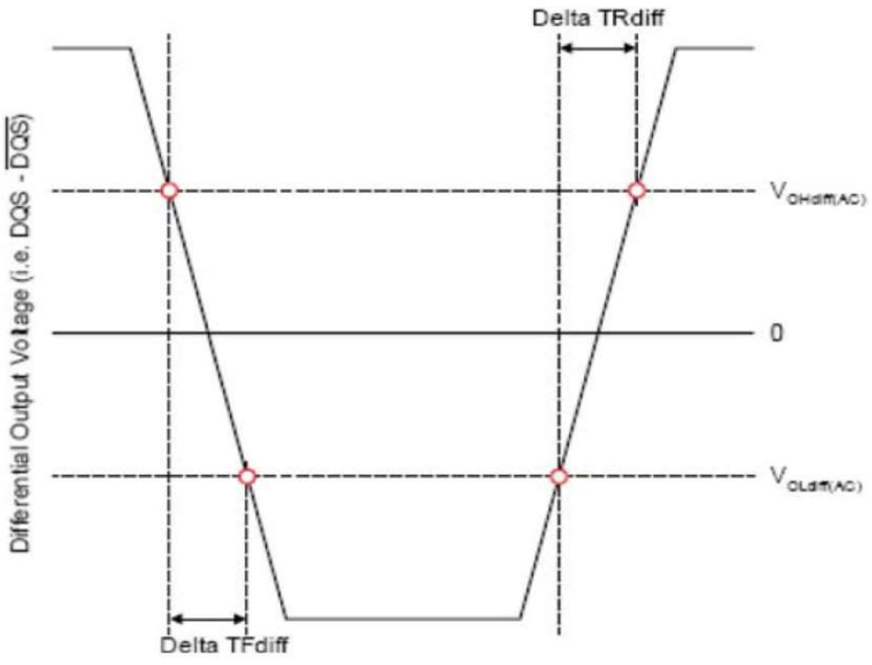
Case 1 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are static (i.e. they stay at either high or low).

Case 2 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are switching into the opposite direction (i.e. from low to high or high to low respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 5 V/ns applies.

Differential Output Slew Rate

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	VOLdiff(AC)	VOHdiff(AC)	[VOHdiff(AC)-VOLdiff(AC)] / DeltaTRdiff
Differential output slew rate for falling edge	VOHdiff(AC)	VOLdiff(AC)	[VOHdiff(AC)-VOLdiff(AC)] / DeltaTFdiff
Note: Output slew rate is verified by design and characterization, and may not be subject to production test.			

Differential Output Slew Rate Definition



Differential Output Slew Rate

Parameter	Symbol	Option	DDR3L-1066/1333/1866		Unit
			Min.	Max.	
Differential Output Slew Rate	SRQdiff	DDR3	5	10	V/ns
		DDR3L	3.5	12	

Note:

SR: Slew Rate.

Q: Query Output (like in DQ, which stands for Data-in, Query -Output).

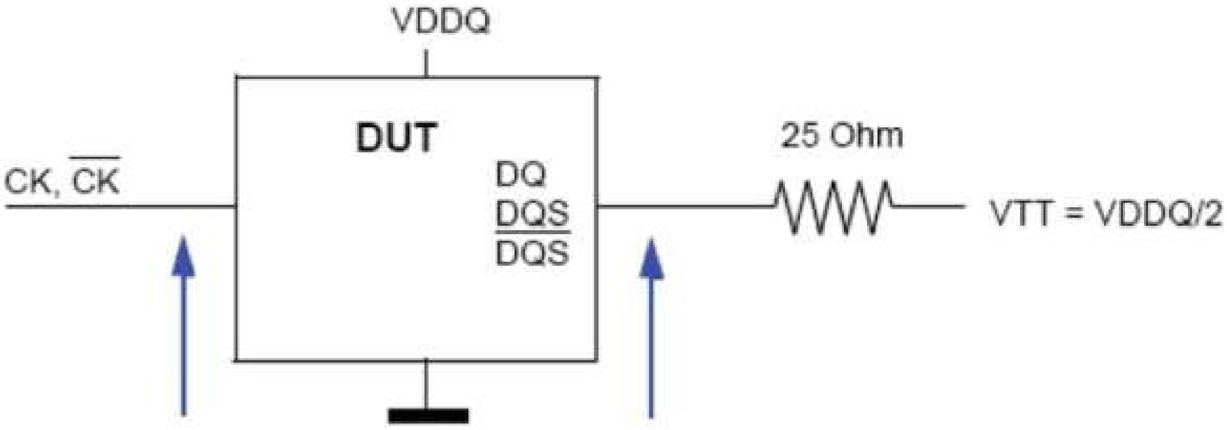
diff: Differential signals.

For Ron = RZQ/7 setting.

4.15 Reference Load for AC Timing and Output Slew Rate

The following figure represents the effective reference load of 25 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.



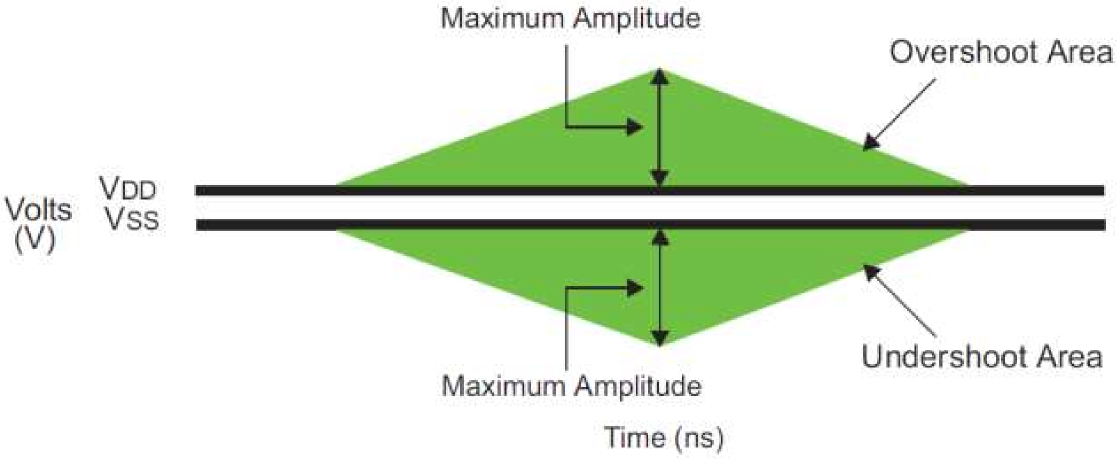
4.16 Overshoot and Undershoot Specifications

AC Overshoot/Undershoot Specification for Address and Control Pins

Item	DDR3L-1066	DDR3L-1333	DDR3L-1600	DDR3L-1866	Units
Maximum peak amplitude allowed for overshoot area	0.4	0.4	0.4	0.4	V
Maximum peak amplitude allowed for undershoot area	0.4	0.4	0.4	0.4	V
Maximum overshoot area above VDD	0.5	0.4	0.33	0.28	V-ns
Maximum undershoot area below VSS	0.5	0.4	0.33	0.28	V-ns
(A0-A14, BA0-BA3, CS#, RAS#,CAS#, WE#, CKE, ODT)					

Notes:

1. The sum of the applied voltage (VDD) and peak amplitude overshoot voltage is not to exceed absolute maximum DC atings
2. The sum of applied voltage (VDD) and the peak amplitude undershoot voltage is not to exceed absolute maximum DC ratings



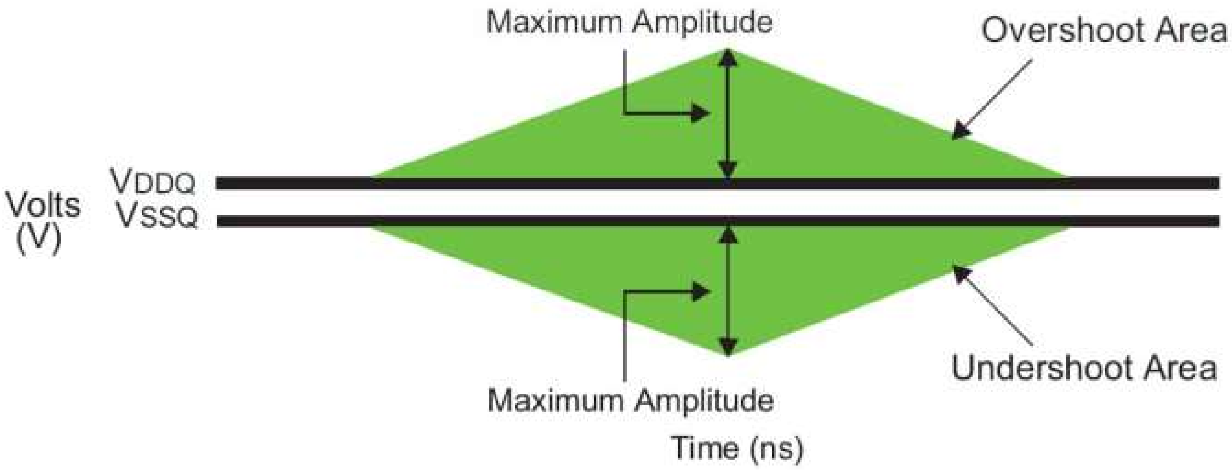
Overshoot and Undershoot Specifications

AC Overshoot/Undershoot Specification for Clock, Data, Strobe, and Mask

Item	DDR3L-1066	DDR3L-1333	DDR3L-1600	DDR3L-1866	Units
Maximum peak amplitude allowed for overshoot area	0.4	0.4	0.4	0.4	V
Maximum peak amplitude allowed for undershoot area	0.4	0.4	0.4	0.4	V
Maximum overshoot area above VDD	0.19	0.15	0.13	0.11	V-ns
Maximum undershoot area below VSS	0.19	0.15	0.13	0.11	V-ns
(CK, CK#, DQ, DQS, DQS#, DM)					

Notes:

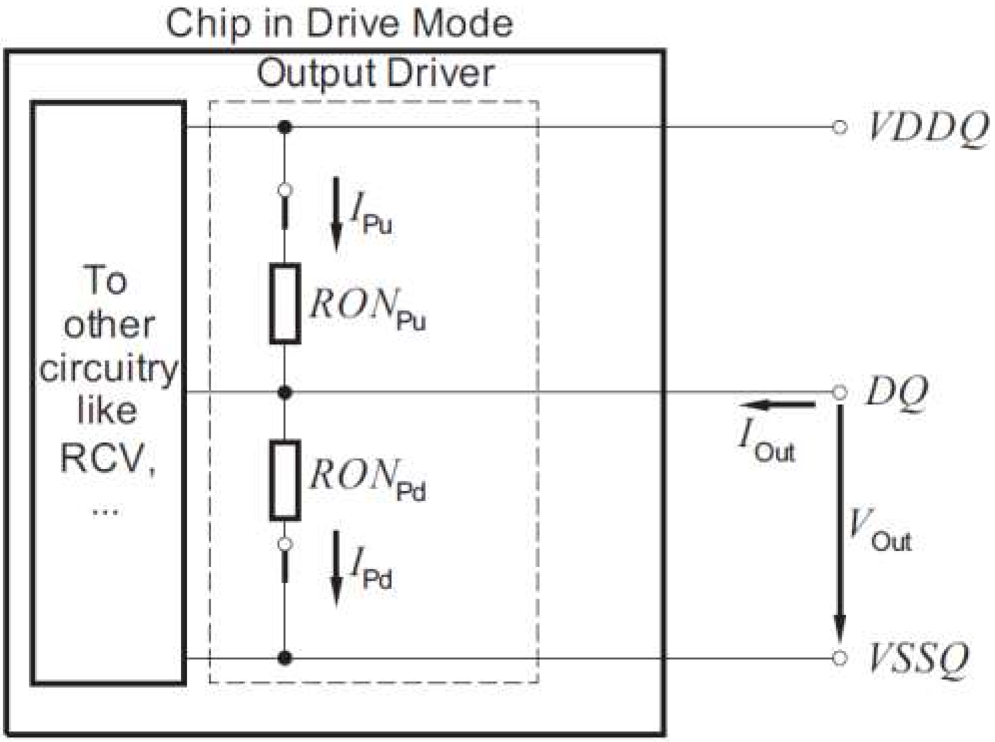
1. The sum of the applied voltage (VDD) and peak amplitude overshoot voltage is not to exceed absolute maximum DC ratings
2. The sum of applied voltage (VDD) and the peak amplitude undershoot voltage is not to exceed absolute maximum DC ratings



34 Ohm Output Driver DC Electrical Characteristics

A Functional representation of the output buffer is shown as below. Output driver impedance RON is defined by the value of the external reference resistor RZQ as follows:
RON34 = RZQ / 7 (nominal 34.4ohms +/-10% with nominal RZQ=240ohms)
The individual pull-up and pull-down resistors (RONPu and RONPd) are defined as follows:
RONPu = [VDDQ-Vout] / l Iout l ------------------- under the condition that RONPd is turned off (1)
RONPd = Vout / l Iout l -------------------------------under the condition that RONPu is turned off (2)

Output Driver: Definition of Voltages and Currents



Output Driver DC Electrical Characteristics, assuming RZQ = 240ohms; entire operating temperature range; after proper ZQ calibration

RONNom	Resistor	Vout	Min.	Nom.	Max.	Units	Notes
DDR3							
34 ohms	RON34Pd	VOLdc = 0.2 x VDDQ	0.6	1.0	1.1	RZQ/7	1,2,3
		VOMdc = 0.5 x VDDQ	0.9	1.0	1.1	RZQ/7	1,2,3
		VOHdc = 0.8 x VDDQ	0.9	1.0	1.4	RZQ/7	1,2,3
	RON34Pu	VOLdc = 0.2 x VDDQ	0.9	1.0	1.4	RZQ/7	1,2,3
		VOMdc = 0.5 x VDDQ	0.9	1.0	1.1	RZQ/7	1,2,3
		VOHdc = 0.8 x VDDQ	0.6	1.0	1.1	RZQ/7	1,2,3
40 ohms	RON40pd	VOLdc = 0.2 × VDDQ	0.6	1.0	1.1	RZQ/6	1,2,3
		VOMdc = 0.5 × VDDQ	0.9	1.0	1.1	RZQ/6	1,2,3
		VOHdc = 0.8 × VDDQ	0.9	1.0	1.4	RZQ/6	1,2,3
	RON40pu	VOLdc = 0.2 × VDDQ	0.9	1.0	1.4	RZQ/6	1,2,3
		VOMdc = 0.5 × VDDQ	0.9	1.0	1.1	RZQ/6	1,2,3
		VOHdc = 0.8 × VDDQ	0.6	1.0	1.1	RZQ/6	1,2,3
Mismatch between pull-up and pull-down, MMPuPd		VOMdc = 0.5 x VDDQ	-10		+10	%	1,2,4
DDR3L							
34 ohms	RON34Pd	VOLdc = 0.2 x VDDQ	0.6	1.0	1.15	RZQ/7	1,2,3
		VOMdc = 0.5 x VDDQ	0.9	1.0	1.15	RZQ/7	1,2,3
		VOHdc = 0.8 x VDDQ	0.9	1.0	1.45	RZQ/7	1,2,3
	RON34Pu	VOLdc = 0.2 x VDDQ	0.9	1.0	1.45	RZQ/7	1,2,3
		VOMdc = 0.5 x VDDQ	0.9	1.0	1.15	RZQ/7	1,2,3
		VOHdc = 0.8 x VDDQ	0.6	1.0	1.15	RZQ/7	1,2,3
40 ohms	RON40pd	VOLdc = 0.2 × VDDQ	0.6	1.0	1.15	RZQ/6	1,2,3
		VOMdc = 0.5 × VDDQ	0.9	1.0	1.15	RZQ/6	1,2,3
		VOHdc = 0.8 × VDDQ	0.9	1.0	1.45	RZQ/6	1,2,3
	RON40pu	VOLdc = 0.2 × VDDQ	0.9	1.0	1.45	RZQ/6	1,2,3
		VOMdc = 0.5 × VDDQ	0.9	1.0	1.15	RZQ/6	1,2,3
		VOHdc = 0.8 × VDDQ	0.6	1.0	1.15	RZQ/6	1,2,3
Mismatch between pull-up and pull-down, MMPuPd		VOMdc = 0.5 x VDDQ	-10		+10	%	1,2,4

Notes:

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
2. The tolerance limits are specified under the condition that VDDQ = VDD and that VSSQ = VSS.
3. Pull-down and pull-up output driver impedances are recommended to be calibrated at 0.5 x VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above. e.g. calibration at 0.2 x VDDQ and 0.8 x VDDQ.
4. Measurement definition for mismatch between pull-up and pull-down, MMPuPd:

   Measure RONPu and RONPd, but at 0.5 x VDDQ:

$$MM_{PuPd} = \frac{Ron_{Pu} - Ron_{Pd}}{Ron_{Nom}} \times 100$$

Output Driver Temperature and Voltage Sensitivity

If temperature and/or voltage after calibration, the tolerance limits widen according to the following table.
Delta T = T - T(@calibration); Delta V = VDDQ - VDDQ(@calibration); VDD = VDDQ
Note: dRONdT and dRONdV are not subject to production test but are verified by design and characterization.

Output Driver Sensitivity Definition

Item	Min.	Max.	Units
RONPU@VOHdc	0.6 - dRONdTH*lDelta Tl - dRONdVH*lDelta Vl	1.1 + dRONdTH*lDelta Tl - dRONdVH*lDelta Vl	RZQ/7
RON@VOMdc	0.9 - dRONdTM*lDelta Tl - dRONdVM*lDelta Vl	1.1 + dRONdTM*lDelta Tl - dRONdVM*lDelta Vl	RZQ/7
RONPD@VOLdc	0.6 - dRONdTL*lDelta Tl - dRONdVL*lDelta Vl	1.1 + dRONdTL*lDelta Tl - dRONdVL*lDelta Vl	RZQ/7

Output Driver Voltage and Temperature Sensitivity

Speed Bin	DDR3-1066/1333		DDR3-1600/1866		Units
Item	Min	Max	Min	Max	
dRONdTM	0	1.5	0	1.5	%/°C
dRONdVM	0	0.15	0	0.13	%/mV
dRONdTL	0	1.5	0	1.5	%/°C
dRONdVL	0	0.15	0	0.13	%/mV
dRONdTH	0	1.5	0	1.5	%/°C
dRONdVH	0	0.15	0	0.13	%/mV

Note:
These parameters may not be subject to production test. They are verified by design and characterization.

On-Die Termination (ODT) Levels and I-V Characteristics

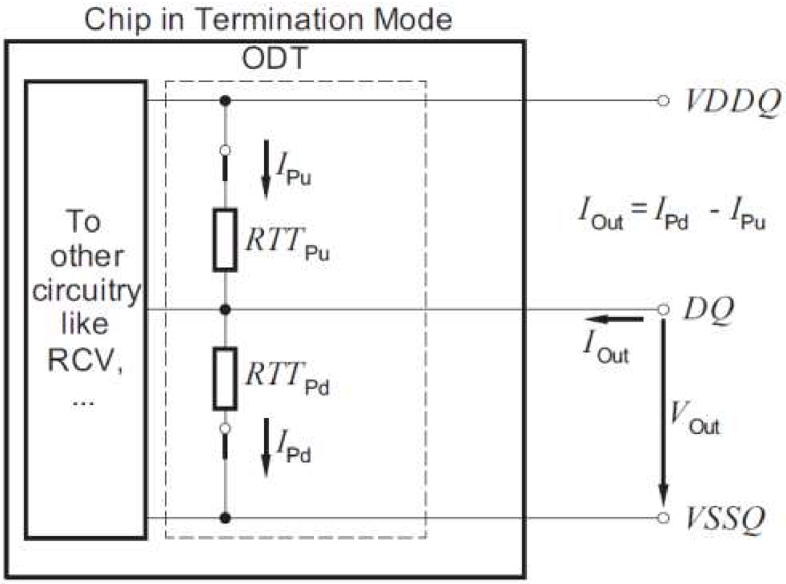
On-Die Termination effective resistance RTT is defined by bits A9, A6, and A2 of the MR1 Register.
ODT is applied to the DQ, DM, DQS, DQS pins.

A functional representation of the on-die termination is shown in the following figure. The individual pull-up and pull-down resistors (RTTPu and RTTPd) are defined as follows:

$$RTT_{Pu} = \frac{VDDQ - V_{Out}}{|\, I_{Out} \,|} \qquad \text{under the condition that RTTPd is turned off (3)}$$

$$RTT_{Pd} = \frac{V_{Out}}{|\, I_{Out} \,|} \qquad \text{under the condition that RTTPu is turned off (4)}$$

On-Die Termination: Definition of Voltages and Currents



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ODT DC Electrical Characteristics

The following table provides an overview of the ODT DC electrical characteristics. The values for RTT60Pd120, RTT60Pu120, RTT120Pd240, RTT120Pu240, RTT40Pd80, RTT40Pu80, RTT30Pd60, RTT30Pu60, RTT20Pd40, RTT20Pu40 are not specification requirements, but can be used as design guide lines:

ODT DC Electrical Characteristics, assuming RZQ = 240ohms +/- 1% entire operating temperature range; after proper ZQ calibration (DDR3L)

MR1 [A9,A6,A2]	RTT	Resistor	Vout	Min	Nom	Max	Units	Notes
0,1,0	120Ω	RTT120Pd240	VOLdc = 0.2 x VDDQ	0.6	1.0	1.15	RZQ	1,2,3,4
			0.5 x VDDQ	0.9	1.0	1.15	RZQ	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.9	1.0	1.45	RZQ	1,2,3,4
		RTT120Pu240	VOLdc = 0.2 x VDDQ	0.9	1.0	1.45	RZQ	1,2,3,4
			0.5 x VDDQ	0.9	1.0	1.15	RZQ	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.9	1.0	1.15	RZQ	1,2,3,4
		RTT120	VIL(ac) to VIH(ac)	0.9	1.0	1.65	RZQ	1,2,5
0, 0,1	60Ω	RTT60Pd120	VOLdc = 0.2 x VDDQ	0.6	1.0	1.15	RZQ/2	1,2,3,4
			0.5 x VDDQ	0.9	1.0	1.15	RZQ/2	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.9	1.0	1.45	RZQ/2	1,2,3,4
		RTT60Pu120	VOLdc = 0.2 x VDDQ	0.9	1.0	1.45	RZQ/2	1,2,3,4
			0.5 x VDDQ	0.9	1.0	1.15	RZQ/2	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.6	1.0	1.15	RZQ/2	1,2,3,4
		RTT60	VIL(ac) to VIH(ac)	0.9	1.0	1.65	RZQ/4	1,2,5
0, 1, 1	40Ω	RTT40Pd80	VOLdc = 0.2 x VDDQ	0.6	1.0	1.15	RZQ/3	1,2,3,4
			0.5 x VDDQ	0.9	1.0	1.15	RZQ/3	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.9	1.0	1.45	RZQ/3	1,2,3,4
		RTT40Pu80	VOLdc = 0.2 x VDDQ	0.9	1.0	1.45	RZQ/3	1,2,3,4
			0.5 x VDDQ	0.9	1.0	1.15	RZQ/3	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.6	1.0	1.15	RZQ/3	1,2,3,4
		RTT40	VIL(ac) to VIH(ac)	0.9	1.0	1.65	RZQ/6	1,2,5
1, 0,1	30Ω	RTT30Pd60	VOLdc = 0.2 x VDDQ	0.6	1.0	1.15	RZQ/4	1,2,3,4
			0.5 x VDDQ	0.9	1.0	1.15	RZQ/4	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.9	1.0	1.45	RZQ/4	1,2,3,4
		RTT30Pu60	VOLdc = 0.2 x VDDQ	0.9	1.0	1.45	RZQ/4	1,2,3,4
			0.5 x VDDQ	0.9	1.0	1.15	RZQ/4	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.6	1.0	1.15	RZQ/4	1,2,3,4
		RTT30	VIL(ac) to VIH(ac)	0.9	1.0	1.65	RZQ/6	1,2,5
1, 0, 0	20Ω	RTT20Pd40	VOLdc = 0.2 x VDDQ	0.6	1.0	1.15	RZQ/6	1,2,3,4
			0.5 x VDDQ	0.9	1.0	1.15	RZQ/6	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.9	1.0	1.45	RZQ/6	1,2,3,4
		RTT20Pu40	VOLdc = 0.2 x VDDQ	0.9	1.0	1.45	RZQ/6	1,2,3,4
			0.5 x VDDQ	0.9	1.0	1.45	RZQ/6	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.6	1.0	1.15	RZQ/6	1,2,3,4
		RTT20	VIL(ac) to VIH(ac)	0.9	1.0	1.65	RZQ/12	1,2,5
Deviation of VM w.r.t. VDDQ/2, DVM				-5		+5	%	1,2,5,6

ODT DC Electrical Characteristics, assuming RZQ = 240ohms +/- 1% entire operating temperature range; after proper ZQ calibration (DDR3)

MR1 [A9,A6,A2]	RTT	Resistor	Vout	Min	Nom	Max	Units	Notes
0,1,0	120Ω	RTT120Pd240	VOLdc = 0.2 x VDDQ	0.6	1.0	1.1	RZQ	1,2,3,4
			0.5 x VDDQ	0.9	1.0	1.1	RZQ	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.9	1.0	1.4	RZQ	1,2,3,4
		RTT120Pu240	VOLdc = 0.2 x VDDQ	0.9	1.0	1.4	RZQ	1,2,3,4
			0.5 x VDDQ	0.9	1.0	1.1	RZQ	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.9	1.0	1.1	RZQ	1,2,3,4
		RTT120	VIL(ac) to VIH(ac)	0.9	1.0	1.6	RZQ	1,2,5
0, 0,1	60Ω	RTT60Pd120	VOLdc = 0.2 x VDDQ	0.6	1.0	1.1	RZQ/2	1,2,3,4
			0.5 x VDDQ	0.9	1.0	1.1	RZQ/2	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.9	1.0	1.4	RZQ/2	1,2,3,4
		RTT60Pu120	VOLdc = 0.2 x VDDQ	0.9	1.0	1.4	RZQ/2	1,2,3,4
			0.5 x VDDQ	0.9	1.0	1.1	RZQ/2	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.6	1.0	1.1	RZQ/2	1,2,3,4
		RTT60	VIL(ac) to VIH(ac)	0.9	1.0	1.6	RZQ/4	1,2,5
0, 1, 1	40Ω	RTT40Pd80	VOLdc = 0.2 x VDDQ	0.6	1.0	1.1	RZQ/3	1,2,3,4
			0.5 x VDDQ	0.9	1.0	1.1	RZQ/3	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.9	1.0	1.4	RZQ/3	1,2,3,4
		RTT40Pu80	VOLdc = 0.2 x VDDQ	0.9	1.0	1.4	RZQ/3	1,2,3,4
			0.5 x VDDQ	0.9	1.0	1.1	RZQ/3	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.6	1.0	1.1	RZQ/3	1,2,3,4
		RTT40	VIL(ac) to VIH(ac)	0.9	1.0	1.6	RZQ/6	1,2,5
1, 0,1	30Ω	RTT30Pd60	VOLdc = 0.2 x VDDQ	0.6	1.0	1.1	RZQ/4	1,2,3,4
			0.5 x VDDQ	0.9	1.0	1.1	RZQ/4	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.9	1.0	1.4	RZQ/4	1,2,3,4
		RTT30Pu60	VOLdc = 0.2 x VDDQ	0.9	1.0	1.4	RZQ/4	1,2,3,4
			0.5 x VDDQ	0.9	1.0	1.1	RZQ/4	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.6	1.0	1.6	RZQ/4	1,2,3,4
		RTT30	VIL(ac) to VIH(ac)	0.9	1.0	1.1	RZQ/6	1,2,5
1, 0, 0	20Ω	RTT20Pd40	VOLdc = 0.2 x VDDQ	0.6	1.0	1.1	RZQ/6	1,2,3,4
			0.5 x VDDQ	0.9	1.0	1.1	RZQ/6	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.9	1.0	1.4	RZQ/6	1,2,3,4
		RTT20Pu40	VOLdc = 0.2 x VDDQ	0.9	1.0	1.4	RZQ/6	1,2,3,4
			0.5 x VDDQ	0.9	1.0	1.1	RZQ/6	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.6	1.0	1.1	RZQ/6	1,2,3,4
		RTT20	VIL(ac) to VIH(ac)	0.9	1.0	1.6	RZQ/12	1,2,5
Deviation of VM w.r.t. VDDQ/2, DVM				-5		+5	%	1,2,5,6

Notes:

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
2. The tolerance limits are specified under the condition that VDDQ = VDD and that VSSQ = VSS.
3. Pull-down and pull-up ODT resistors are recommended to be calibrated at 0.5 x VDDQ. Other calibration may be used to achieve the linearity spec shown above.
4. Not a specification requirement, but a design guide line.
5. Measurement definition for RTT:

   Apply VIH(ac) to pin under test and measure current / (VIH(ac)), then apply VIL(ac) to pin under test and measure current / (VIL(ac)) respectively.

$$RTT = \frac{VIH(ac) - VIL(ac)}{I(VIH(ac)) - I(VIL(ac))}$$

6. Measurement definition for VM and DVM:
   Measure voltage (VM) at test pin (midpoint) with no lead:

$$\triangle VM = \left(\frac{2 \times VM}{VDDQ} - 1 \right) \times 100$$

ODT Temperature and Voltage sensitivity

If temperature and/or voltage after calibration, the tolerance limits widen according to the following table.
Delta T = T - T(@calibration); Delta V = VDDQ - VDDQ(@calibration); VDD = VDDQ

ODT Sensitivity Definition

Item	Min.	Max.	Units
RTT	0.9 - dRTTdT*|Delta T| - dRTTdV*|Delta V|	1.6 + dRTTdT*|Delta T| + dRTTdV*|Delta V|	RZQ/2,4,6,8,12

ODT Voltage and Temperature Sensitivity

Item	Min.	Max.	Units
dRTTdT	0	1.5	%/°C
dRTTdV	0	0.15	%/mV

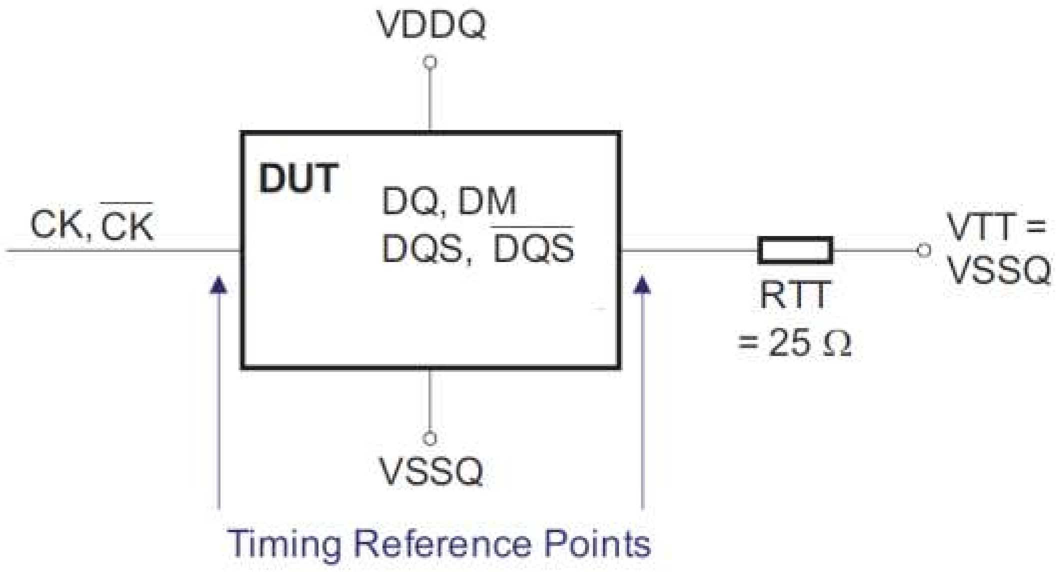
Note:

These parameters may not be subject to production test. They are verified by design and characterization.

Test Load for ODT Timings

Different than for timing measurements, the reference load for ODT timings is defined in the following figure.

ODT Timing Reference Load



ODT Timing Definitions

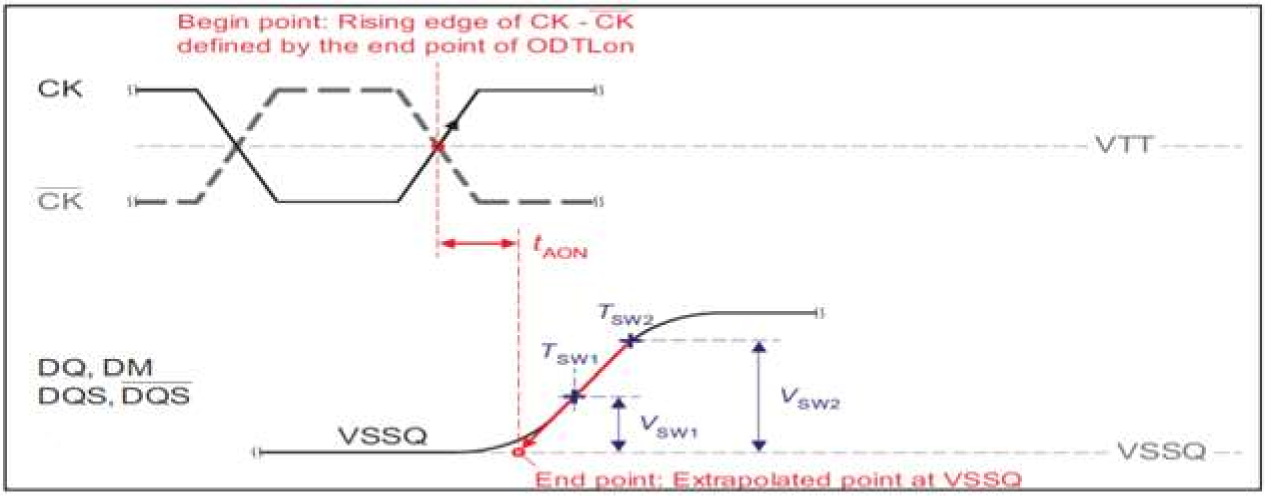
Definitions for tAON, tAONPD, tAOF, tAOFPD, and tADC are provided in the following table and subsequent figures.

Symbol	Begin Point Definition	End Point Definition
tAON	Rising edge of CK - CK defined by the end point of ODTL	Extrapolated point at VSSQ
tAONPD	Rising edge of CK - CK with ODT being first registered high	Extrapolated point at VSSQ
tAOF	Rising edge of CK - CK defined by the end point of ODTLoff	End point: Extrapolated point at VRTT_Nom
tAOFPD	Rising edge of CK - CK with ODT being first registered low	End point: Extrapolated point at VRTT_Nom
tADC	Rising edge of CK - CK defined by the end point of ODTLcnw, ODTLcwn4, or ODTLcwn8	End point: Extrapolated point at VRTT_Wr and VRTT_Nom respectively

Reference Settings for ODT Timing Measurements

Measured Parameter	RTT_Nom	RTT_Wr	DDR3		DDR3L	
			VSW1[V]	VSW2[V]	VSW1[V]	VSW2[V]
tAON	RZQ/4	NA	0.05	0.10	0.05	0.10
	RZQ/12	NA	0.10	0.20	0.10	0.20
tAONPD	RZQ/4	NA	0.05	0.10	0.05	0.10
	RZQ/12	NA	0.10	0.20	0.10	0.20
tAOF	RZQ/4	NA	0.05	0.10	0.05	0.10
	RZQ/12	NA	0.10	0.20	0.10	0.20
tAOFPD	RZQ/4	NA	0.05	0.10	0.05	0.10
	RZQ/12	RZQ/2	0.10	0.20	0.10	0.20
tADC	RZQ/12	RZQ/2	0.20	0.30	0.20	0.25

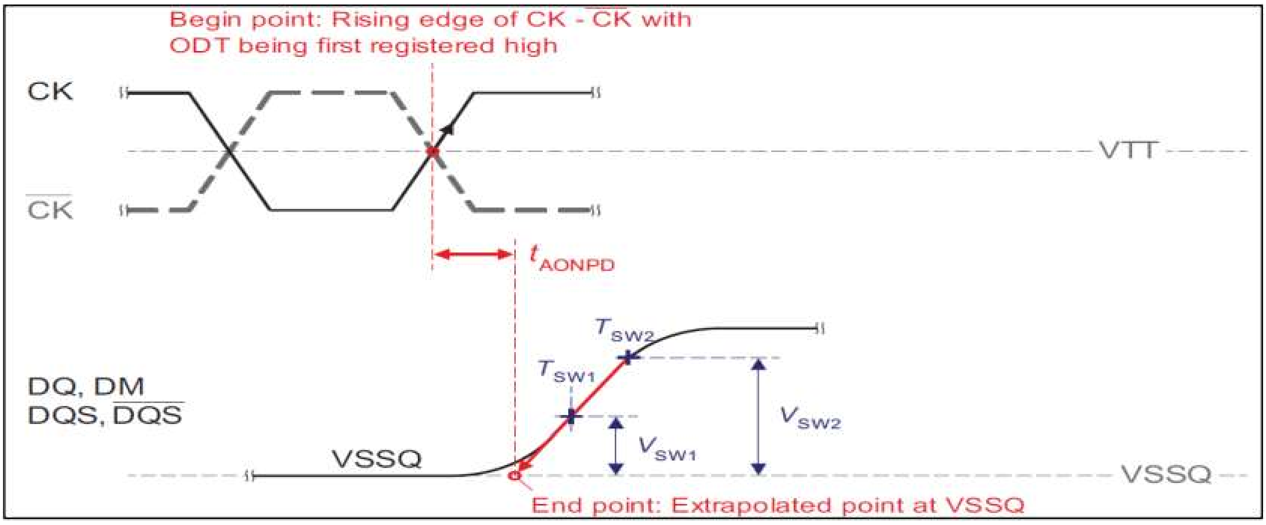
Definition of tAON



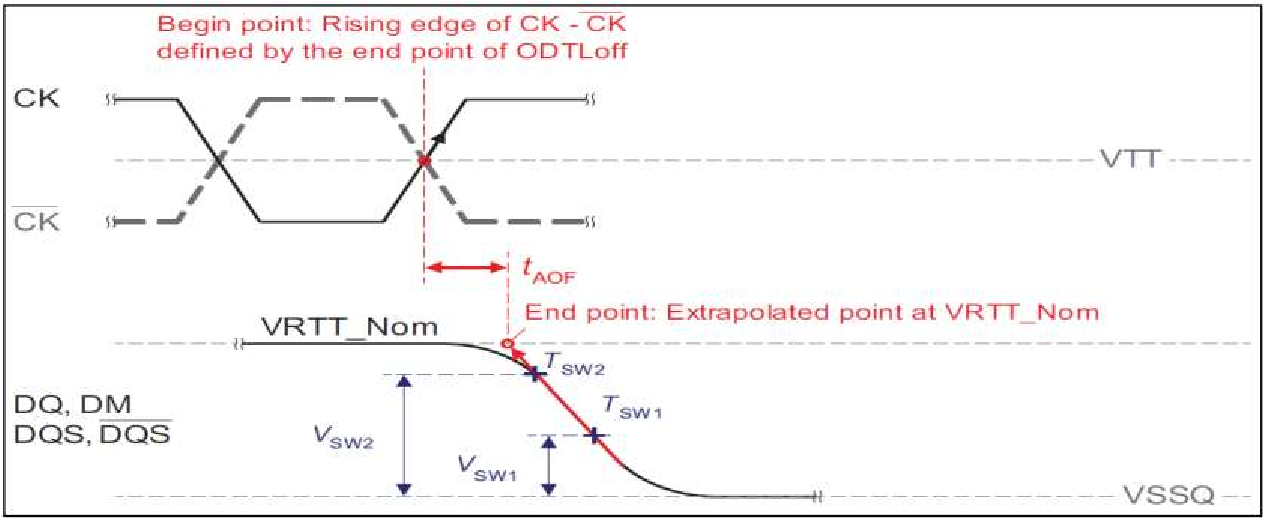
Begin point: Rising edge of CK - $\overline{CK}$ defined by the end point of ODTLon

End point: Extrapolated point at VSSQ

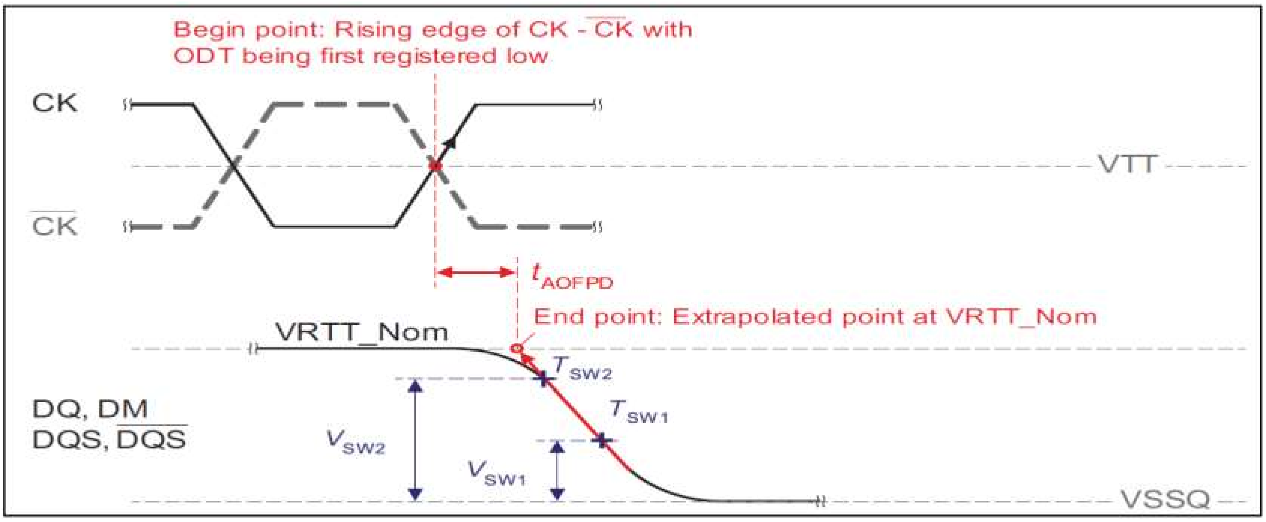
Definition of tAONPD



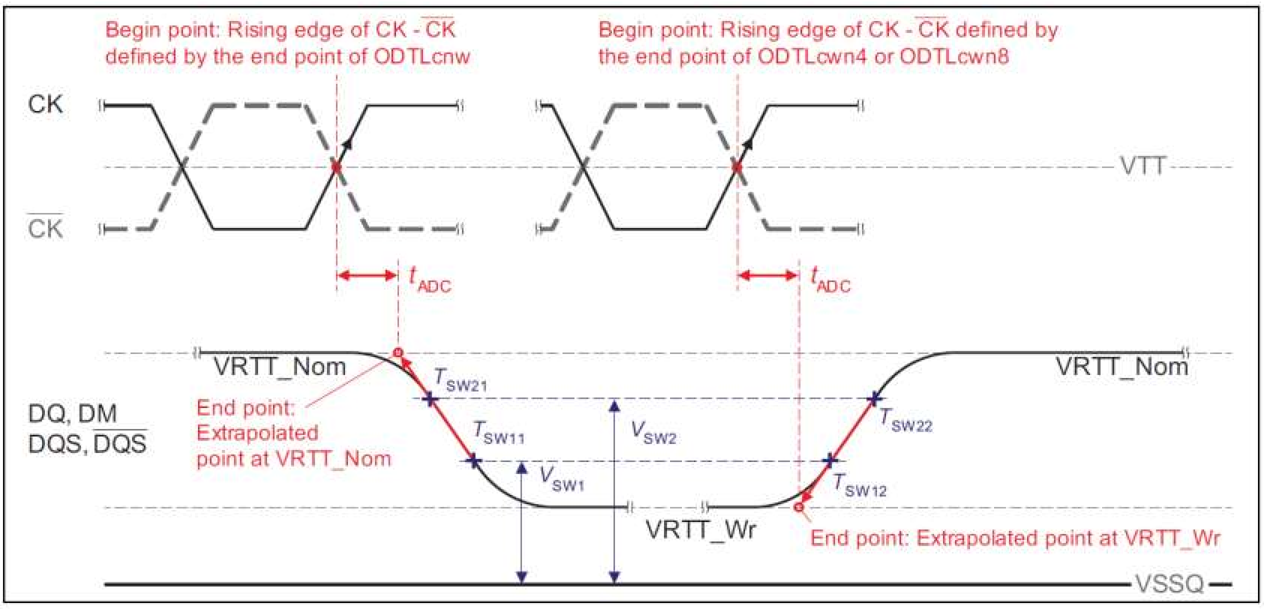
Definition of tAOF



Definition of tAOFPD



Definition of tADC



Input / Output Capacitance

Symbol	Parameter	DDR3L-1066		DDR3L-1333		DDR3L-1600		DDR3L-1866		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
CIO (DDR3)	Input/output capacitance (DQ, DM, DQS, DQS#)	1.2	2.7	1.2	2.5	1.2	2.3	1.2	2.2	pF	1,2,3
CIO (DDR3L)		1.2	2.5	1.2	2.3	1.2	2.3	1.2	2.1	pF	1,2,3
CCK	Input capacitance delta, CK and CK#	0.6	1.6	0.6	1.4	0.6	1.4	0.6	1.3	pF	2,3
CDCK	Input capacitance delta, CK and CK#	0	0.15	0	0.15	0	0.15	0	0.15	pF	2,3,4
CDDQS	Input/output capacitance delta, DQS and DQS#	0	0.2	0	0.15	0	0.15	0	0.15	pF	2,3,5
CI (DDR3)	Input capacitance, (CTRL, ADD, CMD input-only pins)	0.55	1.35	0.55	1.3	0.55	1.3	0.55	1.2	pF	2,3,6
CI (DDR3L)		0.55	1.3	0.55	1.3	0.55	1.2	0.55	1.2	pF	2,3,6
CDI_CTRL	Input capacitance delta, All CTRL input-only pins	-0.5	0.3	-0.4	0.2	-0.4	0.2	-0.4	0.2	pF	2,3,7,8
CDI_ADD_CMD	Input capacitance delta, All ADD/CMD input-only pins	-0.5	0.5	-0.4	0.4	-0.4	0.4	-0.4	0.4	pF	2,3,9, 10
CDIO	Input/output capacitance delta, DQ, DM, DQS, DQS#	-0.5	0.3	-0.5	0.3	-0.5	0.3	-0.5	0.3	pF	2,3,11
CZQ	Input/output capacitance of ZQ pin	-	3	-	3	-	3	-	3	pF	2,3,12

Notes:

1. Although the DM pins have different functions, the loading matches DQ and DQS.

2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147("PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER(VNA)") with VDD, VDDQ, VSS, VSSQ applied and all other pins floating (except the pin under test, CKE, RESET and ODT as necessary).

   VDD=VDDQ=1.5V, VBIAS=VDD/2 and ondie termination off.
3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
4. Absolute value of CCK-CCK
5. Absolute value of CIO(DQS)-CIO(DQS#).
6. CI applies to ODT, CS, CKE, A0-A15, BA0-BA2, RAS#, CAS#,WE#.
7. CDI_CTRL applies to ODT, CS# and CKE
8. CDI_CTRL=CI(CTRL)-0.5*(CI(CLK)+CI(CLK#))
9. CDI_ADD_CMD applies to A0-A15, BA0-BA2, RAS#, CAS# and WE#
10. CDI_ADD_CMD=CI(ADD_CMD) - 0.5*(CI(CLK)+CI(CLK#))
11. CDIO=CIO(DQ,DM) - 0.5*(CIO(DQS)+CIO(DQS#))
12. Maximum external load capacitance on ZQ pin: 5 pF.

4.17 IDD Specifications and Measurement Conditions

IDD Specifications (DDR3L)

Symbol	Parameter	Width	DDR3L-1600 11-11-11	DDR3L-1866 13-13-13	Units
IDD0	Operating Current 0 One Bank Activate -> Precharge	x16	TBD	TBD	mA
IDD1	Operating Current 1 One Bank Activate -> Read -> Precharge	x16	TBD	TBD	mA
IDD2P0	Precharge Power-Down Current Slow Exit - MR0 bit A12 = 0	x16	TBD	TBD	mA
IDD2P1	Precharge Power-Down Current Fast Exit - MR0 bit A12 = 1	x16	TBD	TBD	mA
IDD2Q	Precharge Quiet Standby Current	x16	TBD	TBD	mA
IDD2N	Precharge Standby Current	x16	TBD	TBD	mA
IDD2NT	Precharge Standby ODT Current	x16	TBD	TBD	mA
IDD3N	Active Standby Current	x16	TBD	TBD	mA
IDD3P	Active Power-Down Current Always Fast Exit	x16	TBD	TBD	mA
IDD4R	Operating Current Burst Read	x16	TBD	TBD	mA
IDD4W	Operating Current Burst Write	x16	TBD	TBD	mA
IDD5B	Burst Refresh Current	x16	TBD	TBD	mA
IDD6	Self-Refresh Current Normal	x16	TBD	TBD	mA
IDD6ET	Self-Refresh Current Extended	x16	TBD	TBD	mA
IDD7	All Bank Interleave Read Current	x16	TBD	TBD	mA
IDD8	RESET Low Current	x16	TBD	TBD	mA

Notes:

1. TC = 85°C; SRT and ASR are disabled.
2. Enabling ASR could increase IDDx by up to an additional 2mA.
3. Restricted to TC (MAX) = 85°C.
4. TC = 85°C; ASR and ODT are disabled; SRT is enabled.
5. When TC > +95°C: all IDDx values must be derated (increased) by 30% from the 85°C specifications.
6. When TC > +105°C: all IDDx values must be derated (increased) by 50% from the 85°C specifications.
7. When TC >105°C: 8X refresh is required, self refresh mode is not available.

IDD Specifications (DDR3)

Symbol	Parameter	Width	DDR3-1600 11-11-11	DDR3-1866 13-13-13	Unit
IDD0	Operating Current 0 One Bank Activate -> Precharge	x16	TBD	TBD	mA
IDD1	Operating Current 1 One Bank Activate -> Read ->Precharge	x16	TBD	TBD	mA
IDD2P0	Precharge Power-Down Current Slow Exit - MR0 bit A12 = 0	x16	TBD	TBD	mA
IDD2P1	Precharge Power-Down Current Fast Exit - MR0 bit A12 = 1	x16	TBD	TBD	mA
IDD2Q	Precharge Quiet Standby Current	x16	TBD	TBD	mA
IDD2N	Precharge Standby Current	x16	TBD	TBD	mA
IDD2NT	Precharge Standby ODT Current	x16	TBD	TBD	mA
IDD3N	Active Standby Current	x16	TBD	TBD	mA
IDD3P	Active Power-Down Current Always Fast Exit	x16	TBD	TBD	mA
IDD4R	Operating Current Burst Read	x16	TBD	TBD	mA
IDD4W	Operating Current Burst Write	x16	TBD	TBD	mA
IDD5B	Burst Refresh Current	x16	TBD	TBD	mA
IDD6	Self-Refresh Current Normal	x16	TBD	TBD	mA
IDD6ET	Self-Refresh Current Extended	x16	TBD	TBD	mA
IDD7	All Bank Interleave Read Current	x16	TBD	TBD	mA
IDD8	RESET Low Current	x16	TBD	TBD	mA

Notes

1. TC = 85°C; SRT and ASR are disabled.
2. Enabling ASR could increase IDDx by up to an additional 2mA.
3. Restricted to TC (MAX) = 85°C.
4. TC = 85°C; ASR and ODT are disabled; SRT is enabled.
5. When TC > +95°C: all IDDx values must be derated (increased) by 30% from the 85°C specifications.
6. When TC > +105°C: all IDDx values must be derated (increased) by 50% from the 85°C specifications.
7. When TC >105°C: 8X refresh is required, self refresh mode is not available.

IDD Measurement Conditions

Symbol	Parameter
IDD0	Operating One Bank Active-Precharge Current CKE: High; External clock: On; tCK, nRC, nRAS, CL: see the table of Timings used for IDD and IDDQ; BL: 8(1); AL: 0; CS#: High between ACT and PRE; Command, Address, Bank Address Inputs: partially toggling; Data IO: MID-LEVEL; DM:stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers(2); ODT Signal: stable at 0;
IDD1	Operating One Bank Active-Read-Precharge Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: see see the table of Timings used for IDD and IDDQ; BL: 8(1,7); AL:0; CS#: High between ACT, RD and PRE; Command, Address, Bank Address Inputs, Data IO: partially toggling; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers(2); ODT Signal: stable at 0;
IDD2N	Precharge Standby Current CKE: High; External clock: On; tCK, CL: see the table of Timings used for IDD and IDDQ; BL: 8(1); AL: 0; CS#: stable at 1; Command, Address, Bank Address Inputs: partially toggling; Data IO: MID-LEVEL; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers(2); ODT Signal: stable at 0;
IDD2P0	Precharge Power-Down Current Slow Exit CKE: Low; External clock: On; tCK, CL: see the table of Timings used for IDD and IDDQ; BL: 8(1); AL: 0; CS#: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID-LEVEL; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers(2); ODT Signal: stable at 0; Pecharge Power Down Mode: Slow Exit(3)
IDD2P1	Precharge Power-Down Current Fast Exit CKE: Low; External clock: On; tCK, CL: see the table of Timings used for IDD and IDDQ; BL: 8(1); AL: 0; CS#: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID-LEVEL; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers(2); ODT Signal: stable at 0; Pecharge Power Down Mode: Fast Exit(3)

IDD Measurement Conditions (continue)

Symbol	Parameter
IDD2Q	Precharge Quiet Standby Current CKE: High; External clock: On; tCK, CL: see the table of Timings used for IDD and IDDQ; BL: 8(1); AL: 0; CS#: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID-LEVEL; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers(2); ODT Signal: stable at 0
IDD3N	Active Standby Current CKE: High; External clock: On; tCK, CL: see the table of Timings used for IDD and IDDQ; BL: 8(1); AL: 0; CS#: stable at 1; Command, Address, Bank Address Inputs: partially toggling; Data IO: MID-LEVEL; DM:stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers(2); ODT Signal: stable at 0;
IDD3P	Active Power-Down Current CKE: Low; External clock: On; tCK, CL: see the table of Timings used for IDD and IDDQ; BL: 8(1); AL: 0; CS#: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID-LEVEL; DM:stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers(2); ODT Signal: stable at 0
IDD4R	Operating Burst Read Current CKE: High; External clock: On; tCK, CL: see the table of Timings used for IDD and IDDQ; BL: 8(1,7); AL: 0; CS#: High between RD; Command, Address, Bank Address Inputs: partially toggling; Data IO: seamless read data burst with different data between one burst and the next one; DM:stable at 0; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers(2); ODT Signal: stable at 0;

IDD Measurement Conditions (continue)

Symbol	Parameter
IDD4W	**Operati**ng Burst Write Current CKE: High; External clock: On; tCK, CL: see the table of Timings used for IDD and IDDQ; BL: 8(1); AL: 0; CS#: High between WR; Command, Address, Bank Address Inputs: partially toggling; Data IO: seamless write data burst with different data between one burst and the next one ; DM: stable at 0; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers(2); ODT Signal: stable at HIGH;
IDD5B	Burst Refresh Current CKE: High; External clock: On; tCK, CL, nRFC: see the table of Timings used for IDD and IDDQ; BL: 8(1); AL: 0; CS#: High between REF; Command, Address, Bank Address Inputs: partially toggling; Data IO: MID-LEVEL; DM:stable at 0; Bank Activity: REF command every nRFC; Output Buffer and RTT: Enabled in Mode Registers(2); ODT Signal: stable at 0;
IDD6	Self Refresh Current: Normal Temperature Range TCASE: 0 - 85°C; Auto Self-Refresh (ASR): Disabled(4); Self-Refresh Temperature Range (SRT):Normal(5); CKE: Low; External clock: Off; CK and CK#: LOW; CL: see the table of Timings used for IDD and IDDQ; BL: 8(1);AL: 0; CS#, Command, Address, Bank Address, Data IO: MID-LEVEL; DM:stable at 0; Bank Activity:Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers(2); ODT Signal: MID-LEVEL
IDD6ET	Self-Refresh Current: Extended Temperature Range (optional)(6) TCASE: 0 - 95°C; Auto Self-Refresh (ASR): Disabled(4); Self-Refresh Temperature Range (SRT):Extended(5); CKE: Low; External clock: Off; CK and CK#: LOW; CL: see the table of Timings used for IDD and IDDQ; BL: 8(1);AL: 0; CS#, Command, Address, Bank Address, Data IO: MID-LEVEL; DM:stable at 0; Bank Activity:Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers(2); ODT Signal: MID-LEVEL

IDD Measurement Conditions (continue)

Symbol	Parameter
IDD6TC	Auto Self-Refresh Current (optional)(6) TCASE: 0 - 95°C; Auto Self-Refresh (ASR): Enabled(4); Self-Refresh Temperature Range (SRT):Normal(5); CKE: Low; External clock: Off; CK and CK#: LOW; CL: see the table of Timings used for IDD and IDDQ; BL: 8(1);AL: 0; CS#, Command, Address, Bank Address, Data IO: MID-LEVEL; DM:stable at 0; Bank Activity:Auto Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers(2); ODT Signal: MIDLEVEL
IDD7	Operating Bank Interleave Read Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: see the table of Timings used for IDD and IDDQ; BL: 8(1,7); AL: CL-1; CS#: High between ACT and RDA; Command, Address, Bank Address Inputs:partially toggling; Data IO: read data bursts with different data between one burst and the next one; DM:stable at 0; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers(2); ODT Signal: stable at 0;
IDD8	RESET Low Current RESET: LOW; External clock: Off; CK and CK#: LOW; CKE: FLOATING; CS#, Command, Address,Bank Address, Data IO: FLOATING; ODT Signal: FLOATING RESET Low current reading is valid once power is stable and RESET has been LOW for at least 1ms.

Notes:

1. Burst Length: BL8 fixed by MRS: set MR0 A[1,0]=00B
2. Output Buffer Enable: set MR1 A[12] = 0B; set MR1 A[5,1] = 01B; RTT_Nom enable: set MR1 A[9,6,2] = 011B; RTT_Wr enable: set MR2 A[10,9] = 10B
3. Pecharge Power Down Mode: set MR0 A12=0B for Slow Exit or MR0 A12=1B for Fast Exit
4. Auto Self-Refresh (ASR): set MR2 A6 = 0B to disable or 1B to enable feature
5. Self-Refresh Temperature Range (SRT): set MR2 A7=0B for normal or 1B for extended temperature range
6. Refer to DRAM supplier data sheet and/or DIMM SPD to determine if optional features or requirements are supported by DDR3 SDRAM device
7. Read Burst Type: Nibble Sequential, set MR0 A[3] = 0B

IDD0 Measurement-Loop Pattern

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1,2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	D#, D#	1	1	1	1	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRAS-1, truncate if necessary												
			nRAS	PRE	0	0	1	0	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRC-1, truncate if necessary												
			1*nRC+0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			1*nRC+1,2	D, D	1	0	0	0	0	0	00	0	0	F	0	-
			1*nRC+3,4	D#, D#	1	1	1	1	0	0	00	0	0	F	0	-
			...	repeat pattern nRC+1,...,4 until 1*nRC+nRAS-1, truncate if necessary												
			1*nRC+nRAS	PRE	0	0	1	0	0	0	00	0	0	F	0	-
			...	repeat nRC+1,...,4 until 2*nRC-1, truncate if necessary												
		1	2*nRC	repeat Sub-Loop 0, use BA[2:0]=1 instead												
		2	4*nRC	repeat Sub-Loop 0, use BA[2:0]=2 instead												
		3	6*nRC	repeat Sub-Loop 0, use BA[2:0]=3 instead												
		4	8*nRC	repeat Sub-Loop 0, use BA[2:0]=4 instead												
		5	10*nRC	repeat Sub-Loop 0, use BA[2:0]=5 instead												
		6	12*nRC	repeat Sub-Loop 0, use BA[2:0]=6 instead												
		7	14*nRC	repeat Sub-Loop 0, use BA[2:0]=7 instead												

Notes:

1. DM must be driven LOW all the time. DQS, DQS# are MID-LEVEL.
2. DQ signals are MID-LEVEL.

IDD 1 Measurement-Loop Pattern

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1,2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	D#, D#	1	1	1	1	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRCD-1, truncate if necessary												
			nRCD	RD	0	1	0	1	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRAS-1, truncate if necessary												
			nRAS	PRE	0	0	1	0	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRC-1, truncate if necessary												
			1*nRC+0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			1*nRC+1,2	D, D	1	0	0	0	0	0	00	0	0	F	0	-
			1*nRC+3,4	D#, D#	1	1	1	1	0	0	00	0	0	F	0	-
			...	repeat pattern nRC+1,...,4 until nRC+nRCD-1, truncate if necessary												
			1*nRC+nRCD	RD	0	1	0	1	0	0	00	0	0	F	0	-
			...	repeat pattern nRC+1,...,4 until nRC+nRAS-1, truncate if necessary												
			1*nRC+nRAS	PRE	0	0	1	0	0	0	00	0	0	F	0	-
			...	repeat nRC+1,...,4 until 2*nRC-1, truncate if necessary												
		1	2*nRC	repeat Sub-Loop 0, use BA[2:0]=1 instead												
		2	4*nRC	repeat Sub-Loop 0, use BA[2:0]=2 instead												
		3	6*nRC	repeat Sub-Loop 0, use BA[2:0]=3 instead												
		4	8*nRC	repeat Sub-Loop 0, use BA[2:0]=4 instead												
		5	10*nRC	repeat Sub-Loop 0, use BA[2:0]=5 instead												
		6	12*nRC	repeat Sub-Loop 0, use BA[2:0]=6 instead												
		7	14*nRC	repeat Sub-Loop 0, use BA[2:0]=7 instead												

Notes:

1. DM must be driven LOW all the time. DQS, DQS# are MID-LEVEL.
2. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID-LEVEL.

IDD2N and IDD3N Measurement-Loop Pattern

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data
toggling	Static High	0	0	D	1	0	0	0	0	0	00	0	0	0	0	-
			1	D	1	0	0	0	0	0	00	0	0	0	0	-
			2	D#	1	1	1	1	0	0	00	0	0	F	0	-
			3	D#	1	1	1	1	0	0	00	0	0	F	0	-
		1	4-7	repeat Sub-Loop 0, use BA[2:0]=1 instead												
		2	8-11	repeat Sub-Loop 0, use BA[2:0]=2 instead												
		3	12-15	repeat Sub-Loop 0, use BA[2:0]=3 instead												
		4	16-19	repeat Sub-Loop 0, use BA[2:0]=4 instead												
		5	20-23	repeat Sub-Loop 0, use BA[2:0]=5 instead												
		6	24-27	repeat Sub-Loop 0, use BA[2:0]=6 instead												
		7	28-31	repeat Sub-Loop 0, use BA[2:0]=7 instead												

Notes:

1. DM must be driven LOW all the time. DQS, DQS# are MID-LEVEL.
2. DQ signals are MID-LEVEL.

IDD4R and IDDQ4R Measurement-Loop Pattern

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data
toggling	Static High	0	0	RD	0	1	0	1	0	0	00	0	0	0	0	00000000
			1	D	1	0	0	0	0	0	00	0	0	0	0	-
			2,3	D#, D#	1	1	1	1	0	0	00	0	0	0	0	-
			4	RD	0	1	0	1	0	0	00	0	0	F	0	00110011
			5	D	1	0	0	0	0	0	00	0	0	F	0	-
			6,7	D#, D#	1	1	1	1	0	0	00	0	0	F	0	-
		1	8-15	repeat Sub-Loop 0, but BA[2:0]=1												
		2	16-23	repeat Sub-Loop 0, but BA[2:0]=2												
		3	24-31	repeat Sub-Loop 0, but BA[2:0]=3												
		4	32-39	repeat Sub-Loop 0, but BA[2:0]=4												
		5	40-47	repeat Sub-Loop 0, but BA[2:0]=5												
		6	48-55	repeat Sub-Loop 0, but BA[2:0]=6												
		7	56-63	repeat Sub-Loop 0, but BA[2:0]=7												

Notes:

1. DM must be driven LOW all the time. DQS, DQS# are used according to RD Commands, otherwise MID-LEVEL.
2. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID-LEVEL.

IDD4W Measurement-Loop Pattern

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data
toggling	Static High	0	0	WR	0	1	0	0	1	0	00	0	0	0	0	00000000
			1	D	1	0	0	0	1	0	00	0	0	0	0	-
			2,3	D#, D#	1	1	1	1	1	0	00	0	0	0	0	-
			4	WR	0	1	0	0	1	0	00	0	0	F	0	00110011
			5	D	1	0	0	0	1	0	00	0	0	F	0	-
			6,7	D#, D#	1	1	1	1	1	0	00	0	0	F	0	-
		1	8-15	repeat Sub-Loop 0, but BA[2:0]=1												
		2	16-23	repeat Sub-Loop 0, but BA[2:0]=2												
		3	24-31	repeat Sub-Loop 0, but BA[2:0]=3												
		4	32-39	repeat Sub-Loop 0, but BA[2:0]=4												
		5	40-47	repeat Sub-Loop 0, but BA[2:0]=5												
		6	48-55	repeat Sub-Loop 0, but BA[2:0]=6												
		7	56-63	repeat Sub-Loop 0, but BA[2:0]=7												

Notes:

1. DM must be driven LOW all the time. DQS, DQS# are used according to WR Commands, otherwise MID-LEVEL.
2. Burst Sequence driven on each DQ signal by Write Command. Outside burst operation, DQ signals are MID-LEVEL.

IDD5B Measurement-Loop Pattern

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data
toggling	Static High	0	0	REF	0	0	0	1	0	0	00	0	0	0	0	-
		1	1,2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	D#, D#	1	1	1	1	0	0	00	0	0	F	0	-
			5…8	repeat cycles 1…4, but BA[2:0]=1												
			9…12	repeat cycles 1…4, but BA[2:0]=2												
			13…16	repeat cycles 1…4, but BA[2:0]=3												
			17…20	repeat cycles 1…4, but BA[2:0]=4												
			21…24	repeat cycles 1…4, but BA[2:0]=5												
			25…28	repeat cycles 1…4, but BA[2:0]=6												
			29…32	repeat cycles 1…4, but BA[2:0]=7												
		2	33 ... nRFC-1	repeat Sub-Loop 1, until nRFC-1. Truncate if necessary												

Notes:

1. DM must be driven Low all the time. DQS, DQS# are MID-LEVEL.
2. DQ signals are MID-LEVEL.

IDD7 Measurement-Loop Pattern

ATTENTION: Sub-Loops 10-19 have inverse A[6:3] Pattern and Data Pattern than Sub-Loops 0-9

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1	RDA	0	1	0	1	0	0	00	1	0	0	0	00000000
			2	D	1	0	0	0	0	0	00	0	0	0	0	-
			...	repeat above D command until nRRD-1												
		1	nRRD	ACT	0	0	1	1	0	1	00	0	0	F	0	-
			nRRD+1	RDA	0	1	0	1	0	1	00	1	0	F	0	00110011
			nRRD+2	D	1	0	0	0	0	1	00	0	0	F	0	-
			...	repeat above D Command until 2*nRRD -1												
		2	2*nRRD	repeat Sub-Loop 0, but BA[2:0] = 2												
		3	3*nRRD	repeat Sub-Loop 1, but BA[2:0] = 3												
		4	4*nRRD	D	1	0	0	0	0	3	00	0	0	F	0	-
			...	Assert and repeat above D Command until nFAW - 1, if necessary												
		5	nFAW	repeat Sub-Loop 0, but BA[2:0] = 4												
		6	nFAW+nRRD	repeat Sub-Loop 1, but BA[2:0] = 5												
		7	nFAW+2*nRRD	repeat Sub-Loop 0, but BA[2:0] = 6												
		8	nFAW+3*nRRD	repeat Sub-Loop 1, but BA[2:0] = 7												
		9	nFAW+4*nRRD	D	1	0	0	0	0	7	00	0	0	F	0	-
				Assert and repeat above D Command until 2 * nFAW - 1, if necessary												
		10	2*nFAW+0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			2*nFAW+1	RDA	0	1	0	1	0	0	00	1	0	F	0	00110011
			2*nFAW+2	D	1	0	0	0	0	0	00	0	0	F	0	-
				Repeat above D Command until 2 * nFAW + nRRD - 1												
		11	2*nFAW+nRRD	ACT	0	0	1	1	0	1	00	0	0	0	0	-
			2*nFAW+nRRD+1	RDA	0	1	0	1	0	1	00	1	0	0	0	00000000
			2*nFAW+nRRD+2	D	1	0	0	0	0	1	00	0	0	0	0	-
				repeat above D Command until 2 * nFAW + 2 * nRRD -1												
		12	2*nFAW+2*nRRD	repeat Sub-Loop 10, but BA[2:0] = 2												
		13	2*nFAW+3*nRRD	repeat Sub-Loop 11, but BA[2:0] = 3												
		14	2*nFAW+4*nRRD	D	1	0	0	0	0	3	00	0	0	0	0	-
				Assert and repeat above D Command until 3 * nFAW - 1, if necessary												
		15	3*nFAW	repeat Sub-Loop 10, but BA[2:0] = 4												
		16	3*nFAW+nRRD	repeat Sub-Loop 11, but BA[2:0] = 5												
		17	3*nFAW+2*nRRD	repeat Sub-Loop 10, but BA[2:0] = 6												
		18	3*nFAW+3*nRRD	repeat Sub-Loop 11, but BA[2:0] = 7												
		19	3*nFAW+4*nRRD	D	1	0	0	0	0	7	00	0	0	0	0	-
				Assert and repeat above D Command until 4 * nFAW - 1, if necessary												

Notes:

1. DM must be driven LOW all the time. DQS, DQS# are used according to RD Commands, otherwise MID-LEVEL.
2. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID-LEVEL.

Fundamental AC Specifications – Operating Frequency

DDR3-1866 and DDR3L-1866

Speed Bin			DDR3(L)-1866		Units
CL-nRCD-nRP			13-13-13		ns
Parameter			Min.	Max.	ns
tCK (Avg)	CL=5	CWL=5	Reserved		ns
		CWL=6/7/8/9	Reserved		ns
	CL=6	CWL=5	2.5	3.3	ns
		CWL=6	Reserved		ns
		CWL=7/8/9	Reserved		ns
	CL=7	CWL=5	Reserved		ns
		CWL=6	1.875	< 2.5	ns
		CWL=7/8/9	Reserved		ns
	CL=8	CWL=5	Reserved		ns
		CWL=6	1.875	< 2.5	ns
		CWL=7	Reserved		ns
		CWL=8/9	Reserved		ns
	CL=9	CWL=5/6	Reserved		ns
		CWL=7	1.5	<1.875	ns
		CWL=8	Reserved		ns
		CWL=9	Reserved		ns
	CL=10	CWL=5/6	Reserved		ns
		CWL=7	1.5	<1.875	ns
		CWL=8/9	Reserved		ns
	CL=11	CWL=5/6/7	Reserved		ns
		CWL=8	1.25	<1.5	ns
		CWL=9	Reserved		ns
	CL=12	CWL=5/6/7/8	Reserved		ns
		CWL=9	Reserved		ns
	CL=13	CWL=5/6/7/8	Reserved		ns
		CWL=9	1.07	<1.25	ns
Supported CL			6,7,8,9,10,11,13		nCK
Supported CWL			5,6,7,8,9		nCK

Fundamental AC Specifications – Operating Frequency

DDR3-1600 and DDR3L-1600

Speed Bin			**DDR3(L)-1600**		**Units**
CL-nRCD-nRP			**11-11-11**		**ns**
Parameter			**Min.**	**Max.**	**ns**
tCK (Avg)	CL=5	CWL=5	3.0	3.3	ns
		CWL=6/7/8	Reserved		ns
	CL=6	CWL=5	2.5	3.3	ns
		CWL=6	Reserved		ns
		CWL=7/8	Reserved		ns
	CL=7	CWL=5	Reserved		ns
		CWL=6	1.875	< 2.5	ns
		CWL=7	Reserved		ns
		CWL=8	Reserved		ns
	CL=8	CWL=5	Reserved		ns
		CWL=6	1.875	< 2.5	ns
		CWL=7	Reserved		ns
		CWL=8	Reserved		ns
	CL=9	CWL=5/6	Reserved		ns
		CWL=7	1.5	<1.875	ns
		CWL=8	Reserved		ns
	CL=10	CWL=5/6	Reserved		ns
		CWL=7	1.5	<1.875	ns
		CWL=8	Reserved		ns
	CL=11	CWL=5/6/7	Reserved		ns
		CWL=8	1.25	<1.5	ns
Supported CL			5,6,7,8,9,10,11		nCK
Supported CWL			5,6,7,8		nCK

Fundamental AC Specifications – Operating Frequency

DDR3-1333 and DDR3L-1333

Speed Bin			DDR3(L)-1333		DDR3(L)-1333		Units
CL-nRCD-nRP			**9-9-9**		**10-10-10**		**ns**
Parameter			**Min.**	**Max.**	**Min.**	**Max.**	**ns**
tCK (Avg)	CL=5	CWL=5	3.0	3.3	3.0	3.3	ns
		CWL=6	Reserved		Reserved		ns
		CWL=7	Reserved		Reserved		ns
	CL=6	CWL=5	2.5	3.3	2.5	3.3	ns
		CWL=6	Reserved		Reserved		ns
		CWL=7	Reserved		Reserved		ns
	CL=7	CWL=5	Reserved		Reserved		ns
		CWL=6	1.875	< 2.5	Reserved		ns
		CWL=7	Reserved		Reserved		ns
	CL=8	CWL=5	Reserved		Reserved		ns
		CWL=6	1.875	< 2.5	1.875	< 2.5	ns
		CWL=7	Reserved		Reserved		ns
	CL=9	CWL=5	Reserved		Reserved		ns
		CWL=6	Reserved		Reserved		ns
		CWL=7	1.5	< 1.875	Reserved		ns
	CL=10	CWL=5	Reserved		Reserved		ns
		CWL=6	Reserved		Reserved		ns
		CWL=7	1.5	< 1.875	1.5	< 1.875	ns
Supported CL			5,6,7,8,9,(10)		5,6,8,10		nCK
Supported CWL			5,6,7		5,6,7		nCK

Fundamental AC Specifications – Operating Frequency

DDR3-1066 and DDR3L-1066

Speed Bin			DDR3(L)-1066		DDR3(L)-1066		Units
CL-nRCD-nRP			7-7-7		8-8-8		ns
Parameter			Min.	Max.	Min.	Max.	ns
tCK (Avg)	CL=5	CWL=5	3.0	3.3	3.0	3.3	ns
		CWL=6	Reserved		Reserved		ns
	CL=6	CWL=5	2.5	3.3	2.5	3.3	ns
		CWL=6	Reserved		Reserved		ns
	CL=7	CWL=5	Reserved		Reserved		ns
		CWL=6	1.875	< 2.5	Reserved		ns
	CL=8	CWL=5	Reserved		Reserved		ns
		CWL=6	1.875	< 2.5	1.875	< 2.5	ns
Supported CL			5,6,7,8		5,6,8		nCK
Supported CWL			5,6		5,6		nCK

Notes:

1. The CL setting and CWL setting result in tCK(AVG).MIN and tCK(AVG).MAX requirements. When making a selection of tCK(AVG), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(AVG).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(AVG) value (3.0, 2.5, 1.875, 1.5, 1.25, 1.07, or 0.938 ns) when calculating CL [nCK] = tAA [ns] / tCK(AVG) [ns], rounding up to the next 'Supported CL', where tCK(AVG) = 3.0 ns should only be used for CL = 5 calculation.
3. tCK(AVG).MAX limits: Calculate tCK(AVG) = tAA.MAX / CL SELECTED and round the resulting tCK(AVG) down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875 ns or 1.5 ns or 1.25 ns or 1.07 ns or 0.938 ns). This result is tCK(AVG).MAX corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.
6. Any DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
9. Any DDR3-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.

10. For devices supporting optional down binning to CL=7 and CL=9, tAA/tRCD/tRPmin must be 13.125 ns. SPD settings must be programmed to match. For example, DDR3-1333(9-9-9) devices supporting down binning to DDR3- 1066(7-7-7) should program 13.125 ns in SPD bytes for tAAmin (Byte 16), tRCDmin (Byte 18), and tRPmin (Byte 20). DDR3-1600(11-11-11) devices supporting down binning to DDR3-1333(9-9-9) or DDR3-1066(7-7-7) should program 13.125 ns in SPD bytes for tAAmin (Byte16), tRCDmin (Byte 18), and tRPmin (Byte 20). Once tRP (Byte 20) is programmed to 13.125ns, tRCmin (Byte 21, 23) also should be programmed accodingly. For example, 49.125ns (tRASmin + tRPmin = 36 ns + 13.125 ns) for DDR3-1333(9-9-9) and 48.125ns (tRASmin + tRPmin = 35 ns + 13.125 ns) for DDR3-1600(11-11-11).
11. For CL5 support, refer to DIMM SPD information. DRAM is required to support CL5. CL5 is not mandatory in SPD coding.
12. For devices supporting optional down binning to CL=11, CL=9 and CL=7, tAA/tRCD/tRPmin must be 13.125ns. SPD setting must be programed to match. For example, DDR3-1866(13-13-13) devices supporting down binning to DDR3- 1600(11-11-11) or DDR3-1333(9-9-9) or 1066(7-7-7) should program 13.125ns in SPD bytes for tAAmin(byte16), tRCDmin(Byte18) and tRPmin (byte20). Once tRP (Byte 20) is programmed to 13.125ns, tRCmin (Byte 21, 23) also should be programmed accordingly. For example, 47.125ns (tRASmin + tRPmin = 34 ns+ 13.125 ns).

Electrical Characteristics & AC Timing

Timing Parameter by Speed Bin (DDR3(L)-1066)

Parameter	Symbol	DDR3-1066(L)		Units
		Min.	Max.	
Clock Timing				
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	-	ns
Average Clock Period	tCK(avg)	Refer to “Fundamental AC Specifications”		ps
Average high pulse width	tCH(avg)	0.47	0.53	tCK(avg)
Average low pulse width	tCL(avg)	0.47	0.53	tCK(avg)
Absolute Clock Period	tCK(abs)	Min.: tCK(avg)min + tJIT(per)min Max.: tCK(avg)max + tJIT(per)max		ps
Absolute clock HIGH pulse width	tCH(abs)	0.43	-	tCK(avg)
Absolute clock LOW pulse width	tCL(abs)	0.43	-	tCK(avg)
Clock Period Jitter	tJIT(per)	-90	90	ps
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-80	80	ps
Cycle to Cycle Period Jitter	tJIT(cc)	180		ps
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	160		ps
Duty Cycle Jitter	tJIT(duty)	-	-	ps
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	tERR(nper)min = (1 + 0.68ln(n)) * tJIT(per)min tERR(nper)max = (1 + 0.68ln(n)) * tJIT(per)max		ps
Data Timing				
DQS,DQS# to DQ skew, per group, per access	tDQSQ	-	150	ps
DQ output hold time from DQS, DQS#	tQH	0.38	-	tCK(avg)
DQ low-impedance time from CK, CK#	tLZ(DQ)	-600	300	ps
DQ high impedance time from CK, CK#	tHZ(DQ)	-	300	ps

Timing Parameter by Speed Bin (DDR3(L)-1066) (continue)

Parameter	Symbol	DDR3-1066(L)		Units
		Min.	Max.	
Data setup time to DQS, DQS# referenced to Vih(ac) /Vil(ac) levels	tDS(base) DDR3 -AC175	25	-	ps
	tDS(base) DDR3-AC150	75	-	ps
	tDS(base) DDR3L -AC160	40	-	ps
	tDS(base) DDR3L -AC135	90	-	
Data hold time from DQS, DQS# referenced to Vih(dc) / Vil(dc) levels	tDH(base) DDR3 -DC100	100	-	
	tDH(base) DDR3L -DC90	110	-	
DQ and DM Input pulse width for each input	tDIPW	490	-	ps
Data Strobe Timing				
DQS,DQS# differential READ Preamble	tRPRE	0.9	Note 19	tCK(avg)
DQS, DQS# differential READ Postamble	tRPST	0.3	Note 11	tCK(avg)
DQS, DQS# differential output high time	tQSH	0.38	-	tCK(avg)
DQS, DQS# differential output low time	tQSL	0.38	-	tCK(avg)
DQS, DQS# differential WRITE Preamble	tWPRE	0.9	-	tCK(avg)
DQS, DQS# differential WRITE Postamble	tWPST	0.3	-	tCK(avg)
DQS, DQS# rising edge output access time from rising CK, CK#	tDQSCK	-300	300	ps
DQS and DQS# low-impedance time (Referenced from RL - 1)	tLZ(DQS)	-600	300	ps
DQS and DQS# high-impedance time (Referenced from RL + BL/2)	tHZ(DQS)	-	300	ps
DQS, DQS# differential input low pulse width	tDQSL	0.45	0.55	tCK(avg)
DQS, DQS# differential input high pulse width	tDQSH	0.45	0.55	tCK(avg)
DQS, DQS# rising edge to CK, CK# rising edge	tDQSS	-0.25	0.25	tCK(avg)
DQS, DQS# falling edge setup time to CK, CK#rising edge	tDSS	0.2	-	tCK(avg)
DQS, DQS# falling edge hold time from CK, CK# rising edge	tDSH	0.2	-	tCK(avg)

Timing Parameter by Speed Bin (DDR3(L)-1066) (continue)

Parameter	Symbol	DDR3-1066(L)		Units
		Min.	Max.	
Command and Address Timing				
DLL locking time	tDLLK	512	-	nCK
Internal READ Command to PRECHARGE Command delay	tRTP	max(4nCK, 7.5ns)	-	
Delay from start of internal write transaction to internal read command	tWTR	max(4nCK, 7.5ns)	-	
WRITE recovery time	tWR	15	-	ns
Mode Register Set command cycle time	tMRD	4	-	nCK
Mode Register Set command update delay	tMOD	max(12nCK, 15ns)	-	
ACT to internal read or write delay time	tRCD	See “Fundamental AC Specification”		
PRE command period	tRP			
ACT to ACT or REF command period	tRC			
ACTIVE to PRECHARGE command period	tRAS			
CAS#to CAS# command delay	tCCD	4	-	nCK
Auto precharge write recovery + precharge time	tDAL(min)	WR + roundup(tRP / tCK(avg))		nCK
Multi-Purpose Register Recovery Time	tMPRR	1	-	nCK
ACTIVE to ACTIVE command period for 1KB page size	tRRD	max(4nCK, 7.5ns)	-	
ACTIVE to ACTIVE command period for 2KB page size	tRRD	max(4nCK, 10ns)	-	
Four activate window for 1KB page size	tFAW	37.5	-	ns
Four activate window for 2KB page size	tFAW	50	-	ns
Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	tIS(BASE) DDR3 -AC175	125	-	ps
	tIS(BASE) DDR3 -AC150	275	-	ns
	tIS(BASE) DDR3L -AC160	140	-	ps
	tIS(BASE) DDR3L -AC135	290	-	ns

Timing Parameter by Speed Bin (DDR3(L)-1066) (continue)

Parameter	Symbol	DDR3-1066(L)		Units
		Min.	Max.	
Command and Address hold time from CK, CK# referenced to Vih(dc) / Vil(dc) levels	tIH(BASE) DDR3 -DC100	200	-	ns
	tIH(BASE) DDR3L -DC90	210	-	ns
Control and Address Input pulse width for each input	tIPW	780	-	ps
Calibration Timing				
Power-up and RESET calibration time	tZQinit	tZQINITmin: max(512tCK, 640ns) tZQINITmax: -		nCK
Normal operation Full calibration time	tZQoper	tZQOPERmin: max(256tCK, 320ns) tZQOPERmax: -		nCK
Normal operation Short calibration time	tZQCS	tZQCSmin: max(64 tCK, 80ns) tZQCSmax: -		nCK
Reset Timing				
Exit Reset from CKE HIGH to a valid command	tXPR	max(5nCK, tRFC(min) + 10ns)	-	
Self Refresh Timings				
Exit Self Refresh to commands not requiring a locked DLL	tXS	max(5nCK, tRFC(min) + 10ns)	-	
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	nCK
Minimum CKE low width for Self Refresh entry to exit timing	tCKESR	tCKE(min) + 1 nCK	-	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK, 10 ns)	-	
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK, 10 ns)	-	

Timing Parameter by Speed Bin (DDR3(L)-1066) (continue)

Parameter	Symbol	DDR3-1066(L)		Units
		Min.	Max.	
Power Down Timings				
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max(3nCK, 7.5ns)	-	
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	max(10nCK, 24ns)	-	
CKE minimum pulse width	tCKE	max(3nCK, 5.625ns)	-	
Command pass disable delay	tCPDED	1	-	nCK
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	
Timing of ACT command to Power Down entry	tACTPDEN	1	-	nCK
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	nCK
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	nCK
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL + 4 + (tWR /tCK(avg))	-	nCK
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	-	nCK
Timing of WR command to Power Down entry (BC4MRS)	tWRPDEN	WL + 2 + (tWR /tCK(avg))	-	nCK
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPDEN	WL + 2 +WR + 1	-	nCK
Timing of REF command to Power Down entry	tREFPDEN	1	-	nCK
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	

Timing Parameter by Speed Bin (DDR3(L)-1066) (continue)

Parameter	Symbol	DDR3-1066(L)		Units
		Min.	Max.	
ODT Timings				
ODT turn on Latency	ODTLon	WL-2=CWL+AL-2	-	nCK
ODT turn off Latency	ODTLoff	WL-2=CWL+AL-2		nCK
ODT high time without write command or with write command and BC4	ODTH4	4	-	nCK
ODT high time with Write command and BL8	ODTH8	6	-	nCK
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONPD	2	8.5	ns
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFPD	2	8.5	ns
RTT turn-on	tAON	-300	300	ps
RTT_Nom and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	tCK(avg)
RTT dynamic change skew	tADC	0.3	0.7	tCK(avg)
Write Leveling Timings				
First DQS/DQS# rising edge after write leveling mode is programmed	tWLMRD	40	-	nCK
DQS/DQS# delay after write leveling mode is programmed	tWLDQSEN	25	-	nCK
Write leveling setup time from rising CK, CK# crossing to rising DQS,DQS# crossing	tWLS	245	-	ps
Write leveling hold time from rising DQS,DQS# crossing to rising CK, CK# crossing	tWLH	245	-	ps
Write leveling output delay	tWLO	0	9	ns
Write leveling output error	tWLOE	0	2	ns

Electrical Characteristics & AC Timing

Timing Parameter by Speed Bin (DDR3(L)-1333)

Parameter	Symbol	DDR3-1333(L)		Units
		Min.	Max.	
Clock Timing				
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	-	ns
Average Clock Period	tCK(avg)	Refer to “Fundamental AC Specifications”		ps
Average high pulse width	tCH(avg)	0.47	0.53	tCK(avg)
Average low pulse width	tCL(avg)	0.47	0.53	tCK(avg)
Absolute Clock Period	tCK(abs)	Min.: tCK(avg)min + tJIT(per)min Max.: tCK(avg)max + tJIT(per)max		ps
Absolute clock HIGH pulse width	tCH(abs)	0.43	-	tCK(avg)
Absolute clock LOW pulse width	tCL(abs)	0.43	-	tCK(avg)
Clock Period Jitter	tJIT(per)	-80	80	ps
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-70	70	ps
Cycle to Cycle Period Jitter	tJIT(cc)	160		ps
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	140		ps
Duty Cycle Jitter	tJIT(duty)	-	-	ps
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	tERR(nper)min = (1 + 0.68ln(n)) * tJIT(per)min tERR(nper)max = (1 + 0.68ln(n)) * tJIT(per)max		ps

Timing Parameter by Speed Bin (DDR3(L)-1333 (continue)

Parameter	Symbol	DDR3-1333(L)		Units
		Min.	Max.	
Data Timing				
DQS,DQS# to DQ skew, per group, per access	tDQSQ	-	125	ps
DQ output hold time from DQS, DQS#	tQH	0.38	-	tCK(avg)
DQ low-impedance time from CK, CK#	tLZ(DQ)	-500	250	ps
DQ high impedance time from CK, CK#	tHZ(DQ)	-	250	ps
Data setup time to DQS,DQS# referenced to Vih(ac) /Vil(ac) levels	tDS(base) DDR3-AC175	-	-	ps
	tDS(base) DDR3-AC150	30	-	ps
	tDS(base) DDR3L-AC160	-	-	ps
	tDS(base) DDR3L-AC135	45	-	
Data hold time from DQS,DQS# referenced to Vih(dc) / Vil(dc) levels	tDH(base) DDR3-DC100	65	-	
	tDH(base) DDR3L-DC90	75	-	
DQ and DM Input pulse width for each input	tDIPW	400	-	ps

Timing Parameter by Speed Bin (DDR3(L)-1333 (continue))

Parameter	Symbol	DDR3-1333(L)		Units
		Min.	Max.	
Data Strobe Timing				
DQS,DQS# differential READ Preamble	tRPRE	0.9	Note 19	tCK(avg)
DQS,DQS# differential READ Postamble	tRPST	0.3	Note 11	tCK(avg)
DQS,DQS# differential output high time	tQSH	0.4	-	tCK(avg)
DQS,DQS# differential output low time	tQSL	0.4	-	tCK(avg)
DQS,DQS# differential WRITE Preamble	tWPRE	0.9	-	tCK(avg)
DQS,DQS# differential WRITE Postamble	tWPST	0.3	-	tCK(avg)
DQS,DQS# rising edge output access time from rising CK, CK#	tDQSCK	-255	255	ps
DQS andDQS# low-impedance time (Referenced from RL - 1)	tLZ(DQS)	-500	250	ps
DQS andDQS# high-impedance time (Referenced from RL + BL/2)	tHZ(DQS)	-	250	ps
DQS,DQS# differential input low pulse width	tDQSL	0.45	0.55	tCK(avg)
DQS,DQS# differential input high pulse width	tDQSH	0.45	0.55	tCK(avg)
DQS,DQS# rising edge to CK, CK# rising edge	tDQSS	-0.25	0.25	tCK(avg)
DQS,DQS# falling edge setup time to CK, CK# rising edge	tDSS	0.2	-	tCK(avg)
DQS,DQS# falling edge hold time from CK, CK# rising edge	tDSH	0.2	-	tCK(avg)
Command and Address Timing				
DLL locking time	tDLLK	512	-	nCK
Internal READ Command to PRECHARGE Command delay	tRTP	max(4nCK, 7.5ns)	-	
Delay from start of internal write transaction to internal read command	tWTR	max(4nCK, 7.5ns)	-	
WRITE recovery time	tWR	15	-	ns
Mode Register Set command cycle time	tMRD	4	-	nCK
Mode Register Set command update delay	tMOD	max(12nCK, 15ns)	-	

Timing Parameter by Speed Bin (DDR3(L)-1333 (continue)

Parameter	Symbol	DDR3-1333(L)		Units
		Min.	Max.	
Command and Address Timing				
ACT to internal read or write delay time	tRCD	See "Fundamental AC Specification"		
PRE command period	tRP			
ACT to ACT or REF command period	tRC			
ACTIVE to PRECHARGE command period	tRAS			
CK#to CK#- command delay	tCCD	4	-	nCK
Auto precharge write recovery + precharge time	tDAL(min)	WR + roundup(tRP / tCK(avg))		nCK
Multi-Purpose Register Recovery Time	tMPRR	1	-	nCK
ACTIVE to ACTIVE command period for 1KB page size	tRRD	max(4nCK, 6ns)	-	
ACTIVE to ACTIVE command period for 2KB page size	tRRD	max(4nCK, 7.5ns)	-	
Four activate window for 1KB page size	tFAW	30	-	ns
Four activate window for 2KB page size	tFAW	45	-	ns
Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	tIS(BASE) DDR3-AC175	65	-	ps
	tIS(BASE) DDR3-AC150	190	-	ns
	tIS(BASE) DDR3L-AC160	80	-	ps
	tIS(BASE) DDR3L-AC135	205	-	ns
Command and Address hold time from CK, CK# referenced to Vih(dc) / Vil(dc) levels	tIH(BASE) DDR3-DC100	140	-	ns
	tIH(BASE) DDR3L-DC90	150	-	ns
Control and Address Input pulse width for each input	tIPW	620	-	ps

Timing Parameter by Speed Bin (DDR3(L)-1333 (continue)

Parameter	Symbol	DDR3-1333(L)		Units
		Min.	Max.	
Calibration Timing				
Power-up and RESET calibration time	tZQinit	tZQINITmin: max(512tCK, 640ns) tZQINITmax: -		nCK
Normal operation Full calibration time	tZQoper	tZQOPERmin: max(256tCK, 320ns) tZQOPERmax: -		nCK
Normal operation Short calibration time	tZQCS	tZQCSmin: max(64 tCK, 80ns) tZQCSmax: -		nCK
Reset Timing				
Exit Reset from CKE HIGH to a valid command	tXPR	max(5nCK, tRFC(min) + 10ns)	-	
Self Refresh Timings				
Exit Self Refresh to commands not requiring a locked DLL	tXS	max(5nCK, tRFC(min) + 10ns)	-	
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	nCK
Minimum CKE low width for Self Refresh entry to exit timing	tCKESR	tCKE(min) + 1 nCK	-	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK, 10 ns)	-	
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK, 10 ns)	-	
Power Down Timings				
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max(3nCK, 6ns)	-	
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	max(10nCK, 24ns)	-	
CKE minimum pulse width	tCKE	max(3nCK, 5.625ns)	-	
Command pass disable delay	tCPDED	1	-	nCK
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	
Timing of ACT command to Power Down entry	tACTPDEN	1	-	nCK

Timing Parameter by Speed Bin (DDR3(L)-1333 (continue)

Parameter	Symbol	DDR3-1333(L)		Units
		Min.	Max.	
Power Down Timings				
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	nCK
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	nCK
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL + 4 + (tWR /tCK(avg))	-	nCK
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	-	nCK
Timing of WR command to Power Down entry (BC4MRS)	tWRPDEN	WL + 2 + (tWR /tCK(avg))	-	nCK
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPDEN	WL + 2 +WR + 1	-	nCK
Timing of REF command to Power Down entry	tREFPDEN	1	-	nCK
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	
ODT Timings				
ODT turn on Latency	ODTLon	WL-2=CWL+AL-2	-	nCK
ODT turn off Latency	ODTLoff	WL-2=CWL+AL-2		nCK
ODT high time without write command or with write command and BC4	ODTH4	4	-	nCK
ODT high time with Write command and BL8	ODTH8	6	-	nCK
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONPD	2	8.5	ns
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFPD	2	8.5	ns
RTT turn-on	tAON	-250	250	ps
RTT_Nom and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	tCK(avg)
RTT dynamic change skew	tADC	0.3	0.7	tCK(avg)

Timing Parameter by Speed Bin (DDR3(L)-1333 (continue)

Parameter	Symbol	DDR3-1333(L)		Units
		Min.	Max.	
Write Leveling Timings				
First DQS/DQS# rising edge after write leveling mode is programmed	tWLMRD	40	-	nCK
DQS/DQS# delay after write leveling mode is programmed	tWLDQSEN	25	-	nCK
Write leveling setup time from rising CK, CK# crossing to rising DQS,DQS# crossing	tWLS	195	-	ps
Write leveling hold time from rising DQS,DQS# crossing to rising CK, CK# crossing	tWLH	195	-	ps
Write leveling output delay	tWLO	0	9	ns
Write leveling output error	tWLOE	0	2	ns

Electrical Characteristics & AC Timing

Timing Parameter by Speed Bin (DDR3(L)-1600/1866)

Parameter	Symbol	DDR3(L)-1600		DDR3-1866(L)		Unit
		Min.	Max.	Min.	Max.	
Clock Timing						
Minimum Clock Cycle Time (DLL off mode)	tCK(DLL_OFF)	8	-	8	-	ns
Average Clock Period	tCK(avg)	Refer to “Fundamental AC Specifications”				ps
Average high pulse width	tCH(avg)	0.47	0.53	0.47	0.53	tCK(avg)
Average low pulse width	tCL(avg)	0.47	0.53	0.47	0.53	tCK(avg)
Absolute Clock Period	tCK(abs)	Min.: tCK(avg)min + tJIT(per)min Max.: tCK(avg)max + tJIT(per)max				
Absolute clock HIGH pulse width	tCH(abs)	0.43	-	0.43	-	tCK(avg)
Absolute clock LOW pulse width	tCL(abs)	0.43	-	0.43	-	tCK(avg)
Clock Period Jitter	tJIT(per)	-70	70	-60	60	ps
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-60	60	-50	50	ps
Cycle to Cycle Period Jitter	tJIT(cc)	140		120		
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	120		100		
Duty Cycle Jitter	tJIT(duty)	-	-	-	-	ps
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	tERR(nper)min = (1 + 0.68ln(n)) * tJIT(per)min tERR(nper)max = (1 + 0.68ln(n)) * tJIT(per)max				ps

Timing Parameter by Speed Bin (DDR3(L)-1600/1866) (continue)

Parameter	Symbol	DDR3(L)-1600		DDR3-1866(L)		Unit
		Min.	Max.	Min.	Max.	
Data Timing						
DQS,DQS# to DQ skew, per group, per access	tDQSQ	-	100	-	85	ps
DQ output hold time from DQS,DQS#	tQH	0.38	-	0.38	-	tCK(avg)
DQ low-impedance time from CK, CK#	tLZ(DQ)	-450	225	-390	195	ps
DQ high impedance time from CK, CK#-	tHZ(DQ)	-	225	-	195	ps
Data setup time to DQS,DQS# referenced to Vih(ac) /Vil(ac) levels	tDS(base) DDR3-1600 (AC175) DDR3-1866 (AC150)	-	-	-	-	ps
	tDS(base) DDR3-1600 (AC150) DDR3-1866 (AC135)	10	-	68	-	ps
	tDS(base) DDR3L-1600 (AC135),SR=1V/ns DDR3L-1866 (AC130),SR=2V/ns	25	-	70	-	ps
Data hold time from DQS, DQS# referenced toVih(dc) / Vil(dc) levels	tDH(base) DC100	45	-	-	-	ps
	tDH(base)DC90 DDR3L-1600 (SR=1V/ns) DDR3L-1866 (SR=2V/ns)	55	-	75	-	ps
DQ and DM Input pulse width for each input	tDIPW	360	-	320	-	ps

Timing Parameter by Speed Bin (DDR3(L)-1600/1866) (continue)

Parameter	Symbol	DDR3(L)-1600		DDR3-1866(L)		Unit
		Min.	Max.	Min.	Max.	
Data Strobe Timing						
DQS, DQS# differential READ Preamble	tRPRE	0.9	Note 19	0.9	Note 19	tCK(avg)
DQS, DQS# differential READ Postamble	tRPST	0.3	Note 11	0.3	Note 11	tCK(avg)
DQS, DQS# differential output high time	tQSH	0.4	-	0.4	-	tCK(avg)
DQS, DQS# differential output low time	tQSL	0.4	-	0.4	-	tCK(avg)
DQS, DQS# differential WRITE Preamble	tWPRE	0.9	-	0.9	-	tCK(avg)
DQS, DQS# differential WRITE Postamble	tWPST	0.3	-	0.3	-	tCK(avg)
DQS, DQS# rising edge output access time from rising CK, CK#	tDQSCK	-225	225	-195	195	ps
DQS and DQS# low-impedance time (Referenced from RL - 1)	tLZ(DQS)	-450	225	-390	195	ps
DQS and DQS# high-impedance time (Referenced from RL + BL/2)	tHZ(DQS)	-	225	-	195	ps
DQS, DQS# differential input low pulse width	tDQSL	0.45	0.55	0.45	0.55	tCK(avg)
DQS, DQS# differential input high pulse width	tDQSH	0.45	0.55	0.45	0.55	tCK(avg)
DQS, DQS# rising edge to CK, CK# rising edge	tDQSS	-0.27	0.27	-0.27	0.27	tCK(avg)
DQS, DQS# falling edge setup time to CK, CK# rising edge	tDSS	0.18	-	0.18	-	tCK(avg)
DQS, DQS# falling edge hold time from CK, CK# rising edge	tDSH	0.18	-	0.18	-	tCK(avg)

Timing Parameter by Speed Bin (DDR3(L)-1600/1866) (continue)

Parameter	Symbol	DDR3(L)-1600		DDR3-1866(L)		Unit
		Min.	Max.	Min.	Max.	
Command and Address Timing						
DLL locking time	tDLLK	512	-	512	-	nCK
Internal READ Command to PRECHARGE Command delay	tRTP	tRTPmin.: max(4nCK, 7.5ns) tRTPmax.: -				
Delay from start of internal write transaction to internal read command	tWTR	tWTRmin.: max(4nCK, 7.5ns) tWTRmax.: -				
WRITE recovery time	tWR	15	-	15	-	ns
Mode Register Set command cycle time	tMRD	4	-	4	-	nCK
Mode Register Set command update delay	tMOD	tMODmin.: max(12nCK, 15ns) tMODmax.:				
ACT to internal read or write delay time	tRCD	Refer to “Fundamental AC Specifications”				
PRE command period	tRP					
ACT to ACT or REF command period	tRC					
ACTIVE to PRECHARGE command period	tRAS					
CAS# to CAS# command delay	tCCD	4	-	4	-	nCK
Auto precharge write recovery + precharge time	tDAL(min)	WR + roundup(tRP / tCK(avg))				nCK
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	nCK
ACTIVE to ACTIVE command period for 1KB page size	tRRD	tRRDmin.: max(4nCK, 6ns) tRRDmax.:				
ACTIVE to ACTIVE command period for 2KB page size	tRRD	tRRDmin.: max(4nCK, 7.5ns) tRRDmax.:				
Four activate window for 1KB page size	tFAW	30	-	27	-	ns
Four activate window for 2KB page size	tFAW	40	-	35	-	ns

Timing Parameter by Speed Bin (DDR3(L)-1600/1866) (continue)

Parameter	Symbol	DDR3(L)-1600		DDR3-1866(L)		Unit
		Min.	Max.	Min.	Max.	
Command and Address Timing						
Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	tIS(BASE) DDR3-1600(AC175) DDR3-1866(AC150)	45	-	-	-	ps
	tIS(BASE) DDR3-1600(AC150) DDR3- 866(AC125)	170	-	150	-	ps
	tIS(BASE) DDR3L(AC160)	60	-	-	-	ps
	tIS(BASE) DDR3L(AC135)	185	-	65	-	ps
	tIS(BASE) DDR3L(AC125)	-	-	150	-	ps
Command and Address hold time from CK, CK# referenced to Vih(dc) / Vil(dc) levels	tIH(BASE) DDR3 DC100	120	-	100	-	ps
	tIH(BASE) DDR3L DC90	130	-	110	-	ps
Control and Address Input pulse width for each input	tIPW	560	-	535	-	ps
Calibration Timing						
Power-up and RESET calibration time	tZQinit	tZQINITmin: max(512tCK, 640ns) tZQINITmax: -				
Normal operation Full calibration time	tZQoper	tZQOPERmin: max(256tCK, 320ns) tZQOPERmax: -				
Normal operation Short calibration time	tZQCS	tZQCSmin: max(64 tCK, 80ns) tZQCSmax: -				
Reset Timing						
Exit Reset from CKE HIGH to a valid command	tXPR	tXPRmin.: max(5nCK, tRFC(min) + 10ns) tXPRmax.: -				
Self Refresh Timing						
Exit Self Refresh to commands not requiring a locked DLL	tXS	tXSmin.: max(5nCK, tRFC(min) + 10ns) tXSmax.: -				

Timing Parameter by Speed Bin (DDR3(L)-1600/1866) (continue)

Parameter	Symbol	DDR3(L)-1600		DDR3-1866(L)		Unit
		Min.	Max.	Min.	Max.	
Self Refresh Timing						
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tXSDLLmin.: tDLLK(min) tXSDLLmax.: -				nCK
Minimum CKE low width for Self Refresh entry to exit timing	tCKESR	tCKESRmin.: tCKE(min) + 1 nCK tCKESRmax.: -				
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	tCKSREmin.: max(5 nCK, 10 ns) tCKSREmax.: -				
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	tCKSRXmin.: max(5 nCK, 10 ns) tCKSRXmax.: -				
Power Down Timing						
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	tXPmin.: max(3nCK, 6ns) tXPmax.: -				
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	tXPDLLmin.: max(10nCK, 24ns) tXPDLLmax.: -				
CKE minimum pulse width	tCKE	tCKEmin.: max(3nCK ,5ns) tCKEmax.: -				
Command pass disable delay	tCPDED	tCPDEDmin.: 1 tCPDEDmax.: -				nCK
Power Down Entry to Exit Timing	tPD	tPDmin : tCKE(min) tPDmax : 9*tREFI				
Timing of ACT command to Power Down entry	tACTPDEN	tACTPDENmin.: 1 tACTPDENmax.: -				nCK
Timing of PRE or PREA command to Power Down entry	tPRPDEN	tPRPDENmin.: 1 tPRPDENmax.: -				nCK
Timing of RD/RDA command to Power Down entry	tRDPDEN	tRDPDENmin.: RL+4+1 tRDPDENmax.: -				nCK
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	tWRPDENmin.: WL + 4 + (tWR /tCK(avg)) tWRPDENmax.: -				nCK

Timing Parameter by Speed Bin (DDR3(L)-1600/1866) (continue)

Parameter	Symbol	DDR3(L)-1600		DDR3-1866(L)		Unit
		Min.	Max.	Min.	Max.	
Self Refresh Timing						
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	tWRAPDENmin.: WL+4+WR+1 tWRAPDENmax.: -				nCK
Timing of WR command to Power Down entry (BC4MRS)	tWRPDEN	tWRPDENmin.: WL + 2 + (tWR /tCK(avg)) tWRPDENmax.: -				nCK
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPDEN	tWRAPDENmin.: WL + 2 +WR + 1 tWRAPDENmax.: -				nCK
Timing of REF command to Power Down entry	tREFPDEN	tREFPDENmin.: 1 tREFPDENmax.: -				nCK
Timing of MRS command to Power Down entry	tMRSPDEN	tMRSPDENmin.: tMOD(min) tMRSPDENmax.: -				
ODT Timing						
ODT turn on Latency	ODTLon	WL-2=CWL+AL-2				nCK
ODT turn off Latency	ODTLoff	WL-2=CWL+AL-2				nCK
ODT high time without write command or with write command and BC4	ODTH4	ODTH4min.: 4 ODTH4max.: -				nCK
ODT high time with Write command and BL8	ODTH8	ODTH8min.: 6 ODTH8max.: -				nCK
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONPD	2	8.5	2	8.5	ns
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFPD	2	8.5	2	8.5	ns
RTT turn-on	RTT turn-on	-225	225	-195	195	ps
RTT_Nom and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	0.3	0.7	tCK(avg)
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	tCK(avg)

Timing Parameter by Speed Bin (DDR3(L)-1600/1866) (continue)

Parameter	Symbol	DDR3(L)-1600		DDR3-1866(L)		Unit
		Min.	Max.	Min.	Max.	
Write Leveling Timing						
First DQS/ DQS# rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	nCK
DQS/ DQS# delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	nCK
Write leveling setup time from rising CK, CK# crossing to rising DQS, DQS# crossing	tWLS	165	-	140	-	ps
Write leveling hold time from rising DQS, DQS# crossing to rising CK, CK# crossing	tWLH	165	-	140	-	ps
Write leveling output delay	tWLO	0	7.5	0	7.5	ns
Write leveling output error	tWLOE	0	2	0	2	ns

Jitter Notes

1. Unit "Tck(avg)" represents the actual Tck(avg) of the input clock under operation. Unit "Nck" represents one clock cycle of the input clock, counting the actual clock edges. Ex) Tmrd=4 [Nck] means; if one Mode Register Set command is regis-tered at Tm, anther Mode Register Set command may be registered at Tm+4, even if (Tm+4-Tm) is 4 x Tck(avg) + Terr(4per), min.
2. These parameters are measured from a command/address signal (CKE, CS#, RAS#, CAS# , WE#, ODT, BA0, A0, A1, etc) transition edge to its respective clock signal (CK, CK#) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. Tjit(per), Tjit(cc), etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.
3. These parameters are measured from a data strobe signal (DQS(L/U), DQS#(L/U)) crossing to its respective clock signal (CK, CK#) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. Tjit(per), Tjit(cc), etc), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.
4. These parameters are measured from a data signal (DM(L/U), DQ(L/U)0, DQ(L/U)1, etc.) transition edge to its respective data strobe signal (DQS(L/U), DQS# (L/U)) crossing.
5. For these parameters, the DDR3(L) SDRAM device supports tnPARAM [Nck] = RU{Tparam[ns] / tCK(avg)[ns]}, which is in clock cycles, assuming all input clock jitter specifications are satisfied.
6. When the device is operated with input clock jitter, this parameter needs to be derated by the actual Terr(mper), act of the input clock, where 2 <= m <=12. (Output derating is relative to the SDRAM input clock.)
7. When the device is operated with input clock jitter, this parameter needs to be derated by the actual Tjit(per),act of the input clock. (Output deratings are relative to the SDRAM input clock.)

Timing Parameter Notes

1. Actual value dependent upon measurement level definitions which are TBD.
2. Commands requiring a locked DLL are: READ (and RAP) are synchronous ODT commands.
3. The max values are system dependent.
4. WR as programmed in mode register.
5. Value must be rouned-up to next higher integer value.
6. There is no maximum cycle time limit besides the need to satisfy the refresh interval, tREFI.
7. For definition of RTT-on time tAON See "Timing Parameters".
8. For definition of RTT-off time tAOF See "Timing Parameters".
9. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR / tCK to the next integer.
10. WR in clock cycles are programmed in MR0.
11. The maximum read postamble is bounded by tDQSCK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side.
12. Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by TBD.
13. Value is only valid for RON34.
14. Single ended signal parameter.
15. tREFI depends on TOPER.
16. tIS(base) and tIH(base) values are for 1V/ns CMD/ADD single-ended slew rate and 2V/ns CK, CK differential slew rate. Note for DQ and DM signals, VREF(DC)=VRefDQ(DC). For input only pins except RESET, VRef(DC)=VRefCA(DC).
17. tDS(base) and tDH(base) values are for 1V/ns DQ single-ended slew rate and 2V/ns DQS, DQS differential slew rate. Note for DQ and DM signals, VREF(DC)=VRefDQ(DC). For input only pins except RESET, VRef(DC)=VRefCA(DC).
18. Start of internal write transaction is defined as follows:
    For BL8 (fixed by MRS and on-the-fly): Rising clock edge 4 clock cycles after WL.
    For BC4 (on-the-fly): Rising clock edge 4 clock cycles after WL.
    For BC4 (fixed by MRS): Rising clock edge 2 clock cycles after WL.
19. The maximum preamble is bound by tLZ (DQS) max on the left side and tDQSCK(max) on the right side.
20. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
21. Although CKE is allowed to be registered LOW after a REFRESH command once tREFPDEN (min) is satisfied, there are cases where additional time such as tXPDLL (min) is also required.
22. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.

23. One ZQCS command can effectively correct a minimum of 0.5% (ZQCorrection) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the "Output Driver Voltage and Temperature Sensitivity" and "ODT Voltage and Temperature Sensitivity" tables. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters.
    One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. the interval could be defined by the following formula: ZQCorrection / [(TSens x Tdriftrate) + (VSens x Vdriftrate)] where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities.
    For example, if TSens = 1.5%/C, VSens = 0.15%/mV, Tdriftrate = 1 C/sec and Vdriftrate = 15mV/sec, then the interval between ZQCS commands is calculated as 0.5 / [(1.5x1)+(0.15x15)] = 0.133 ~ 128ms24. n = from 13 cycles to 50 cycles. This row defines 38 parameters.
24. n = from 13 cycles to 50 cycles. This row defines 38 parameters.
25. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
26. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
27. The tIS(base) AC150 specifications are adjusted from the tIS(base) specification by adding an additional 100ps of derating to accommodate for the lower altemate threshold of 150mV and another 25ps to account for the earlier reference point [(175mV - 150mV) / 1V/ns].

Address / Command Setup, Hold, and Derating

For all input signals the total tIS (setup time) and tIH (hold time) required is calculated by adding the data sheet tIS(base) and tIH(base) and tIH(base) value to the delta tIS and delta tIH derating value respectively.

Example: tIS (total setup time) = tIS(base) + delta tIS

Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of Vref(dc) and the first crossing of VIH(ac)min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of Vref(dc) and the first crossing of VIL(ac)max. If the actual signal is always earlier than the nominal slew rate line between shaded 'Vref(dc) to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded 'Vref(dc) to ac region', the slew rate of the tangent line to the actual signal from the ac level to dc level is used for derating value.

Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(dc)max and the first crossing of Vref(dc). Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(dc)min and the first crossing of Vref(dc). If the actual signal is always later than the nominal slew rate line between shaded 'dc to Vref(dc) region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to Vref(dc) region', the slew rate of a tangent line to the actual signal from the dc level to Vref(dc) level is used for derating value. For a valid transition the input signal has to remain above/below VIH/IL(ac) for some time tVAC. Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached VIH/IL(ac) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL(ac).

ADD/CMD Setup and Hold Base-Values for 1V/ns

Grade	Symbol	Reference	1066	1333	1600	1866	Unit	Notes
DDR3	tIS(base) AC175	VIH/L(ac)	125	65	45	-	ps	1
	tIS(base) AC150	VIH/L(ac)	275	190	170	-	ps	1
	tIS(base) AC135	VIH/L(ac)	-	-	-	65	ps	1
	tIS(base) AC125	VIH/L(ac)	-	-	-	150	ps	1
	tIH(base) DC100	VIH/L(dc)	200	140	120	100	ps	1
DDR3L	tIS(base) AC160	VIH/L(ac)	140	80	60	-	ps	1
	tIS(base) AC135	VIH/L(ac)	290	205	185	65	ps	1,2
	tIS(base) AC125	VIH/L(ac)	-	-	-	150	ps	1,3
	tIH(base) DC90	VIH/L(ac)	210	150	130	110	ps	1

Notes:

1. (AC/DC referenced for 1 V/ns Address/Command slew rate and 2 V/ns differential CK- CK# slew rate)
2. The tIS(base) AC135 specifications are adjusted from the tIS(base) AC160 specification by adding an additional 125 ps for DDR3L-800/1066 or 100 ps for DDR3L-1333/1600 of derating to accommodate for the lower alternate threshold of 135 mV and another 25 ps to account for the earlier reference point [(160 mV - 135 mV) / 1 V/ns].
3. The tIS(base) AC125 specifications are adjusted from the tIS(base) AC135 specification by adding an additional 75 ps for DDR3L- 1866 of derating to accommodate for the lower alternate threshold of 135 mV and another 10 ps to account for the earlier reference point [(135 mV - 125 mV) / 1 V/ns].

Derating values DDR3L-1066/1333/1600 tIS/tIH - AC/DC based AC160 Threshold

		DDR3L AC160 Threshold -> VIH(ACAC)=VREF(DC)+160 mV, VIL(AC)=VREF(DC)-160 mV															
		CK, CK# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ADD Slew Rate (V/ns)	**2**	80	45	80	45	80	45	88	53	96	61	104	69	112	79	120	95
	1.5	53	30	53	30	53	30	61	38	69	46	77	54	85	64	93	80
	1	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	-1	-3	-1	-3	-1	-3	7	5	15	13	23	21	31	31	39	47
	0.8	-3	-8	-3	-8	-3	-8	5	1	13	9	21	17	29	27	37	43
	0.7	-5	-13	-5	-13	-5	-13	3	-5	11	3	19	11	27	21	35	37
	0.6	-8	-20	-8	-20	-8	-20	0	-12	8	-4	16	4	24	14	32	30
	0.5	-20	-30	-20	-30	-20	-30	-12	-22	-4	-14	4	-6	12	4	20	20
	0.4	-40	-45	-40	-45	-40	-45	-32	-37	-24	-29	-16	-21	-8	-11	0	5

Derating values DDR3-1066/1333/1600 tIS/tIH - AC/DC based AC135 Threshold

		DDR3L Alternate AC135 Threshold -> VIH(AC)=VREF(DC)+135 mV, VIL(AC)=VREF(DC)-135 mV															
		CK, CK# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ADD Slew Rate (V/ns)	**2**	68	45	68	45	68	45	76	53	84	61	92	69	100	79	108	95
	1.5	45	30	45	30	45	30	53	38	61	46	69	54	77	64	85	80
	1	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	2	-3	2	-3	2	-3	10	5	18	13	26	21	34	31	42	47
	0.8	3	-8	3	-8	3	-8	11	1	19	9	27	17	35	27	43	43
	0.7	6	-13	6	-13	6	-13	14	-5	22	3	30	11	38	21	46	37
	0.6	9	-20	9	-20	9	-20	17	-12	25	-4	33	4	41	14	49	30
	0.5	5	-30	5	-30	5	-30	13	-22	21	-14	29	-6	37	4	45	20
	0.4	-3	-45	-3	-45	-3	-45	6	-37	14	-29	22	-21	30	-11	38	5

Derating values DDR3L-1866 tIS/tIH - AC/DC based AC125 Threshold

		DDR3L Alternate AC135 Threshold -> VIH(AC)=VREF(DC)+125 mV, VIL(AC)=VREF(DC)-125 mV															
		CK, CK# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ADD Slew Rate (V/ns)	**2**	63	45	63	45	63	45	71	53	79	61	87	69	95	79	103	95
	1.5	42	30	42	30	42	30	50	38	58	46	66	54	74	64	82	80
	1	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	3	-3	3	-3	3	-3	11	5	19	13	27	21	35	31	43	47
	0.8	6	-8	6	-8	6	-8	14	1	22	9	30	17	38	27	46	43
	0.7	10	-13	10	-13	10	-13	18	-5	26	3	34	11	42	21	50	37
	0.6	16	-20	16	-20	16	-20	24	-12	32	4	40	-4	48	14	56	30
	0.5	15	-30	15	-30	15	-30	23	-22	31	-14	39	-6	47	4	55	20
	0.4	13	-45	13	-45	13	-45	21	-37	29	-29	37	-21	45	-11	53	5

Derating values DDR3-1066/1333/1600 tIS/tIH - AC/DC based AC175 Threshold

		DDR3 AC175 Threshold -> VIH(ac)=VREF(dc)+175mV, VIL(ac)=VREF(dc)-175mV															
		CK, CK# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ADD Slew Rate (V/ns)	**2.0**	88	50	88	50	88	50	96	58	104	66	112	74	120	84	128	100
	1.5	59	34	59	34	59	34	67	42	75	50	83	58	91	68	99	84
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	-2	-4	-2	-4	-2	-4	6	4	14	12	22	20	30	30	38	46
	0.8	-6	-10	-6	-10	-6	-10	2	-2	10	6	18	14	26	24	34	40
	0.7	-11	-16	-11	-16	-11	-16	-3	-8	5	0	13	8	21	18	29	34
	0.6	-17	-26	-17	-26	-17	-26	-9	-18	-1	-10	7	-2	15	8	23	24
	0.5	-35	-40	-35	-40	-35	-40	-27	-32	-19	-24	-11	-16	-2	-6	5	10
	0.4	-62	-60	-62	-60	-62	-60	-54	-52	-46	-44	-38	-36	-30	-26	-22	-10

Derating values DDR3-1066/1333/1600 tIS/tIH - AC/DC based AC150 Threshold

		DDR3 Alternate AC150 Threshold -> VIH(ac)=VREF(dc)+150mV, VIL(ac)=VREF(dc)-150mV															
		CK, CK# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ADD Slew Rate (V/ns)	**2**	75	50	75	50	75	50	83	58	91	66	99	74	107	84	115	100
	1.5	50	34	50	34	50	34	58	42	66	50	74	58	82	68	90	84
	1	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	0	-4	0	-4	0	-4	8	4	16	12	24	20	32	30	40	46
	0.8	0	-10	0	-10	0	-10	8	-2	16	6	24	14	32	24	40	40
	0.7	0	-16	0	-16	0	-16	8	-8	16	0	24	8	32	18	40	34
	0.6	-1	-26	-1	-26	-1	-26	7	-18	15	-10	23	-2	31	8	39	24
	0.5	-10	-40	-10	-40	-10	-40	-2	-32	6	-24	14	-16	22	-6	30	10
	0.4	-25	-60	-25	-60	-25	-60	-17	-52	-9	-44	-1	-36	7	-26	15	-10

Derating values DDR3-1866 tIS/tIH - AC/DC based AC135 Threshold

		DDR3 Alternate AC135 Threshold -> VIH(ac)=VREF(dc)+135mV, VIL(ac)=VREF(dc)-135mV															
		CK, CK# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ADD Slew Rate (V/ns)	**2**	68	50	68	50	68	50	76	58	84	66	92	74	100	84	108	100
	1.5	45	34	45	34	45	34	53	42	61	50	69	58	77	68	85	84
	1	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	2	-4	2	-4	2	-4	10	4	18	12	26	20	34	30	42	46
	0.8	3	-10	3	-10	3	-10	11	-2	19	6	27	14	35	24	43	40
	0.7	6	-16	6	-16	6	-16	14	-8	22	0	30	8	38	18	46	34
	0.6	9	-26	9	-26	9	-26	17	-18	25	-10	33	-2	41	8	49	24
	0.5	5	-40	5	-40	5	-40	13	-32	21	-24	29	-16	37	-6	45	10
	0.4	-3	-60	-3	-60	-3	-60	6	-52	14	-44	22	-36	30	-26	38	-10

Derating values DDR3-1866 tIS/tIH - AC/DC based AC125 Threshold

		DDR3 Alternate AC125 Threshold -> VIH(ac)=VREF(dc)+125mV, VIL(ac)=VREF(dc)-125mV															
		CK, CK# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ADD Slew Rate (V/ns)	**2**	63	50	63	50	63	50	71	58	79	66	87	74	95	84	103	100
	1.5	42	34	42	34	42	34	50	42	58	50	66	58	74	68	82	84
	1	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	4	-4	4	-4	4	-4	12	4	20	12	28	20	36	30	44	46
	0.8	6	-10	6	-10	6	-10	14	-2	22	6	30	14	38	24	46	40
	0.7	11	-16	11	-16	11	-16	19	-8	27	0	35	8	43	18	51	34
	0.6	16	-26	16	-26	16	-26	24	-18	32	-10	40	-2	48	8	56	24
	0.5	15	-40	15	-40	15	-40	23	-32	31	-24	39	-16	47	-6	55	10
	0.4	13	-60	13	-60	13	-60	21	-52	29	-44	37	-36	45	-26	53	-10

Required time tVAC above VIH(ac) {below VIL(ac)} for ADD/CMD transition

Slew Rate [V/ns]	DDR3				DDR3L				Unit
	1066/1333/1600		1866		1066/1333/1600		1866		
	175mV [ps]	150mV[ps]	135mV [ps]	125mV [ps]	160 mV [ps]	135 mV [ps]	135 mV [ps]	125 mV [ps]	
> 2.0	75	175	168	173	200	213	200	205	ps
2.0	57	170	168	173	200	213	200	205	ps
1.5	50	167	145	152	173	190	178	184	ps
1.0	38	130	100	110	120	145	133	143	ps
0.9	34	113	85	96	102	130	118	129	ps
0.8	29	93	66	79	80	111	99	111	ps
0.7	22	66	42	56	51	87	75	89	ps
0.6	note	30	10	27	13	55	43	59	ps
0.5	note	note	note	note	Note	10	Note	18	ps
<0.5	note	note	note	note	Note	10	Note	18	ps

NOTE:

1. Rising input signal shall become equal to or greater than VIH(ac) level and falling input signal shall become equal to or less than VIL(ac) level.

Data Setup, Hold, and Slew Rate De-rating

For all input signals the total tDS (setup time) and tDH (hold time) required is calculated by adding the data sheet tDH(base) and tDH(base) value to the delta tDS and delta tDH derating value respectively. Example: tDS (total setup time) = tDS(base) + delta tDS

Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of Vref(dc) and the first crossing of VIH(ac)min. Setup (tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of Vref(dc) and the first crossing of VIL(ac)max. If the actual signal is always earlier than the nominal slew rate line between shaded 'Vref(dc) to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded 'Vref(dc) to ac region', the slew rate of the tangent line to the actual signal from the ac level to dc level is used for derating value.

Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(dc)max and the first crossing of Vref(dc). Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(dc)min and the first crossing of Vref(dc). If the actual signal is always later than the nominal slew rate line between shaded 'dc level to Vref(dc) region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to Vref(dc) region', the slew rate of a tangent line to the actual signal from the dc level to Vref(dc) level is used for derating value.

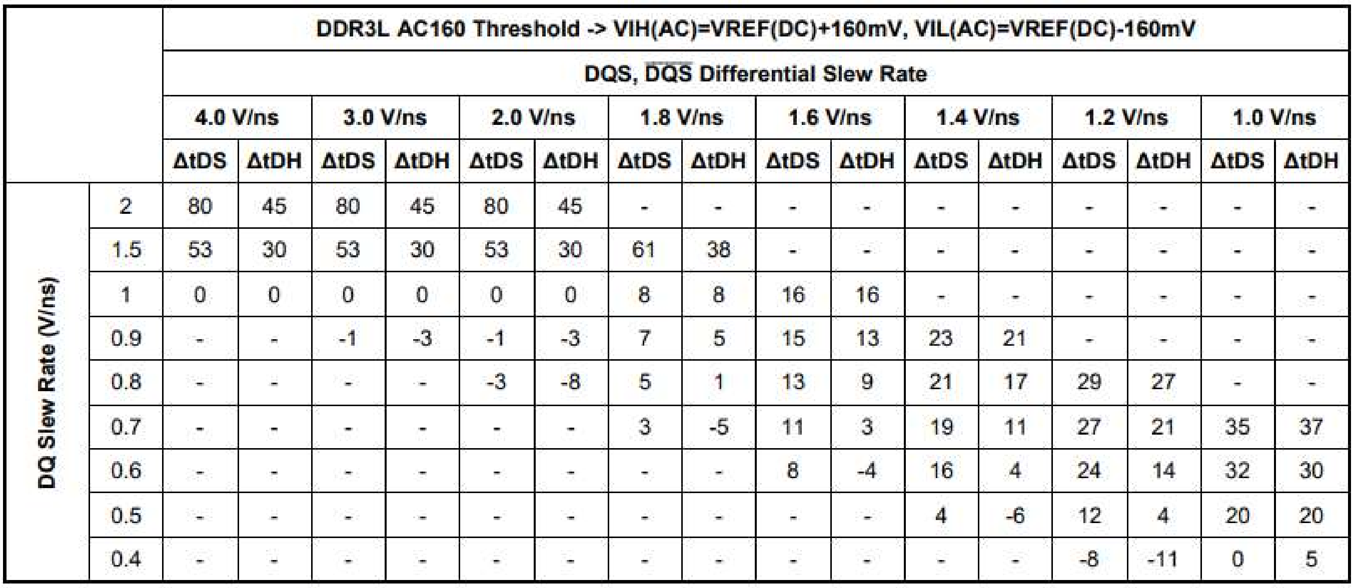
For a valid transition the input signal has to remain above/below VIH/IL(ac) for some time tVAC.

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached VIH/IL(ac) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL(ac).

For slew rates in between the values listed in the following tables, the derating values may be obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

Derating values DDR3L-1066 tDS/tDH - AC/DC based AC160 Threshold



		DDR3L AC160 Threshold -> VIH(AC)=VREF(DC)+160mV, VIL(AC)=VREF(DC)-160mV															
		DQS, $\overline{\text{DQS}}$ Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate (V/ns)	2	80	45	80	45	80	45	-	-	-	-	-	-	-	-	-	-
	1.5	53	30	53	30	53	30	61	38	-	-	-	-	-	-	-	-
	1	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	-1	-3	-1	-3	7	5	15	13	23	21	-	-	-	-
	0.8	-	-	-	-	-3	-8	5	1	13	9	21	17	29	27	-	-
	0.7	-	-	-	-	-	-	3	-5	11	3	19	11	27	21	35	37
	0.6	-	-	-	-	-	-	-	-	8	-4	16	4	24	14	32	30
	0.5	-	-	-	-	-	-	-	-	-	-	4	-6	12	4	20	20
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-8	-11	0	5

NOTE1: Cell contents shaded in gray are defined as 'not supported'.

Derating values DDR3L- 1066/1333/1600 tDS/tDH - AC/DC based AC135 Threshold

		DDR3L Alternate AC135 Threshold -> VIH(AC)=VREF(DC)+135mV, VIL(AC)=VREF(DC)-135mV															
		DQS, $\overline{\text{DQS}}$ Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate (V/ns)	2	45	68	45	68	45	-	-	-	-	-	-	-	-	-	-	-
	1.5	45	30	45	30	45	30	53	38	-	-	-	-	-	-	-	-
	1	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	2	-3	2	-3	10	5	18	13	26	21	-	-	-	-
	0.8	-	-	-	-	3	-8	11	1	19	9	27	17	35	27	-	-
	0.7	-	-	-	-	-	-	14	-5	22	3	30	11	38	21	46	37
	0.6	-	-	-	-	-	-	-	-	25	-4	33	4	41	14	49	30
	0.5	-	-	-	-	-	-	-	-	-	-	29	-6	37	4	45	20
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	30	-11	38	5

Derating values DDR3L- 1866 tDS/tDH - AC/DC based AC130 Threshold

		DDR3L Alternate AC130 Threshold -> VIH(AC)=VREF(DC)+130mV, VIL(AC)=VREF(DC)-130mV																							
		DQS, $\overline{\text{DQS}}$ Differential Slew Rate																							
		8.0 V/ns		7.0 V/ns		6.0 V/ns		5.0 V/ns		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate (V/ns)	4	33	23	33	23	33	23	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	3.5	28	19	28	19	28	19	28	19	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	3	22	15	22	15	22	15	22	15	22	15	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	2.5	-	-	13	9	13	9	13	9	13	9	13	9	-	-	-	-	-	-	-	-	-	-	-	-
	2	-	-	-	-	0	0	0	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-22	-15	-22	-15	-22	-15	-22	-15	-14	-7	-	-	-	-	-	-	-	-
	1	-	-	-	-	-	-	-	-	-65	-45	-65	-45	-65	-45	-57	-37	-49	-29	-	-	-	-	-	-
	0.9	-	-	-	-	-	-	-	-	-	-	-62	-48	-62	-48	-54	-40	-46	-32	-38	-24	-	-	-	-
	0.8	-	-	-	-	-	-	-	-	-	-	-	-	-61	-53	-53	-45	-45	-37	-37	-29	-29	-19	-	-
	0.7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-49	-50	-41	-42	-33	-34	-25	-24	-17	-8
	0.6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-37	-49	-29	-41	-21	-31	-13	-15
	0.5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-31	-51	-23	-41	-15	-25
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-28	-56	-20	-40

Derating values DDR3- 1066 tDS/tDH - AC/DC based AC175 Threshold

		DDR3 AC175 Threshold															
		DQS, $\overline{DQS}$ Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate (V/ns)	2.0	2	50	88	50	88	50	-	-	-	-	-	-	-	-	-	-
	1.5	59	34	59	34	59	34	67	42	-	-	-	-	-	-	-	-
	1	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	-2	-4	-2	-4	6	4	14	12	22	20	-	-	-	-
	0.8	-	-	-	-	-6	-10	2	-2	10	6	18	14	26	24	-	-
	0.7	-	-	-	-	-	-	-3	-8	5	0	13	8	21	18	29	34
	0.6	-	-	-	-	-	-	-	-	-1	-10	7	-2	15	8	23	24
	0.5	-	-	-	-	-	-	-	-	-	-	-11	-16	-2	-6	5	10
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-30	-26	-22	-10

Derating values DDR3- 1066/1333/1600 tDS/tDH - AC/DC based AC150 Threshold

		DDR3 AC150 Threshold															
		DQS, $\overline{DQS}$ Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate (V/ns)	2	50	75	50	75	50	-	-	-	-	-	-	-	-	-	-	-
	1.5	50	34	50	34	50	34	58	42	-	-	-	-	-	-	-	-
	1	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	0	-4	0	-4	8	4	16	12	24	20	-	-	-	-
	0.8	-	-	-	-	0	-10	8	-2	16	6	24	14	32	24	-	-
	0.7	-	-	-	-	-	-	8	-8	16	0	24	8	32	18	40	34
	0.6	-	-	-	-	-	-	-	-	15	-10	23	-2	31	8	39	24
	0.5	-	-	-	-	-	-	-	-	-	-	14	-16	22	-6	30	10
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	7	-26	15	-10

Derating values DDR3- 1866 tDS/tDH - AC/DC based AC135 Threshold

	DDR3 Alternate AC135 Threshold -> VIH(ac)=VREF(dc)+135mV, VIL(ac)=VREF(dc)-135mV Alternate DC100 Threshold -> VIH(dc)=VREF(dc)+100mV, VIL(dc)=VREF(dc)-100mV																							
	DQS, $\overline{\text{DQS}}$ Differential Slew Rate																							
	8.0 V/ns		7.0 V/ns		6.0 V/ns		5.0 V/ns		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate (V/ns) 4	34	25	34	25	34	25	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
3.5	29	21	29	21	29	21	29	21	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
3	23	17	23	17	23	17	23	17	23	17	-	-	-	-	-	-	-	-	-	-	-	-	-	-
2.5	-	-	14	10	14	10	14	10	14	10	14	10	-	-	-	-	-	-	-	-	-	-	-	-
2	-	-	-	-	0	0	0	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-
1.5	-	-	-	-	-	-	-23	-17	-23	-17	-23	-17	-23	-17	-15	-9	-	-	-	-	-	-	-	-
1	-	-	-	-	-	-	-	-	-68	-50	-68	-50	-68	-50	-60	-42	-52	-34	-	-	-	-	-	-
0.9	-	-	-	-	-	-	-	-	-	-	-66	-54	-66	-54	-58	-46	-50	-38	-42	-30	-	-	-	-
0.8	-	-	-	-	-	-	-	-	-	-	-	-	-64	-60	-56	-52	-48	-44	-40	-36	-32	-26	-	-
0.7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-53	-59	-45	-51	-37	-43	-29	-33	-21	-17
0.6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-43	-61	-35	-53	-27	-43	-19	-27
0.5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-39	-66	-31	-56	-23	-40
0.4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-38	-76	-30	-60

Derating values DDR3- 1066/1333/1600 tDS/tDH - AC/DC based AC135 Threshold

	DDR3 Alternate AC135 Threshold -> VIH(ac)=VREF(dc)+135mV, VIL(ac)=VREF(dc)-135mV Alternate DC100 Threshold -> VIH(dc)=VREF(dc)+100mV, VIL(dc)=VREF(dc)-100mV															
	DQS, $\overline{\text{DQS}}$ Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate (V/ns) 2	68	50	68	50	68	50	-	-	-	-	-	-	-	-	-	-
1.5	45	34	45	34	45	34	53	42	-	-	-	-	-	-	-	-
1	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
0.9	-	-	2	-4	2	-4	10	4	18	12	26	20	-	-	-	-
0.8	-	-	-	-	3	-10	11	-2	19	6	27	14	35	24	-	-
0.7	-	-	-	-	-	-	14	-8	22	0	30	8	38	18	46	34
0.6	-	-	-	-	-	-	-	-	25	-10	33	-2	41	8	49	24
0.5	-	-	-	-	-	-	-	-	-	-	29	-16	37	-6	45	10
0.4	-	-	-	-	-	-	-	-	-	-	-	-	30	-26	38	-10

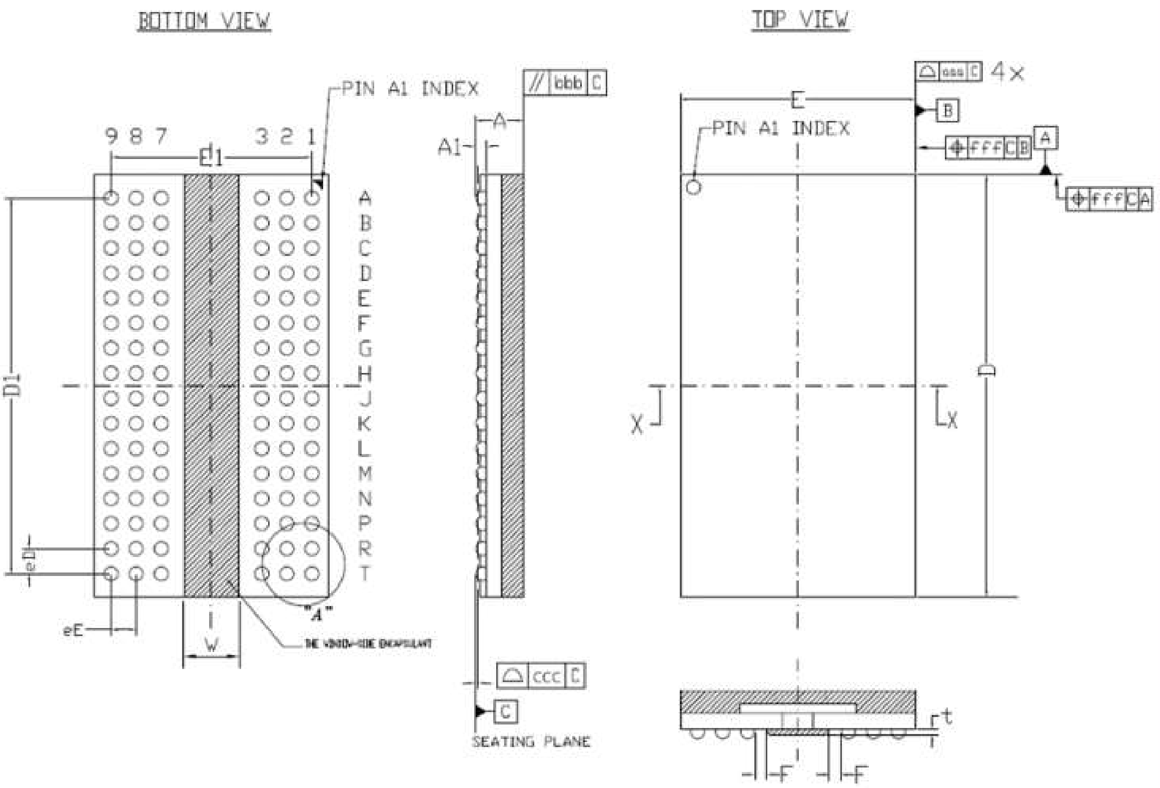
Required time tVAC above VIH(ac) {below VIL(ac)} for DQ transition

Slew Rate [V/ns]	DDR3				DDR3L			Unit
	1066	1066/1333/1600	1066/1333/1600	1866	1066	1066/1333/ 1600	1866	
	175mV[ps]	150mV[ps]	135mV [ps]	135mV [ps]	160 mV[ps]	135 mV[ps]	130 mV[ps]	
> 2.0	75	105	113	93	165	113	95	ps
2.0	57	105	113	93	165	113	95	ps
1.5	50	80	90	70	138	90	73	ps
1.0	38	30	45	25	85	45	30	ps
0.9	34	13	30	note	67	30	16	ps
0.8	29	note	11	note	45	11	Note	ps
0.7	note	note	note	-	16	Note	-	ps
0.6	note	note	note	-	Note	Note	-	ps
0.5	note	note	note	-	Note	Note	-	ps
<0.5	note	note	note	-	Note	Note	-	ps

Note:

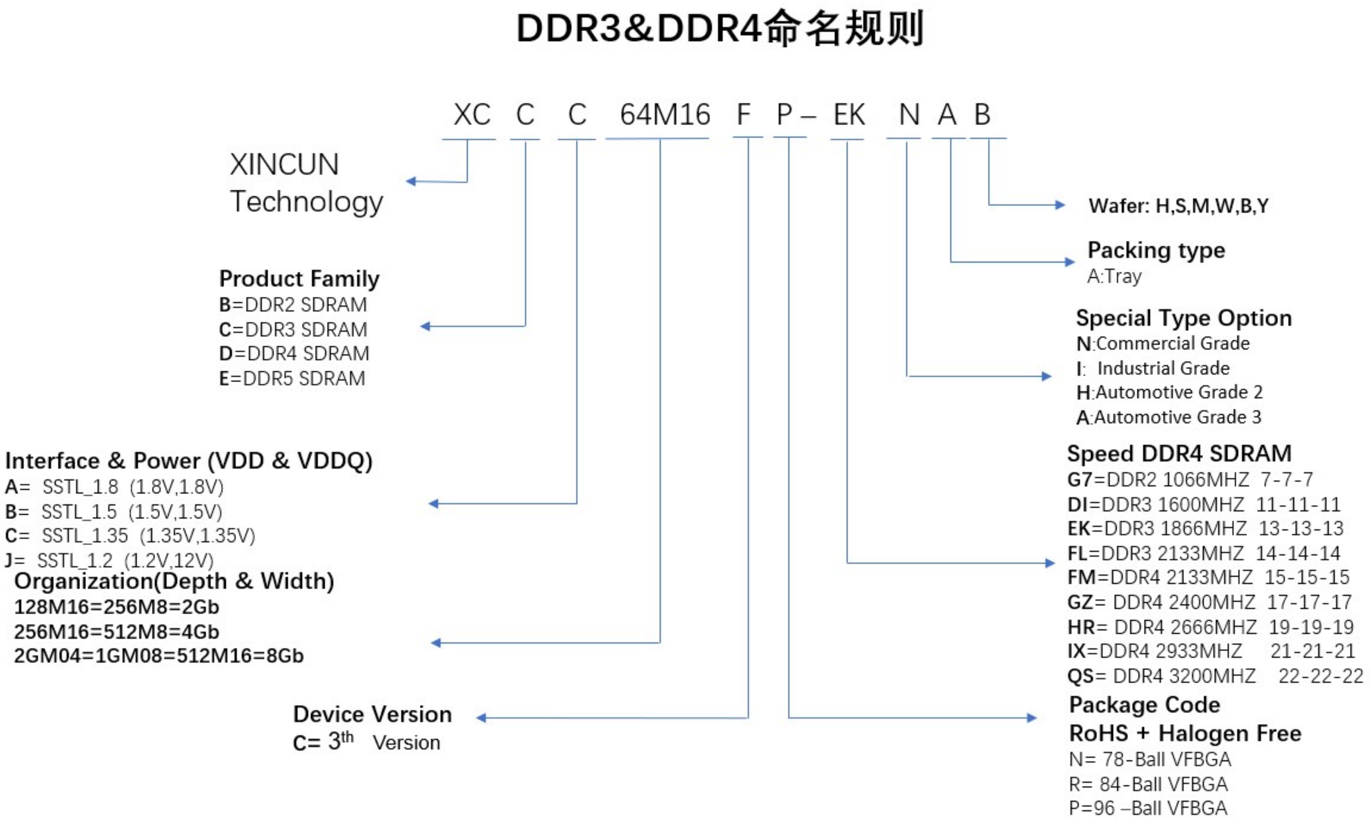
1. Rising input signal shall become equal to or greater than VIH(ac) level and falling input signal shall become equal to or less than VIL(ac) level.

5. PACKAGE DIMENSION (96Ball FBGA, 7.5x13.5x1.2mm)



REF.	Dimension in mm		
	MIN.	NOM.	MAX.
A	---	---	1.20
A1	0.30	0.35	0.40
b	0.40	0.45	0.50
D	13.40	13.50	13.60
E	7.40	7.50	7.60
D1	12.00 BSC		
E1	6.40 BSC		
eE	0.80 BSC		
eD	0.80 BSC		
aaa	---	---	0.10
bbb	---	---	0.10
ccc	---	---	0.08
ddd	---	---	0.15
eee	---	---	0.05
fff	---	---	0.20
F	0.1	---	---
t	0.10	0.15	0.20
W	---	---	2.00

6. PART NUMBER LOGIC



DDR3&DDR4命名规则

XC C C 64M16 F P – EK N A B

XINCUN
Technology

Product Family
B=DDR2 SDRAM
C=DDR3 SDRAM
D=DDR4 SDRAM
E=DDR5 SDRAM

Interface & Power (VDD & VDDQ)
A= SSTL_1.8 (1.8V,1.8V)
B= SSTL_1.5 (1.5V,1.5V)
C= SSTL_1.35 (1.35V,1.35V)
J= SSTL_1.2 (1.2V,12V)

Organization(Depth & Width)
128M16=256M8=2Gb
256M16=512M8=4Gb
2GM04=1GM08=512M16=8Gb

Device Version
C= 3th Version

Wafer: H,S,M,W,B,Y

Packing type
A:Tray

Special Type Option
N:Commercial Grade
I: Industrial Grade
H:Automotive Grade 2
A:Automotive Grade 3

Speed DDR4 SDRAM
G7=DDR2 1066MHZ 7-7-7
DI=DDR3 1600MHZ 11-11-11
EK=DDR3 1866MHZ 13-13-13
FL=DDR3 2133MHZ 14-14-14
FM=DDR4 2133MHZ 15-15-15
GZ= DDR4 2400MHZ 17-17-17
HR= DDR4 2666MHZ 19-19-19
IX=DDR4 2933MHZ 21-21-21
QS= DDR4 3200MHZ 22-22-22

Package Code
RoHS + Halogen Free
N= 78-Ball VFBGA
R= 84-Ball VFBGA
P=96 –Ball VFBGA

XIN XC CUN

http//www.szxincun.com