DDR3 SDRAM 2Gbit Datesheet

XCCB128M16FP-EKNAH

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Using This Document

This document is intended for hardware and software engineer’s general information on the XCCB128M16FP-EKNAH.Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

Revision History

Revision	Date	Description
Rev 1.0	2021/11/30	Create new document
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Document Index

1. INTRODUCTION 3
1.1 Application 3
1.2 Features 3
1.3 Device Features and Ordering Information 4
2. FUNCTION DIAGRAM 4
2.1 DDR3 SDRAM 5
3. PIN CONFIGURATION 6
3.1 Pin Assignment 6
3.2 Pin Descriptions 7
3.3 ROW AND COLUMN ADDRESS TABLE 9
4. DDR3 SDRAM SPECIFICATION 10
4.1 Absolute Maximum Ratings 10
4.2 DRAM Component Operating Temperature Range 10
4.3 AC & DC Operating Conditions 11
4.4 IDD and IDDQ Specification Parameters and Test Conditions 12
4.5 State Diagram 30
4.6 Operation Mode Truth Table 31
4.7 Register Definition 35
4.8 READ Operation 64
4.9 Writer Operation 68
4.10 Power-Down Modes 70
4.11 On-Die Termination(ODT) 71
4.12 ZQ Calibration Commands 76
5. PACKAGE DIMENSION (96Ball FBGA,7.5x13x1.1mm) 108
6. PART NUMBER LOGIC 109

1. INTRODUCTION

XCCB128M16FP-EKNAH is a 2,147,483,648-bit CMOS Double Data Rate III (DDR3) Synchronous DRAM, ideally suited for the main memory applications which requires large memory density and high bandwidth. XINCUN 2Gb DDR3 SDRAMs offer fully synchronous operations ref-erenced to both rising and falling edges of the clock. While all addresses and control inputs are latched on the rising edges of the CK (falling edges of the CK), Data, Data strobes and Write data masks inputs are sampled on both rising and falling edges of it. The data paths are internally pipelined and 8-bit prefetched to achieve very high bandwidth.

1.1 Application

- Compact DSC / CAR Black Box / Action Cam / 360 Cam
- Drone
- Wearable

1.2 Features

PRODUCT LIST

- XCCB128M16FP-EKNAH
  - DDR3 SDRAM: 2G bits (16Mx8-Bank x16-bit)

POWER SUPPLY

- DDR3 SDRAM
  - DDR3 : 1.5V ±0.075V

PACKAGE

- FBGA 7.5 x 13 x 1.1mm, 96 Balls
- Ball Pitch: 0.8mm
- Weight: 200mg ±5mg

Temperature

- Operating: 0 to +95°C
- Storage: -55 to +125°C

1.3 Device Features and Ordering Information

- VDD=VDDQ=1.5V +/- 0.075V
- Fully differential clock inputs (CK, $\overline{CK}$) operation
- Differential Data Strobe (DQS, $\overline{DQS}$)
- On chip DLL align DQ, DQS and $\overline{DQS}$ transition with CK transition
- DM masks write data-in at the both rising and falling edges of the data strobe
- All addresses and control inputs except data,

data strobes and data masks latched on the rising edges of the clock

- Programmable CAS latency 5, 6, 7, 8, 9, 10, 11, 12, 13 and 14 supported
- Programmable additive latency 0, CL-1, and CL-2 supported
- Programmable CAS Write latency (CWL) = 5, 6, 7, 8 9 and 10
- Programmable burst length 4/8 with both nibble sequential and interleave mode
- BL switch on the fly

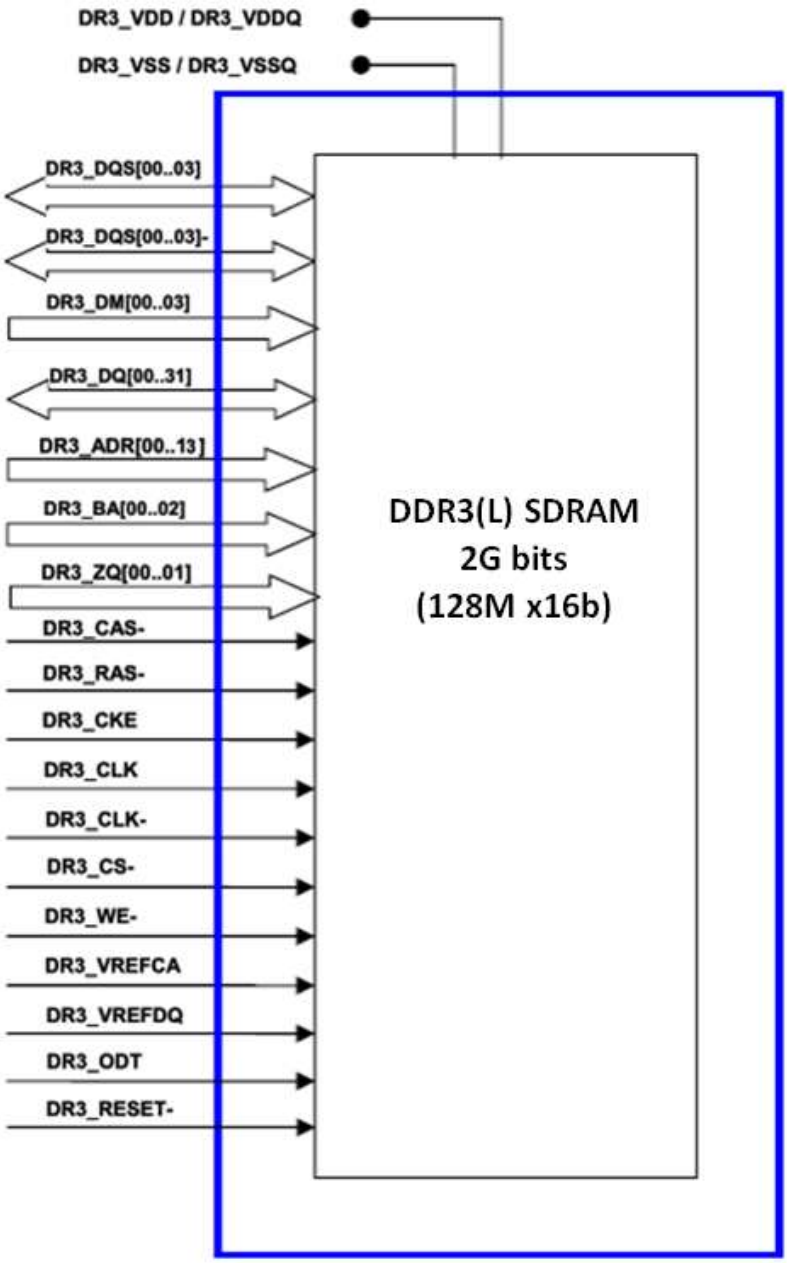
- 8banks
- AverageRefreshCycle(Tcase0 °C~95°C)
  - 7.8 µs at 0°C ~ 85 °C
  - 3.9 µs at 85°C ~ 95 °C

    Commercial Temperature(0°C ~ 95 °C)

    Industrial Temperature(-40°C ~ 95 °C)
- JEDEC standard 96ball FBGA(x16)
- Driver strength selected by EMRS
- Dynamic On Die Termination supported
- Asynchronous RESET pin supported
- ZQ calibration supported
- TDQS (Termination Data Strobe) supported (x8 only)
- Write Levelization supported
- 8 bit pre-fetch

2. FUNCTION DIAGRAM

2.1 DDR3 SDRAM



3.0 PIN CONFIGURATION

3.1 Pin Assignment

	1	2	3	4	5	6	7	8	9
A	DR3_VDDQ	DR3_DQ13	DR3_DQ15				DR3_DQ12	DR3_VDDQ	DR3_VSS
B	DR3_VSSQ	DR3_VDD	DR3_VSS				DR3_DQS01-	DR3_DQ14	DR3_VSSQ
C	DR3_VDDQ	DR3_DQ11	DR3_DQ09				DR3_DQS01	DR3_DQ10	DR3_VDDQ
D	DR3_VSSQ	DR3_VDDQ	DR3_DM01				DR3_DQ08	DR3_VSSQ	DR3_VDD
E	DR3_VSS	DR3_VSSQ	DR3_DQ00				DR3_DM00	DR3_VSSQ	DR3_VDDQ
F	DR3_VDDQ	DR3_DQ02	DR3_DQS00				DR3_DQ01	DR3_DQ03	DR3_VSSQ
G	DR3_VSSQ	DR3_DQ06	DR3_DQS00-				DR3_VDD	DR3_VSS	DR3_VSSQ
H	DR3_VREFDQ	DR3_VDDQ	DR3_DQ04				DR3_DQ07	DR3_DQ05	DR3_VDDQ
J	NC	DR3_VSS	DR3_RAS-				DR3_CLK	DR3_VSS	NC
K	DR3_ODT00	DR3_VDD	DR3_CAS-				DR3_CLK-	DR3_VDD	DR3_CKE00
L	NC	DR3_CS00-	DR3_WE-				DR3_ADR10/AP	DR3_ZQ00	NC
M	DR3_VSS	DR3_BA00	DR3_BA02				NC/DR3_ADR15	DR3_VREFCA	DR3_VSS
N	DR3_VDD	DR3_ADR03	DR3_ADR00				DR3_ADR12	DR3_BA01	DR3_VDD
P	DR3_VSS	DR3_ADR05	DR3_ADR02				DR3_ADR01	DR3_ADR04	DR3_VSS
R	DR3_VDD	DR3_ADR07	DR3_ADR09				DR3_ADR11	DR3_ADR06	DR3_VDD
T	DR3_VSS	DR3_RESET-	DR3_ADR13				NC/DR3_ADR14	DR3_ADR08	DR3_VSS

TOP VIEW

3.2 Pin Descriptions

Type Symbol	Description	Type Symbol	Description
I	Input	P	Power
O	Output	G	Ground
I/O	Bi-direction	X	No connect (No function, don't care)

Symbol	Type	Count	Description
DR3_ADR[00..13] (A0~A13)	I	14	**Address inputs:** Provide the row address for ACTIVATE commands, and the columnaddress and auto precharge bit (A10) for READ/WRITE commands, to select onelocation out of the memory array in the respective bank. A10 sampled during aPRECHARGE command determines whether the PRECHARGE applies to one bank (A10LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to V_{REFCA}. A12/$\overline{BC}$: When enabled in the mode register (MR), A12 is sampled during READand WRITE commands to determine whether burst chop (on-the-fly) will be performed(HIGH = BL8 or no burst chop, LOW = BC4). See Table 4-63.
DR3_BA[00..02] (BA0~BA2/ BA[2:0])	I	3	**Bank address inputs:** BA[2:0] define the bank to which an ACTIVATE, READ, WRITE,or PRECHARGE command is being applied. BA[2:0] define which moderegister (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. BA[2:0]are referenced to V_{REFCA}.
DR3_RESET- (/ RESET or $\overline{RESET}$)	I	1	**Reset:** $\overline{RESET}$ is an active LOW CMOS input referenced to V_{SS}. The $\overline{RESET}$ input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 × V_{DD} andDC LOW ≤ 0.2 × V_{DDQ}. RESET# assertion and de-assertion are asynchronous.
DR3_DQ[00..15] (DQ0~DQ15)	I/O	16	**Data Inputs/Output:** Bi-directional data bus, Referenced to V_{REFDQ}.
DR3_RAS-, DR3_CAS-, DR3_WE- ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	I	3	**Command inputs:** $\overline{RAS}$ $\overline{CAS}$, and $\overline{WE}$ (along with $\overline{CS}$) define the commandbeing entered and are referenced to V_{REFCA}.
DR3_CKE (CKE)	I	1	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) internalcircuitry and clocks on the DRAM. The specific circuitry that is enabled/disabled is dependent upon the DDR3 SDRAM configuration and operating mode. Taking CKE LOWprovides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle),oractive power-down (row active in any bank). CKE is synchronous forpower-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, $\overline{CK}$, CKE, $\overline{RESET}$, and ODT) are disabled duringPOWER-DOWN. Input buffers (excluding CKE and $\overline{RESET}$) are disabled during SELF REFRESH. CKE is referenced to V_{REFCA}.

Symbol	Type	Count	Description
DR3_CKE (CKE)	I	1	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) internalcircuitry and clocks on the DRAM. The specific circuitry that is enabled/disabled is dependent upon the DDR3 SDRAM configuration and operating mode. Taking CKE LOWprovides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle),oractive power-down (row active in any bank). CKE is synchronous forpower-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, $\overline{CK}$, CKE, $\overline{RESET}$, and ODT) are disabled duringPOWER-DOWN. Input buffers (excluding CKE and $\overline{RESET}$) are disabled during SELF REFRESH. CKE is referenced to V_{REFCA}.
DR3_CLK, DR3_CLK- (CK,$\overline{CK}$)	I	2	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All control and address input signalsare sampled on the crossing of the positive edge of CK and the negative edge of $\overline{CK}$.Output data strobe (DQS, $\overline{DQS}$) is referenced to the crossings of CK and $\overline{CK}$.
DR3_CS- ($\overline{CS}$)	I	1	**Chip select:** $\overline{CS}$ enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external rank selection on systems with multiple ranks. $\overline{CS}$ is considered part of the command code. $\overline{CS}$ is referenced to V_{REFCA}.
DR3_ODT (ODT)	I	1	**On-die termination:** ODT enables (registered HIGH) and disables (registered LOW)termination resistance internal to the DDR3 SDRAM. When enabled in normaloperation, ODT is only applied to each of the following balls: DQ[7:0], DQS, $\overline{DQS}$,and DM for the x8; DQ[3:0], DQS, $\overline{DQS}$, and DM for the x4. The ODT input isignored if disabled via the LOAD MODE command. ODT is referenced to V_{REFCA}.
DR3_DQS00 (LDQS), DR3_DQS00- (/LDQS) DR3_DQS01 (UDQS), DR3_DQS01- (/UDQS) (DQS,$\overline{DQS}$)	I/O	4	**Lower byte data strobe:** Output with read data. Edge-aligned with read data. Inputwith write data. Center-aligned to write data. **Upper byte data strobe:** Output with read data. Edge-aligned with read data. Inputwith write data. DQS is center-aligned to write data.
DR3_DM00 (LDM) DR3_DM01 (UDM)	I	2	**Input data mask:** DM is an input mask signal for write data. Input data is maskedwhen DM is sampled HIGH along with the input data during a write access.Although the DM ball is input-only, the DM loading is designed to match that of theDQ and DQS balls. DM is referenced to V_{REFDQ}.
DR3_VREFCA (VREFCA)	P	1	Reference voltage for control, command, and address: VREFCA must be maintained at all times (including self refresh) for proper device operation.
DR3_VREFDQ (VREFDQ)	P	1	Reference voltage for data: VREFDQ must be maintained at all times (excluding selfrefresh) for proper device operation.
DR3_ZQ (ZQ)	P	1	External reference ball for output drive calibration: This ball is tied to external240Ω resistor RZQ, which is tied to VSSQ.

Symbol	Type	Count	Description
DR3_VDD (VDD)	P	9	Power Supply:1.5V (1.425–1.575V)
DR3_VDDQ (VDDQ)	P	9	DQ Power Supply: 1.5V (1.425–1.575V)
DR3_VSS (VSS)	G	12	Ground
DR3_VSSQ (VSSQ)	G	9	DQ Ground
NC	X	6	Not Connect Pin (Don't Care)

Note:

Input only pins (BA0-BA2, A0-A15, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, ODT, DM, and $\overline{RESET}$) do not supply termination.

3.3 ROW AND COLUMN ADDRESS TABLE

Configuration	128Mb x 16
# of Banks	8
Bank Address	BA0 - BA2
Auto precharge	A10/AP
BL switch on the fly	A12/BC
Row Address	A0 - A13
Column Address	A0 - A9
Page size [1]	2 KB

Note1: Page size is the number of bytes of data delivered from the array to the internal sense amplifiers when an ACTIVE command is registered. Page size is per bank, calculated as follows:

$$\textbf{page size} = 2^{\textbf{COLBITS}} * \textbf{ORG} \div 8$$

where COLBITS = the number of column address bits, ORG = the number of I/O (DQ) bits

4.0 DDR3 SDRAM SPECIFICATION

4.1 Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
VDD	Voltage on VDD pin relative to Vss	0.4V-1.8V	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	0.4V-1.8V	V	1,3
V_{IN}, V_{OUT}	Voltage on any pin relative to Vss	0.4V-1.8V	V	1
T_{STG}	Storage Temperature	-55 to +125	oC	1, 2

Notes:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300mV of each other at all times; and VREF must not be greater than 0.6XVDDQ,When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

4.2 DRAM Component Operating Temperature Range

Temperature Range

Symbol	Parameter	Rating	Units	Notes
T_{OPER}	Normal Operating Temperature Range	0 to 85	oC	1,2
	Extended Temperature Range	85 to 95	oC	1,4
	Industrial Temperature Range	-40 to 95	oC	1,3,4

Notes:

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.

2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 - 85oC under all operating conditions.

3. The Industrial Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between -40 - 85oC under all operating conditions.

4. Some applications require operation of the DRAM in the Extended Temperature Range between 85oC and 95oC case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply: a. Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs.

b. If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b).

4.3 AC & DC Operating Conditions

Recommended DC Operating Conditions

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.425	1.500	1.575	V	1,2
VDDQ	Supply Voltage for Output	1.425	1.500	1.575	V	1,2

Notes:

1. Under all conditions, VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

4.4 IDD and IDDQ Specification Parameters and Test Conditions

IDD and IDDQ Measurement Conditions

In this chapter, IDD and IDDQ measurement conditions such as test load and patterns are defined. Figure 1. shows the setup and test load for IDD and IDDQ measurements.

- IDD currents (such as IDD0, IDD1, IDD2N, IDD2NT, IDD2P0, IDD2P1, IDD2Q, IDD3N, IDD3P, IDD4R, IDD4W, IDD5B, IDD6, IDD6ET, IDD6TC and IDD7) are measured as time-averaged currents with all VDD balls of the DDR3 SDRAM under test tied together. Any IDDQ current is not included in IDD currents.
- IDDQ currents (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR3 SDRAM under test tied together. Any IDD current is not included in IDDQ cur-rents.

  Attention: IDDQ values cannot be directly used to calculate IO power of the DDR3 SDRAM. They can be used to support correlation of simulated IO power to actual IO power as outlined in Figure 2. In DRAM module application, IDDQ cannot be measured separately since VDD and VDDQ are using one merged-power layer in Module PCB.

  For IDD and IDDQ measurements, the following definitions apply:

- ”0” and “LOW” is defined as VIN <= $V_{ILAC(max)}$.
- ”1” and “HIGH” is defined as VIN >= $V_{IHAC(max)}$.
- “MID_LEVEL” is defined as inputs are VREF = VDD/2.
- Timing used for IDD and IDDQ Measurement-Loop Patterns are provided in Table 1.
- Basic IDD and IDDQ Measurement Conditions are described in Table 2.
- Detailed IDD and IDDQ Measurement-Loop Patterns are described in Table 3 through Table 10.
- IDD Measurements are done after properly initializing the DDR3 SDRAM. This includes but is not limited to setting

  RON = RZQ/7 (34 Ohm in MR1);

  Qoff = 0_B (Output Buffer enabled in MR1); RTT_Nom = RZQ/6 (40 Ohm in MR1); RTT_Wr = RZQ/2 (120 Ohm in MR2); TDQS Feature disabled in MR1
- Attention: The IDD and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.
- Define D = {$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$}:= {HIGH, LOW, LOW, LOW}
- Define D = {$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$}:= {HIGH, HIGH, HIGH, HIGH}

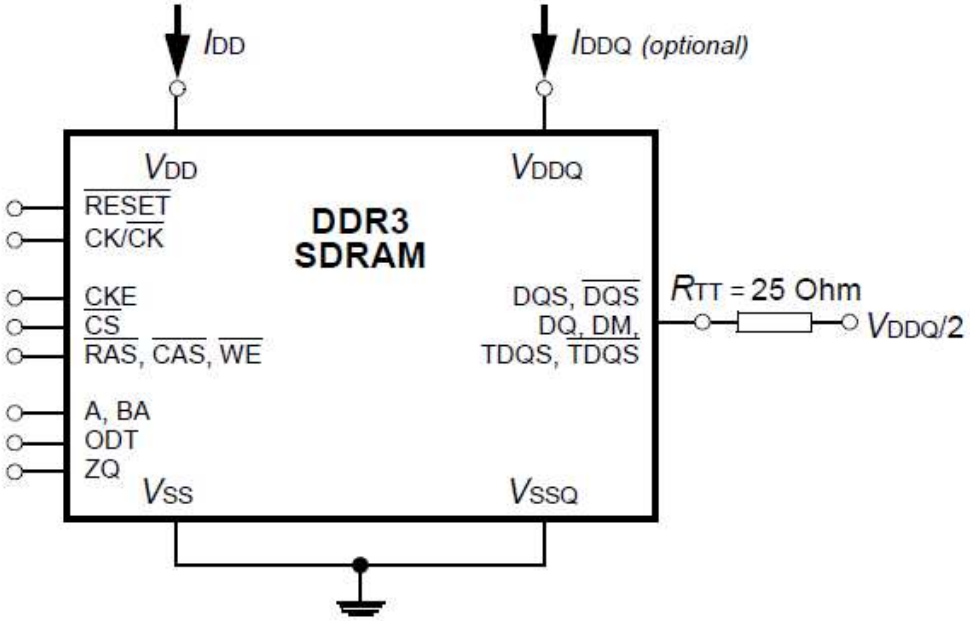


Figure 1 - Measurement Setup and Test Load for IDD and IDDQ (optional) Measurements [Note: DIMM level Output test load condition may be different from above]

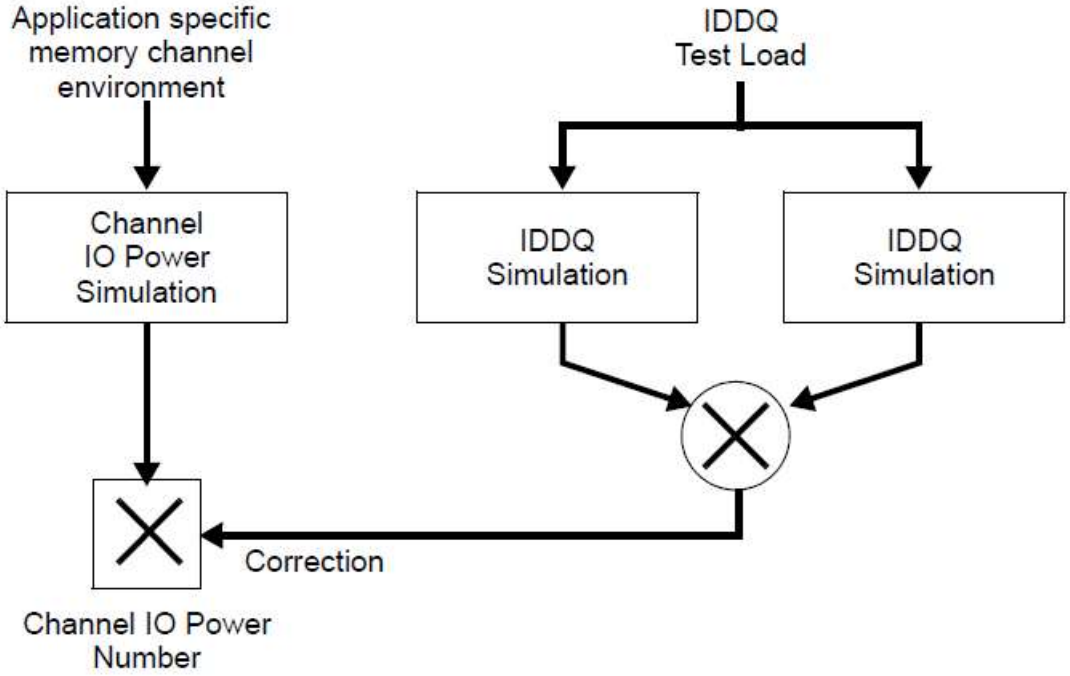


Figure 2 - Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement

Table 1 -Timings used for IDD and IDDQ Measurement-Loop Patterns

Symbol		DDR3-1600	DDR3-1866	Unit
		11-11-11	13-13-13	
^{t}CK		1.25	1.07	ns
CL		11	13	nCK
^{n}RCD		11	13	nCK
^{n}RC		39	45	nCK
^{n}RAS		28	32	nCK
^{n}RP		11	13	nCK
^{n}FAW	1KB page size	24	26	nCK
		32	33	nCK
^{n}RRD	2KB page size	5	5	nCK
		6	6	nCK
n_{RFC} -512Mb		72	85	nCK
n_{RFC}-1 Gb		88	103	nCK
n_{RFC}- 2 Gb		128	150	nCK
n_{RFC}- 4 Gb		240	281	nCK
n_{RFC}- 8 Gb		280	328	nCK

Table 2 -Basic IDD and IDDQ Measurement Conditions

Symbol	Description
I_{DD0}	Operating One Bank Active-Precharge Current CKE: High; External clock: On; tCK, nRC, nRAS, CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$: High between ACT and PRE; Command, Address, Bank Address Inputs: partially toggling according to Table 3; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 3); Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Pattern Details: see Table 3.

Symbol	Description
I_{DD1}	Operating One Bank Active-Read-Precharge Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$: High between ACT, RD and PRE; Command, Address; Bank Address Inputs, Data IO: partially toggling according to Table 4; DM: stable at 0; Bank Activity: Cycling with on bank active at a time: 0,0,1,1,2,2,... (see Table 4); Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Pattern Details: see Table 4.
I_{DD2N}	Precharge Standby Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: partially toggling according to Table 5; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Pattern Details: see Table 5.
I_{DD2NT}	Precharge Standby ODT Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: partially toggling according to Table 6; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: toggling according to Table 6; Pattern Details: see Table 6.
I_{DD2P0}	Precharge Power-Down Current Slow Exit CKE: Low; External clock: On; tCK, CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Precharge Power Down Mode: Slow Exit[c]
I_{DD2P1}	Precharge Power-Down Current Fast Exit CKE: Low; External clock: On; tCK, CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Precharge Power Down Mode: Fast Exit[c]
I_{DD2Q}	Precharge Quiet Standby Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0

Symbol	Description
I_{DD3N}	Active Standby Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: partially toggling according to Table 5; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Pattern Details: see Table 5.
I_{DD3P}	Active Power-Down Current CKE: Low; External clock: On; tCK, CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0
I_{DD4R}	Operating Burst Read Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$: High between RD; Command, Address, Bank Address Inputs: partially toggling according to Table 7; Data IO: seamless read data burst with different data between one burst and the next one according to Table 7; DM: stable at 0; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,...(see Table 7); Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Pattern Details: see Table 7.
I_{DD4W}	Operating Burst Write Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$: High between WR; Command, Address, Bank Address Inputs: partially toggling according to Table 8; Data IO: seamless read data burst with different data between one burst and the next one according to Table 8; DM: stable at 0; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,...(see Table 8); Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at HIGH; Pattern Details: see Table 8.
I_{DD5B}	Burst Refresh Current CKE: High; External clock: On; tCK, CL, nRFC: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$: High between REF; Command, Address, Bank Address Inputs: partially toggling according to Table 9; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: REF command every nREF (see Table 9); Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Pattern Details: see Table 9.
I_{DD6}	Self-Refresh Current: Normal Temperature Range T_{CASE}: 0 - 85 °C; Auto Self-Refresh (ASR): Disabled[d];Self-Refresh Temperature Range (SRT): Normal[e]; CKE: Low; External clock: Off; CK and $\overline{CK}$: LOW; CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$, Command, Address, Bank Address Inputs, Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: MID_LEVEL

Symbol	Description
I_{DD6ET}	Self-Refresh Current: Extended Temperature Range (optional)[f] T_{CASE}: 0 - 95 °C; Auto Self-Refresh (ASR): Disabled[d];Self-Refresh Temperature Range (SRT): Extended[e]; CKE: Low; External clock: Off; CK and $\overline{CK}$: LOW; CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$, Command, Address, Bank Address Inputs, Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: MID_LEVEL
I_{DD7}	Operating Bank Interleave Read Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, NRRD, nFAW, CL: see Table 1; BL: 8[a], [f]; AL: CL-1; $\overline{CS}$: High between ACT and RDA; Command, Address, Bank Address Inputs: partially toggling according to Table 10; Data IO: read data burst with different data between one burst and the next one according to Table 10; DM: stable at 0; Bank Activity: two times interleaved cycling through banks (0, 1,...7) with different addressing, wee Table 10; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Pattern Details: see Table 10.

a) Burst Length: BL8 fixed by MRS: set MR0 A[1,0]=00B

b) Output Buffer Enable: set MR1 A[12] = 0B; set MR1 A[5,1] = 01B; RTT_Nom enable: set MR1 A[9,6,2] = 011B; RTT_Wr enable: set MR2 A[10,9] = 10B

c) Precharge Power Down Mode: set MR0 A12=0B for Slow Exit or MR0 A12 = 1B for Fast Exit

d) Auto Self-Refresh (ASR): set MR2 A6 = 0B to disable or 1B to enable feature

e) Self-Refresh Temperature Range (SRT): set MR2 A7 = 0B for normal or 1B for extended temperature range

f) Read Burst Type: Nibble Sequential, set MR0 A[3] = 0B

Table 3 - IDD0 Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1,2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary												
			nRAS	PRE	0	0	1	0	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary												
			1*nRC+0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			1*nRC+1, 2	D, D	1	0	0	0	0	0	00	0	0	F	0	-
			1*nRC+3, 4	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	F	0	-
			...	repeat pattern 1...4 until 1*nRC + nRAS - 1, truncate if necessary												
			1*nRC+nRAS	PRE	0	0	1	0	0	0	00	0	0	F	0	-
			...	repeat pattern 1...4 until 2*nRC - 1, truncate if necessary												
		1	2*nRC	repeat Sub-Loop 0, use BA[2:0] = 1 instead												
		2	4*nRC	repeat Sub-Loop 0, use BA[2:0] = 2 instead												
		3	6*nRC	repeat Sub-Loop 0, use BA[2:0] = 3 instead												
		4	8*nRC	repeat Sub-Loop 0, use BA[2:0] = 4 instead												
		5	10*nRC	repeat Sub-Loop 0, use BA[2:0] = 5 instead												
		6	12*nRC	repeat Sub-Loop 0, use BA[2:0] = 6 instead												
		7	14*nRC	repeat Sub-Loop 0, use BA[2:0] = 7 instead												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are MID-LEVEL.

b) DQ signals are MID-LEVEL.

Table 4 - IDD1 Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1,2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRCD - 1, truncate if necessary												
			nRCD	RD	0	1	0	1	0	0	00	0	0	0	0	00000000
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary												
			nRAS	PRE	0	0	1	0	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary												
			1*nRC+0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			1*nRC+1,2	D, D	1	0	0	0	0	0	00	0	0	F	0	-
			1*nRC+3,4	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	F	0	-
			...	repeat pattern nRC + 1,...4 until nRC + nRCE - 1, truncate if necessary												
			1*nRC+nRCD	RD	0	1	0	1	0	0	00	0	0	F	0	00110011
			...	repeat pattern nRC + 1,...4 until nRC + nRAS - 1, truncate if necessary												
			1*nRC+nRAS	PRE	0	0	1	0	0	0	00	0	0	F	0	-
			...	repeat pattern nRC + 1,...4 until *2 nRC - 1, truncate if necessary												
		1	2*nRC	repeat Sub-Loop 0, use BA[2:0] = 1 instead												
		2	4*nRC	repeat Sub-Loop 0, use BA[2:0] = 2 instead												
		3	6*nRC	repeat Sub-Loop 0, use BA[2:0] = 3 instead												
		4	8*nRC	repeat Sub-Loop 0, use BA[2:0] = 4 instead												
		5	10*nRC	repeat Sub-Loop 0, use BA[2:0] = 5 instead												
		6	12*nRC	repeat Sub-Loop 0, use BA[2:0] = 6 instead												
		7	14*nRC	repeat Sub-Loop 0, use BA[2:0] = 7 instead												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are used according to RD Commands, otherwise MID-LEVEL.

b) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID_LEVEL.

Table 5 - IDD2N and IDD3N Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	D	1	0	0	0	0	0	0	0	0	0	0	-
			1	D	1	0	0	0	0	0	0	0	0	0	0	-
			2	$\overline{D}$	1	1	1	1	0	0	0	0	0	F	0	-
			3	$\overline{D}$	1	1	1	1	0	0	0	0	0	F	0	-
		1	4-7	repeat Sub-Loop 0, use BA[2:0] = 1 instead												
		2	8-11	repeat Sub-Loop 0, use BA[2:0] = 2 instead												
		3	12-15	repeat Sub-Loop 0, use BA[2:0] = 3 instead												
		4	16-19	repeat Sub-Loop 0, use BA[2:0] = 4 instead												
		5	20-23	repeat Sub-Loop 0, use BA[2:0] = 5 instead												
		6	24-17	repeat Sub-Loop 0, use BA[2:0] = 6 instead												
		7	28-31	repeat Sub-Loop 0, use BA[2:0] = 7 instead												

Table 6 - IDD2NT and IDDQ2NT Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	D	1	0	0	0	0	0	0	0	0	0	0	-
			1	D	1	0	0	0	0	0	0	0	0	0	0	-
			2	$\overline{D}$	1	1	1	1	0	0	0	0	0	F	0	-
			3	$\overline{D}$	1	1	1	1	0	0	0	0	0	F	0	-
		1	4-7	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 1												
		2	8-11	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 2												
		3	12-15	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 3												
		4	16-19	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 4												
		5	20-23	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 5												
		6	24-17	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 6												
		7	28-31	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 7												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are MID-LEVEL.

b) DQ signals are MID-LEVEL.

Table 7 - IDD4R and IDDQ4R Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	RD	0	1	0	1	0	0	00	0	0	0	0	00000000
			1	D	1	0	0	0	0	0	00	0	0	0	0	-
			2,3	$\overline{D}$,$\overline{D}$	1	1	1	1	0	0	00	0	0	0	0	-
			4	RD	0	1	0	1	0	0	00	0	0	F	0	00110011
			5	D	1	0	0	0	0	0	00	0	0	F	0	-
			6,7	$\overline{D}$,$\overline{D}$	1	1	1	1	0	0	00	0	0	F	0	-
		1	8-15	repeat Sub-Loop 0, but BA[2:0] = 1												
		2	16-23	repeat Sub-Loop 0, but BA[2:0] = 2												
		3	24-31	repeat Sub-Loop 0, but BA[2:0] = 3												
		4	32-39	repeat Sub-Loop 0, but BA[2:0] = 4												
		5	40-47	repeat Sub-Loop 0, but BA[2:0] = 5												
		6	48-55	repeat Sub-Loop 0, but BA[2:0] = 6												
		7	56-63	repeat Sub-Loop 0, but BA[2:0] = 7												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are used according to RD Commands, otherwise MID-LEVEL.

b) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID-LEVEL.

Table 8 - IDD4W Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	WR	0	1	0	0	1	0	00	0	0	0	0	00000000
			1	D	1	0	0	0	1	0	00	0	0	0	0	-
			2,3	$\overline{D}$,$\overline{D}$	1	1	1	1	1	0	00	0	0	0	0	-
			4	WR	0	1	0	0	1	0	00	0	0	F	0	00110011
			5	D	1	0	0	0	1	0	00	0	0	F	0	-
			6,7	$\overline{D}$,$\overline{D}$	1	1	1	1	1	0	00	0	0	F	0	-
		1	8-15	repeat Sub-Loop 0, but BA[2:0] = 1												
		2	16-23	repeat Sub-Loop 0, but BA[2:0] = 2												
		3	24-31	repeat Sub-Loop 0, but BA[2:0] = 3												
		4	32-39	repeat Sub-Loop 0, but BA[2:0] = 4												
		5	40-47	repeat Sub-Loop 0, but BA[2:0] = 5												
		6	48-55	repeat Sub-Loop 0, but BA[2:0] = 6												
		7	56-63	repeat Sub-Loop 0, but BA[2:0] = 7												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are used according to WR Commands, otherwise MID-LEVEL.

c) Burst Sequence driven on each DQ signal by Write Command. Outside burst operation, DQ signals are MID-LEVEL.

Table 9 - IDD5B Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	REF	0	0	0	1	0	0	0	0	0	0	0	-
		1	1.2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	F	0	-
			5...8	repeat cycles 1...4, but BA[2:0] = 1												
			9...12	repeat cycles 1...4, but BA[2:0] = 2												
			13...16	repeat cycles 1...4, but BA[2:0] = 3												
			17...20	repeat cycles 1...4, but BA[2:0] = 4												
			21...24	repeat cycles 1...4, but BA[2:0] = 5												
			25...28	repeat cycles 1...4, but BA[2:0] = 6												
			29...32	repeat cycles 1...4, but BA[2:0] = 7												
		2	33...nRFC-1	repeat Sub-Loop 1, until nRFC - 1. Truncate, if necessary.												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are MID-LEVEL.

b) DQ signals are MID-LEVEL.

Table 10 - IDD7 Measurement-Loop Pattern[a)]

ATTENTION! Sub-Loops 10-19 have inverse A[6:3] Pattern and Data Pattern than Sub-Loops 0-9

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1	RDA	0	1	0	1	0	0	00	1	0	0	0	00000000
			2	D	1	0	0	0	0	0	00	0	0	0	0	-
			...	repeat above D Command until nRRD - 1												
		1	nRRD	ACT	0	0	1	1	0	1	00	0	0	F	0	-
			nRRD+1	RDA	0	1	0	1	0	1	00	1	0	F	0	00110011
			nRRD+2	D	1	0	0	0	0	1	00	0	0	F	0	-
			...	repeat above D Command until 2* nRRD - 1												
		2	2*nRRD	repeat Sub-Loop 0, but BA[2:0] = 2												
		3	3*nRRD	repeat Sub-Loop 1, but BA[2:0] = 3												
		4	4*nRRD	D	1	0	0	0	0	3	00	0	0	F	0	-
				Assert and repeat above D Command until nFAW - 1, if necessary												
		5	nFAW	repeat Sub-Loop 0, but BA[2:0] = 4												
		6	nFAW+nRRD	repeat Sub-Loop 1, but BA[2:0] = 5												
		7	nFAW+2*nRRD	repeat Sub-Loop 0, but BA[2:0] = 6												
		8	nFAW+3*nRRD	repeat Sub-Loop 1, but BA[2:0] = 7												
		9	nFAW+4*nRRD	D	1	0	0	0	0	7	00	0	0	F	0	-
				Assert and repeat above D Command until 2* nFAW - 1, if necessary												
		10	2*nFAW+0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			2*nFAW+1	RDA	0	1	0	1	0	0	00	1	0	F	0	00110011
			2&nFAW+2	D	1	0	0	0	0	0	00	0	0	F	0	-
				Repeat above D Command until 2* nFAW + nRRD - 1												
		11	2*nFAW+nRRD	ACT	0	0	1	1	0	1	00	0	0	0	0	-
			2*nFAW+nRRD+1	RDA	0	1	0	1	0	1	00	1	0	0	0	00000000
			2&nFAW+nRRD+2	D	1	0	0	0	0	1	00	0	0	0	0	-
				Repeat above D Command until 2* nFAW + 2* nRRD - 1												
		12	2*nFAW+2*nRRD	repeat Sub-Loop 10, but BA[2:0] = 2												
		13	2*nFAW+3*nRRD	repeat Sub-Loop 11, but BA[2:0] = 3												
		14	2*nFAW+4*nRRD	D	1	0	0	0	0	3	00	0	0	0	0	-
				Assert and repeat above D Command until 3* nFAW - 1, if necessary												
		15	3*nFAW	repeat Sub-Loop 10, but BA[2:0] = 4												
		16	3*nFAW+nRRD	repeat Sub-Loop 11, but BA[2:0] = 5												
		17	3*nFAW+2*nRRD	repeat Sub-Loop 10, but BA[2:0] = 6												
		18	3*nFAW+3*nRRD	repeat Sub-Loop 11, but BA[2:0] = 7												
		19	3*nFAW+4*nRRD	D	1	0	0	0	0	7	00	0	0	0	0	-
				Assert and repeat above D Command until 4* nFAW - 1, if necessary												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are used according to RD Commands, otherwise MID-LEVEL.

b) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID-LEVEL.

IDD Specifications

IDD values are for full operating range of voltage and temperature unless otherwise noted.

IDD Specifications

Speed Grade Bin Symbol		DDR3 - 1600 11-11-11 Max.	DDR3 - 1866 13-13-13 Max.	Unit	Notes
I_{DD0}		32	32	mA	x8
		38	39	mA	x16
I_{DD01}		36	36	mA	x8
		50	50	mA	x16
I_{DD2P0}		11	11	mA	x8/16
I_{DD2P1}		11	11	mA	x8
		11	11	mA	x16
I_{DD2N}		14	16	mA	x8/16
I_{DD2NT}		19	21	mA	x8
		19	21	mA	x16
I_{DD2Q}		16	16	mA	x8
		16	16	mA	x16
I_{DD3P}		21	22	mA	x8
		24	26	mA	x16
I_{DD3N}		27	28	mA	x8
		32	35	mA	x16
I_{DD4R}		82	92	mA	x8
		125	135	mA	x16
I_{DD4w}		82	92	mA	x8
		125	135	mA	x16
I_{DD5B}		147	147	mA	x8
		155	156	mA	x16
I_{DD6}	Normal	10	10	mA	x8/16
		6	6	mA	x8
	Low power	6	6	mA	x16
		12	12	mA	x8/16
I_{DD6ET}		120	135	mA	x8
I_{DD7}		194	198	mA	x16

Notes:

1. Applicable for MR2 settings A6=0 and A7=0. Temperature range for IDD6 is 0 - 85°C.
2. Applicable for MR2 settings A6=0 and A7=1. Temperature range for IDD6ET is 0 - 95°C.

Input/Output Capacitance

Parameter	Symbol	DDR3-1600		DDR3-1866		Units	Notes
		Min	Max	Min	Max		
Input/output capacitance (DQ,DM,DQS,DQS,TDQS,TDQS)	C_{IO}	1.5	2.3	1.4	2.2	pF	1,2,3
Input capacitance, CK and CK	C_{CK}	0.8	1.4	0.8	1.3	pF	2,3
Input capacitance delta DQS and DQS	C_{DCK}	0	0.15	0	0.15	pF	2,3,4
Input capacitance delta,DQS and DQS	C_{DDQS}	0	0.15	0	0.15	pF	2,3,5
Input capacitance(All other input-only pins)	CI	0.75	1.3	0.75	1.2	pF	2,3,6
Input capacitance delta(All CTRL input-only pins)	C_{DI_CTRL}	-0.4	0.2	-0.4	0.2	pF	2,3,7,8
Input capacitance delta(All ADD/CMD input-only pins)	$C_{DI\_ADD\_CMD}$	-0.4	0.4	-0.4	0.4	pF	2,3,9,10
Input/output capacitance delta(DQ,DM,DQS,DQS)	C_{DIO}	-0.5	0.3	-0.5	0.3	pF	2,3,11
Input/output capacitance of ZQ pin	C_{ZQ}	-	3	-	3	pF	2,3,12

NOTES

1. Although the DM, TDQS and $\overline{TDQS}$ pins have different functions, the loading matches DQ and DQS.
2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147("PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER(VNA)") with VDD, VDDQ, VSS,VSSQ applied and all other pins floating (except the pin under test, CKE, $\overline{RESET}$ and ODT as necessary). VDD=VDDQ=1.5V, VBIAS=VDD/2 and on-die termination off.
3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
4. Absolute value of C_{CK}-$C_{\overline{CK}}$.
5. Absolute value of C_{IO}(DQS)-C_{IO}(DQS).
6. CI applies to ODT, $\overline{CS}$, CKE, A0-A15, BA0-BA2, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$.
7. CDI_CTR applies to ODT, CS and CKE.
8. C_{DI_CTRL}=C_I(CNTL) - 0.5 * C_I(CLK) + C_I($\overline{CLK}$))
9. $C_{DI\_ADD\_CMD}$ applies to A0-A15, BA0-BA2, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
10. CDI_ADD_CMD=C_I(ADD_CMD) - 0.5*(C_I(CLK)+C_I($\overline{CLK}$))
11. C_{DIO}=C_{IO}(DQ) - 0.5*(C_{IO}(DQS)+C_{IO}($\overline{DQS}$))
12. Maximum external load capacitance an ZQ pin: 5 pF.

Standard Speed Bins

DDR3 SDRAM Standard Speed Bins include tCK, tRCD, tRP, tRAS and tRC for each corresponding bin.

DDR3-1600 Speed Bins

For specific Notes See "Speed Bin table Notes" on page 29.

Speed Bin			DDR3-1600K		Unit	Note
CL - nRCD - nRP			11-11-11			
Parameter		Symbol	min	max		
Internal read command to first data		t_{AA}	13.75 (13.125)[11]	20	ns	
ACT to internal read or write delay time		t_{RCD}	13.75 (13.125)[11]	—	ns	
PRE command period		t_{RP}	13.75 (13.125)[11]	—	ns	
ACT to ACT or REF command period		t_{RC}	48.75 (48.125)[11]	—	ns	
ACT to PRE command period		t_{RAS}	35	9 * tREFI	ns	
CL = 5	CWL = 5	$t_{CK(AVG)}$	3.0	3.3	ns	1, 2, 3, 4, 8, 12, 13
	CWL = 6, 7	$t_{CK(AVG)}$	Reserved		ns	4
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1, 2, 3, 8
	CWL = 6	$t_{CK(AVG)}$	Reserved		ns	1, 2, 3, 4, 8
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	4
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5 (Optional)[5]	ns	1, 2, 3, 4, 8
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1, 2, 3, 4, 8
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	4
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1, 2, 3, 8
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1, 2, 3, 4, 8
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	1, 2, 3, 4
CL = 9	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875 (Optional)[5]	ns	1, 2, 3, 4, 8
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	1, 2, 3, 4
CL = 10	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	ns	1, 2, 3, 8
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	1, 2, 3, 4
CL = 11	CWL = 5, 6,7	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 8	$t_{CK(AVG)}$	1.25	<1.5	ns	1, 2, 3
Supported CL Settings			5, 6, (7), 8, (9), 10, 11		n_{CK}	
Supported CWL Settings			5, 6, 7, 8		n_{CK}	

DDR3-1866 Speed Bins

For specific Notes See "Speed Bin Table Notes" on page 29.

Speed Bin			DDR3-1866M		Unit	Note
CL - nRCD - nRP			13-13-13			
Parameter		Symbol	min	max		
Internal read command to first data		t_{AA}	13.91 (13.125)[13]	20	ns	
ACT to internal read or write delay time		t_{RCD}	13.91 (13.125)[13]	—	ns	
PRE command period		t_{RP}	13.91 (13.125)[13]	—	ns	
ACT to PRE command period		t_{RAS}	34	9 * tREFI	ns	
ACT to ACT or PRE command period		t_{RC}	47.91 (47.125)[13]	-	ns	
CL = 5	CWL = 5	$t_{CK(AVG)}$	3.0	3.3	ns	1, 2, 3, 4, 9
	CWL = 6,7,8,9	$t_{CK(AVG)}$	Reserved		ns	4
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1, 2, 3, 9
	CWL = 6	$t_{CK(AVG)}$	Reserved		ns	1, 2, 3, 4, 9
	CWL = 7,8,9	$t_{CK(AVG)}$	Reserved		ns	4
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1, 2, 3, 4, 9
	CWL = 7,8,9	$t_{CK(AVG)}$	Reserved		ns	4
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1, 2, 3, 9
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1, 2, 3, 4, 9
	CWL = 8,9	$t_{CK(AVG)}$	Reserved		ns	4
CL = 9	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	ns	1, 2, 3, 4, 9
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	1, 2, 3, 4, 9
	CWL = 9	$t_{CK(AVG)}$	Reserved		ns	4
CL = 10	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	ns	1, 2, 3, 9
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	1, 2, 3, 4, 9
CL = 11	CWL = 5,6,7	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 8	$t_{CK(AVG)}$	1.25	<1.5	ns	1, 2, 3, 4, 9
	CWL = 9	$t_{CK(AVG)}$	Reserved		ns	1, 2, 3, 4
CL = 12	CWL = 5,6,7,8	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 9	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4
CL = 13	CWL = 5,6,7,8	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 9	$t_{CK(AVG)}$	1.07	<1.25	ns	1, 2, 3
Supported CL Settings			5, 6, 7, 8, 9, 10, 11, 13		n_{CK}	
Supported CWL Settings			5, 6, 7, 8, 9		n_{CK}	

Speed Bin Table Notes

Absolute Specification (T_{OPER}; V_{DDQ} = V_{DD} = 1.5V +/- 0.075 V);

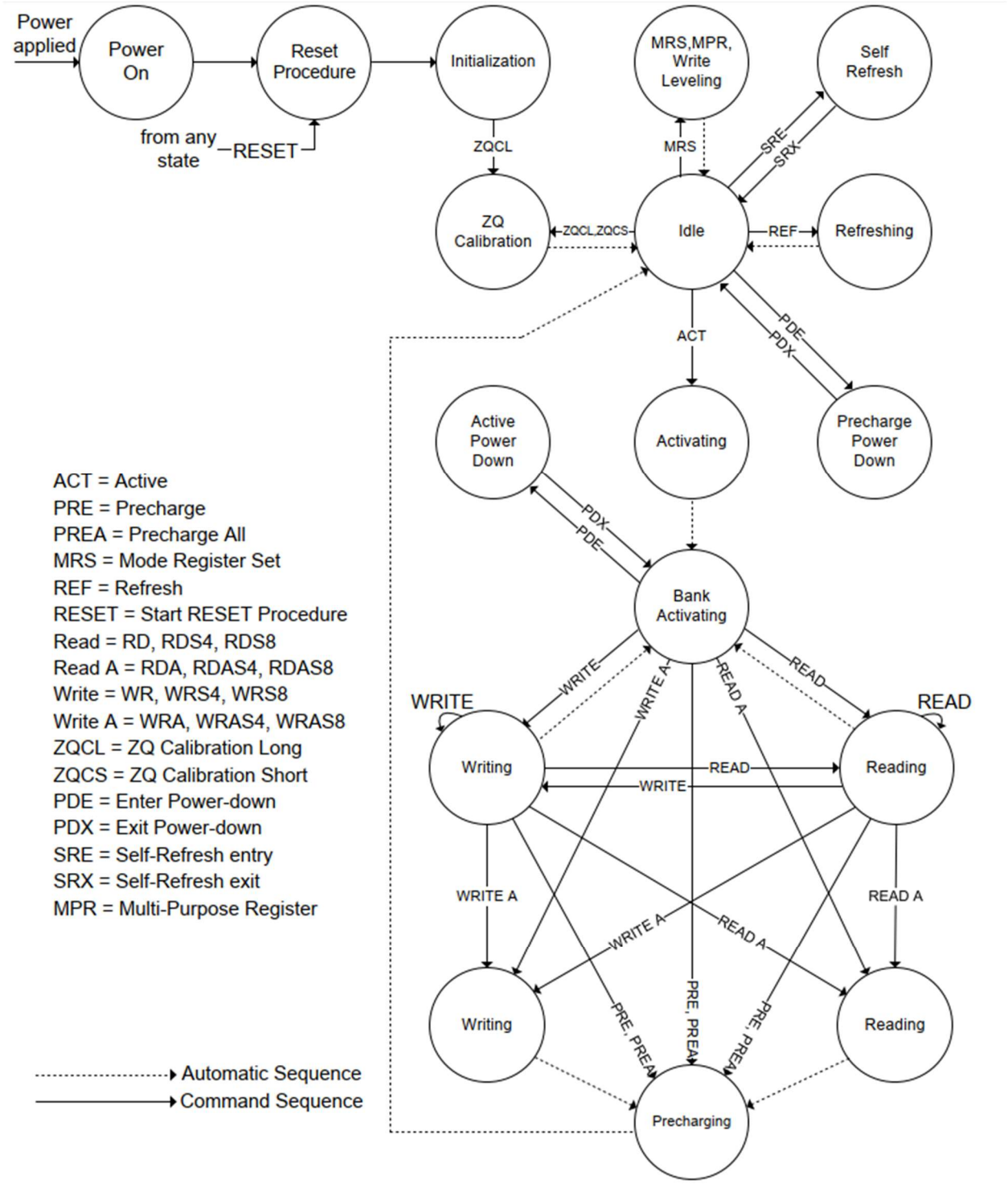
1. The CL setting and CWL setting result in tCK(AVG).MIN and tCK(AVG).MAX requirements. When making a selection of tCK(AVG), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(AVG).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(AVG) value (3.0, 2.5, 1.875, 1.5, or 1.25 ns) when calculating CL [nCK] = tAA [ns] / tCK(AVG) [ns], rounding up to the next 'Supported CL', where tCK(AVG) = 3.0 ns should only be used for CL = 5 calculation.
3. tCK(AVG).MAX limits: Calculate tCK(AVG) = tAA.MAX / CL SELECTED and round the resulting tCK(AVG) down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875 ns or 1.25 ns). This result is tCK(AVG).MAX corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to XINCUN DIMM data sheet and/or the DIMM SPD information if and how this setting is supported.
6. Any DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
9. Any DDR3-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
10. Any DDR3-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
11. XINCUN DDR3 SDRAM devices supporting optional down binning to CL=7 and CL=9, and tAA/tRCD/tRP must be 13.125 ns or lower. SPD settings must be programmed to match. For example, DDR3-1333H devices supporting down binning to DDR3-1066F should program 13.125 ns in SPD bytes for tAAmin (Byte 16), tRCDmin (Byte 18), and tRPmin (Byte 20). DDR3-1600K devices supporting down binning to DDR3-1333H or DDR3-1600F should program 13.125 ns in SPD bytes for tAAmin (Byte 16), tRCDmin (Byte 18), and tRPmin (Byte 20). Once tRP (Byte 20) is programmed to 13.125ns, tRCmin (Byte 21,23) also should be programmed accordingly. For example, 49.125ns (tRASmin + tRPmin = 36 ns + 13.125 ns) for DDR3-1333H and 48.125ns (tRASmin + tRPmin = 35 ns + 13.125 ns) for DDR3-1600K.
12. DDR3 800 AC timing apply if DRAM operates at lower than 800 MT/s data rate.

13. For CL5 support, refer to DIMM SPD information. DRAM is required to support CL5. CL5 is not mandatory in SPD coding.
14. XINCUNDDR3 SDRAM devices supporting optional down binning to CL=11, CL=9 and CL=7, tAA/ tRCD/tRPmin must be 13.125ns. SPD setting must be programed to match. For example, DDR3-1866M devices supporting down binning to DDR3-1600K or DDR3-1333H or 1066F should program 13.125ns in SPD bytes for tAAmin(byte 16), tRCDmin(byte 18) and tRPmin(byte 20) is programmed to 13.125ns, tRCmin(byte 21,23) also should be programmed accordingly. For example, 47.125ns (tRASmin + tRPmin = 34ns +13.125ns)

4.5 State Diagram

This simplified State Diagram is intended to provide an overview of the possible state transitions and the commands to control them. Situations involving more than one bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.

Simplified State Diagram



4.6 Operation Mode Truth Table

The following tables provide a quick reference of available DDR3 SDRAM commands, including CKE powerdown modes and bank-to-bank commands.

Table 11-1 Truth Table

Command	State	CKEn-1[3]	CKEn	DM	BA0-2	A10/AP	A0-9, 11, 13	A12/BC#	CS#	RAS#	CAS#	WE#
BankActivate	Idle(4)	H	H	X	V	Row address			L	L	H	H
Single Bank Precharge	Any	H	H	X	V	L	V	V	L	L	H	L
All Banks Precharge	Any	H	H	X	V	H	V	V	L	L	H	L
Write (Fixed BL8 or BC4)	Active(4)	H	H	X	V	L	V	V	L	H	L	L
Write (BC4, on the fly)	Active(4)	H	H	X	V	L	V	L	L	H	L	L
Write (BL8, on the fly)	Active(4)	H	H	X	V	L	V	H	L	H	L	L
Write with Autoprecharge (Fixed BL8 or BC4)	Active(4)	H	H	X	V	H	V	V	L	H	L	L
Write with Autoprecharge (BC4, on the fly)	Active(4)	H	H	X	V	H	V	L	L	H	L	L
Write with Autoprecharge (BL8, on the fly)	Active(4)	H	H	X	V	H	V	H	L	H	L	L
Read (Fixed BL8 or BC4)	Active(4)	H	H	X	V	L	V	V	L	H	L	H
Read (BC4, on the fly)	Active(4)	H	H	X	V	L	V	L	L	H	L	H
Read (BL8, on the fly)	Active(4)	H	H	X	V	L	V	H	L	H	L	H
Read with Autoprecharge (Fixed BL8 or BC4)	Active(4)	H	H	X	V	H	V	V	L	H	L	H
Read with Autoprecharge (Fixed BC4 or BC4)	Active(4)	H	H	X	V	H	V	L	L	H	L	H
Read with Autoprecharge (BL8, on the fly)	Active(4)	H	H	X	V	H	V	H	L	H	L	H
(Extended) Mode Register Set	Idle	H	H	X	V	OP code			L	L	L	L
No-Operation	Any	H	H	X	V	V	V	V	L	H	H	H
Device Deselect	Any	H	H	X	X	X	X	X	H	X	X	X
Refresh	Idle	H	H	X	V	V	V	V	L	L	L	H
SelfRefresh Entry	Idle	H	L	X	V	V	V	V	L	L	L	H
SelfRefresh Exit	Idle	L	H	X	X	X	X	X	H	X	X	X
					V	V	V	V	L	H	H	H
Power Down Mode Entry	Idle	H	L	X	X	X	X	X	H	X	X	X
					V	V	V	V	L	H	H	H

Table 11-1 Truth Table (continue)

Command	State	CKEn-1(3)	CKEn	DM	BA0-2	A10/AP	A0-9, 11, 13	A12/BC#	CS#	RAS#	CAS#	WE#
Power Down Mode Exit	Any	L	H	X	X	X	X	X	H	X	X	X
					V	V	V	V	L	H	H	H
Data Input Mask Disable	Active	H	X	L	X	X	X	X	X	X	X	X
Data Input Mask Enable(5)	Active	H	X	H	X	X	X	X	X	X	X	X
ZQ Calibration Long	Idle	H	H	X	X	H	X	X	L	H	H	L
ZQ Calibration Short	Idle	H	H	X	X	L	X	X	L	H	H	L

Notes:

1. V=Valid data, X=Don't Care, L=Low level, H=High level
2. CKEn signal is input level when commands are provided.
3. CKEn-1 signal is input level one clock cycle before the commands are provided.
4. These are states of bank designated by BA signal.
5. LDM and UDM can be enabled respectively.

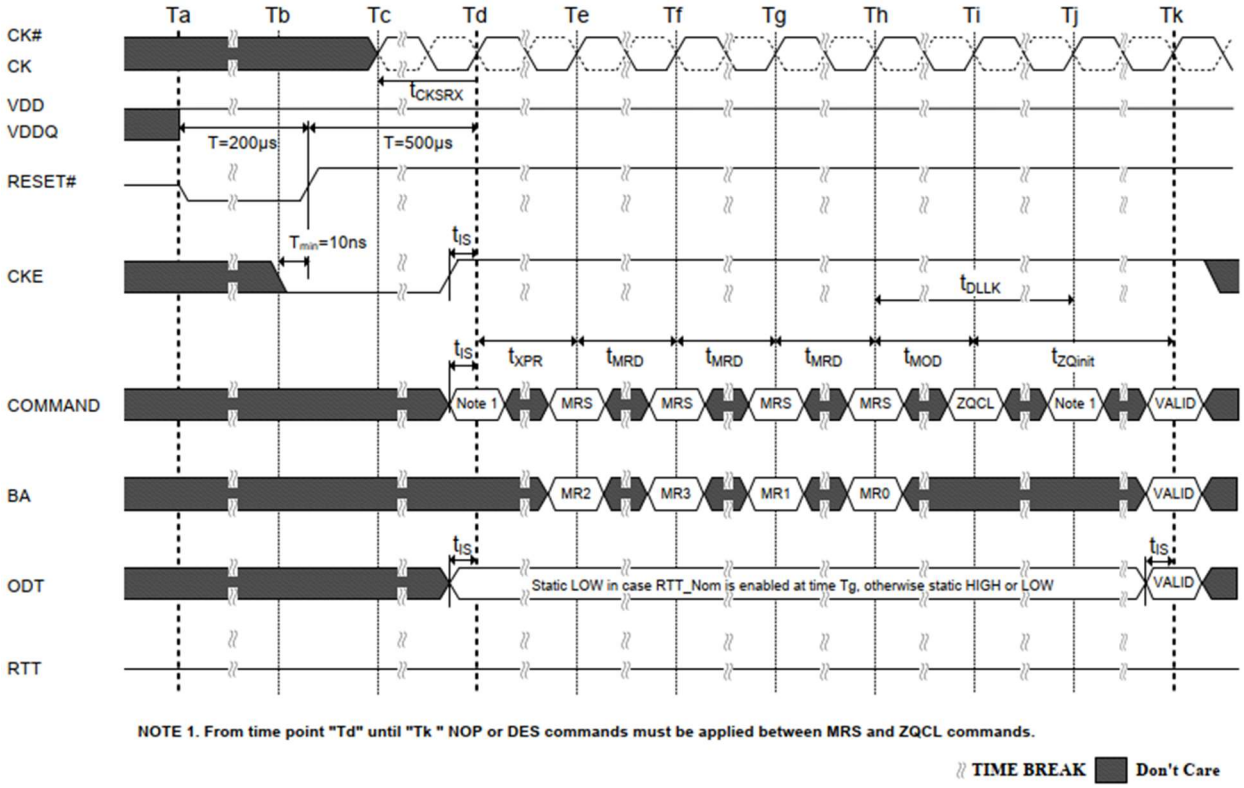
Functional Description

The DDR3 SDRAM is a high-speed dynamic random access memory internally configured as an eight-bank DRAM. The DDR3 SDRAM uses an 8n prefetch architecture to achieve high speed operation. The 8n Prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR3 SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and two corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write operation to the DDR3 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a ‘chopped’ burst of four in a programmed sequence. Operation begins with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be activated (BA0-BA2 select the bank; A0-A13 select the row). The address bit registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode ‘on the fly’ (via A12) if enabled in the mode register.

Prior to normal operation, the DDR3 SDRAM must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions and device operation.

Figure 4-1 Reset and Initialization Sequence at Power-on Ramping



NOTE 1. From time point "Td" until "Tk " NOP or DES commands must be applied between MRS and ZQCL commands.

TIME BREAK Don't Care

Power-up and Initialization

The Following sequence is required for POWER UP and Initialization

1. Apply power (RESET# is recommended to be maintained below 0.2 x VDD, all other inputs may be undefined). RESET# needs to be maintained for minimum 200us with stable power. CKE is pulled “Low” anytime before RESET# being de-asserted (min. time 10ns). The power voltage ramp time between 300mV to VDDmin must be no greater than 200ms; and during the ramp, VDD>VDDQ and (VDD-VDDQ) <0.3 Volts.
   - VDD and VDDQ are driven from a single power converter output, AND
   - The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side. In addition, VTT is limited to 0.95V max once power ramp is finished, AND
   - Vref tracks VDDQ/2.

   OR
   - Apply VDD without any slope reversal before or at the same time as VDDQ.
   - Apply VDDQ without any slope reversal before or at the same time as VTT &Vref.
   - The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.
2. After RESET# is de-asserted, wait for another 500us until CKE become active. During this time, the DRAM will start internal state initialization; this will be done independently of external clocks.
3. Clock (CK, CK#) need to be started and stabilized for at least 10ns or 5tCK (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding set up time to clock (tIS) must be meeting. Also a NOP or Deselect command must be registered (with tIS set up time to clock) before CKE goes active. Once the CKE registered “High” after Reset, CKE needs to be continuously registered “High” until the initialization sequence is finished, including expiration of tDLLK and tZQinit.
4. The DDR3 DRAM will keep its on-die termination in high impedance state as long as RESET# is asserted. Further, the DRAM keeps its on-die termination in high impedance state after RESET# deassertion until CKE is registered HIGH. The ODT input signal may be in undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT_NOM is to be enabled in MR1, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of tDLLK and tZQinit.
5. After CKE being registered high, wait minimum of Reset CKE Exit time, tXPR, before issuing the first MRS command to load mode register.(tXPR=max (tXS, 5tCK))

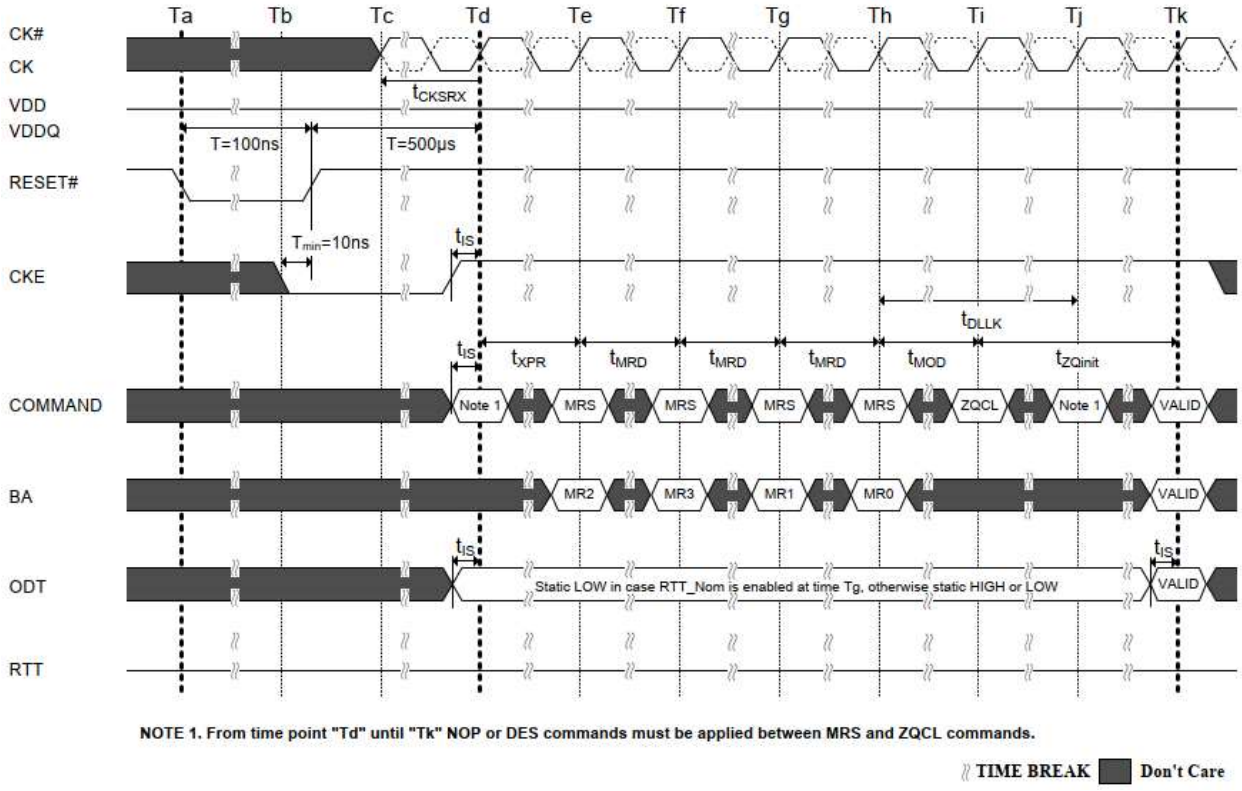
6. Issue MRS command to load MR2 with all application settings. (To issue MRS command for MR2, provide “Low” to BA0 and BA2, “High” to BA1)
7. Issue MRS Command to load MR3 with all application settings. (To issue MRS command for MR3, provide “Low” to BA2, “High” to BA0 and BA1)
8. Issue MRS Command to load MR1 with all application settings and DLL enabled. (To issue “DLL Enable” command, provide “Low” to A0, “High” to BA0 and “Low” to BA1 and BA2)
9. Issue MRS Command to load MR0 with all application settings and “DLL reset”. (To issue DLL reset command provide “High” to A8 and “Low” to BA0-BA2)
10. Issue ZQCL command to starting ZQ calibration.
11. Wait for both tDLLK and tZQinit completed.
12. The DDR3 SDRAM is now ready for normal operation.

Reset Procedure at Stable Power

The following sequence is required for RESET at no power interruption initialization.

1. Asserted RESET below 0.2*VDD anytime when reset is needed (all other inputs may be undefined). RESET needs to be maintained for minimum 100ns. CKE is pulled “Low” before RESET being de-asserted (min. time 10ns).
2. Follow Power-up Initialization Sequence step 2 to 11.
3. The Reset sequence is now completed. DDR3 SDRAM is ready for normal operation.

Figure 4-2 Reset Procedure at Power Stable Condition



NOTE 1. From time point "Td" until "Tk" NOP or DES commands must be applied between MRS and ZQCL commands.

TIME BREAK Don't Care

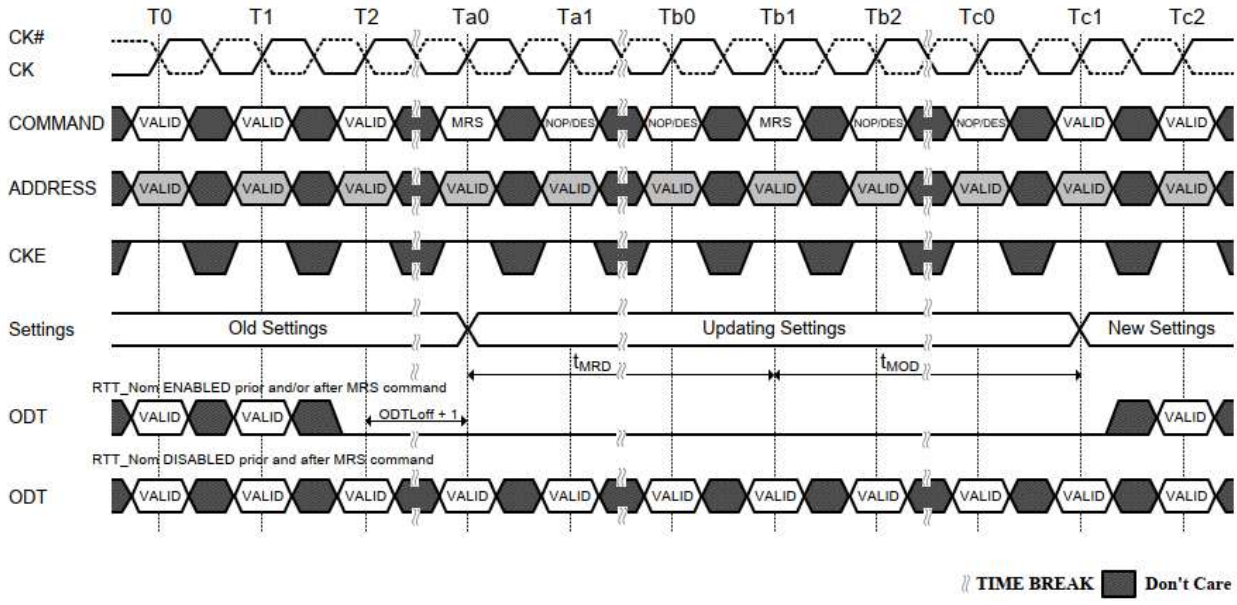
4.7 Register Definition

Programming the Mode Registers

For application flexibility, various functions, features, and modes are programmable in four Mode Registers, provided by the DDR3 SDRAM, as user defined variables and they must be programmed via a Mode Register Set (MRS) command. As the default values of the Mode Registers are not defined, contents of Mode Registers must be fully initialized and/or re-initialized, i.e., written, after power up and/or reset for proper operation. Also the contents of the Mode Registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS command and DLL Reset do not affect array contents, which mean these commands can be executed any time after power-up without affecting the array contents.

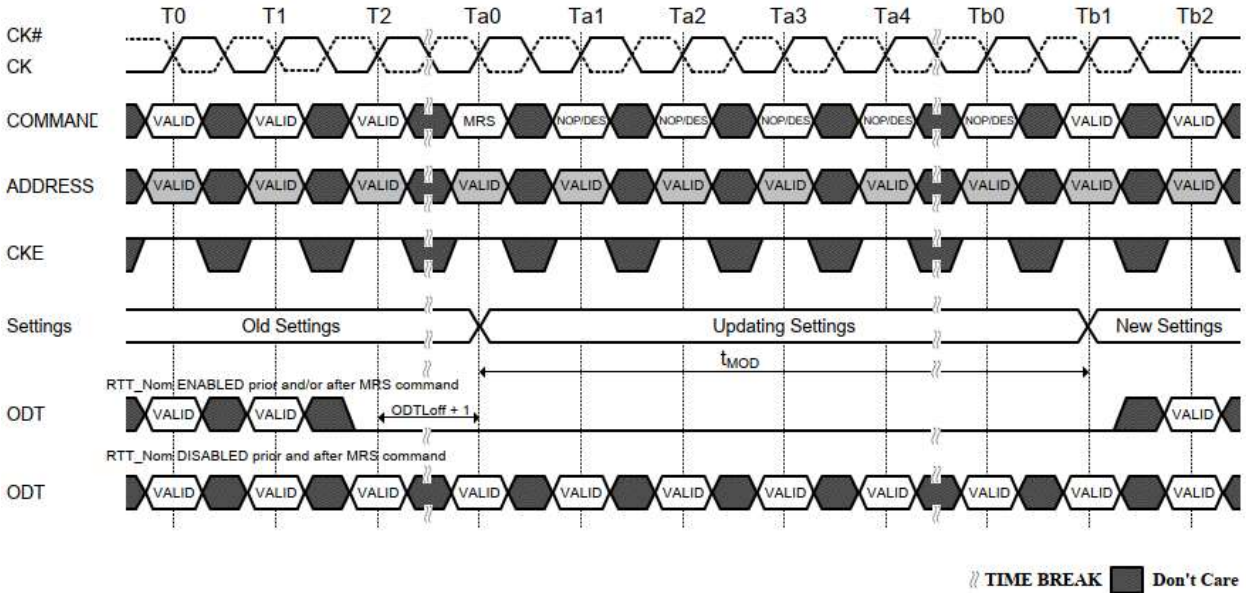
The mode register set command cycle time, tMRD is required to complete the write operation to the mode register and is the minimum time required between two MRS commands shown in Figure of tMRD timing.

Figure 4-3 tMRD timing



The MRS command to Non-MRS command delay, tMOD, is require for the DRAM to update the features except DLL reset, and is the minimum time required from an MRS command to a non-MRS command excluding NOP and DES shown in Figure of tMOD timing.

Figure 4-4 tMOD timing



The mode register contents can be changed using the same command and timing requirements during normal operation as long as the DRAM is in idle state, i.e., all banks are in the precharged state with tRP satisfied, all data bursts are completed and CKE is high prior to writing into the mode register. The mode registers are divided into various fields depending on the functionality and/or modes.

Mode Register MR0

The mode-register MR0 stores data for controlling various operating modes of DDR3 SDRAM. It controls burst length, read burst type, CAS latency, test mode, DLL reset, WR, and DLL control for precharge Power-Down, which include various vendor specific options to make DDR3 DRAM useful for various applications. The mode register is written by asserting low on CS#, RAS#, CAS#, WE#, BA0, BA1, and BA2, while controlling the states of address pins according to the following figure.

Table 4-2 Mode Register Bitmap

BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0*1	0	0	0*1	PPD	WR			DLL	TM	CAS Latency			RBT	CL	BL		Address Field / Mode Register (0)

BA1	BA0	MRS mode
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

A7	Mode
0	Normal
1	Test

A3	Read Burst Type
0	Nibble Sequential
1	Interleave

A1	A0	BL
0	0	8 (Fixed)
0	1	BC4 or 8 (on the fly)
1	0	BC4 (Fixed)
1	1	Reserved

A11	A10	A9	WR (cycles) *2
0	0	0	16
0	0	1	5
0	1	0	6
0	1	1	7
1	0	0	8
1	0	1	10
1	1	0	12
1	1	1	14

A6	A5	A4	A2	CAS Latency
0	0	0	0	Reserved
0	0	1	0	5
0	1	0	0	6
0	1	1	0	7
1	0	0	0	8
1	0	1	0	9
1	1	0	0	10
1	1	1	0	11
0	0	0	1	12
0	0	1	1	13
0	1	0	1	Reserved
0	1	1	1	Reserved
1	0	0	1	Reserved
1	0	1	1	Reserved
1	1	0	1	Reserved
1	1	1	1	Reserved

A12	DLL Control for Precharge PD
0	Slow exit (DLL off)
1	Fast exit (DLL on)

A8	DLL Reset
0	No
1	Yes

Notes:

1. Reserved for future use and must be set to 0 when programming the MR.
2. WR (write recovery for autoprecharge) min in clock cycles is calculated by dividing tWR (ns) by tCK (ns) and rounding up to the next integer WRmin [cycles] =Roundup (tWR / tCK). The value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with tRP to determine tDAL.

CAS Latency

The CAS Latency is defined by MR0 (bit A2, A4~A6) as shown in the MR0 Definition figure. CAS Latency is the delay, in clock cycles, between the internal Read command and the availability of the first bit of output data. DDR3 SDRAM does not support any half clock latencies. The overall Read Latency (RL) is defined as Additive Latency (AL) + CAS Latency (CL); RL = AL + CL.

Test Mode

The normal operating mode is selected by MR0 (bit7=0) and all other bits set to the desired values shown in the MR0 definition figure. Programming bit A7 to a '1' places the DDR3 SDRAM into a test mode that is only used by the DRAM manufacturer and should not be used. No operations or functionality is guaranteed if A7=1.

Burst Length, Type, and Order

Accesses within a given burst may be programmed to sequential or interleaved order. The burst type is selected via bit A3 as shown in the MR0 Definition as above figure. The ordering of access within a burst is determined by the burst length, burst type, and the starting column address. The burst length is defined by bits A0-A1. Burst lengths options include fix BC4, fixed BL8, and on the fly which allow BC4 or BL8 to be selected coincident with the registration of a Read or Write command via A12/BC#.

Table 4-3 Burst Type and Burst Order

Burst Length	Read Write	Starting Column Address			Sequential A3=0	Interleave A3=1	Note
		A2	A1	A0			
4 Chop	Read	0	0	0	0, 1, 2, 3, T, T, T, T	0, 1, 2, 3, T, T, T, T	1, 2, 3
		0	0	1	1, 2, 3, 0, T, T, T, T	1, 0, 3, 2, T, T, T, T	
		0	1	0	2, 3, 0, 1, T, T, T, T	2, 3, 0, 1, T, T, T, T	
		0	1	1	3, 0, 1, 2, T, T, T, T	3, 2, 1, 0, T, T, T, T	
		1	0	0	4, 5, 6, 7, T, T, T, T	4, 5, 6, 7, T, T, T, T	
		1	0	1	5, 6, 7, 4, T, T, T, T	5, 4, 7, 6, T, T, T, T	
		1	1	0	6, 7, 4, 5, T, T, T, T	6, 7, 4, 5, T, T, T, T	
		1	1	1	7, 4, 5, 6, T, T, T, T	7, 6, 5, 4, T, T, T, T	
	Write	0	V	V	0, 1, 2, 3, X, X, X, X	0, 1, 2, 3, X, X, X, X	1, 2, 4, 5
		1	V	V	4, 5, 6, 7, X, X, X, X	4, 5, 6, 7, X, X, X, X	
8	Read	0	0	0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	2
		0	0	1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6	
		0	1	0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5	
		0	1	1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4	
		1	0	0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3	
		1	0	1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2	
		1	1	0	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1	
		1	1	1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0	
	Write	V	V	V	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	2,4

Notes:

1. In case of burst length being fixed to 4 by MR0 setting, the internal write operation starts two clock cycles earlier than for the BL8 mode. This means that the starting point for tWR and tWTR will be pulled in by two clocks. In case of burst length being

selected on-the-fly via A12/BC#, the internal write operation starts at the same point in time like a burst of 8 write operation. This means that during on-the-fly control, the starting point for tWR and tWTR will not be pulled in by two clocks.

2. 0~7 bit number is value of CA[2:0] that causes this bit to be the first read during a burst.
3. T: Output driver for data and strobes are in high impedance.
4. V: a valid logic level (0 or 1), but respective buffer input ignores level on input pins.
5. X: Don't Care.

DLL Reset

The DLL Reset bit is self-clearing, meaning it returns back to the value of '0' after the DLL reset function has been issued. Once the DLL is enabled, a subsequent DLL Reset should be applied. Anytime the DLL reset function is used, tDLLK must be met before any functions that require the DLL can be used (i.e. Read commands or ODT synchronous operations.)

Write Recovery

The programmed WR value MR0 (bits A9, A10, and A11) is used for the auto precharge feature along with tRP to determine tDAL. WR (write recovery for auto-precharge) min in clock cycles is calculated by dividing tWR (ns) by tCK (ns) and rounding up to the next integer: WR min [cycles] = Roundup (tWR [ns]/tCK [ns]). The WR must be programmed to be equal or larger than tWR (min).

Precharge PD DLL

MR0 (bit A12) is used to select the DLL usage during precharge power-down mode. When MR0 (A12=0), or 'slow-exit', the DLL is frozen after entering precharge power-down (for potential power savings) and upon exit requires tXPDLL to be met prior to the next valid command. When MR0 (A12=1), or 'fast-exit', the DLL is maintained after entering precharge power-down and upon exiting power-down requires tXP to be met prior to the next valid command.

Mode Register MR1

The Mode Register MR1 stores the data for enabling or disabling the DLL, output strength, Rtt_Nom impedance, additive latency, WRITE leveling enable and Qoff. The Mode Register 1 is written by asserting low on CS#, RAS#, CAS#, WE#, high on BA0 and low on BA1 and BA2, while controlling the states of address pins according to the following figure.

Table 4-4 Extended Mode Register EMR (1) Bitmap

BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Field
0*1	0	1	0*1	Qoff	0*1	0*1	Rtt	0*1	Level	Rtt	D.I.C	AL		Rtt	D.I.C	DLL	Mode Register (1)

BA1	BA0	MRS mode
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

A4	A3	Additive Latency
0	0	0 (AL disabled)
0	1	CL – 1
1	0	CL – 2
1	1	Reserved

A0	DLL Enable
0	Enable
1	Disable

A12	Qoff *2
0	Output buffer enabled
1	Output buffer disabled

A9	A6	A2	Rtt_Nom *3
0	0	0	Rtt_Nom disabled
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/12 *4
1	0	1	RZQ/8 *4
1	1	0	Reserved
1	1	1	Reserved

Note: RZQ = 240 Ω

A7	Write leveling enable
0	Disabled
1	Enabled

Note: RZQ = 240 Ω

A5	A1	Output Driver Impedance Control
0	0	RZQ/6
0	1	RZQ/7
1	0	Reserved
1	1	Reserved

Notes:

1. Reserved for future use and must be set to 0 when programming the MR.
2. Outputs disabled - DQs, DQSs, $\overline{\text{DQS}}$s.
3. In Write leveling Mode (MR1 [bit7] = 1) with MR1 [bit12] =1, all RTT_Nom settings are allowed; in Write Leveling Mode (MR1 [bit7] = 1) with MR1 [bit12]=0, only RTT_Nom settings of RZQ/2, RZQ/4 and RZQ/6 are allowed.
4. If RTT_Nom is used during Writes, only the values RZQ/2, RZQ/4 and RZQ/6 are allowed.

DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. During normal operation (DLL-on) with MR1 (A0=0), the DLL is automatically disabled when entering Self-Refresh operation and is automatically reenable upon exit of SelfRefresh operation. Any time the DLL is enabled and subsequently reset, tDLLK clock cycles must occur before a Read or synchronous ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tDQSCK, tAON, or tAOF parameters. During tDLLK, CKE must continuously be registered high. DDR3 SDRAM does not require DLL for any Write operation, expect when RTT_WR is enabled and the DLL is required for proper ODT operation. For more detailed information on DLL Disable operation are described in DLL-off Mode. The direct ODT feature is not supported during DLL-off mode. The on-die termination resistors must be disabled by continuously registering the ODT pin low and/or by programming the RTT_Nom bits MR1{A9,A6,A2} to {0,0,0} via a mode register set command during DLL-off mode.

The dynamic ODT feature is not supported at DLL-off mode. User must use MRS command to set Rtt_WR, MR2 {A10, A9} = {0, 0}, to disable Dynamic ODT externally

Output Driver Impedance Control

The output driver impedance of the DDR3 SDRAM device is selected by MR1 (bit A1 and A5) as shown in MR1 definition figure.

ODT Rtt Values

DDR3 SDRAM is capable of providing two different termination values (Rtt_Nom and Rtt_WR). The nominal termination value Rtt_Nom is programmable in MR1. A separate value (Rtt_WR) may be programmable in MR2 to enable a unique Rtt value when ODT is enabled during writes. The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled.

Additive Latency (AL)

Additive Latency (AL) operation is supported to make command and data bus efficient for sustainable bandwidth in DDR3 SDRAM. In this operation, the DDR3 SDRAM allows a read or write command (either with or without autoprecharge) to be issued immediately after the active command. The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of the AL and CAS Latency (CL) register settings. Write Latency (WL) is controlled by the sum of the AL and CAS Write Latency (CWL) register settings. A summary of the AL register options are shown in MR.

Write leveling

For better signal integrity, DDR3 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has benefits from reducing number of stubs and their length but in other aspect, causes flight time skew between clock and strobe at every DRAM on DIMM. It makes difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the controller should support ‘write leveling’in DDR3 SDRAM to compensate for skew.

Output Disable

The DDR3 SDRAM outputs maybe enable/disabled by MR1 (bit 12) as shown in MR1 definition. When this feature is enabled (A12=1) all output pins (DQs, DQS, DQS#, etc.) are disconnected from the device removing any loading of the output drivers. This feature may be useful when measuring modules power for example. For normal operation A12 should be set to ‘0’.

Mode Register MR2

The Mode Register MR2 stores the data for controlling refresh related features, Rtt_WR impedance, and CAS write latency. The Mode Register 2 is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, high on BA1 and low on BA0 and BA2, while controlling the states of address pins according to the table below.

Table 4-5 Extended Mode Register EMR (2) Bitmap

BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Field
0*1	1	0	0*1			Rtt_WR		0*1	SRT	0*1	CWL			PASR			Mode Register (2)

BA1	BA0	MRS mode
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

A10	A9	RTT_WR *2
0	0	Dynamic ODT off (Write does not affect Rtt value)
0	1	RZQ/4
1	0	RZQ/2
1	1	Reserved

A7	Self-Refresh Temperature (SRT) Range
0	Normal operating temperature range
1	Extended (optional) operating temperature range

A2	A1	A0	Partial Array Self-Refresh (Optional)
0	0	0	Full Array
0	0	1	Half Array (BA[2:0]=000,001,010,&011)
0	1	0	Quarter Array (BA[2:0]=000,&001)
0	1	1	1/8th Array (BA[2:0]=000)
1	0	0	3/4 Array (BA[2:0]=010,011,100.101,110,&111)
1	0	1	Half Array (BA[2:0]=100,101,110,&111)
1	1	0	Quarter Array (BA[2:0]=110,&111)
1	1	1	1/8th Array (BA[2:0]=111)

A5	A4	A3	CAS write Latency (CWL)
0	0	0	5 (tCK(avg)≧2.5ns)
0	0	1	6 (2.5ns＞tCK(avg)≧1.875ns)
0	1	0	7 (1.875ns＞tCK(avg)≧1.5ns)
0	1	1	8 (1.5ns＞tCK(avg)≧1.25ns)
1	0	0	9 (1.25ns＞tCK(avg)≧1.07ns)
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Notes:

1. BA2, A6, A8 and A11~ A13 are RFU and must be programmed to 0 during MRS.
2. The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled. During write leveling, Dynamic ODT is not available.

Partial Array Self-Refresh (PASR)

If PASR (Partial Array Self-Refresh) is enabled, data located in areas of the array beyond the specified address range will be lost if Self-Refresh is entered. Data integrity will be maintained if tREFI conditions are met and no SelfRefresh command is issued.

CAS Write Latency (CWL)

The CAS Write Latency is defined by MR2 (bits A3-A5) shown in MR2. CAS Write Latency is the delay, in clock cycles, between the internal Write command and the availability of the first bit of input data. DDR3 DRAM does not support any half clock latencies. The overall Write Latency (WL) is defined as Additive Latency (AL) + CAS Write Latency (CWL); WL=AL+CWL.

For more information on the supported CWL and AL settings based on the operating clock frequency, refer to "Standard Speed Bins". For detailed Write operation refer to "WRITE Operation".

Dynamic ODT (Rtt_WR)

DDR3 SDRAM introduces a new feature "Dynamic ODT". In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3 SDRAM can be changed without issuing an MRS command. MR2 Register locations A9 and A10 configure the Dynamic ODT settings.

DDR3 SDRAM introduces a new feature "Dynamic ODT". In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3 SDRAM can be changed without issuing an MRS command. MR2 Register locations A9 and A10 configure the Dynamic ODT settings. In Write leveling mode, only RTT_Nom is available. For details on Dynamic ODT operation, refer to "Dynamic ODT".

Self-Refresh Temperature (SRT)

Mode register MR2[7] is used to disable/enable the SRT function. When SRT is disabled, the self refresh mode's refresh rate is assumed to be at the normal 85°C limit (sometimes referred to as 1x refresh rate). In the disabled mode, SRT requires the user to ensure the DRAM never exceeds a TC of 85°C while in self refresh mode.

When SRT is enabled, the DRAM self refresh is changed internally from 1x to 2x, regardless of the case temperature. This enables the user to operate the DRAM beyond the standard 85°C limit up to the optional extended temperature range of 95°C while in self refresh mode. The standard self refresh current test specifies test conditions to normal case temperature (85°C) only, meaning if SRT is enabled, the standard self refresh current specifications do not apply (see Extended Temperature Usage).

Extended Temperature Usage

DDR3 SDRAM supports the optional extended case temperature (TC) range of 0°C to 95°C. The extended temperature range DRAM must be refreshed externally at 2x (double refresh) anytime the case temperature is above 85°C (and does not exceed 95°C). The external refresh requirement is accomplished by reducing the refresh period from 64ms to 32ms. Thus, SRT must be enabled when TC is above 85°C or self refresh cannot be used until TC is at or below 85°C.

Table 4-6 Self-Refresh mode summary

MR2 A[7]	Self-Refresh operation	Allowed Operating Temperature Range for Self-Refresh mode
0	Self-Refresh rate appropriate for the Normal Temperature Range	Normal (0°C ~ 85°C)
1	Self-Refresh appropriate for either the Normal or Extended Temperature Ranges.The DRAM must support Extended Temperature Range. The value of the SRT bit can effect self-refresh power consumption, please refer to the IDD table for details.	Normal and Extended (0°C ~ 95°C)

Mode Register MR3

The Mode Register MR3 controls Multi-purpose registers. The Mode Register 3 is written by asserting low on CS#, RAS#, CAS#, WE#, high on BA1 and BA0, and low on BA2 while controlling the states of address pins according to the table below.

Table 4-7 Extended Mode Register EMR (3) Bitmap

BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Field
0*1	1	1	0*1											MPR	MPR Loc		Mode Register (3)

BA1	BA0	MRS mode
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

A2	MPR
0	Normal operation *3
1	Dataflow from MPR

A1	A0	MPR location
0	0	Predefined pattern *2
0	1	RFU
1	0	RFU
1	1	RFU

Notes:

1. BA2, A3 - A13 are RFU and must be programmed to 0 during MRS.
2. The predefined pattern will be used for read synchronization.
3. When MPR control is set for normal operation (MR3 A[2] = 0) then MR3 A[1:0] will be ignored.

Table 4-8 Single-Ended AC and DC Input Levels for Command and Address

Symbol	Parameter	DDR3-1866/1600		Unit	Note
		Min.	Max.		
VIH.CA(DC90)	DC input logic high	VREF+0.09	VDD	V	1,5
VIL.CA(DC90)	DC input logic Low	VSS	VREF-0.09	V	1,6
VIH.CA(AC160)	AC input logic high	VREF+0.16	-	V	1,2
VIL.CA(AC160)	AC input logic low	-	VREF-0.16	V	1,2
VIH.CA(AC150)	AC input logic high	VREF+0.135	-	V	1,2
VIL.CA(AC150)	AC input logic low	-	VREF-0.135	V	1,2
VIH.CA(AC140)	AC input logic high	-	-	V	1,2
VIL.CA(AC140)	AC input logic Low	-	-	V	1,2
VRefCA(DC)	Reference Voltage for ADD, CMD inputs	0.49xVDD	0.51xVDD	V	3,4

Notes:

1. For input only pins except RESET#. Vref = VrefCA(DC).
2. See “Overshoot and Undershoot Specifications”.
3. The ac peak noise on VRef may not allow VRef to deviate from VRefCA(DC) by more than ±1% VDD.
4. For reference: approx. VDD/2 ±13.5 mV.
5. VIH(dc) is used as a simplified symbol for VIH.CA(DC90)
6. VIL(dc) is used as a simplified symbol for VIL.CA(DC90)
7. VIH(ac) is used as a simplified symbol for VIH.CA(AC160), VIH.CA(AC1500 is used when Vref + 0.160V is referenced, VIH. CA(AC1500) value is used VIH.CA(AC125) value is used when Vref + 0.125V is referenced.
8. VIL(ac) is used as a simplified symbol for VIL.CA(AC160), VIL.CA(AC1500), VIL.CA(AC125) and VIL.CA(AC160) value is used when Vref - 0.160V is referenced, VIL.CA(AC1500) value is used when Vref - 0.135V is referenced, VIL.CA(AC125) value is used when Vref - 0.125V is referenced.

Table 4-9 Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	DDR3-1866/1600		Unit	Note
		Min.	Max.		
VIH.DQ(DC90)	DC input logic high	VREF+0.09	VDD	V	1,5
VIL.DQ(DC90)	DC input logic Low	VSS	VREF-0.09	V	1,6
VIH.DQ(AC1500)	AC input logic high	VREF+0.135	-	V	1,2
VIL.DQ(AC1500)	AC input logic low	-	VREF-0.135	V	1,2
VIH.DQ(AC130)	AC input logic high	-	-	V	1,2
VIL.DQ(AC130)	AC input logic low	-	-	V	1,2
VRefDQ(DC)	Reference Voltage for DQ, DM inputs	0.49xVDD	0.51xVDD	V	3,4

Notes:

1. Vref = VrefDQ(DC).
2. See “Overshoot and Undershoot Specifications”
3. The ac peak noise on VRef may not allow VRef to deviate from VRefDQ(DC) by more than ±1% VDD.
4. For reference: approx. VDD/2 ±13.5 mV.
5. VIH(dc) is used as a simplified symbol for VIH.DQ(DC90)
6. VIL(dc) is used as a simplified symbol for VIL.DQ(DC90)
7. VIH(ac) is used as a simplified symbol for VIH.DQ(AC1500, VIH.DQ(AC130) and VIH.DQ(AC1500) value is used when Vref + 0.135V is referenced, VIH.DQ(AC130) value is used when Vref + 0.13V is referenced.
8. VIL(ac) is used as a simplified symbol for VIL.DQ(AC1500), VIL.DQ(AC130) and VIL.DQ(AC1500) value is used when Vref - 0.135V is referenced, VIL.DQ(AC130) value is used when Vref - 0.13V is referenced.

Table 4-10 Differential AC and DC Input Levels

Symbol	Parameter	Values		Unit	Note
		Min.	Max.		
VIHdiff	Differential input high	+ 0.18	Note 3	V	1
VILdiff	Differential input logic low	Note 3	- 0.18	V	1
VIHdiff(ac)	Differential input high ac	2 x (VIH(ac) - VREF)	Notes 3	V	2
VILdiff(ac)	Differential input low ac	Note 3	2 x (VIL(ac) - VREF)	V	2

Notes:

1. Used to define a differential signal slew-rate.
2. For CK - CK# use VIH/VIL(ac) of ADD/CMD and VREFCA; for DQSL, DQSL#, DQSU, DQSU# use VIH/VIL(ac) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined; however, the single-ended signals CK, CK#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot.

Table 4-11 Capacitance (VDD = 1.5V)

Symbol	Parameter	DDR3-1866		DDR3-1600		Unit	Note
		Min.	Max.	Min.	Max.		
CIO	Input/output capacitance, (DQ, DM, DQS, DQS#)	1.4	2.2	1.4	2.3	pF	1, 2, 3
CCK	Input capacitance, CK and CK#	0.8	1.4	0.8	1.4	pF	2, 3
CDCK	Input capacitance delta, CK and CK#	0	0.15	0	0.15	pF	2, 3, 4
CDDQS	Input/output capacitance delta, DQS and DQS#	0	0.15	0	0.15	pF	2, 3, 5
CI	Input capacitance, (CTRL, ADD, CMD input-only pins)	0.75	1.2	0.75	1.3	pF	2, 3, 6
CDI_CTRL	Input capacitance delta, (All CTRL input-only pins)	-0.4	0.2	-0.4	0.2	pF	2, 3, 7, 8
CDI_ADD_CMD	Input capacitance delta, (All ADD, CMD input-only pins)	-0.4	0.4	-0.4	0.4	pF	2, 3, 9, 10
CDIO	Input/output capacitance delta, (DQ, DM, DQS, DQS#)	-0.5	0.3	-0.5	0.3	pF	2, 3, 11
CZQ	Input/output capacitance of ZQ pin	-	3	-	3	pF	2, 3, 12

Notes:

1. Although the DM pins have different functions, the loading matches DQ and DQS.
2. This parameter is not subject to production test. It is verified by design and characterization. VDD=VDDQ=1.5V, VBIAS=VDD/2 and ondie termination off.
3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here.
4. Absolute value of CCK-C$\overline{CK}$.
5. Absolute value of CIO(DQS)-CIO($\overline{DQS}$).
6. CI applies to ODT, $\overline{CS}$, CKE, A0-A13, BA0-BA2, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$.
7. CDI_CTRL applies to ODT, $\overline{CS}$ and CKE.
8. CDI_CTRL=CI(CTRL)-0.5*(CI(CK)+CI($\overline{CK}$)).
9. CDI_ADD_CMD applies to A0-A13, BA0-BA2, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
10. CDI_ADD_CMD=CI(ADD_CMD) - 0.5*(CI(CK)+CI($\overline{CK}$)).
11. CDIO=CIO(DQ,DM) - 0.5*(CIO(DQS)+CIO($\overline{DQS}$)).
12. Maximum external load capacitance on ZQ pin: 5 pF.

Table 4-12 IDD specification parameters and test conditions (VDD = 1.5V)

Parameter & Test Condition	Symbol	DDR3-1866	DDR3-1600	Unit
		Max.		
Operating One Bank Active-Precharge Current CKE: High; External clock: On; BL: 8*1; AL: 0; $\overline{CS}$: High between ACT and PRE; Command, Address, Bank Address Inputs: partially toggling; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,...;Output Buffer and RTT: Enabled in Mode Registers*2; ODT Signal: stable at 0.	IDD0	70	65	mA
Operating One Bank Active-Read-Precharge Current CKE: High; External clock: On; BL: 8*1, 5; AL:0; $\overline{CS}$: High between ACT, RD and PRE; Command, Address, Bank Address Inputs, Data IO: partially toggling; DM:stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers*2; ODT Signal: stable at 0.	IDD1	80	75	mA
Precharge Standby Current CKE: High; External clock: On; BL: 8*1; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: partially toggling; Data IO: MID-LEVEL; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers*2; ODT Signal: stable at 0.	IDD2N	35	30	mA
Precharge Power-Down Current Slow Exit CKE: Low; External clock: On; BL: 8*1; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID-LEVEL; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers*2; ODT Signal: stable at 0; Pecharge Power Down Mode: Slow Exit.*3	IDD2P0	15	15	mA
Precharge Power-Down Current Fast Exit CKE: Low; External clock: On; BL: 8*1; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID-LEVEL; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers*2; ODT Signal: stable at 0; Pecharge Power Down Mode: Fast Exit.*3	IDD2P1	22	20	mA
Precharge Quiet Standby Current CKE: High; External clock: On; BL: 8*1; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID-LEVEL; DM: stable at 0;Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers*2; ODT Signal: stable at 0.	IDD2Q	35	30	mA
Active Standby Current CKE: High; External clock: On; BL: 8*1; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: partially toggling; Data IO: MID-LEVEL; DM:stable at 0;Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers*2; ODT Signal: stable at 0.	IDD3N	55	53	mA
Active Power-Down Current CKE: Low; External clock: On; BL: 8*1; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID-LEVEL;DM:stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers*2; ODT Signal: stable at 0	IDD3P	35	30	mA
Operating Burst Read Current CKE: High; External clock: On; BL: 8*1, 5; AL: 0; $\overline{CS}$: High between RD; Command, Address, Bank Address Inputs: partially toggling; DM: stable at 0; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,...; tput Buffer and RTT: Enabled in Mode Registers*2; ODT Signal: stable at 0.	IDD4R	155	150	mA

Table 4-15 IDD specification parameters and test conditions (VDD = 1.5V) (continue)

Parameter & Test Condition		Symbol	DDR3-1866	DDR3-1600	Unit
			Max.		
Operating Burst Write Current CKE: High; External clock: On; BL: 8*1; AL: 0; $\overline{CS}$: High between WR; Command, Address, Bank Address Inputs: partially toggling; DM: stable at 0; Bank Activity: all banks open. Output Buffer and RTT: Enabled in Mode Registers*2; ODT Signal: stable at HIGH.		IDD4W	160	150	mA
Burst Refresh Current CKE: High; External clock: On; BL: 8*1; AL: 0; $\overline{CS}$: High between tREF; Command, Address, Bank Address Inputs: partially toggling; Data IO: MID LEVEL; DM: stable at 0; Bank Activity: REF command every tRFC; Output Buffer and RTT: Enabled in Mode Registers*2; ODT Signal: stable at 0.		IDD5B	145	140	mA
Self Refresh Current: Self-Refresh Temperature Range (SRT): Normal*4; CKE: Low; External clock: Off; CK and $\overline{CK}$: LOW; BL: 8*1; AL: 0; $\overline{CS}$, Command, Address, Bank Address, Data IO: MID-LEVEL; DM:stable at 0; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers*2; ODT Signal: MID-LEVEL	TCASE: 0 - 85°C	IDD6	15	15	mA
	TCASE: 0 - 95°C	IDD6ET	20	20	mA
Operating Bank Interleave Read Current CKE: High; External clock: On; BL: 8*1, 5; AL: CL-1; $\overline{CS}$: High between ACT and RDA; Command, Address, Bank Address Inputs: partially toggling; DM:stable at 0; Output Buffer and RTT: Enabled in Mode Registers*2; ODT Signal: stable at 0.		IDD7	240	230	mA
RESET Low Current RESET: LOW; External clock: Off; CK and $\overline{CK}$: LOW; CKE: FLOATING; CS#, Command, Address, Bank Address, Data IO: FLOATING; ODT Signal: FLOATING RESET Low current reading is valid once power is stable and RESET has been LOW for at least 1ms.		IDD8	14	14	mA

Notes:

1. Burst Length: BL8 fixed by MRS: set MR0 A[1,0]=00B.
2. Output Buffer Enable: set MR1 A[12] = 0B; set MR1 A[5,1] = 01B; RTT_Nom enable: set MR1 A[9,6,2] = 011B; RTT_Wr enable: set MR2 A[10,9] = 10B.
3. Pecharge Power Down Mode: set MR0 A12=0B for Slow Exit or MR0 A12=1B for Fast Exit.
4. Self-Refresh Temperature Range (SRT): set MR2 A7=0B for normal or 1B for extended temperature range.
5. Read Burst Type: Nibble Sequential, set MR0 A[3] = 0B.
6. Supporting 0 - 85 °C with full JEDEC AC & DC specifications. This is the minimum requirements for all operating temperature options. However, for applications operating in Extended Temperature 85°C ~ 95°C, some optional spec is required.

Table 4-16 Electrical Characteristics and Recommended A.C. Operating Conditions (VDD = 1.5V)

Symbol	Parameter & Test Condition		DDR3-1866		DDR3-1600		Unit	Note
			Min.	Max.	Min.	Max.		
tAA	Internal read command to first data		13.75	20	13.5	20	ns	
tRCD	ACT to internal read or write delay time		13.75	-	13.5	-	ns	
tRP	PRE command period		13.75	-	13.5	-	ns	
tRC	ACT to ACT or REF command period		48.75	-	49.5	-	ns	
tRAS	ACTIVE to PRECHARGE command period		35	9 x tREFI	36	9 x tREFI	ns	
tCK(avg)	Average clock period	CL=5, CWL=5	3.0	3.3	3.0	3.3	ns	33
		CL=6, CWL=5	2.5	3.3	2.5	3.3	ns	33
		CL=7, CWL=6	1.875	<2.5	1.875	<2.5	ns	33
		CL=8, CWL=6	1.875	<2.5	1.875	<2.5	ns	33
		CL=9, CWL=7	1.5	<1.875	1.5	<1.875	ns	33
		CL=10, CWL=7	1.5	<1.875	-	-	ns	33
		CL=11, CWL=8	1.25	<1.5	-	-	ns	33
		CL=12, CWL=8	-	-	-	-	ns	33
		CL=13, CWL=9	-	-	-	-	ns	33
tCK (DLL_OFF)	Minimum Clock Cycle Time (DLL off mode)		8	-	8	-	ns	6
tCH(avg)	Average clock HIGH pulse width		0.47	0.53	0.47	0.53	tck	
tCL(avg)	Average Clock LOW pulse width		0.47	0.53	0.47	0.53	tck	
tDQSQ	DQS, $\overline{DQS}$ to DQ skew, per group, per access		-	100	-	125	ps	13
tQH	DQ output hold time from DQS, $\overline{DQS}$		0.38	-	0.38	-	tck	13
tLZ(DQ)	DQ low-impedance time from CK, $\overline{CK}$		-450	225	-500	250	ps	13,14
tHZ(DQ)	DQ high impedance time from CK, $\overline{CK}$		-	225	-	250	ps	13,14
tDS (base)	Data setup time to DQS, $\overline{DQS}$ referenced to Vih(ac) / Vil(ac) levels	AC150	25	-	45	-	ps	17
		AC130	-	-	-	-	ps	17
tDH (base)	Data hold time from DQS, $\overline{DQS}$ referenced to Vih(dc) / Vil(dc) levels	DC90	55	-	75	-	ps	17
tDIPW	DQ and DM Input pulse width for each input		360	-	400	-	ps	
tRPRE	DQS,$\overline{DQS}$ differential READ Preamble		0.9	-	0.9	-	tck	13,19
tRPST	DQS, $\overline{DQS}$ differential READ Postamble		0.3	-	0.3	-	tck	11,13
tQSH	DQS, $\overline{DQS}$ differential output high time		0.4	-	0.4	-	tck	13
tQSL	DQS, $\overline{DQS}$ differential output low time		0.4	-	0.4	-	tck	13
tWPRE	DQS, $\overline{DQS}$ differential WRITE Preamble		0.9	-	0.9	-	tck	1
tWPST	DQS, $\overline{DQS}$ differential WRITE Postamble		0.3	-	0.3	-	tck	1
tDQSCK	DQS, $\overline{DQS}$ rising edge output access time from rising CK, $\overline{CK}$		-225	225	-255	255	ps	13
tLZ(DQS)	DQS and DQS# low-impedance time (Referenced from RL - 1)		-450	225	-500	250	ps	13,14
tHZ(DQS)	DQS and $\overline{DQS}$ high-impedance time (Referenced from RL + BL/2)		-	225	-	250	ps	13,14
tDQSL	DQS, $\overline{DQS}$ differential input low pulse width		0.45	0.55	0.45	0.55	tck	29,31
tDQSH	DQS, $\overline{DQS}$ differential input high pulse width		0.45	0.55	0.45	0.55	tck	30,31
tDQSS	DQS, $\overline{DQS}$ rising edge to CK, $\overline{CK}$ rising edge		-0.27	0.27	-0.25	0.25	tck	
tDSS	DQS, $\overline{DQS}$ falling edge setup time to CK, $\overline{CK}$ rising edge		0.18	-	0.2	-	tck	32

Table 4-16 Electrical Characteristics and Recommended A.C. Operating Conditions (VDD = 1.5V) (continue)

Symbol	Parameter & Test Condition		DDR3-1866		DDR3-1600		Unit	Note
			Min.	Max.	Min.	Max.		
tDSH	DQS, $\overline{DQS}$ falling edge hold time from CK, $\overline{CK}$ rising edge		0.18	-	0.2	-	tck	32
tDLLK	DLL locking time		512	-	512	-	tck	
tRTP	Internal READ Command to PRECHARGE Command delay		max (4tCK, 7.5ns)	-	max (4tCK, 7.5ns)	-	tck	
tWTR	Delay from start of internal write transaction to internal read command		max (4tCK, 7.5ns)	-	max (4tCK, 7.5ns)	-	tck	18
tWR	WRITE recovery time		15	-	15	-	ns	18
tMRD	Mode Register Set command cycle time		4	-	4	-	tck	
tMOD	Mode Register Set command update delay		max (12tCK, 15ns)	-	max (12tCK, 15ns)	-	tck	
tCCD	CAS to $\overline{CAS}$ command delay		4	-	4	-	tck	
tDAL(min)	Auto precharge write recovery + prechargetime		WR + tRP		WR + tRP		tck	
tMPRR	Multi-Purpose Register Recovery Time		1	-	1	-	tck	22
tRRD	ACTIVE to ACTIVE command period		max (4tCK, 7.5ns)	-	max (4tCK, 7.5ns)	-	tck	
tFAW	Four activate window		40	-	45	-	ns	
tIS (base)	Command and Address setup time to CK, $\overline{CK}$ referenced to Vih(ac) / Vil(ac) levels	AC160	60	-	80	-	ps	16
		AC1500	185	-	205	-	ps	16,27
		AC125	-	-	-	-	ps	16,27
tIH (base)	Command and Address hold time from CK, $\overline{CK}$ referenced to Vih(dc) / Vil(dc) levels	DC90	130	-	150	-	ps	16
tIPW	Control and Address Input pulse width for each input		560	-	620	-	ps	28
tZQinit	Power-up and RESET calibration time		512	-	512	-	tck	
tZQoper	Normal operation Full calibration time		256	-	256	-	tck	
tZQCS	Normal operation Short calibration time		64	-	64	-	tck	23
tXPR	Exit Reset from CKE HIGH to a valid command		max (5tCK, tRFC (min) + 10ns)	-	max (5tCK, tRFC (min) + 10ns)	-	tck	
tXS	Exit Self Refresh to commands not requiring a locked DLL		max (5tCK, tRFC (min) + 10ns)	-	max (5tCK, tRFC (min) + 10ns)	-	tck	
tXSDLL	Exit Self Refresh to commands requiring a locked DLL		tDLLK (min)	-	tDLLK (min)	-	tck	
tCKESR	Minimum CKE low width for Self Refresh entry to exit timing		tCKE (min) + 1tCK	-	tCKE (min) + 1tCK	-	tck	

Table 4-16 Electrical Characteristics and Recommended A.C. Operating Conditions (VDD = 1.5V) (continue)

Symbol	Parameter & Test Condition	DDR3-1866		DDR3-1600		Unit	Note
		Min.	Max.	Min.	Max.		
tCKSRE	Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	max (5tCK, 10 ns)	-	max (5tCK, 10 ns)	-		
tCKSRX	Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	max (5tCK, 10 ns)	-	max (5tCK, 10 ns)	-	tck	
tXP	Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	max (3tCK, 6 ns)	-	max (3tCK, 6 ns)	-	tck	
tXPDLL	Exit Precharge Power Down with DLL frozen to commands requiring a lockedDLL	max (10tCK, 24 ns)	-	max (10tCK,24 ns)	-	tck	2
tCKE	CKE minimum pulse width	max (3tCK, 5 ns)	-	max (3tCK, 5.625 ns)	-	tck	
tCPDED	Command pass disable delay	1	-	1	-	tck	
tPD	Power Down Entry to Exit Timing	tCKE (min)	9 x tREFI	tCKE (min)	9 x tREFI		15
tACTPDEN	Timing of ACT command to Power Down entry	1	-	1	-	tck	20
tPRPDEN	Timing of PRE or PREA command to Power Down entry	1	-	1	-	tck	20
tRDPDEN	Timing of RD/RDA command to Power Down entry	RL+4+1	-	RL+4+1	-	tck	
tWRPDEN	Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	WL+4+ (tWR/tCK)	-	WL+4+ (tWR/tCK)	-	tck	9
tWRAPDEN	Timing of WRA command to Power Down entry (BL8OTF, BL8MRS,BC4OTF)	WL+4+ WR+1	-	WL+4+ WR+1	-	tck	10
tWRPDEN	Timing of WR command to Power Down entry (BC4MRS)	WL+2+ (tWR/tCK)	-	WL+2+ (tWR/tCK)	-	tck	9
tWRAPDEN	Timing of WRA command to Power Down entry (BC4MRS)	WL+2+ WR+1	-	WL+2+ WR+1	-	tck	10
tREFPDEN	Timing of REF command to Power Down entry	1	-	1	-	tck	20,21
tMRSPDEN	Timing of MRS command to Power Down entry	tMOD (min)	-	tMOD (min)	-		
ODTLon	ODT turn on Latency	WL - 2 = CWL + AL - 2				tck	
ODTLoff	ODT turn off Latency	WL - 2 = CWL + AL - 2					
ODTH4	ODT high time without write command or with write command and BC4	4	-	4	-	tck	
ODTH8	ODT high time with Write command and BL8	6	-	6	-	tck	
tAONPD	Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	2	8.5	2	8.5	ns	
tAOFPD	Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	2	8.5	2	8.5	ns	
tAON	RTT turn-on	-225	225	-250	250	ps	7
tAOF	RTT_Nom and RTT_WR turn-off time from ODTLoff reference	0.3	0.7	0.3	0.7	tck	8

Table 4-13 Electrical Characteristics and Recommended A.C. Operating Conditions (VDD = 1.5V) (continue)

Symbol	Parameter & Test Condition		DDR3-1866		DDR3-1600		Unit	Note
			Min.	Max.	Min.	Max.		
tADC	namic change skew		0.3	0.7	0.3	0.7	k	
tWLMRD	First DQS/$\overline{DQS}$ rising edge after write leveling mode is programmed		40	-	40	-	tck	3
tWLDQSEN	DQS/$\overline{DQS}$ delay after write leveling mode is programmed		25	-	25	-	tck	3
tWLS	Write leveling setup time from rising CK, CK# crossing to rising DQS, $\overline{DQS}$ rossing		165	-	195	-	ps	
tWLH	Write leveling hold time from rising DQS, DQS# crossing to rising CK, $\overline{CK}$ rossing		165	-	195	-	ps	
tWLO	Write leveling output delay		0	7.5	0	9	ns	
tWLOE	Write leveling output error		0	2	0	2	ns	
tRFC	REF command to ACT or REF command time		160	-	160	-	ns	
tREFI	Average periodic refresh interval	0°C to 85°C	-	7.8	-	7.8	us	
		85°C to 95°C	-	3.9	-	3.9	us	

Notes:

1. Actual value dependant upon measurement level.
2. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
3. The max values are system dependent.
4. WR as programmed in mode register.
5. Value must be rounded-up to next higher integer value.
6. There is no maximum cycle time limit besides the need to satisfy the refresh interval, tREFI.
7. For definition of RTT turn-on time tAON See “Timing Parameters”.
8. For definition of RTT turn-off time tAOF See “Timing Parameters”.
9. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR / tCK to the next integer.
10. WR in clock cycles as programmed in MR0.
11. The maximum read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side. See “Clock to Data Strobe Relationship”.
12. Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by t.b.d.
13. Value is only valid for RON34.
14. Single ended signal parameter.
15. tREFI depends on TOPER.
16. tIS(base) and tIH(base) values are for 1V/ns CMD/ADD single-ended slew rate and 2V/ns CK, $\overline{CK}$ differential slew rate. Note for DQ and DM signals, VREF(DC) = VRefDQ(DC). For input only pins except $\overline{RESET}$, VRef(DC) = VRefCA(DC). See “Address / Command Setup, Hold and Derating”.
17. tDS (base) and tDH (base) values are for a single-ended 1 V/ns slew rate DQs and 2 V/ns slew rate differential DQS, $\overline{DQS}$; when DQ single-ended slew rate is 2V/ns, the DQS differential slew rate is 4V/ns. Note for DQ and DM signals, VREF(DC) = VRefDQ(DC). For input only pins except $\overline{RESET}$, VRef(DC) = VRefCA(DC). See “Data Setup, Hold and Slew Rate Derating”.
18. Start of internal write transaction is defined as follows:
    - For BL8 (fixed by MRS and on- the-fly): Rising clock edge 4 clock cycles after WL.
    - For BC4 (on- the- fly): Rising clock edge 4 clock cycles after WL.
    - For BC4 (fixed by MRS): Rising clock edge 2 clock cycles after WL.
19. The maximum read preamble is bound by tLZ(DQS)min on the left side and tDQSCK(max) on the right side. See “Clock to Data Strobe Relationship”.
20. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
21. Although CKE is allowed to be registered LOW after a REFRESH command once tREFPDEN(min) is satisfied, there are cases where additional time such as tXPDLL(min) is also required. See “Power-Down clarifications-Case 2”
22. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
23. One ZQCS command can effectively correct a minimum of 0.5 % (ZQ Correction) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the ‘Output Driver Voltage and Temperature Sensitivity’ and ‘ODT Voltage and Temperature Sensitivity’ tables. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters.

One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{ZQCorrection}{(TSens \times Tdriftrate) + (VSens \times Vdriftrate)}$$

Where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities.

For example, if TSens = 1.5% / °C, VSens = 0.15% / mV, Tdriftrate = 1 °C / sec and Vdriftrate = 15 mV / sec, then the interval between ZQCS commands is calculated as:

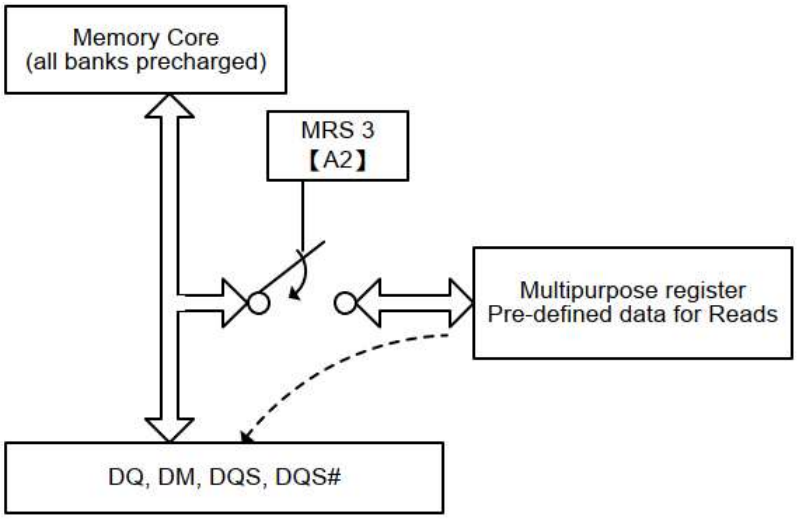
$$\frac{0.5}{(1.5 \times 1) + (0.15 \times 15)} = 0.133 \approx 128ms$$

24. n = from 13 cycles to 50 cycles. This row defines 38 parameters.
25. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
26. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
27. The tIS(base) AC125 specifications are adjusted from the tIS(base) AC1500 specification by adding an additional 75ps of derating to accommodate for the lower alternate threshold of 135 mV and another 10 ps to account for the earlier reference point [(135 mv - 125 mV) / 1 V/ns].
28. Pulse width of a input signal is defined as the width between the first crossing of Vref(dc) and the consecutive crossing of Vref(dc).
29. tDQSL describes the instantaneous differential input low pulse width on DQS - DQS#, as measured from one falling edge to the next consecutive rising edge.
30. tDQSH describes the instantaneous differential input high pulse width on DQS - DQS#, as measured from one rising edge to the next consecutive falling edge.
31. tDQSH,act + tDQSL,act = 1 tCK,act ; with tXYZ,act being the actual measured value of the respective timing parameter in the application.
32. tDSH,act + tDSS,act = 1 tCK,act ; with tXYZ,act being the actual measured value of the respective timing parameter in the application.
33. The CL and CWL settings result in tCK requirements. When making a selection of tCK, both CL and CWL requirement settings need to be fulfilled.

Multi-Purpose Register (MPR)

The Multi Purpose Register (MPR) function is used to Read out a predefined system timing calibration bit sequence.

Figure 4-5 MPR Block Diagram



To enable the MPR, a MODE Register Set (MRS) command must be issued to MR3 Register with bit A2 = 1. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP met). Once the MPR is enabled, any subsequent RD or RDA commands will be redirected to the Multi Purpose Register. The resulting operation, when a RD or RDA command is issued, is defined by MR3 bits A[1:0] when the MPR is enabled as shown in MPR Definition table. When the MPR is enabled, only RD or RDA commands are allowed until a subsequent MRS command is issued with the MPR disabled (MR3 bit A2 = 0). Note that in MPR mode RDA has the same functionality as a READ command which means the auto precharge part of RDA is ignored. Power-Down mode, Self-Refresh and any other non-RD/RDA command is not allowed during MPR enable mode. The RESET function is supported during MPR enable mode.

Table 4-17 MPR MR3 Register Definition

MR3 A[2]	MR3 A[1:0]	Function
MPR	MPR-Loc	
0b	Don't care (0b or 1b)	Normal operation, no MPR transaction. All subsequent Reads will come from DRAM array. All subsequent Write will go to DRAM array.
1b	See MPR Definition table	Enable MPR mode, subsequent RD/RDA commands defined by MR3 A[1:0].

MPR Functional Description

One bit wide logical interface via all DQ pins during READ operation.
Register Read on x16:
DQL[0] and DQU[0] drive information from MPR.
DQL[7:1] and DQU[7:1] either drive the same information as DQL [0], or they drive 0b.
Addressing during for Multi Purpose Register reads for all MPR agents:
BA [2:0]: don't care
A[1:0]: A[1:0] must be equal to '00' b. Data read burst order in nibble is fixed
A[2]: For BL=8, A[2] must be equal to 0b, burst order is fixed to [0,1,2,3,4,5,6,7], *) For Burst Chop 4 cases, the burst order is switched on nibble base A [2]=0b, Burst order: 0,1,2,3 *) A[2]=1b, Burst order: 4,5,6,7 *)
A[9:3]: don't care
A10/AP: don't care
A12/BC: Selects burst chop mode on-the-fly, if enabled within MR0.
A11, A13, … (if available): don't care
Regular interface functionality during register reads:
Support two Burst Ordering which are switched with A2 and A[1:0]=00b.

Support of read burst chop (MRS and on-the-fly via A12/BC)
All other address bits (remaining column address bits including A10, all bank address bits) will be ignored by the DDR3

SDRAM.
Regular read latencies and AC timings apply.
DLL must be locked prior to MPR Reads.
NOTE: Burst order bit 0 is assigned to LSB and burst order bit 7 is assigned to MSB of the selected MPR agent.

Table 4-18 MPR MR3 Register Definition

MR3 A[2]	MR3 A[1:0]	Function	Burst Length	Read Address A[2:0]	Burst Order and Data Pattern
1b	00b	Read Pre-defined Pattern for System Calibration	BL8	000b	Burst order 0,1,2,3,4,5,6,7 Pre-defined Data Pattern [0,1,0,1,0,1,0,1]
			BC4	000b	Burst order 0,1,2,3 Pre-defined Data Pattern [0,1,0,1]
			BC4	100b	Burst order 4,5,6,7 Pre-defined Data Pattern [0,1,0,1]
1b	01b	RFU	BL8	000b	Burst order 0,1,2,3,4,5,6,7
			BC4	000b	Burst order 0,1,2,3
			BC4	100b	Burst order 4,5,6,7
1b	10b	RFU	BL8	000b	Burst order 0,1,2,3,4,5,6,7
			BC4	000b	Burst order 0,1,2,3
			BC4	100b	Burst order 4,5,6,7
1b	11b	RFU	BL8	000b	Burst order 0,1,2,3,4,5,6,7
			BC4	000b	Burst order 0,1,2,3
			BC4	100b	Burst order 4,5,6,7

No Operation (NOP) Command

The No operation (NOP) command is used to instruct the selected DDR3 SDRAM to perform a NOP ($\overline{CS}$ low and $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ high). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

Deselect Command

The Deselect function ($\overline{CS}$ HIGH) prevents new commands from being executed by the DDR3 SDRAM. The DDR3 SDRAM is effectively deselected. Operations already in progress are not affected.

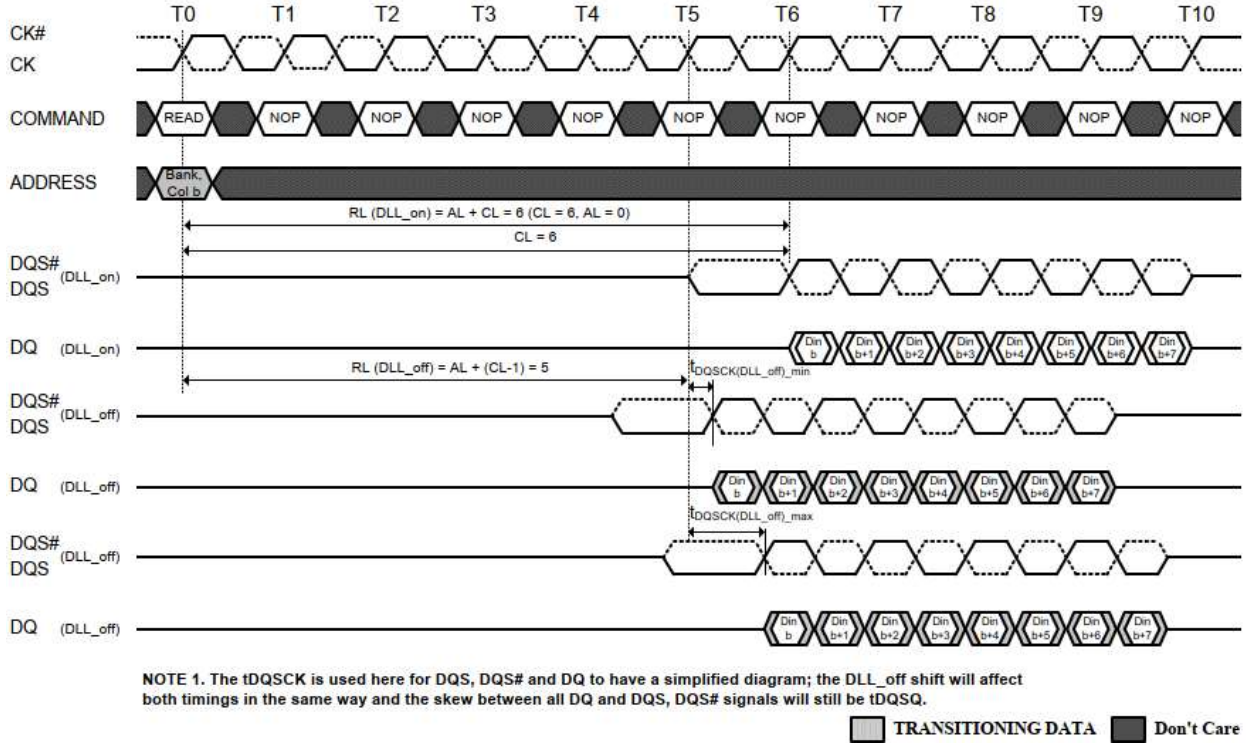
DLL- Off Mode

DDR3 DLL-off mode is entered by setting MR1 bit A0 to “1”; this will disable the DLL for subsequent operations until A0 bit set back to “0”. The MR1 A0 bit for DLL control can be switched either during initialization or later. The DLL-off Mode operations listed below are an optional feature for DDR3. The maximum clock frequency for DLL-off Mode is specified by the parameter tCKDLL_OFF. There is no minimum frequency limit besides the need to satisfy the refresh interval, tREFI.

Due to latency counter and timing restrictions, only one value of CAS Latency (CL) in MR0 and CAS Write Latency (CWL) in MR2 are supported. The DLL-off mode is only required to support setting of both CL=6 and CWL=6. DLL-off mode will affect the Read data Clock to Data Strobe relationship (tDQSCK) but not the data Strobe to Data relationship (tDQSQ, tQH). Special attention is needed to line up Read data to controller time domain. Comparing with DLL-on mode, where tDQSCK starts from the rising clock edge (AL+CL) cycles after the Read command, the DLL-off mode tDQSCK starts (AL+CL-1) cycles after the read command. Another difference is that tDQSCK may not be small compared to tCK (it might even be larger than tCK) and the difference between tDQSCKmin and tDQSCKmax is significantly larger than in DLL-on mode.

The timing relations on DLL-off mode READ operation have shown at the following Timing Diagram (CL=6, BL=8)

Figure 4-6 DLL-off mode READ Timing Operation



NOTE 1. The tDQSCK is used here for DQS, DQS# and DQ to have a simplified diagram; the DLL_off shift will affect both timings in the same way and the skew between all DQ and DQS, DQS# signals will still be tDQSQ.

DLL on/off switching procedure

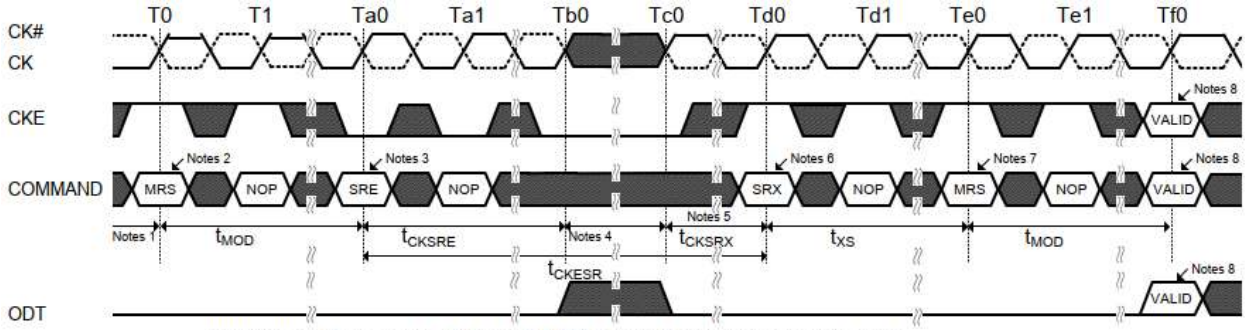
DDR3 DLL-off mode is entered by setting MR1 bit A0 to “1”; this will disable the DLL for subsequent operation until A0 bit set back to “0”.

DLL “on” to DLL “off” Procedure

To switch from DLL “on” to DLL “off” requires the frequency to be changed during Self-Refresh outlined in the following procedure:

1. Starting from Idle state (all banks pre-charged, all timing fulfilled, and DRAMs On-die Termination resistors, RTT, must be in high impedance state before MRS to MR1 to disable the DLL).
2. Set MR1 Bit A0 to “1” to disable the DLL.
3. Wait tMOD.
4. Enter Self Refresh Mode; wait until (tCKSRE) satisfied.
5. Change frequency, in guidance with “Input Clock Frequency Change” section.
6. Wait until a stable clock is available for at least (tCKSRX) at DRAM inputs.
7. Starting with the Self Refresh Exit command, CKE must continuously be registered HIGH until all tMOD timings from any MRS command are satisfied. In addition, if any ODT features were enabled in the mode registers when Self Refresh mode was entered, the ODT signal must continuously be registered LOW until all tMOD timings from any MRS command are satisfied. If both ODT features were disabled in the mode registers when Self Refresh mode was entered, ODT signal can be registered LOW or HIGH.
8. Wait tXS, and then set Mode Registers with appropriate values (especially an update of CL, CWL, and WR may be necessary. A ZQCL command may also be issued after tXS).
9. Wait for tMOD, and then DRAM is ready for next command.

Figure 4-7 DLL Switch Sequence from DLL-on to DLL-off



ODT: Static LOW in case RTT_Nom and RTT_WR is enabled, otherwise static Low or High

TIME BREAK Don't Care

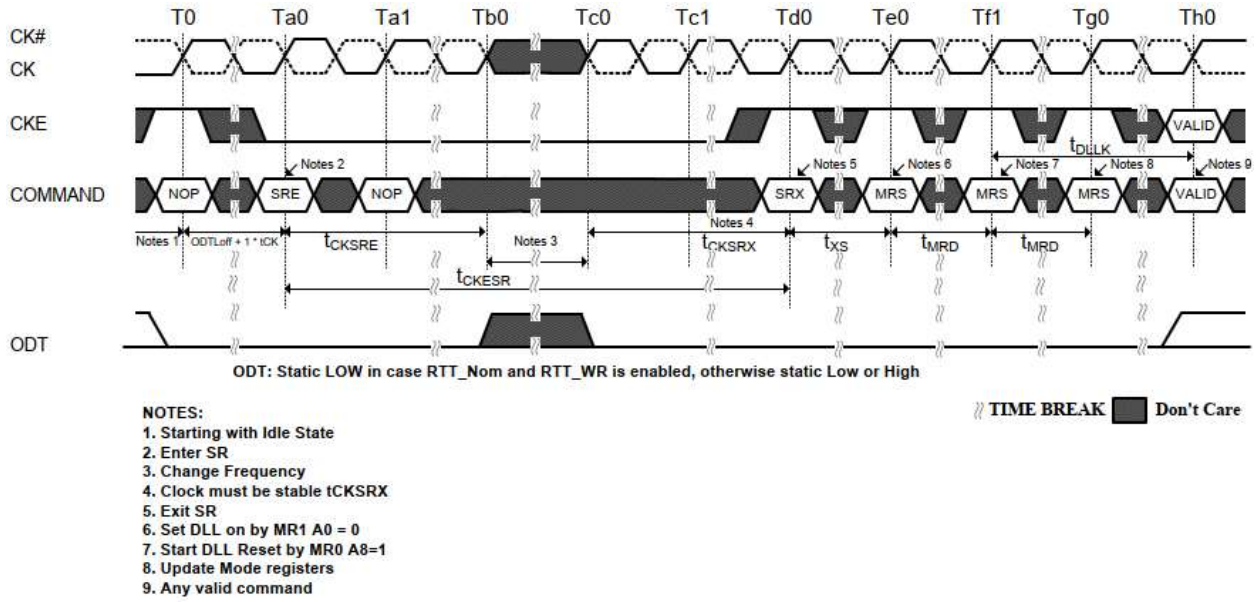
NOTES:
1. Starting with Idle State, RTT in Hi-Z state
2. Disable DLL by setting MR1 Bit A0 to 1
3. Enter SR
4. Change Frequency
5. Clock must be stable tCKSRX
6. Exit SR
7. Update Mode registers with DLL off parameters setting
8. Any valid command

DLL "off" to DLL "on" Procedure

To switch from DLL "off" to DLL "on" (with requires frequency change) during Self-Refresh:

1. Starting from Idle state (all banks pre-charged, all timings fulfilled and DRAMs On-die Termination resistors (RTT) must be in high impedance state before Self-Refresh mode is entered).
2. Enter Self Refresh Mode, wait until tCKSRE satisfied.
3. Change frequency, in guidance with "Input clock frequency change" section.
4. Wait until a stable clock is available for at least (tCKSRX) at DRAM inputs.
5. Starting with the Self Refresh Exit command, CKE must continuously be registered HIGH until tDLLK timing from subsequent DLL Reset command is satisfied. In addition, if any ODT features were enabled in the mode registers when Self Refresh mode was entered, the ODT signal must continuously be registered LOW until tDLLK timings from subsequent DLL Reset command is satisfied. If both ODT features are disabled in the mode registers when Self Refresh mode was entered, ODT signal can be registered LOW or HIGH.
6. Wait tXS, then set MR1 Bit A0 to "0" to enable the DLL.
7. Wait tMRD, then set MR0 Bit A8 to "1" to start DLL Reset.
8. Wait tMRD, then set Mode registers with appropriate values (especially an update of CL, CWL, and WR may be necessary. After tMOD satisfied from any proceeding MRS command, a ZQCL command may also be issued during or after tDLLK).
9. Wait for tMOD, then DRAM is ready for next command (remember to wait tDLLK after DLL Reset before applying command requiring a locked DLL!). In addition, wait also for tZQoper in case a ZQCL command was issued.

Figure 4-8 DLL Switch Sequence from DLL-off to DLL on



NOTES:
1. Starting with Idle State
2. Enter SR
3. Change Frequency
4. Clock must be stable tCKSRX
5. Exit SR
6. Set DLL on by MR1 A0 = 0
7. Start DLL Reset by MR0 A8=1
8. Update Mode registers
9. Any valid command

Jitter Notes

1. Unit 'tCK(avg)' represents the actual tCK(avg) of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.ex) tMRD = 4 [nCK] means; if one Mode Register Set command is registered at Tm, another Mode Register Set command may be registered at Tm+4, even if (Tm+4 - Tm) is 4 x tCK(avg) + tERR(4per),min.
2. These parameters are measured from a command/address signal (CKE, CS#, RAS#, CAS#, WE#, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK/CK#) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.
3. These parameters are measured from a data strobe signal (DQS(L/U), DQS(L/U)#) crossing to its respective clock signal (CK, CK#) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.
4. These parameters are measured from a data signal (DM(L/U), DQ(L/U)0, DQ(L/U)1, etc.) transition edge to its respective data strobe signal (DQS(L/U), DQS(L/U)#) crossing.

5. For these parameters, the DDR3 SDRAM device supports tnPARAM [nCK] = RU{ tPARAM [ns] / tCK(avg) [ns] }, which is in clock cycles, assuming all input clock jitter specifications are satisfied.
6. When the device is operated with input clock jitter, this parameter needs to be derated by the actual tERR(mper),act of the input clock, where 2 <= m <= 12. (output deratings are relative to the SDRAM input clock.)
7. When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(per),act of the input clock. (output deratings are relative to the SDRAM input clock.)

Table 4-19 Input clock jitter spec parameter

Parameter & Test Condition	Symbol	DDR3-1866		DDR3-1600		Unit
		Min.	Max.	Min.	Max.	
Clock period jitter	tJIT (per)	-70	70	-80	80	ps
Clock period jitter during DLL locking period	tJIT (per,lck)	-60	60	-70	70	ps
Cycle to cycle clock period jitter	tJIT (cc)	140		160		ps
Cycle to cycle clock period jitter during DLL locking period	tJIT (cc,lck)	120		140		ps
Cumulative error across 2 cycles	tERR (2per)	-103	103	-118	118	ps
Cumulative error across 3 cycles	tERR (3per)	-122	122	-140	140	ps
Cumulative error across 4 cycles	tERR (4per)	-136	136	-155	155	ps
Cumulative error across 5 cycles	tERR (5per)	-147	147	-168	168	ps
Cumulative error across 6 cycles	tERR (6per)	-155	155	-177	177	ps
Cumulative error across 7 cycles	tERR (7per)	-163	163	-186	186	ps
Cumulative error across 8 cycles	tERR (8per)	-169	169	-193	193	ps
Cumulative error across 9 cycles	tERR (9per)	-175	175	-200	200	ps
Cumulative error across 10 cycles	tERR (10per)	-180	180	-205	205	ps
Cumulative error across 11 cycles	tERR (11per)	-184	184	-210	210	ps
Cumulative error across 12 cycles	tERR (12per)	-188	188	-215	215	ps
Cumulative error across n cycles, n=13...50, inclusive	tERR (nper)	tERR (nper)min = (1+0.68ln(n)) * tJIT (per)min tERR (nper)max = (1+0.68ln(n)) * tJIT (per)max				ps

Input Clock frequency change

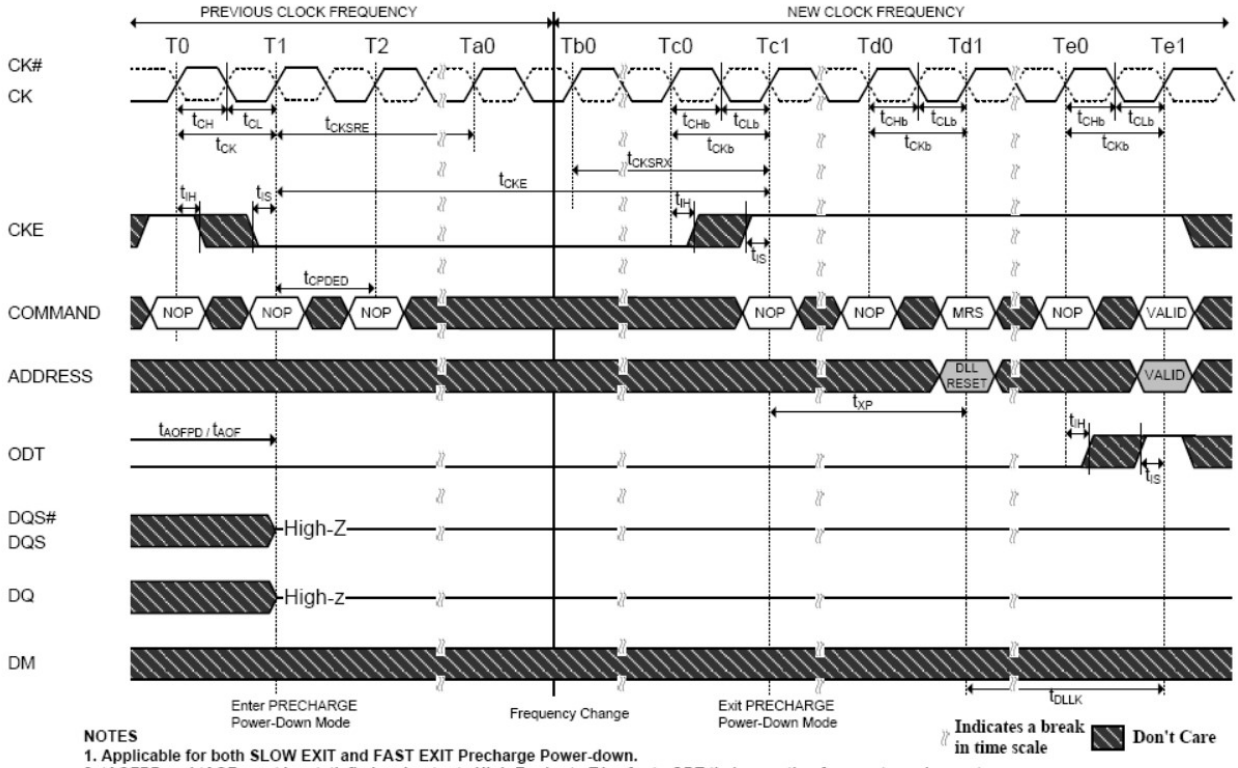
Once the DDR3 SDRAM is initialized, the DDR3 SDRAM requires the clock to be “stable” during almost all states of normal operation. This means once the clock frequency has been set and is to be in the “stable state”, the clock period is not allowed to deviate except for what is allowed for by the clock jitter and SSC (spread spectrum clocking) specification.

The input clock frequency can be changed from one stable clock rate to another stable clock rate under two conditions: (1) Self-Refresh mode and (2) Precharge Power-Down mode. Outside of these two modes, it is illegal to change the clock frequency.

For the first condition, once the DDR3 SDRAM has been successfully placed in to Self-Refresh mode and tCKSRE has been satisfied, the state of the clock becomes a don’t care. Once a don’t care, changing the clock frequency is permissible, provided the new clock frequency is stable prior to tCKSRX. When entering and exiting Self-Refresh mode of the sole purpose of changing the clock frequency, the Self-Refresh entry and exit specifications must still be met. The DDR3 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade.

The second condition is when the DDR3 SDRAM is in Precharge Power-Down mode (either fast exit mode or slow exit mode). If the RTT_Nom feature was enabled in the mode register prior to entering Precharge power down mode, the ODT signal must continuously be registered LOW ensuring RTT is in an off state. If the RTT_Nom feature was disabled in the mode register prior to entering Precharge power down mode, RTT will remain in the off state. The ODT signal can be registered either LOW or HIGH in this case. A minimum of tCKSRE must occur after CKE goes LOW before the clock frequency may change. The DDR3 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade. During the input clock frequency change, ODT and CKE must be held at stable LOW levels. Once the input clock frequency is changed, stable new clocks must be provided to the DRAM tCKSRX before precharge Power Down may be exited; after Precharge Power Down is exited and tXP has expired, the DLL must be RESET via MRS. Depending on the new clock frequency additional MRS commands may need to be issued to appropriately set the WR, CL, and CWL with CKE continuously registered high. During DLL re-lock period, ODT must remain LOW and CKE must remain HIGH. After the DLL lock time, the DRAM is ready to operate with new clock frequency.

Figure 4-9 Change Frequency during Precharge Power-down



NOTES
1. Applicable for both SLOW EXIT and FAST EXIT Precharge Power-down.
2. tAOFPD and tAOF must be statisfied and outputs High-Z prior to T1;refer to ODT timing section for exact requirements
3. If the RTT_NOM feature was enabled in the mode register prior to entering Precharge power down mode, the ODT signal must continuously be registered LOW ensuring RTT is in an off state. If the RTT_NOM feature was disabled in the mode register prior to entering Precharge power down mode, RTT will remain in the off state. The ODT signal can be registered either LOW or HIGH in this case.

Write Leveling

For better signal integrity, DDR3 memory adopted fly by topology for the commands, addresses, control signals, and clocks. The fly by topology has benefits from reducing number of stubs and their length but in other aspect, causes flight time skew between clock and strobe at every DRAM on DIMM. It makes it difficult for the Controller to maintain tDQSS, tDSS, and tDSH pecification. Therefore, the controller should support “write leveling” in DDR3 SDRAM to compensate the skew.

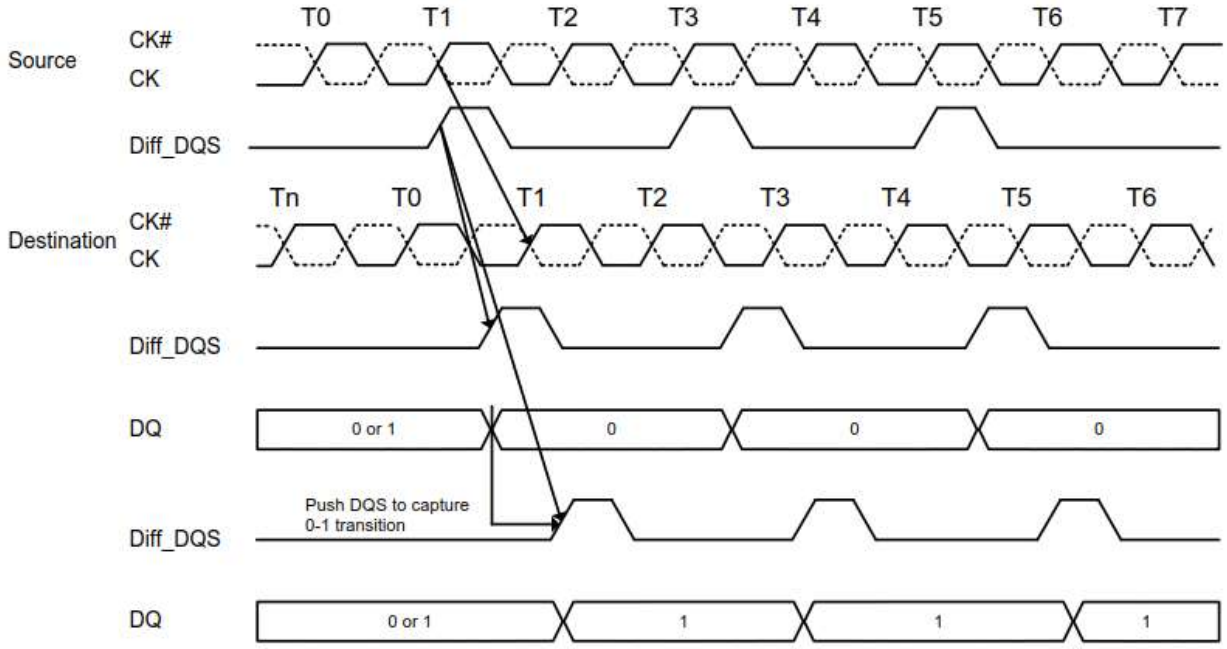
The memory controller can use the “write leveling” feature and feedback from the DDR3 SDRAM to adjust the DQS – DQS# to CK – CK# relationship. The memory controller involved in the leveling must have adjustable delay setting on DQS – DQS# to align the rising edge of DQS – DQS# with that of the clock at the DRAM pin. DRAM asynchronously feeds back CK – CK#, sampled with the rising edge of DQS – DQS#, through the DQ bus. The controller repeatedly delays DQS – DQS# until a transition from 0 to 1 is detected. The DQS – DQS# delay established though this exercise would ensure tDQSS specification.

Besides tDQSS, tDSS, and tDSH specification also needs to be fulfilled. One way to achieve this is to combine the actual tDQSS in the application with an appropriate duty cycle and jitter on the DQS- DQS# signals. Depending on the actual tDQSS in the application, the actual values for tDQSL and tDQSH may have to be better than the absolute limits provided in “AC Timing Parameters” section in order to satisfy tDSS and tDSH specification.

DQS/DQS# driven by the controller during leveling mode must be determined by the DRAM based on ranks populated. Similarly, the DQ bus driven by the DRAM must also be terminated at the controller.

One or more data bits should carry the leveling feedback to the controller across the DRAM configurations X16. On a X16 device, both byte lanes should be leveled independently. Therefore, a separate feedback mechanism should be available for each byte lane. The upper data bits should provide the feedback of the upper diff_DQS (diff_UDQS) to clock relationship whereas the lower data bits would indicate the lower diff_DQS (diff_LDQS) to clock relationship.

Figure 4-10 Write Leveling Concept



Write Leveling

DRAM enters into Write leveling mode if A7 in MR1 set “High” and after finishing leveling, DRAM exits from write leveling mode if A7 in MR1 set “Low”. Note that in write leveling mode, only DQS/DQS# terminations are activated and deactivated via ODT pin not like normal operation.

Table 4-20 DRAM termination function in the leveling mode

ODT pin at DRAM	DQS, DQS# termination	DQs termination
De-asserted	off	off
Asserted	on	off

Note:

1. In write leveling mode with its output buffer disabled (MR1[bit7]=1 with MR1[bit12]=1) all RTT_Nom settings are allowed; in Write Leveling Mode with its output buffer enabled (MR1[bit7]=1 with MR1[bit12]=0) only RTT_Nom settings of RZQ/2, RZQ/4, and RZQ/6 are allowed.

Procedure Description

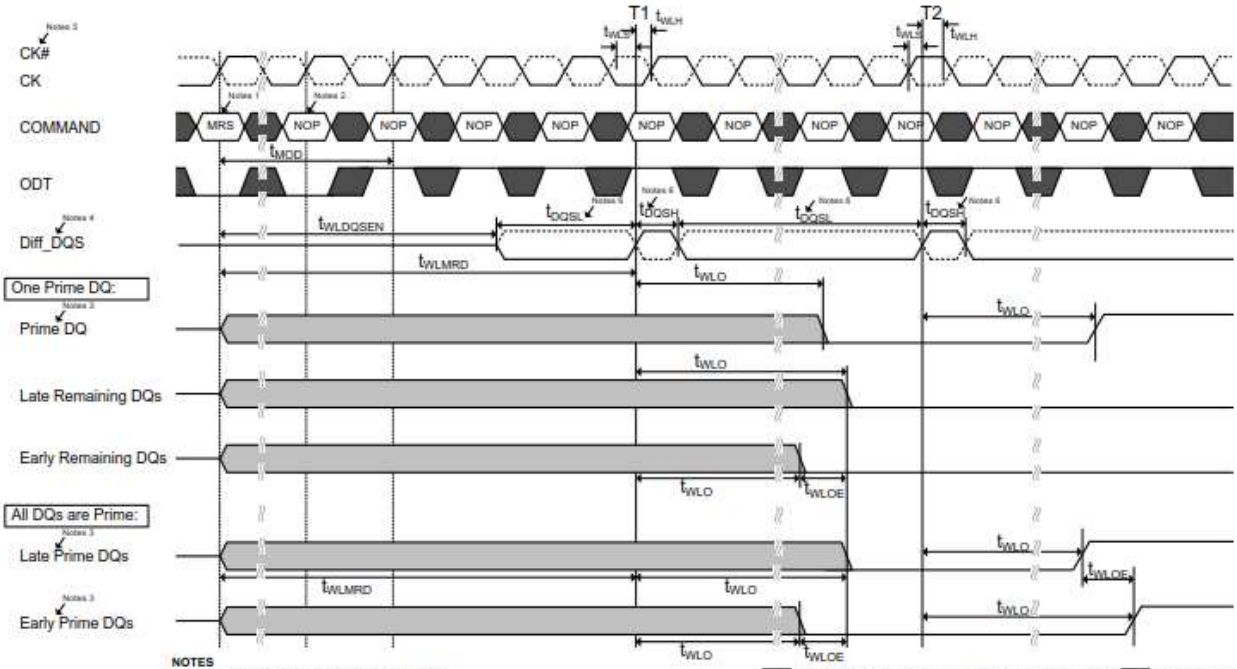
Memory controller initiates Leveling mode of all DRAMs by setting bit 7 of MR1 to 1. With entering write leveling mode, the DQ pins are in undefined driving mode. During write leveling mode, only NOP or Deselect commands are allowed. As well as an MRS command to exit write leveling mode. Since the controller levels one rank at a time, the output of other rank must be disabled by setting MR1 bit A12 to 1. Controller may assert ODT after tMOD, time at which DRAM is ready to accept the ODT signal.

Controller may drive DQS low and DQS# high after a delay of tWLDQSEN, at which time DRAM has applied on-die termination on these signals. After tDQSL and tWLMRD controller provides a single DQS, DQS# edge which is used by the DRAM to sample CK – CK# driven from controller. tWLMRD(max) timing is controller dependent.

DRAM samples CK – CK# status with rising edge of DQS and provides feedback on all the DQ bits asynchronously after tWLO timing. There is a DQ output uncertainty of tWLOE defined to allow mismatch on DQ bits; there are no read strobes (DQS/DQS) needed for these DQs. Controller samples incoming DQ and decides to increment or decrement DQS – DQS# delay setting and launches the next DQS/DQS# pulse after some time, which is controller dependent. Once a 0 to 1 transition is detected, the controller locks DQS – DQS# delay setting and write leveling is achieved for the device.

Figure 4-11 Timing details of Write Leveling sequence

(DQS – DQS# is capturing CK – CK# low at T1 and CK – CK# high at T2)



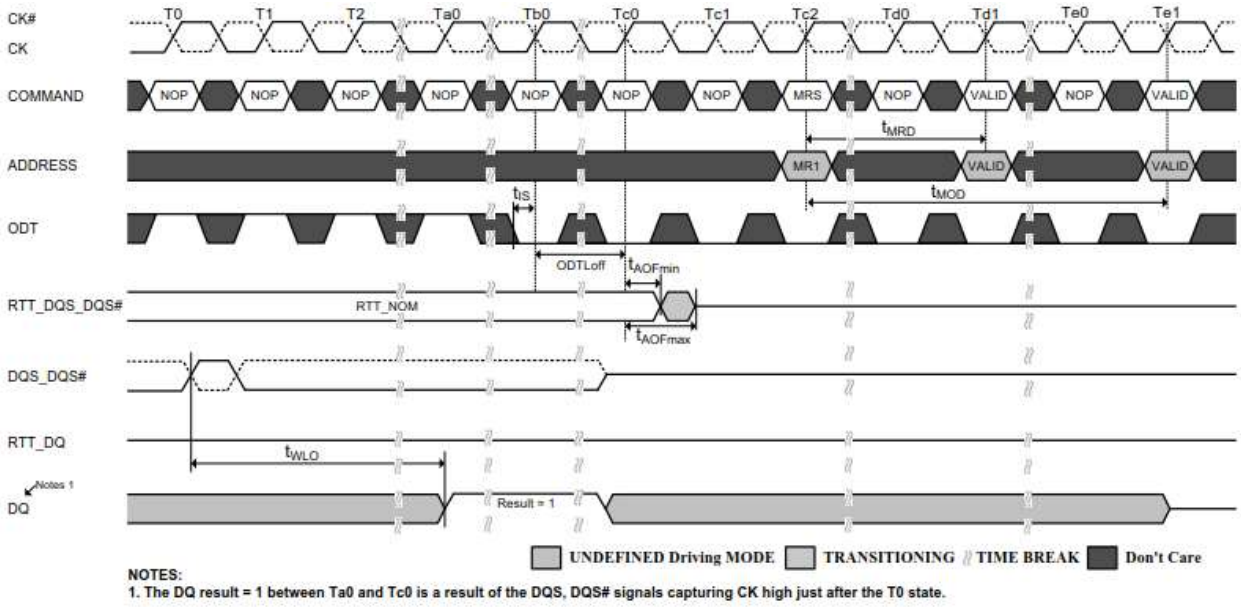
NOTES
1. MRS: Load MR1 to enter write leveling mode.
2. NOP: NOP or Deselect.
3. DRAM has the option to drive leveling feedback on a prime DQ or all DQs. If feedback is driven only on one DQ, the remaining DQs must be driven low, as shown in above Figure, and maintained at this state through out the leveling procedure.
4. diff_DQS is the differential data strobe (DQS, DQS#). Timing reference points are the zero crossings. DQS is shown with solid line, DQS# is shown with dotted line.
5. CK, CK# : CK is shown with solid dark line, where as CK# is drawn with dotted line.
6. DQS, DQS# needs to fulfill minimum pulse width requirements tDQSH(min) and tDQSL(min) as defined for regular Writes; the max pulse width is system dependent.

Write Leveling Mode Exit

The following sequence describes how Write Leveling Mode should be exited:

1. After the last rising strobe edge (see ~T0), stop driving the strobe signals (see ~Tc0). Note: From now on, DQ pins are in undefined driving mode, and will remain undefined, until tMOD after the respective MR command (Te1).
2. Drive ODT pin low (tIS must be satisfied) and keep it low (see Tb0).
3. After the RTT is switched off, disable Write Level Mode via MRS command (see Tc2).
4. After tMOD is satisfied (Te1), any valid command may be registered. (MR commands may be issued after tMRD (Td1).

Figure 4-12 Timing details of Write Leveling exit



NOTES:
1. The DQ result = 1 between Ta0 and Tc0 is a result of the DQS, DQS# signals capturing CK high just after the T0 state.

ACTIVE Command

The ACTIVE command is used to open (or activate) a row in a particular bank for subsequent access. The value on the BA0-BA2 inputs selects the bank, and the addresses provided on inputs A0-A13 selects the row. These rows remain active (or open) for accesses until a precharge command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

PRECHARGE Command

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row activation a specified time (tRP) after the PRECHARGE command is issued, except in the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command is allowed if there is no open row in that bank (idle bank) or if the previously open row is already in the process of precharging. However, the precharge period will be determined by the last PRECHARGE command issued to the bank.

4.8 READ Operation

Read Burst Operation

During a READ or WRITE command DDR3 will support BC4 and BL8 on the fly using address A12 during the READ or WRITE (AUTO PRECHARGE can be enabled or disabled).
A12=0, BC4 (BC4 = burst chop, tCCD=4)
A12=1, BL8
A12 will be used only for burst length control, not a column address.

Figure 4-13 READ Burst Operation RL=5 (AL=0, CL=5, BL=8)

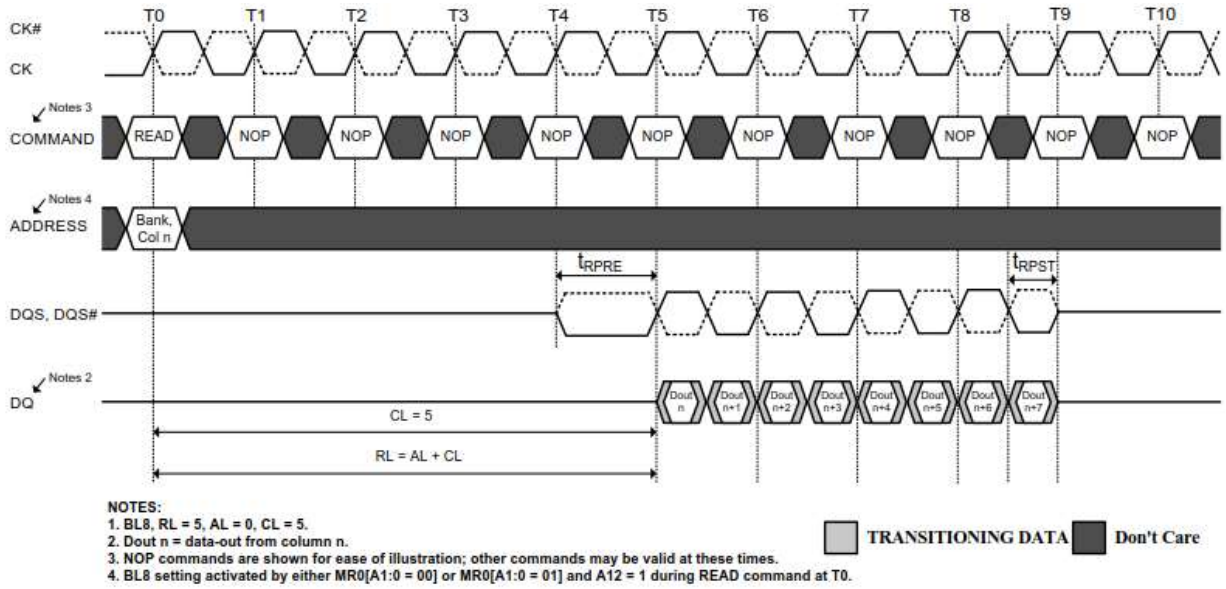
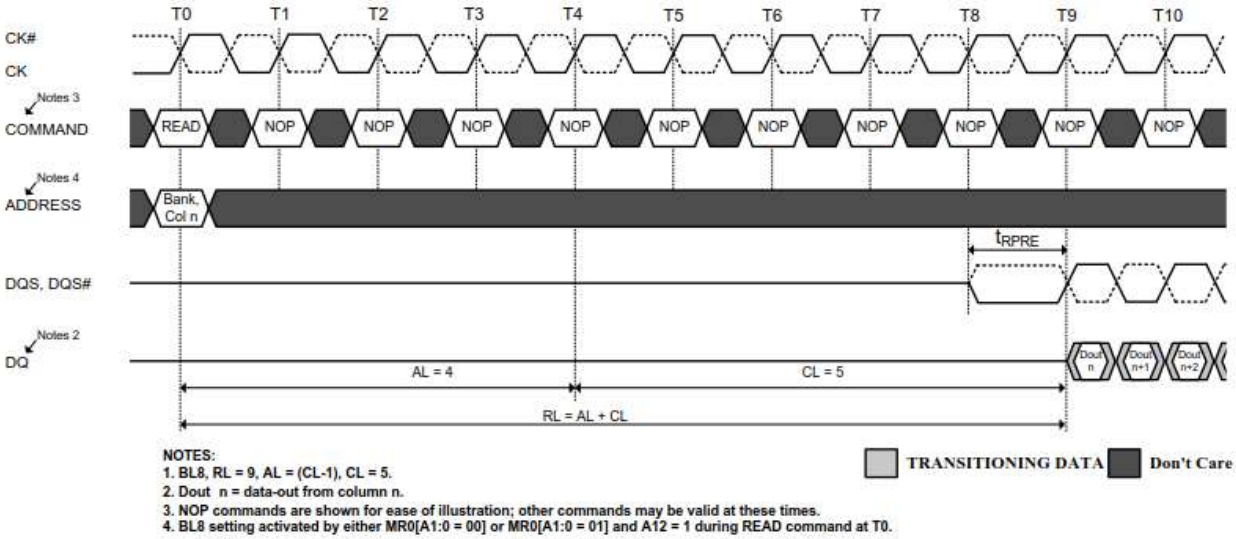


Figure 4-14 READ Burst Operation RL=9 (AL=4, CL=5, BL=8)



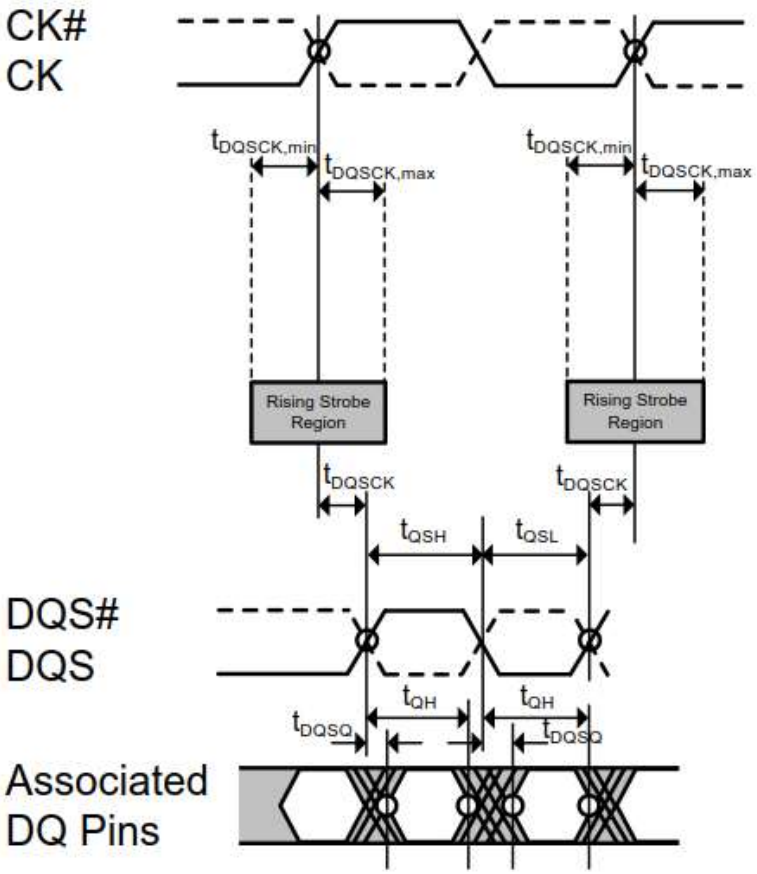
READ Timing Definitions

Read timing is shown in the following figure and is applied when the DLL is enabled and locked.

Rising data strobe edge parameters:
tDQSCK min/max describes the allowed range for a rising data strobe edge relative to CK, CK#. tDQSCK is the actual position of a rising strobe edge relative to CK, CK#. tQSH describes the DQS, DQS# differential output high time. tDQSQ describes the latest valid transition of the associated DQ pins. tQH describes the earliest invalid transition of the associated DQ pins.

Falling data strobe edge parameters:
tQSL describes the DQS, DQS# differential output low time. tDQSQ describes the latest valid transition of the associated DQ pins. tQH describes the earliest invalid transition of the associated DQ pins.
tDQSQ; both rising/falling edges of DQS, no tAC defined.

Figure 4-15 READ timing Definition



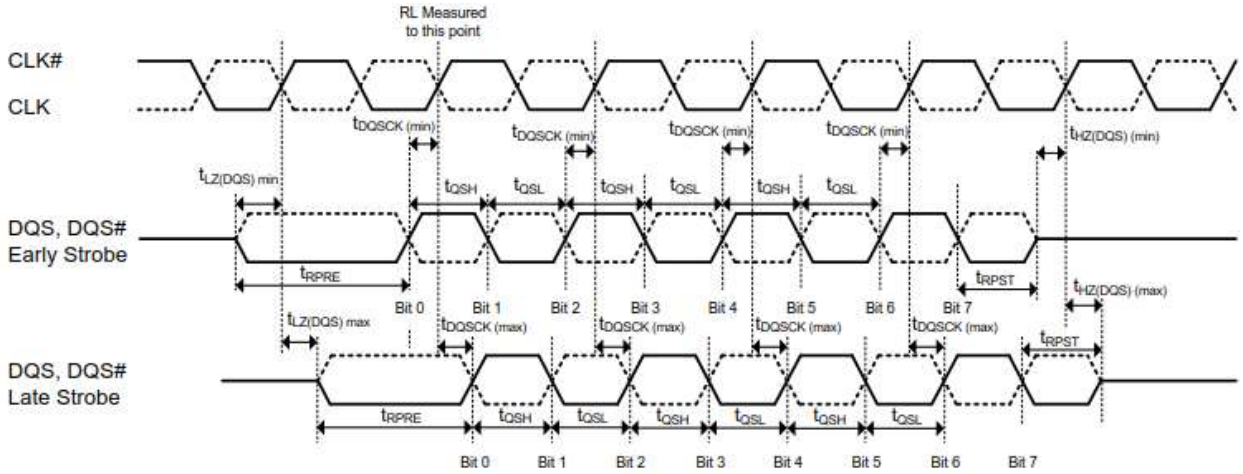
Read Timing; Clock to Data Strobe relationship

Clock to Data Strobe relationship is shown in the following figure and is applied when the DLL is enabled and locked.

Rising data strobe edge parameters:
tDQSCK min/max describes the allowed range for a rising data strobe edge relative to CK and CK#. tDQSCK is the actual position of a rising strobe edge relative to CK and CK#. tQSH describes the data strobe high pulse width.

Falling data strobe edge parameters:
tQSL describes the data strobe low pulse width.

Figure 4-16 Clock to Data Strobe relationship



Notes:

1. Within a burst, rising strobe edge is not necessarily fixed to be always at tDQSCK(min) or tDQSCK(max). Instead, rising strobe edge can vary between tDQSCK(min) and tDQSCK(max).
2. Notwithstanding note 1, a rising strobe edge with tDQSCK(max) at T(n) can not be immediately followed by a rising strobe edge with tDQSCK(min) at T(n+1). This is because other timing relationships (tQSH, tQSL) exist: if tDQSCK(n+1) < 0: tDQSCK(n) < 1.0 tCK - (tQSHmin + tQSLmin) - | tDQSCK(n+1) |
3. The DQS, DQS# differential output high time is defined by tQSH and the DQS, DQS# differential output low time is defined by tQSL.
4. Likewise, tLZ(DQS)min and tHZ(DQS)min are not tied to tDQSCKmin (early strobe case) and tLZ(DQS)max and tHZ(DQS)max are not tied to tDQSCKmax (late strobe case).
5. The minimum pulse width of read preamble is defined by tRPRE(min).
6. The maximum read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZDSQ(max) on the right side.
7. The minimum pulse width of read postamble is defined by tRPST(min).
8. The maximum read preamble is bound by tLZDQS(min) on the left side and tDQSCK(max) on the right side

Read Timing; Data Strobe to Data Relationship

The Data Strobe to Data relationship is shown in the following figure and is applied when the DLL and enabled and locked.

Rising data strobe edge parameters:

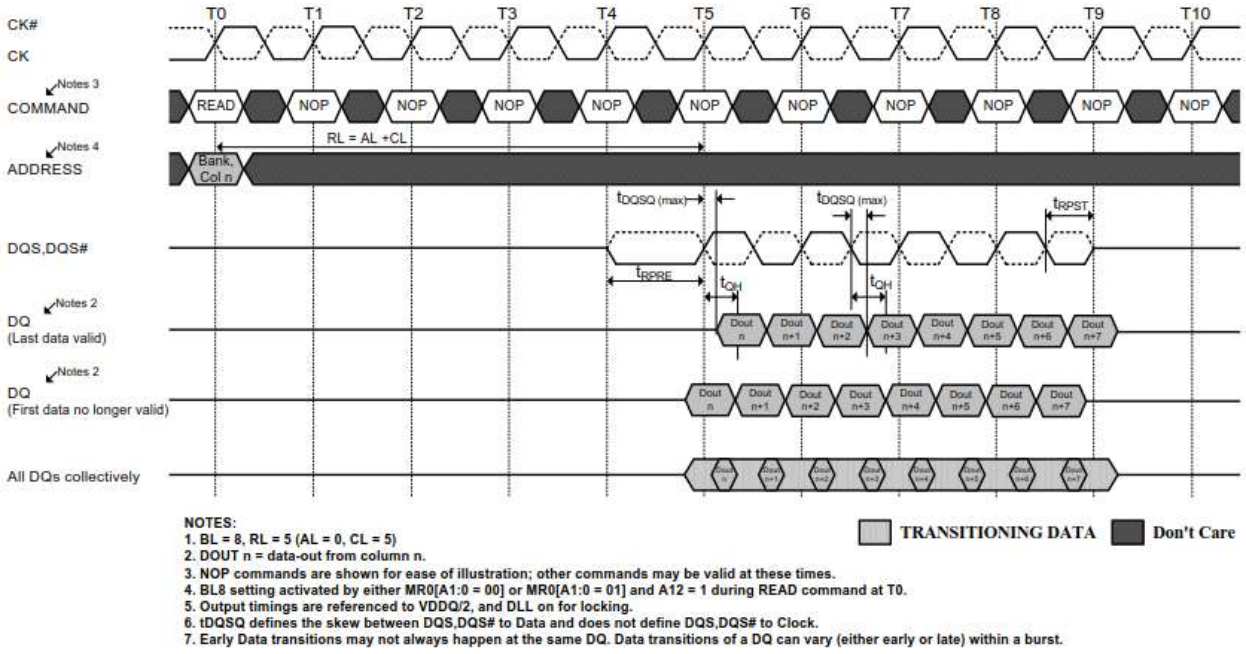
- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

Falling data strobe edge parameters:

- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.
- tDQSQ; both rising/falling edges of DQS, no tAC defined

tDQSQ; both rising/falling edges of DQS, no tAC defined

Figure 4-17 Data Strobe to Data Relationship



NOTES:

1. BL = 8, RL = 5 (AL = 0, CL = 5)
2. DOUT n = data-out from column n.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T0.
5. Output timings are referenced to VDDQ/2, and DLL on for locking.
6. tDQSQ defines the skew between DQS,DQS# to Data and does not define DQS,DQS# to Clock.
7. Early Data transitions may not always happen at the same DQ. Data transitions of a DQ can vary (either early or late) within a burst.

4.9 Write Operation

DDR3 Burst Operatio

During a READ or WRITE command, DDR3 will support BC4 and BL8 on the fly using address A12 during the READ or WRITE (Auto Precharge can be enabled or disabled).
A12=0, BC4 (BC4 = Burst Chop, tCCD=4)
A12=1, BL8
A12 is used only for burst length control, not as a column address.

Write Timing Violations

Generally, if timing parameters are violated, a complete reset/initialization procedure has to be initiated to make sure the DRAM works properly. However, it is desirable for certain minor violations that the DRAM is guaranteed not to "hang up" and errors be limited to that particular operation.
For the following, it will be assumed that there are no timing violations with regard to the Write command itself (including ODT, etc.) and that it does satisfy all timing requirements not mentioned below.

Data Setup and Hold Violations

Should the strobe timing requirements (tDS, tDH) be violated, for any of the strobe edges associated with a write burst, then wrong data might be written to the memory location addressed with the offending WRITE command. Subsequent reads from that location might result in unpredictable read data, however, the DRAM will work properly otherwise.

Strobe to Strobe and Strobe to Clock Violations

Should the strobe timing requirements (tDQSH, tDQSL, tWPRE, tWPST) or the strobe to clock timing requirements (tDSS, tDSH, tDQSS) be violated, for any of the strobe edges associated with a Write burst, then wrong data might be written to the memory location addressed with the offending WRITE command. Subsequent reads from that location might result in unpredictable read data, however the DRAM will work properly otherwise.

Write Timing Parameters

This drawing is for example only to enumerate the strobe edges that "belong" to a write burst. No actual timing violations are shown here. For a valid burst all timing parameters for each edge of a burst need to be satisfied (not only for one edge).

Refresh Command

The Refresh command (REF) is used during normal operation of the DDR3 SDRAMs. This command is not persistent, so it must be issued each time a refresh is required. The DDR3 SDRAM requires Refresh cycles at an average periodic interval of tREFI. When CS#, RAS#, and CAS# are held Low and WE# High at the rising edge of the clock, the chip enters a Refresh cycle. All banks of the SDRAM must be precharged and idle for a minimum of the precharge time tRP(min) before the Refresh Command can be applied. The refresh addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during a Refresh command. An internal address counter suppliers the address during the refresh cycle. No control of the external address bus is required once this cycle has started. When the refresh cycle has completed, all banks of the SDRAM will be in the precharged (idle) state. A delay between the Refresh Command and the next valid command, except NOP or DES, must be greater than or equal to the minimum Refresh cycle time tRFC(min).

In general, a Refresh command needs to be issued to the DDR3 SDRAM regularly every tREFI interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of 8 Refresh commands can be postponed during operation of the DDR3 SDRAM, meaning that at no point in time more than a total of 8 Refresh commands are allowed to be postponed. In case that 8 Refresh commands are postponed in a row, the resulting maximum interval between the surrounding Refresh commands is limited to 9 x tREFI. A maximum of 8 additional Refresh commands can be issued in advance ("pulled in"), with each one reducing the number of regular Refresh commands required later by one. Note that pulling in more than 8 Refresh commands in advance does not further reduce the number of regular Refresh commands required later, so that the resulting maximum interval between two surrounding Refresh command is limited to 9 x tREFI. Before entering Self-Refresh Mode, all postponed Refresh commands must be executed.

Self-Refresh Operation

The Self-Refresh command can be used to retain data in the DDR3 SDRAM, even if the reset of the system is powered down. When in the Self-Refresh mode, the DDR3 SDRAM retains data without external clocking. The DDR3 SDRAM device has a built-in timer to accommodate Self-Refresh operation. The Self-Refresh Entry (SRE) Command is defined by having CS#, RAS#, CAS#, and CKE held low with WE# high at the rising edge of the clock. Before issuing the Self-Refreshing-Entry command, the DDR3 SDRAM must be idle with all bank precharge state with tRP satisfied. Also, on-die termination must be turned off before issuing Self-Refresh-Entry command, by either registering ODT pin low "ODTL + 0.5tCK" prior to the Self-Refresh Entry command or using MRS to MR1 command. Once the Self-Refresh Entry command is registered, CKE must be held low to keep the device in Self-Refresh mode. During normal operation (DLL on), MR1 (A0=0), the DLL is automatically disabled upon entering Self- Refresh and is automatically enabled (including a DLL-RESET) upon exiting Self-Refresh.

When the DDR3 SDRAM has entered Self-Refresh mode, all of the external control signals, except CKE and RESET#, are "don't care". For proper Self-Refresh operation, all power supply and reference pins (VDD, VDDQ, VSS, VSSQ, VRefCA, and VRefDQ) must be at valid levels. The DRAM initiates a minimum of one Refresh command internally within tCKE period once it enters Self-Refresh mode.

The clock is internally disabled during Self-Refresh operation to save power. The minimum time that the DDR3 SDRAM must remain in Self-Refresh mode is tCKE. The user may change the external clock frequency or halt the external clock tCKSRE after Self-Refresh entry is registered; however, the clock must be restarted and stable tCKSRX before the device can exit Self-Refresh mode.

The procedure for exiting Self-Refresh requires a sequence of events. First, the clock must be stable prior to CKE going back HIGH. Once a Self-Refresh Exit Command (SRX, combination of CKE going high and either NOP or Deselect on command bus) is registered, a delay of at least tXS must be satisfied before a valid command not requiring a locked DLL can be issued to the device to allow for any internal refresh in progress. Before a command which requires a locked DLL can be applied, a delay of at least tXSDLL and applicable ZQCAL function requirements [TBD] must be satisfied. Before a command that requires a locked DLL can be applied, a delay of at least tXSDLL must be satisfied.

Depending on the system environment and the amount of time spent in Self-Refresh, ZQ calibration commands may be required to compensate for the voltage and temperature drift as described in "ZQ Calibration Commands". To issue ZQ calibration commands, applicable timing requirements must be satisfied.

CKE must remain HIGH for the entire Self-Refresh exit period tXSDLL for proper operation except for Self-Refresh re-entry. Upon exit from Self-Refresh, the DDR3 SDRAM can be put back into Self-Refresh mode after waiting at least tXS period and issuing one refresh command (refresh period of tRFC). NOP or deselect commands must be registered on each positive clock edge during the Self-Refresh exit interval tXS. ODT must be turned off during tXSDLL. The use of Self-Refresh mode instructs the possibility that an internally times refresh event can be missed when CKE is raised for exit from Self-Refresh mode. Upon exit from Self-Refresh, the DDR3 SDRAM requires a minimum of one extra refresh command before it is put back into Self-Refresh mode.

4.10 Power-Down Modes

Power-Down Entry and Exit

Power-Down is synchronously entered when CKE is registered low (along with NOP or Deselect command). CKE is not allowed to go low while mode register set command, MPR operations, ZQCAL operations, DLL locking or read/write operation are in progress. CKE is allowed to go low while any of other operation such as row activation, precharge or auto precharge and refresh are in progress, but power-down IDD spec will not be applied until finishing those operation.

The DLL should be in a locked state when power-down is entered for fastest power-down exit timing. If the DLL is not locked during power-down entry, the DLL must be reset after exiting power-down mode for proper read operation and synchronous ODT operation. DRAM design provides all AC and DC timing and voltage specification as well proper DLL operation with any CKE intensive operations as long as DRAM controller complies with DRAM specifications.

During Power-Down, if all banks are closed after any in progress commands are completed, the device will be in precharge Power-Down mode; if any bank is open after in progress commands are completed, the device will be in active Power-Down mode.

Entering Power-down deactivates the input and output buffers, excluding CK, CK, ODT, CKE, and RESET#. To protect DRAM internal delay on CKE line to block the input signals, multiple NOP or Deselect commands are needed during the CKE switch off and cycle(s) after, this timing period are defined as tCPDED. CKE_low will result in deactivation of command and address receivers after tCPDED has expired.

Table 4-21 Power-Down Entry Definitions

Status of DRAM	MRS bit A12	DLL	PD Exit	Relevant Parameters
Active (A Bank or more open)	Don't Care	On	Fast	tXP to any valid command.
Precharged (All Banks Precharged)	0	off	Slow	tXP to any valid command. Since it is in precharge state, commands here will be ACT, AR, MRS/EMRS, PR or PRA. tXPDLL to commands who need DLL to operate, such as RD, RDA or ODT control line.
Precharged (All Banks Precharged)	1	off	Fast	tXP to any valid command.

Also the DLL is disabled upon entering precharge power-down (Slow Exit Mode), but the DLL is kept enabled during precharge power-down (Fast Exit Mode) or active power-down. In power-down mode, CKE low, RESET# high, and a stable clock signal must be maintained at the inputs of the DD3 SDRAM, and ODT should be in a valid state but all other input signals are “Don’t care” (If RESET# goes low during Power-Down, the DRAM will be out of PD mode and into reset state).

CKE low must be maintain until tCKE has been satisfied. Power-down duration is limited by 9 times tREFI of the device. The power-down state is synchronously exited when CKE is registered high (along with a NOP or Deselect command).CKE high must be maintained until tCKE has been satisfied. A valid, executable command can be applied with power-down exit latency, tXP and/or tXPDLL after CKE goes high. Power-down exit latency is defined at AC spec table of this datasheet.

4.11 On-Die Termination (ODT)

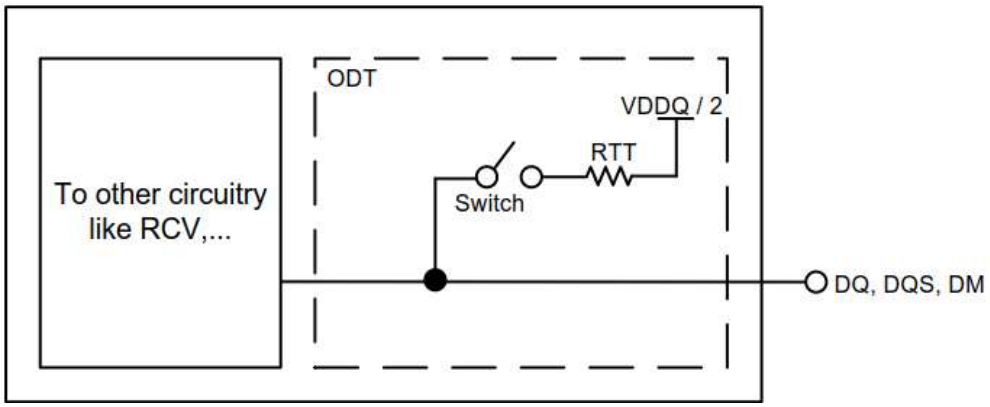
ODT (On-Die Termination) is a feature of the DDR3 SDRAM that allows the DRAM to turn on/off termination resistance. For x16 configuration, ODT is applied to each DQU, DQL, DQSU, DQSU#, DQSL, DQSL#, DMU and DML signal via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.

More details about ODT control modes and ODT timing modes can be found further down in this document.

The ODT feature is turned off and not supported in Self-Refresh mode.

A simple functional representation of the DRAM ODT feature is shown as below.

Figure 4-18 Functional representation of ODT



The switch is enabled by the internal ODT control logic, which uses the external ODT pin and other control information. The value of RTT is determined by the settings of Mode Register bits. The ODT pin will be ignored if the Mode Register MR1 and MR2 are programmed to disable ODT and in self-refresh mode.

ODT Mode Register and ODT Truth Table

The ODT Mode is enabled if either of MR1 {A2, A6, A9} or MR2 {A9, A10} are non-zero. In this case, the value of RTT is determined by the settings of those bits.

Application: Controller sends WR command together with ODT asserted.

One possible application: The rank that is being written to provides termination.

DRAM turns ON termination if it sees ODT asserted (except ODT is disabled by MR) DRAM does not use any write or read command decode information.

Table 4-22 Termination Turth Table

ODT pin	DRAM Termination State
0	OFF
1	On, (Off, if disabled by MR1 (A2, A6, A9) and MR2 (A9, A10) in gereral)

Synchronous ODT Mode

Synchronous ODT mode is selected whenever the DLL is turned on and locked. Based on the powerdown definition, these modes are:

- Any bank active with CKE high
- Refresh with CKE high
- Idle mode with CKE high
- Active power down mode (regardless of MR0 bit A12)
- Precharge power down mode if DLL is enabled during precharge power down by MR0 bit A12

The direct ODT feature is not supported during DLL-off mode. The on-die termination resistors must be disabled by continuously registering the ODT pin low and/or by programming the RTT_Nom bits MR1{A9,A6,A2} to {0,0,0} via a mode register set command during DLL-off mode.

In synchronous ODT mode, RTT will be turned on ODTLon clock cycles after ODT is sampled high by a rising clock edge and turned off ODTLoff clock cycles after ODT is registered low by a rising clock edge. The ODT latency is tied to the write latency (WL) by: ODTLon = WL - 2; ODTLoff = WL-2.

ODT Latency and Posted ODT

In synchronous ODT Mode, the Additive Latency (AL) programmed into the Mode Register (MR1) also applies to the ODT signal. The DRAM internal ODT signal is delayed for a number of clock cycles defined by the Additive Latency (AL) relative to the external ODT signal. ODTLon = CWL + AL - 2; ODTLoff = CWL + AL - 2. For details, refer to DDR3 SDRAM latency definitions.

Table 4-23 ODT Latency

Symbol	Parameter	DDR3-1866/1600	Unit
ODTLon	ODT turn on Latency	WL – 2 = CWL + AL -2	tCK
ODTLoff	ODT turn off Latency	WL – 2 = CWL + AL -2	tCK

Timing Parameters

In synchronous ODT mode, the following timing parameters apply: ODTLon, ODTLoff, tAON min/max, tAOF min/max. Minimum RTT turn-on time (tAON min) is the point in time when the device leaves high impedance and ODT resistance begins to turn on. Maximum RTT turn-on time (tAON max) is the point in time when the ODT resistance is fully on. Both are measured from ODTLon.

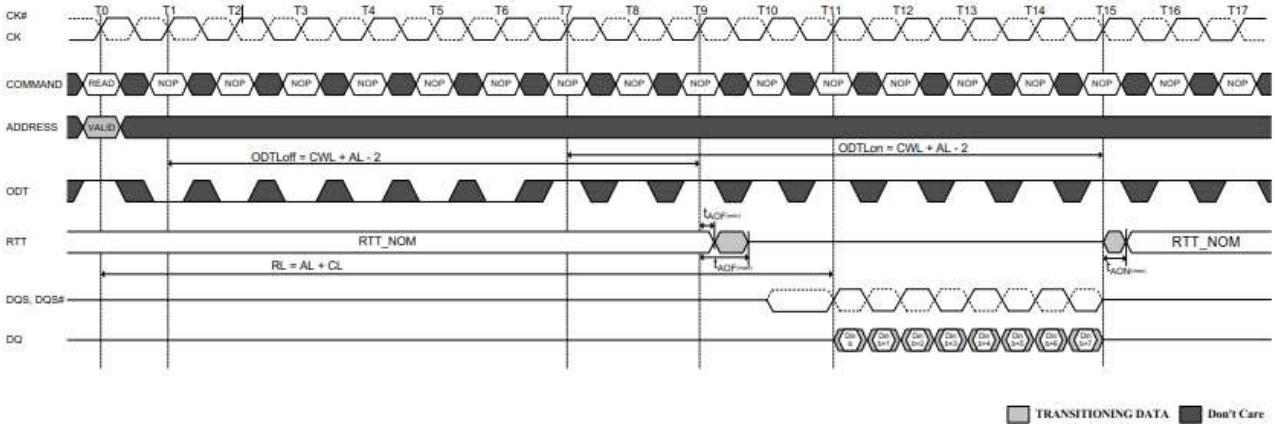
Minimum RTT turn-off time (tAOF min) is the point in time when the device starts to turn off the ODT resistance. Maximum RTT turn off time (tAOF max) is the point in time when the on-die termination has reached high impedance. Both are measured from ODTLoff.

When ODT is asserted, it must remain high until ODTH4 is satisfied. If a Write command is registered by the SDRAM with ODT high, then ODT must remain high until ODTH4 (BL=4) or ODTH8 (BL=8) after the write command. ODTH4 and ODTH8 are measured from ODT registered high to ODT registered low or from the registration of a write command until ODT is registered low.

ODT during Reads

As the DDR3 SDRAM cannot terminate and drive at the same time, RTT must be disabled at least half a clock cycle before the read preamble by driving the ODT pin low appropriately. RTT may not be enabled until the end of the post-amble as shown in the following figure. DRAM turns on the termination when it stops driving which is determined by tHZ. If DRAM stops driving early (i.e. tHZ is early), then tAONmin time may apply. If DRAM stops driving late (i.e. tHZ is late), then DRAM complies with tAONmax timing. Note that ODT may be disabled earlier before the Read and enabled later after the Read than shown in this example.

Figure 4-19 ODT must be disabled externally during Reads by driving ODT low
(CL=6; AL=CL-1=5; RL=AL+CL=11; CWL=5; ODTLon=CWL+AL-2=8; ODTLoff=CWL+AL-2=8)



Dynamic ODT

In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3 SDRAM can be changed without issuing an MRS command. This requirement is supported by the “Dynamic ODT” feature as described as follows:

Functional Description

The Dynamic ODT Mode is enabled if bit (A9) or (A10) of MR2 is set to ‘1’. The function is described as follows:

Two RTT values are available: RTT_Nom and RTT_WR.
- The value for RTT_Nom is preselected via bits A[9,6,2] in MR1.
- The value for RTT_WR is preselected via bits A[10,9] in MR2.

During operation without write commands, the termination is controlled as follows:
- Nominal termination strength RTT_Nom is selected.
- Termination on/off timing is controlled via ODT pin and latencies ODTLon and ODTLoff.

When a Write command (WR, WRA, WRS4, WRS8, WRAS4, WRAS8) is registered, and if Dynamic ODT is enabled, the termination is controlled as follows:
- A latency ODTLcnw after the write command, termination strength RTT_WR is selected.
- A latency ODTLcwn8 (for BL8, fixed by MRS or selected OTF) or ODTLcwn4 (for BC4, fixed by MRS or selected OTF) after the write command, termination strength RTT_Nom is selected.
- Termination on/off timing is controlled via ODT pin and ODTLon, ODTLoff.

The following table shows latencies and timing parameters which are relevant for the on-die termination control in Dynamic ODT mode.

The dynamic ODT feature is not supported at DLL-off mode. User must use MRS command to set RTT_WR, MR2 [A10,A9 = [0,0], to disable Dynamic ODT externally.

When ODT is asserted, it must remain high until ODTH4 is satisfied. If a Write command is registered by the SDRAM with ODT high, then ODT must remain high until ODTH4 (BL=4) or ODTH8 (BL=8) after the Write command. ODTH4 and ODTH8 are measured from ODT registered high to ODT registered low or from the registration of Write command until ODT is register low.

Table 4-24 ODT Latency

Name and Description	Abbr.	Defined from	Defined to	Definition for all DDR3 speed pin	Unit
ODT turn-on Latency	ODTLon	registering external ODT signal high	turning termination on	ODTLon=WL-2	tCK
ODT turn-off Latency	ODTLoff	registering external ODT signal low	turning termination off	ODTLoff=WL-2	tCK
ODT Latency for changing from RTT_Nom to RTT_WR	ODTLcnw	registering external write command	change RTT strength from RTT_Nom to RTT_WR	ODTLcnw=WL-2	tCK
ODT Latency for change from RTT_WR to RTT_Nom (BL=4)	ODTLcwn4	registering external write command	change RTT strength from RTT_WR to RTT_Nom	ODTLcwn4=4+ODTLoff	tCK
ODT Latency for change from RTT_WR to RTT_Nom (BL=8)	ODTLcwn8	registering external write command	change RTT strength from RTT_WR to RTT_Nom	ODTLcwn8=6+ODTLoff	tCK (avg)
Minimum ODT high time after ODT assertion	ODTH4	registering ODT high	ODT registered low	ODTH4=4	tCK (avg)
Minimum ODT high time after Write (BL=4)	ODTH4	registering ODT high	ODT registered low	ODTH4=4	tCK (avg)
Minimum ODT high time after Write (BL=8)	ODTH8	registering write with ODT high	ODT register low	ODTH8=6	tCK (avg)
RTT change skew	tADC	ODTLcnw ODTLcwn	RTT valid	tADC(min)=0.3tCK(avg) tADC(max)=0.7tCK(avg)	tCK (avg)

Note:

1. tAOF, nom and tADC, nom are 0.5tCK (effectively adding half a clock cycle to ODTLoff, ODTcnw, and ODTLcwn)

Asynchronous ODT Mode

Asynchronous ODT mode is selected when DRAM runs in DLLon mode, but DLL is temporarily disabled (i.e. frozen) in precharge power-down (by MR0 bit A12). Based on the power down mode definitions, this is currently Precharge power down mode if DLL is disabled during precharge power down by MR0 bit A12.

In asynchronous ODT timing mode, internal ODT command is NOT delayed by Additive Latency (AL) relative to the external ODT command.

In asynchronous ODT mode, the following timing parameters apply: tAONPD min/max, tAOFPD min/max.

Minimum RTT turn-on time (tAONPD min) is the point in time when the device termination circuit leaves high impedance state and ODT resistance begins to turn on. Maximum RTT turn on time (tAONPD max) is the point in time when the ODT resistance is fully on.

tAONPDmin and tAONPDmax are measured from ODT being sampled high.

Minimum RTT turn-off time (tAOFPDmin) is the point in time when the devices termination circuit starts to turn off the ODT resistance. Maximum ODT turn off time (tAOFPDmax) is the point in time when the on-die termination has reached high impedance. tAOFPDmin and tAOFPDmax are measured from ODT being sample low.

Table 4-25 ODT Latency

Description	Min	Max
ODT to RTT turn-on delay	min{ ODTLon * tCK + tAONmin; tAONPDmin } min{ (WL - 2) * tCK + tAONmin; tAONPDmin }	max{ ODTLon * tCK + tAONmax; tAONPDmax } max{ (WL - 2) * tCK + tAONmax; tAONPFmax }
ODT to RTT turn-off delay	min{ ODTLoff * tCK + tAOFmin; tAOFPDmin } min{ (WL - 2) * tCK + tAOFmin; tAOFPDmin }	max{ ODTLoff * tCK + tAOFmax; tAOFPDmax } max{ (WL - 2) * tCK + tAOFmax; tAOFPDmax }
tANPD	WL - 1	

Synchronous to Asynchronous ODT Mode Transition during Power-Down Entry

If DLL is selected to be frozen in Precharge Power Down Mode by the setting of bit A12 in MR0 to “0”, there is a transition period around power down entry, where the DDR3 SDRAM may show either synchronous or asynchronous ODT behavior.

The transition period is defined by the parameters tANPD and tCPDED(min). tANPD is equal to (WL-1) and is counted backwards in time from the clock cycle where CKE is first registered low. tCPDED(min) starts with the clock cycle where CKE is first registered low. The transition period begins with the starting point of tANPD and terminates at the end point of tCPDED(min). If there is a Refresh command in progress while CKE goes low, then the transition period ends at the later one of tRFC(min) after the Refresh command and the end point of tCPDED(min). Please note that the actual starting point at tANPD is excluded from the transition period, and the actual end point at tCPDED(min) and tRFC(min, respectively, are included in the transition period.

ODT assertion during the transition period may result in an RTT changes as early as the smaller of tAONPDmin and (ODTLon*tck+tAONmin) and as late as the larger of tAONPDmax and (ODTLon*tCK+tAONmax). ODT de-assertion during the transition period may result in an RTT change as early as the smaller of tAOFPDmin and (ODTLoff*tCK+tAOFmin) and as late as the larger of tAOFPDmax and (ODTLoff*tCK+tAOFmax). Note that, if AL has a large value, the range where RTT is uncertain becomes quite large. The following figure shows the three different cases: ODT_A, synchronous behavior before tANPD; ODT_B has a state change during the transition period; ODT_C shows a state change after the transition period.

Asynchronous to Synchronous ODT Mode transition during Power-Down Exit

If DLL is selected to be frozen in Precharge Power Down Mode by the setting of bit A12 in MR0 to “0”, there is also a transition period around power down exit, where either synchronous or asynchronous response to a change in ODT must be expected from the DDR3 SDRAM.

This transition period starts tANPD before CKE is first registered high, and ends tXPDLL after CKE is first registered high. tANPD is equal to (WL -1) and is counted (backwards) from the clock cycle where CKE is first registered high.

ODT assertion during the transition period may result in an RTT change as early as the smaller of tAONPDmin and (ODTLon* tCK+tAONmin) and as late as the larger of tAONPDmax and (ODTLon*tCK+tAONmax). ODT deassertion during the transition period may result in an RTT change as early as the smaller of tAOFPDmin and

(ODTLoff*tCK+tAOFmin) and as late as the larger of tAOFPDmax and (ODToff*tCK+tAOFmax). Note that if AL has a large value, the range where RTT is uncertain becomes quite large. The following figure shows the three different cases: ODT_C, asynchronous response before tANPD; ODT_B has a state change of ODT during the transition period; ODT_A shows a state change of ODT after the transition period with synchronous response.

Asynchronous to Synchronous ODT Mode during short CKE high and short CKE low periods

If the total time in Precharge Power Down state or Idle state is very short, the transition periods for PD entry and PD exit may overlap. In this case, the response of the DDR3 SDRAMs RTT to a change in ODT state at the input may be synchronous or asynchronous from the state of the PD entry transition period to the end of the PD exit transition period (even if the entry ends later than the exit period).

If the total time in Idle state is very short, the transition periods for PD exit and PD entry may overlap. In this case, the response of the DDR3 SDRAMs RTT to a change in ODT state at the input may be synchronous or asynchronous from the state of the PD exit transition period to the end of the PD entry transition period. Note that in the following figure, it is assumed that there was no Refresh command in progress when Idle state was entered.

4.12 ZQ Calibration Commands

ZQ Calibration Description

ZQ Calibration command is used to calibrate DRAM Ron and ODT values. DDR3 SDRAM needs longer time to calibrate output driver and on-die termination circuits at initialization and relatively smaller time to perform periodic calibrations.

ZQCL command is used to perform the initial calibration during power-up initialization sequence. This command may be issued at any time by the controller depending on the system environment. ZQCL command triggers the calibration engine inside the DRAM and once calibration is achieved the calibrated values are transferred from calibration engine to DRAM IO which gets reflected as updated output driver and on-die termination values.

The first ZQCL command issued after reset is allowed a timing period of tZQinit to perform the full calibration and the transfer of values. All other ZQCL commands except the first ZQCL command issued after RESET is allowed a timing period of tZQoper.

ZQCS command is used to perform periodic calibrations to account for voltage and temperature variations. A shorter timing window is provided to perform the calibration and transfer of values as defined by timing parameter tZQCS.

No other activities should be performed on the DRAM channel by the controller for the duration of tZQinit, tZQoper, or tZQCS. The quiet time on the DRAM channel allows calibration of output driver and on-die termination values.

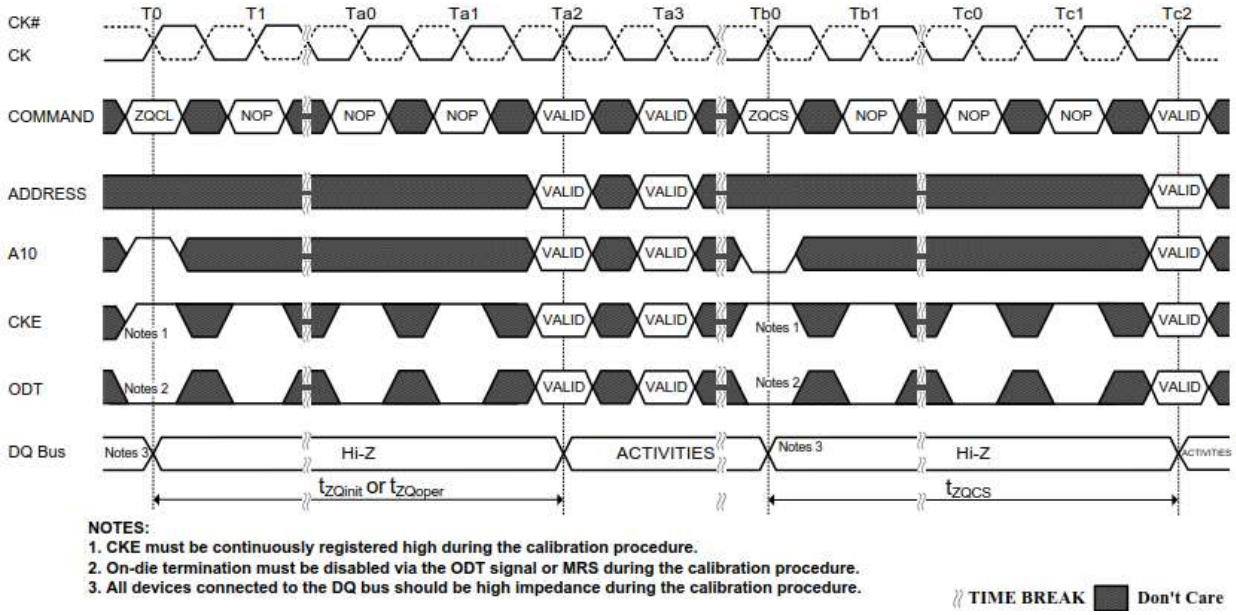
Once DRAM calibration is achieved, the DRAM should disable ZQ current consumption path to reduce power.

All banks must be precharged and tRP met before ZQCL or ZQCS commands are issued by the controller.

ZQ calibration commands can also be issued in parallel to DLL lock time when coming out of self refresh. Upon selfrefresh exit, DDR3 SDRAM will not perform an IO calibration without an explicit ZQ calibration command. The earliest possible time for ZQ Calibration command (short or long) after self refresh exit is tXS.

In systems that share the ZQ resistor between devices, the controller must not allow any overlap of tZQoper, tZQinit, or tZQCS between ranks.

Figure 4-20 ZQ Calibration Timing



ZQ External Resistor Value, Tolerance, and Capacitive loading

In order to use the ZQ calibration function, a 240 ohm ±1% tolerance external resistor connected between the ZQ pin and ground. The single resistor can be used for each SDRAM or one resistor can be shared between two SDRAMs if the ZQ calibration timings for each SDRAM do not overlap. The total capacitive loading on the ZQ pin must be limited.

- Single-ended requirements for differential signals

Each individual component of a differential signal (CK, CK#, LDQS, UDQS, LDQS#, or UDQS#) has also to comply with certain requirements for single-ended signals.

CK and CK# have to approximately reach VSEHmin / VSELmax (approximately equal to the ac-levels (VIH(ac) / VIL(ac)) for ADD/CMD signals) in every half-cycle. LDQS, UDQS, LDQS#, UDQS# have to reach VSEHmin / VSELmax (approximately the ac-levels (VIH(ac) / VIL(ac)) for DQ signals) in every half-cycle proceeding and following a valid transition.

Note that the applicable ac-levels for ADD/CMD and DQ's might be different per speed-bin etc. E.g., if VIH135(ac) / VIL135(ac) is used for ADD/CMD signals, then these ac-levels apply also for the single-ended signals CK and CK#. signals CK and CK#.

Table 4-26 Single-ended levels for CK, DQSL, DQSU, CK#, DQSL# or DQSU#

Symbol	Parameter	Min.	Max.	Unit	Note
VSEH	Single-ended high level for strobes	(VDD / 2) + 0.175	Note 3	V	1,2
	Single-ended high level for CK, CK#	(VDD / 2) + 0.175	Note 3	V	1,2
VSEL	Single-ended low level for strobes	Note 3	(VDD / 2) - 0.175	V	1,2
	Single-ended low level for CK, CK#	Note 3	(VDD / 2) - 0.175	V	1,2

Notes:

1. For CK, CK# use VIH/VIL(ac) of ADD/CMD; for strobes (DQSL, DQSL#, DQSU, DQSU#) use VIH/VIL(ac) of DQs.
2. VIH(ac)/VIL(ac) for DQs is based on VREFDQ; VIH(ac)/VIL(ac) for ADD/CMD is based on VREFCA; if a reduced achigh or ac-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined, however the single-ended signals CK, CK#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot.

- Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, CK# and DQS, DQS#) must meet the requirements in the following

table. The differential input cross point voltage Vix is measured from the actual cross point of true and complete signal to the midlevel between of VDD and VSS.

Table 4-27 Cross point voltage for differential input signals (CK, DQS)

Symbol	Parameter	Min.	Max.	Unit	Note
VIX(CK)	Differential Input Cross Point Voltage relative to VDD/2 for CK, CK#	-150	150	mV	1
VIX(DQS)	Differential Input Cross Point Voltage relative to VDD/2 for DQS, DQS#	-150	150	mV	1

Note:

1. The relation between Vix Min/Max and VSEL/VSEH should satisfy following.
   (VDD/2) + Vix (Min) - VSEL ≧ 25mV
   VSEH - ((VDD/2) + Vix (Max)) ≧ 25mV

- Slew Rate Definition for Differential Input Signals

Input slew rate for differential signals (CK, CK# and DQS, DQS#) are defined and measured as shown below.

Table 4-28 Differential Input Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential input slew rate for rising edge (CK, CK# and DQS, DQS#)	VILdiffmax	VIHdiffmin	[VIHdiffmin-VILdiffmax] / DeltaTRdiff
Differential input slew rate for falling edge (CK, CK# and DQS, DQS#)	VIHdiffmin	VILdiffmax	[VIHdiffmin-VILdiffmax] / DeltaTFdiff

Note:

1. The differential signal (i.e., CK, CK# and DQS, DQS#) must be linear between these thresholds.

Table 4-29 Single-ended AC and DC Output Levels

Symbol	Parameter	Values	Unit	Note
VOH(DC)	DC output high measurement level (for IV curve linearity)	0.8 x VDDQ	V	
VOM(DC)	DC output mid measurement level (for IV curve linearity)	0.5 x VDDQ	V	
VOL(DC)	DC output low measurement level (for IV curve linearity)	0.2 x VDDQ	V	
VOH(AC)	AC output high measurement level (for output SR)	VTT + 0.1 x VDDQ	V	1
VOL(AC)	AC output low measurement level (for output SR)	VTT - 0.1 x VDDQ	V	1

Note:

1. The swing of ± 0.1 × VDDQ is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to VTT = VDDQ/2.

Table 4-30 Differential AC and DC Output Levels

Symbol	Parameter	Values	Unit	Note
VOHdiff(AC)	AC differential output high measurement level (for output SR	+ 0.2 x VDDQ	V	1
VOLdiff(AC)	AC differential output low measurement level (for output SR)	- 0.2 x VDDQ	V	1

Note:

1. The swing of ± 0.2 × VDDQ is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to VTT = VDDQ/2 at each of the differential outputs.

- Single Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC) for single ended signals as shown in Table.

Table 4-31 Output Slew Rate Definition (Single-ended)

Description	Measured		Defined by
	From	To	
Single-ended output slew rate for rising edge	VOL(AC)	VOH(AC)	[VOH(AC) - VOL(AC)] / DeltaTRse
Single-ended output slew rate for falling edge	VOH(AC)	VOL(AC)	[VOH(AC) - VOL(AC)] / DeltaTFse

Note:

1. Output slew rate is verified by design and characterization, and may not be subject to production test.

Table 4-32 Output Slew Rate (Single-ended)

Symbol	Parameter	DDR3-1866/1600		Unit
		Min.	Max.	
SRQse	Single-ended Output Slew Rate	1.75	5	V/ns

Description:

SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

se: Single-ended Signals

For Ron = RZQ/7 setting

Note:

1. In two cases, a maximum slew rate of 6V/ns applies for a single DQ signal within a byte lane.
   Case 1 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are static (i.e. they stay at either high or low).
   Case 2 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are switching into the opposite direction (i.e. from low to high or high to low respectively).F or the remaining DQ signal switching into the opposite direction, the regular maximum limit of 5 V/ns applies.

- Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as shown in Table.

Table 4-33 Output Slew Rate Definition (Differential)

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	VOLdiff(AC)	VOHdiff(AC)	[VOHdiff(AC) - VOLdiff(AC)] / DeltaTRdiff
Differential output slew rate for falling edge	VOHdiff(AC)	VOLdiff(AC)	[VOHdiff(AC) - VOLdiff(AC)] / DeltaTFdiff

Note:

1. Output slew rate is verified by design and characterization, and may not be subject to production test.

Table 4-34 Output Slew Rate (Differential)

Symbol	Parameter	DDR3-1866/1600		Unit
		Min.	Max.	
SRQdiff	Differential Output Slew Rate	3.5	12	V/ns

Description:
SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
diff: Differential Signals
For Ron = RZQ/7 setting

Reference Load for AC Timing and Output Slew Rate

The following figure represents the effective reference load of 25 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

Figure 4-21 Reference Load for AC Timing and Output Slew Rate

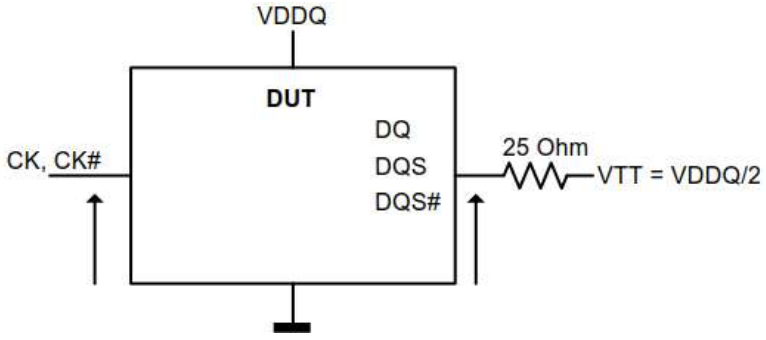


Table 4-35 AC Overshoot/Undershoot Specification for Address and Control Pins

Parameter	DDR3-1866	DDR3-1600	Unit
Maximum peak amplitude allowed for overshoot area.	0.4	0.4	V
Maximum peak amplitude allowed for undershoot area.	0.4	0.4	V
Maximum overshoot area above VDD	0.33	0.4	V-ns
Maximum undershoot area below VSS	0.33	0.4	V-ns

Figure 4-22 AC Overshoot/Undershoot Specification for Address and Control Pins

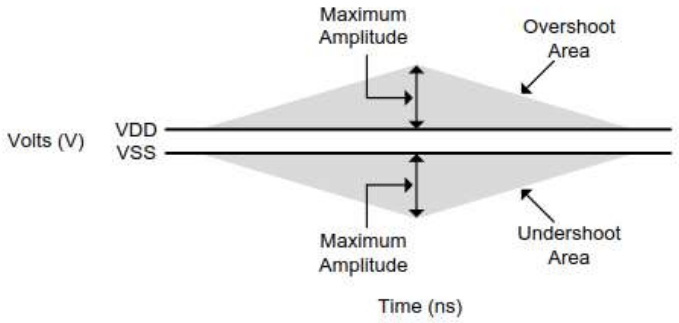
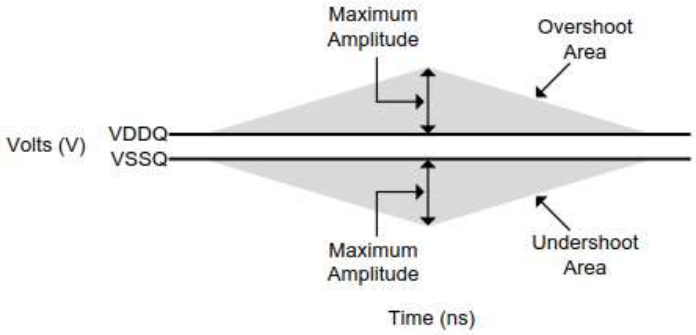


Table 4-36 AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask

Parameter	DDR3-1866	DDR3-1600	Unit
Maximum peak amplitude allowed for overshoot area.	0.4	0.4	V
Maximum peak amplitude allowed for undershoot area.	0.4	0.4	V
MMaximum overshoot area above VDD	0.13	0.15	V-ns
Maximum undershoot area below VSS	0.13	0.15	V-ns

Figure 4-23 Clock, Data, Strobe and Mask Overshoot and Undershoot Definition



- Address / Command Setup, Hold and Derating

For all input signals the total tIS (setup time) and tIH (hold time) required is calculated by adding the data sheet tIS(base) and tIH(base) and tIH(base) value to the delta tIS and delta tIH derating value respectively.

Example: tIS (total setup time) = tIS(base) + delta tIS.

Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of Vref(dc) and the first crossing of VIH(ac)min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of Vref(dc) and the first crossing of VIL(ac)max. If the actual signal is always earlier than the nominal slew rate line between shaded 'Vref(dc) to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded 'Vref(dc) to ac region', the slew rate of the tangent line to the actual signal from the ac level to dc level is used for derating value.

Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(dc)max and the first crossing of Vref(dc). Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(dc)min and the first crossing of Vref(dc). If the actual signal is always later than the nominal slew rate line between shaded 'dc to Vref(dc) region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to Vref(dc) region', the slew rate of a tangent line to the actual signal from the dc level to Vref(dc) level is used for derating value.

For a valid transition the input signal has to remain above/below VIH/IL(ac) for some time tVAC.

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached VIH/IL(ac) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL(ac).

For slew rates in between the values listed in the following tables, the derating values may be obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

Table 4-37 AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask

Symbol	Reference	DDR3-1866	DDR3-1600	Unit
tIS(base) AC160	VIH/L(ac)	60	80	ps
tIS(base) AC1500	VIH/L(ac)	185	205	ps
tIS(base) AC125	VIH/L(ac)	-	-	ps
tIH(base) DC90	VIH/L(dc)	130	150	ps

Notes:

1. ac/dc referenced for 1V/ns Address/Command slew rate and 2 V/ns differential CK-CK# slew rate.
2. The tIS(base) AC1500 specifications are adjusted from the tIS(base) AC160 specification by adding an additional 100ps of derating to accommodate for the lower alternate threshold of 135 mV and another 25 ps to account for the earlier reference point [(160 mv - 135 mV) / 1 V/ns].
3. The tIS(base) AC125 specifications are adjusted from the tIS(base) AC1500 specification by adding an additional 75ps of derating to accommodate for the lower alternate threshold of 135 mV and another 10 ps to account for the earlier reference point [(135 mv - 125 mV) / 1 V/ns].

Table 4-38 Derating values DDR3-1866/1600 tIS/tIH – (AC160)

△tIS, △tIH derating in [ps] AC/DC based AC160 Threshold -> VIH(ac)=VREF(dc)+160mV, VIL(ac)=VREF(dc)-160mV																
CMD/ ADD Slew Rate V/ns	CK, CK# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	Δ_tIS	Δ_tIH	Δ_tIS	Δ_tIH	Δ_tIS	Δ_tIH	Δ_tIS	Δ_tIH	Δ_tIS	Δ_tIH	Δ_tIS	Δ_tIH	Δ_tIS	Δ_tIH	Δ_tIS	Δ_tIH
2.0	80	45	80	45	80	45	88	53	96	61	104	69	112	79	120	95
1.5	53	30	53	30	53	30	61	38	69	46	77	54	85	64	93	80
1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
0.9	–1	–3	–1	–3	–1	–3	7	5	15	13	23	21	31	31	39	47
0.8	–3	–8	–3	–8	–3	–8	5	1	13	9	21	17	29	27	37	43
0.7	–5	–13	–5	–13	–5	–13	3	–5	11	3	19	11	27	21	35	37
0.6	–8	–20	–8	–20	–8	–20	0	–12	8	–4	16	4	24	14	32	30
0.5	–20	–30	–20	–30	–20	–30	–12	–22	–4	–14	4	–6	12	4	20	20
0.4	–40	–45	–40	–45	–40	–45	–32	–37	–24	–29	–16	–21	–8	–11	0	5

- Data Setup, Hold, and Slew Rate De-rating

For all input signals the total tDS (setup time) and tDH (hold time) required is calculated by adding the data sheet tDS(base) and tDH(base) value to the Δ tDS and Δ tDH derating value respectively. Example: tDS (total setup time) = tDS(base) + Δ tDS.

Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of Vref(dc) and the first crossing of VIH(ac)min. Setup (tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of Vref(dc) and the first crossing of VIL(ac)max. If the actual signal is always earlier than the nominal slew rate line between shaded 'Vref(dc) to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded 'Vref(dc) to ac region', the slew rate of the tangent line to the actual signal from the ac level to dc level is used for derating value.

Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(dc)max and the first crossing of Vref(dc). Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(dc)min and the first crossing of Vref(dc). If the actual signal is always later than the nominal slew rate line between shaded 'dc level to Vref(dc) region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to Vref(dc) region', the slew rate of a tangent line to the actual signal from the dc level to Vref(dc) level is used for derating value.

For a valid transition the input signal has to remain above/below VIH/IL(ac) for some time tVAC.

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached VIH/IL(ac) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL(ac).

For slew rates in between the values listed in the following tables, the derating values may be obtained by linear interpolation.

These values are typically not subject to production test. They are verified by designn and characterization.

Table 4-40 Data Setup and Hold Base

Symbol	Reference	DDR3-1866	DDR3-1600	Unit	Note
t_{DS}(base) AC1500	VIH/L(ac)	25	45	ps	1
t_{DS}(base) AC140	VIH/L(ac)			ps	2
t_{DH}(base) DC90	VIH/L(ac)	55	75	ps	1
t_{DH}(base) DC90	VIH/L(dc)			ps	2

Notes:

1. ac/dc referenced for 1V/ns DQ- slew rate and 2 V/ns differential DQS slew rate
2. ac/dc referenced for 2V/ns DQ- slew rate and 4 V/ns differential DQS slew rate.

Table 4-41 Derating values for DDR3-1866/1600 tDS/tDH – (AC150)

△tDS, △tDH derating in [ps] AC/DC based																
DQ Slew rate (V/nS)	DQS, DQS# Differential Slew Rate															
	4.0 V/nS		3.0 V/nS		2.0 V/nS		1.8 V/nS		1.6 V/nS		1.4 V/nS		1.2 V/nS		1.0 V/nS	
	Δ_tDS	Δ_tDH	Δ_tDS	Δ_tDH	Δ_tDS	Δ_tDH	Δ_tDS	Δ_tDH	Δ_tDS	Δ_tDH	Δ_tDS	Δ_tDH	Δ_tDS	Δ_tDH	Δ_tDS	Δ_tDH
2.0	68	45	68	45	68	45	-	-	-	-	-	-	-	-	-	-
1.5	45	30	45	30	45	30	53	38	-	-	-	-	-	-	-	-
1.0	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
0.9	-	-	2	-3	2	-3	10	5	18	13	26	21	-	-	-	-
0.8	-	-	-	-	3	-8	11	1	19	9	27	17	35	27	-	-
0.7	-	-	-	-	-	-	14	-5	22	3	30	11	38	21	46	37
0.6	-	-	-	-	-	-	-	-	25	-4	33	4	41	14	49	30
0.5	-	-	-	-	-	-	-	-	-	-	29	-6	37	4	45	20
0.4	-	-	-	-	-	-	-	-	-	-	-	-	30	-11	38	5

1.5V DDR3 SDRAM VDD/VDDQ Requirements

Table 4-42 Input/Output Functional

Symbol	Type	Function
VDD	Supply	Power Supply: DDR3 operation = 1.425V to 1.575V
VDDQ	Supply	DQ Power Supply: DDR3 operation = 1.425V to 1.575V

Table 4-43 Recommended DC Operating Conditions - DDR3 (1.5V) operation

Symbol	Parameter	Min.	Type.	Max.	Unit	Note
VDD	Power supply voltage	1.425	1.5	1.575	V	1-4
VDDQ	Power supply voltage for outpu	1.425	1.5	1.575	V	1-4

Notes:

1. Maximum DC value may not be greater than 1.575V. The DC value is the linear average of VDD/VDDQ(t) over a very long period of time (e.g., 1 sec).
2. Once initialized for DDR3 operation, DDR3 operation may only be used if the device is in reset while VDD and VDDQ are changed for DDR3 operation (see VDDQ/VDDQ Voltage Switch Between DDR3 and DDR3).
3. Once initialized for DDR3 operation, DDR3 operation may only be used if the device is in reset while VDD and VDDQ are changed for DDR3 operation (see VDDQ/VDDQ Voltage Switch Between DDR3 and DDR3).

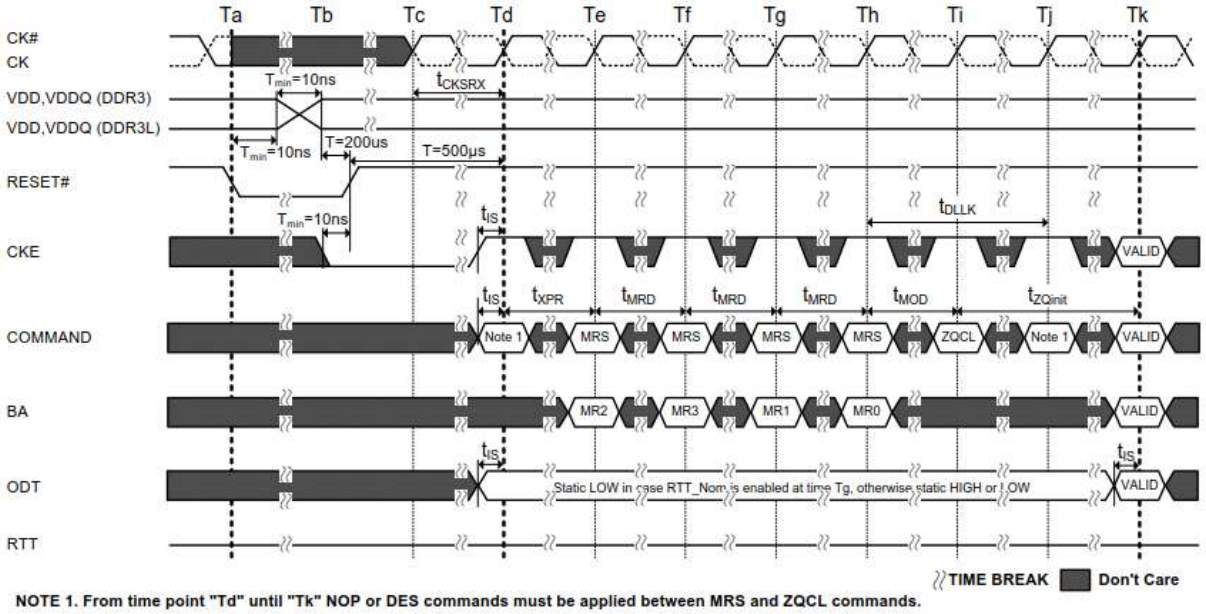
Table 4-44 Recommended DC Operating Conditions - DDR3 (1.5V) operation

Symbol	Parameter	Min.	Type.	Max.	Unit	Note
VDD	Power supply voltage	1.425	1.5	1.575	V	1-4
VDDQ	Power supply voltage for outpu	1.425	1.5	1.575	V	1-4

Notes:

1. If maximum limit is exceeded, input levels shall be governed by DDR3 specifications.
2. Under 1.5V operation, this DDR3 device operates to the DDR3 specifications under the same speed timings as defined for this device.
3. Once initialized for DDR3 operation, DDR3 operation may only be used if the device is in reset while VDD and VDDQ are changed for DDR3 operation (see VDDQ/VDDQ Voltage Switch Between DDR3 and DDR3).

Figure 4-24 MPR Block Diagram VDDQ/VDDQ Voltage Switch Between DDR3 and DDR3



NOTE 1. From time point "Td" until "Tk" NOP or DES commands must be applied between MRS and ZQCL commands.

Timing Waveforms

Figure 4-25 MPR Readout of predefined pattern,BL8 fixed burst order, single readout

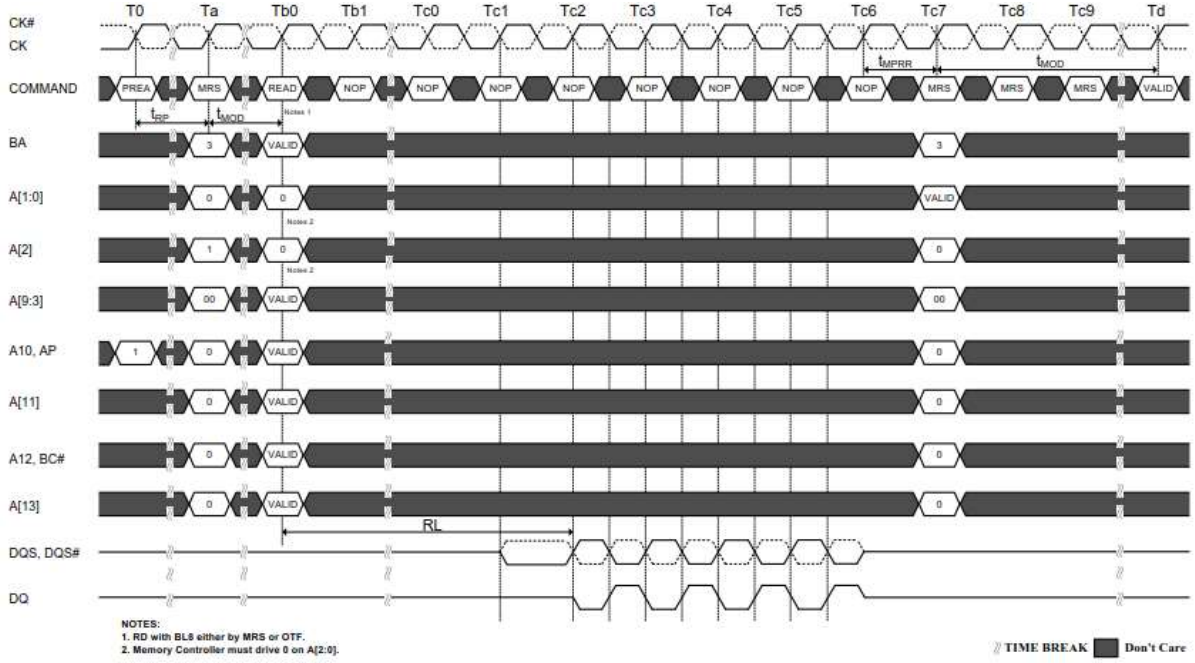


Figure 4-26 MPR Readout of predefined pattern, BL8 fixed burst order, back to back radout

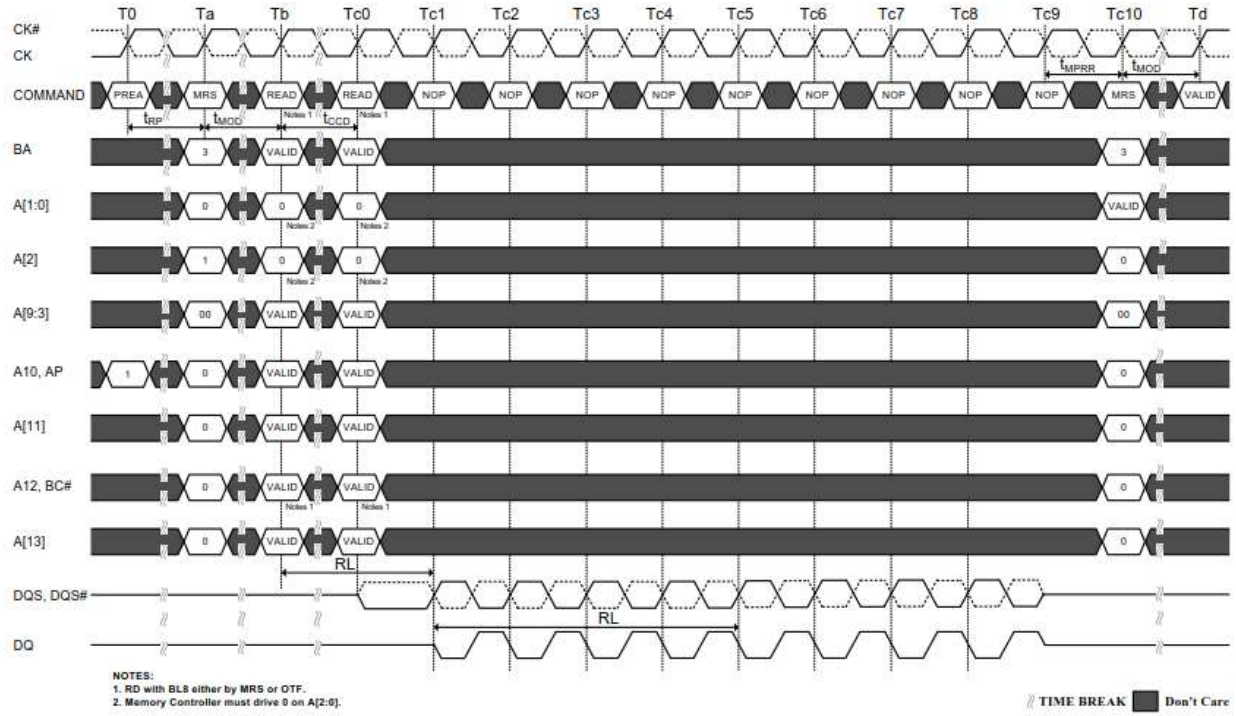


Figure 4-27 MPR Readout of predefined pattern, BC4 lower nibble then upper nibble

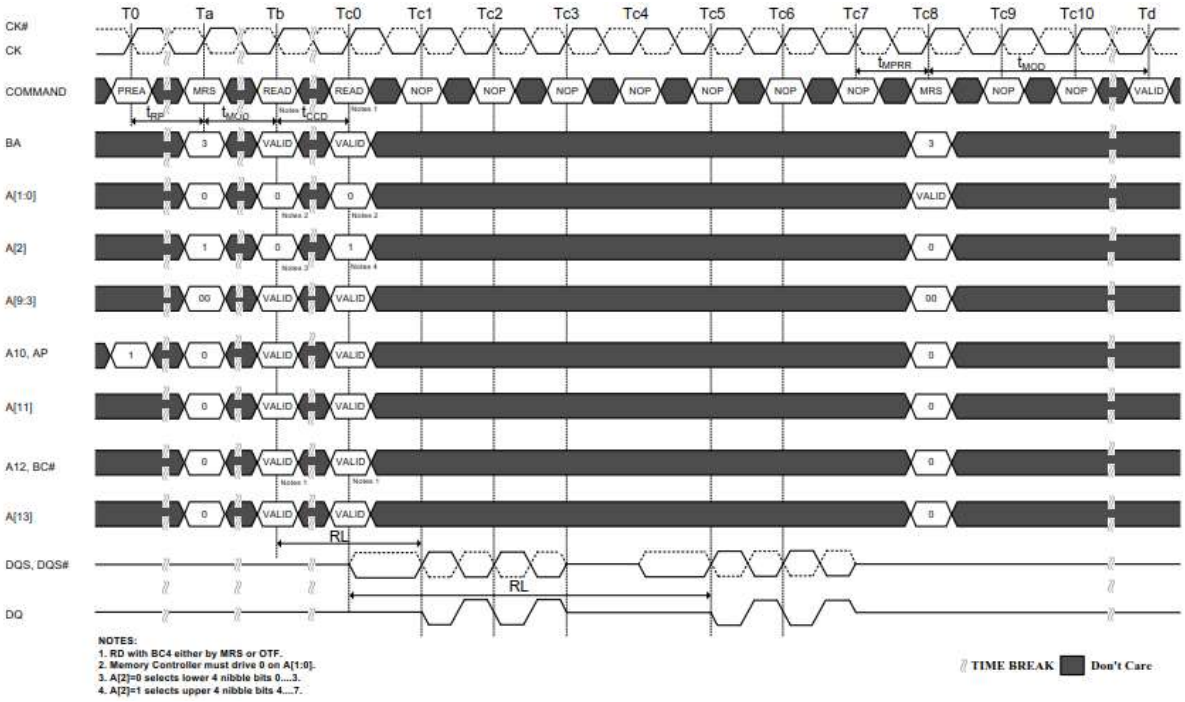


Figure 4-28 MPR Readout of predefined pattern, BC4 upper nibble then lower nibble

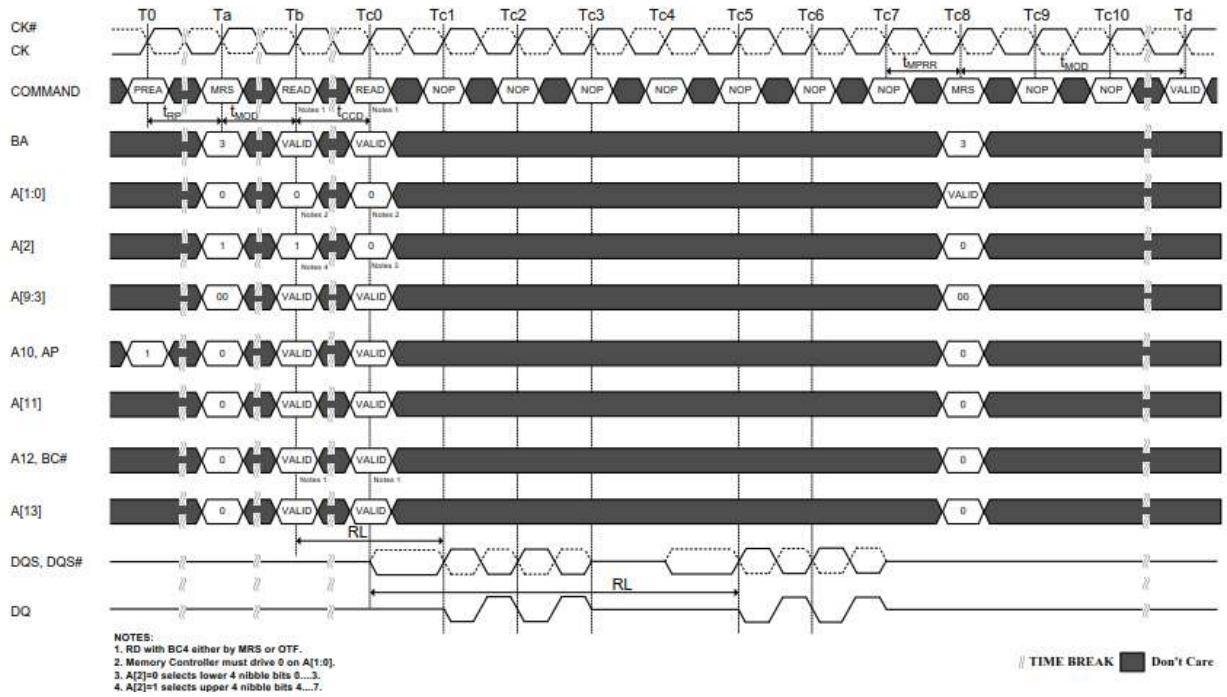


Figure 4-29 READ (BL8) to READ (BL8)

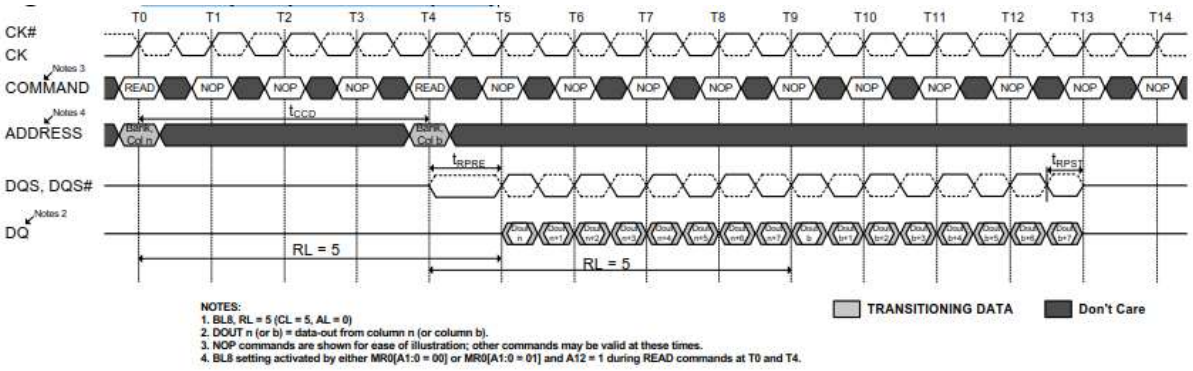


Figure 4-30 Nonconsecutive READ (BL8) to READ (BL8)

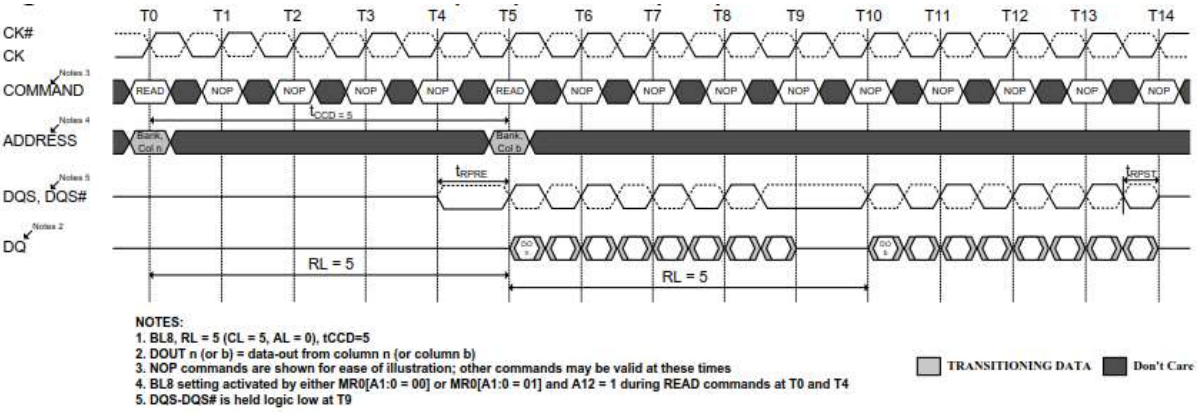
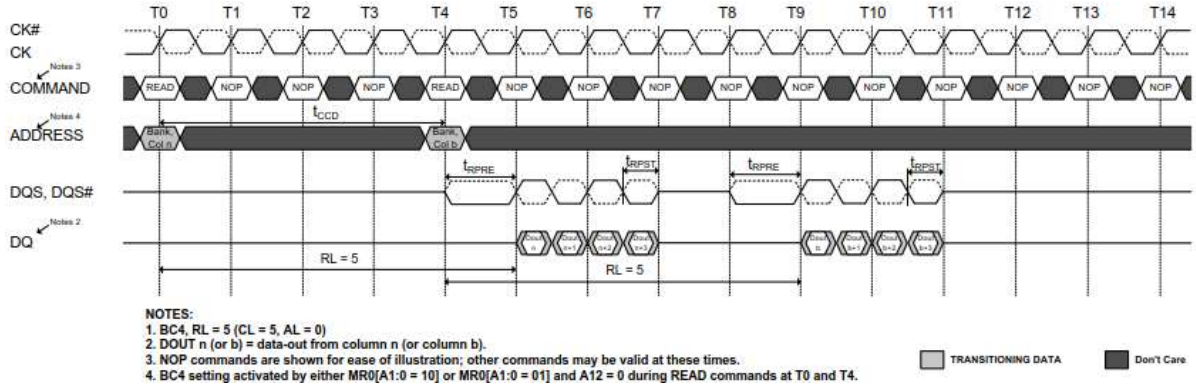
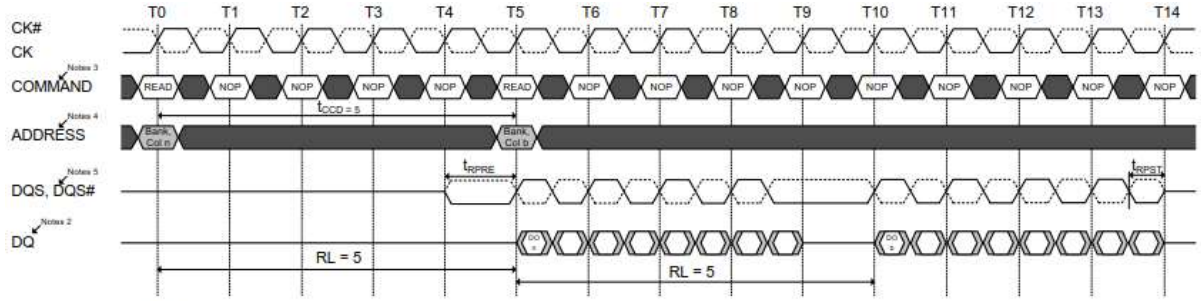


Figure 4-31 READ (BL4) to READ (BL4)



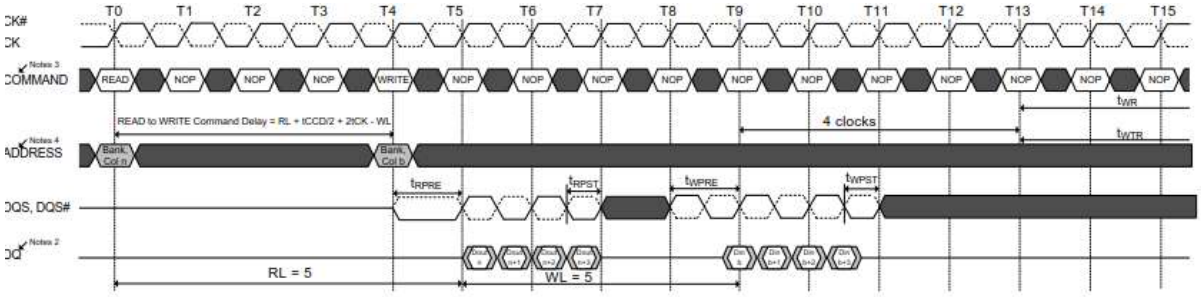
NOTES:
1. BC4, RL = 5 (CL = 5, AL = 0)
2. DOUT n (or b) = data-out from column n (or column b).
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by either MR0[A1:0 = 10] or MR0[A1:0 = 01] and A12 = 0 during READ commands at T0 and T4.

Figure 4-32 READ (BL8) to WRITE (BL8)



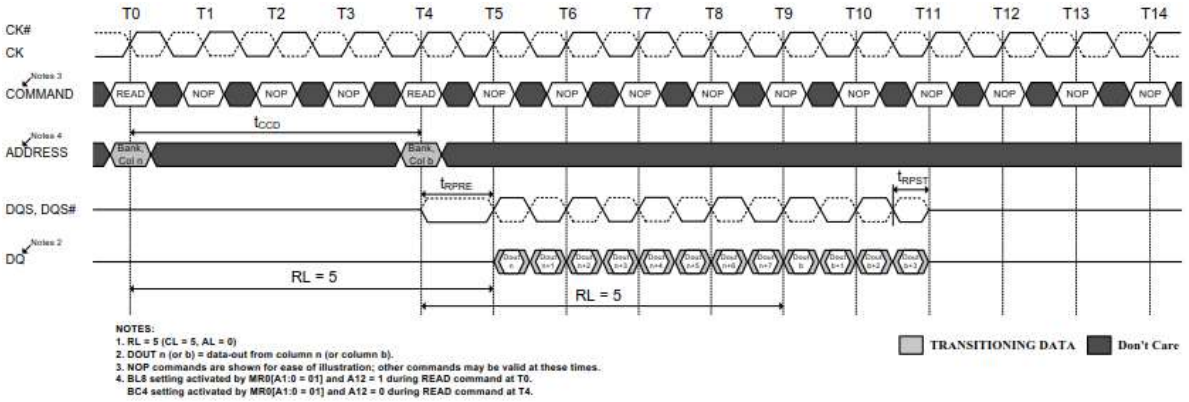
NOTES:
1. BL8, RL = 5 (CL = 5, AL = 0), tCCD=5
2. DOUT n (or b) = data-out from column n (or column b)
3. NOP commands are shown for ease of illustration; other commands may be valid at these times
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ commands at T0 and T4
5. DQS-DQS# is held logic low at T9

Figure 4-33 READ (BL4) to WRITE (BL4) OTF



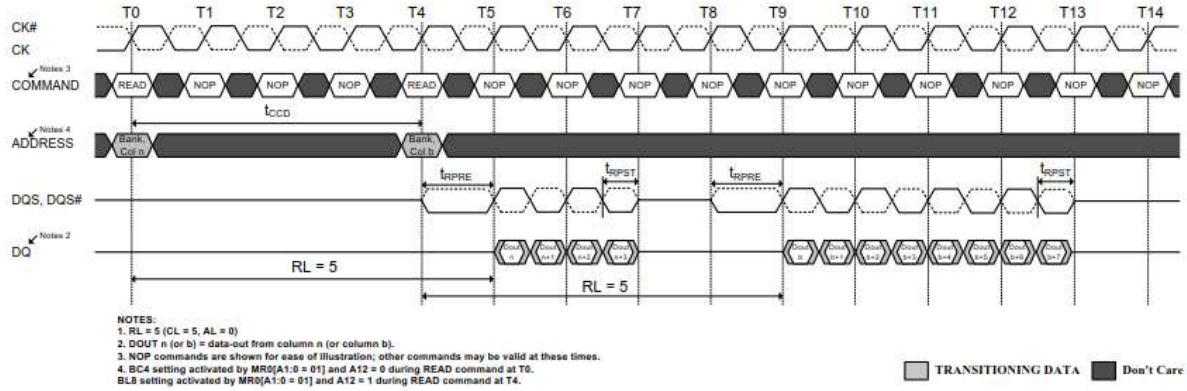
NOTES:
1. BC4, RL = 5 (CL = 5, AL = 0), WL = 5 (CWL = 5, AL = 0)
2. DOUT n = data-out from column, DIN b = data-in from column b.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:0 = 01] and A12 = 0 during READ command at T0 and WRITE command at T4.

Figure 4-34 READ (BL8) to READ (BL4) OTF



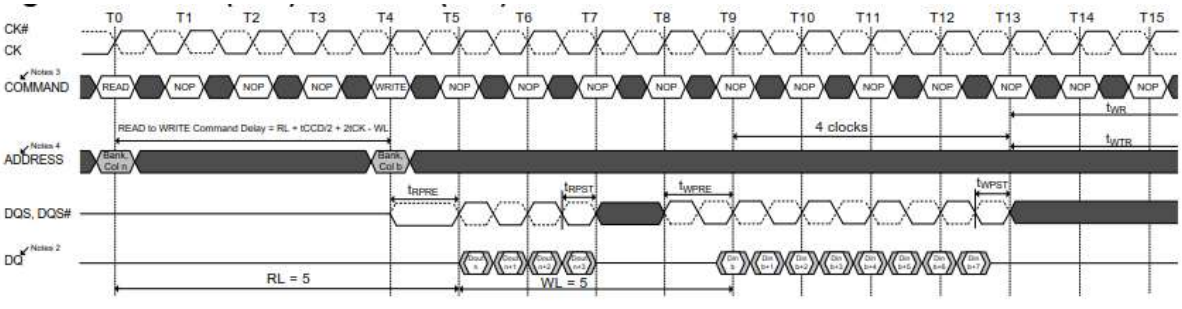
NOTES:
1. RL = 5 (CL = 5, AL = 0)
2. DOUT n (or b) = data-out from column n (or column b).
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0[A1:0 = 01] and A12 = 1 during READ command at T0.
   BC4 setting activated by MR0[A1:0 = 01] and A12 = 0 during READ command at T4.

Figure 4-35 READ (BL4) to READ (BL8) OTF



NOTES:
1. RL = 5 (CL = 5, AL = 0)
2. DOUT n (or b) = data-out from column n (or column b).
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:0 = 01] and A12 = 0 during READ command at T0.
   BL8 setting activated by MR0[A1:0 = 01] and A12 = 1 during READ command at T4.

Figure 4-36 READ (BC4) to WRITE (BL8) OTF



NOTES:
1. BC4, RL = 5 (CL = 5, AL = 0), WL = 5 (CWL = 5, AL = 0)
2. DOUT n = data-out from column, DIN b = data-in from column b.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:0 = 01] and A12 = 0 during READ command at T0 and WRITE command at T4.

Figure 4-37 READ (BL8) to WRITE (BL4) OTF

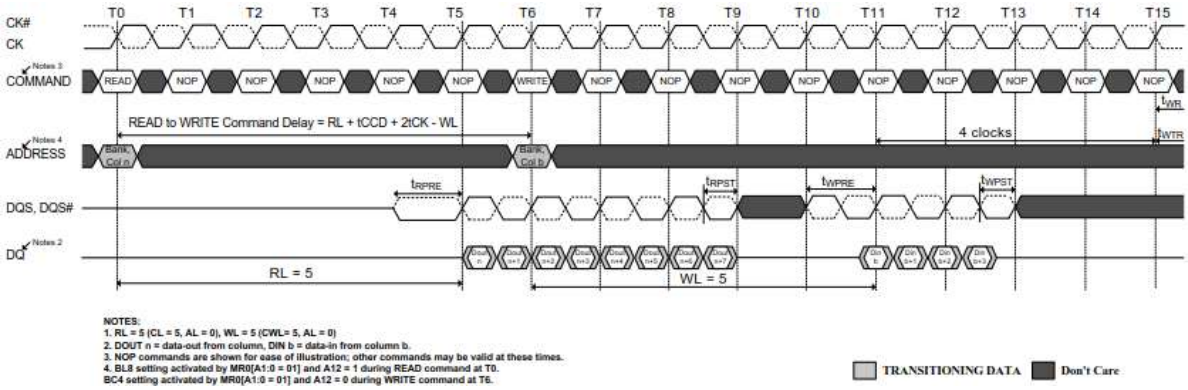


Figure 4-38 READ to PRECHARGE, RL = 5, AL = 0, CL = 5, tRTP = 4, tRP = 5

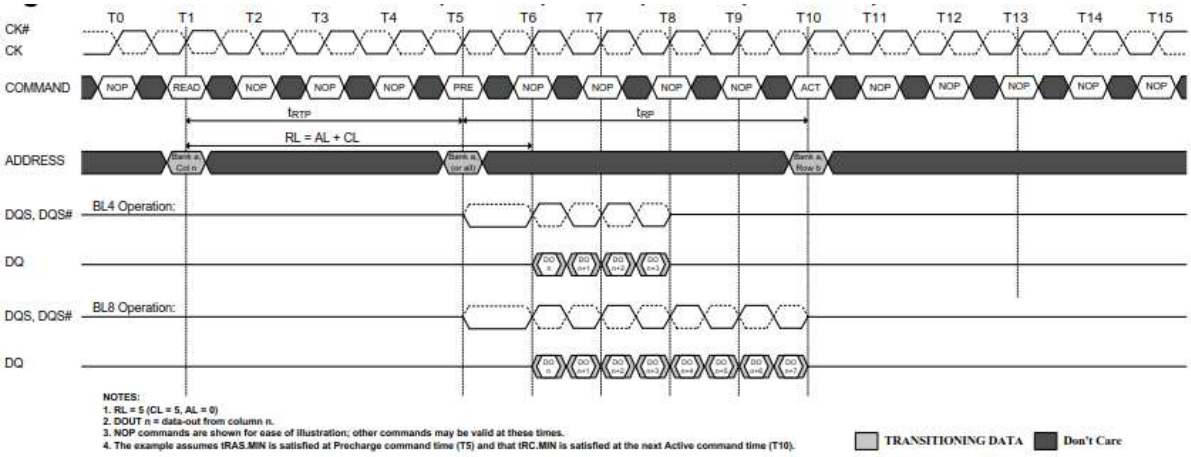


Figure 4-39 READ to PRECHARGE, RL = 8, AL = CL-2, CL = 5, tRTP = 6, tRP = 5

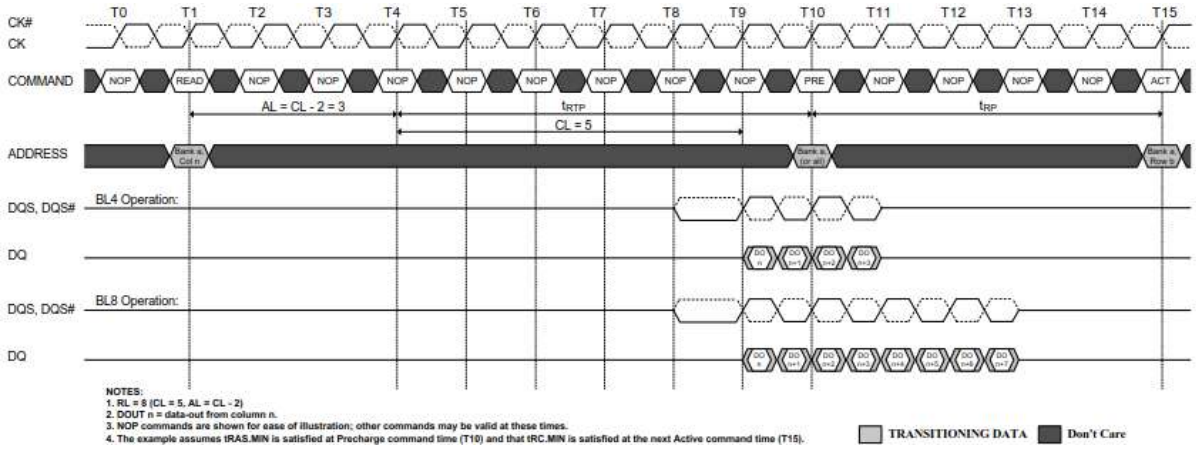


Figure 4-40 Write Timing Definition and parameters

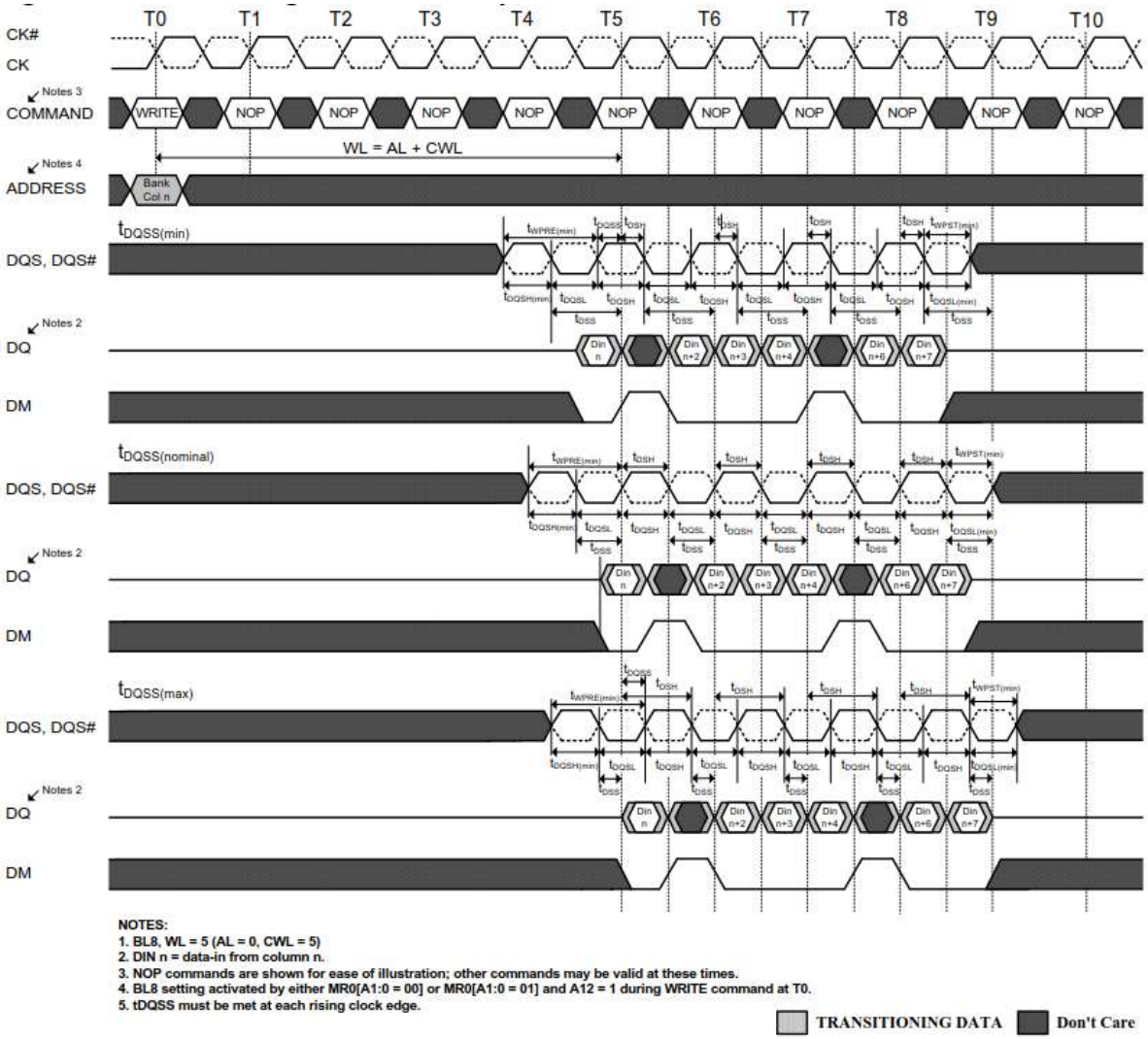


Figure 4-41 WRITE Burst Operation WL = 5 (AL = 0, CWL = 5, BL8)

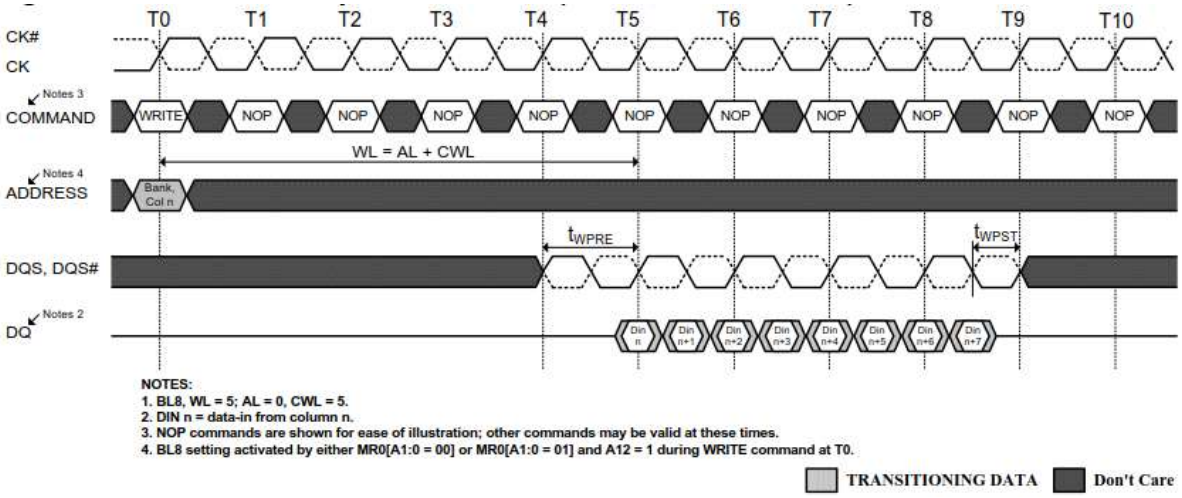
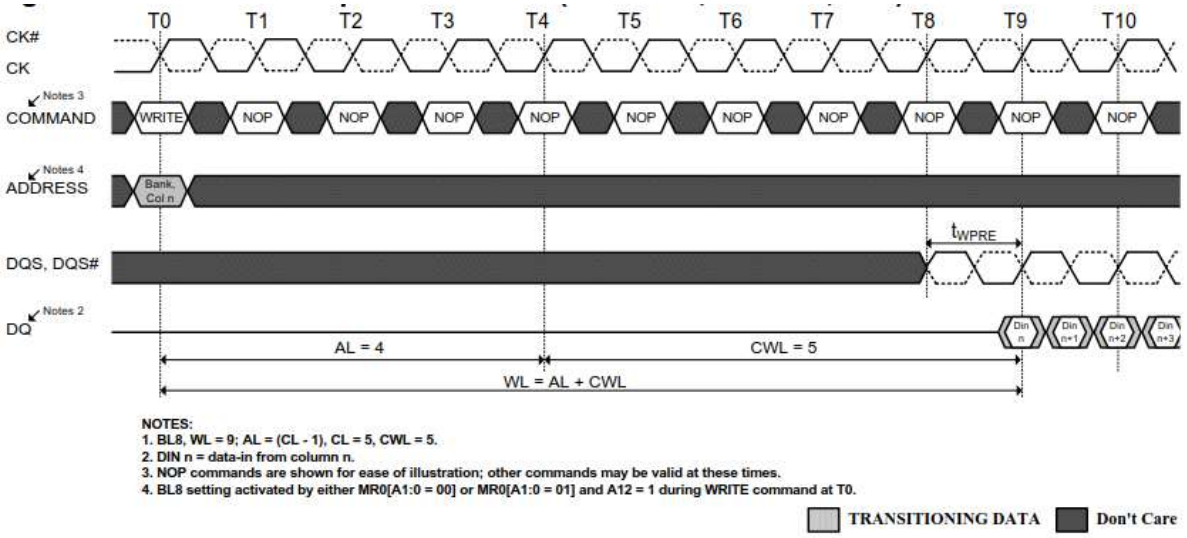


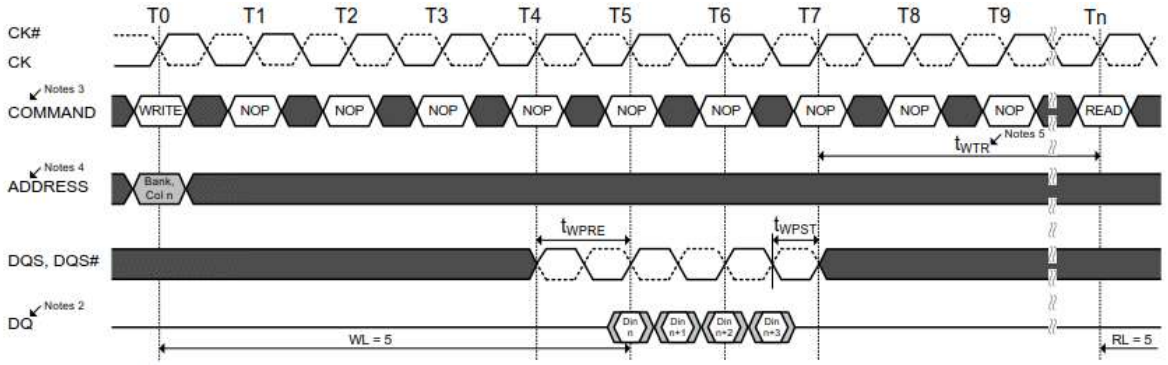
Figure 4-42 WRITE Burst Operation WL = 9 (AL = CL-1, CWL = 5, BL8)



NOTES:
1. BL8, WL = 9; AL = (CL - 1), CL = 5, CWL = 5.
2. DIN n = data-in from column n.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during WRITE command at T0.

TRANSITIONING DATA Don't Care

Figure 4-43 WRITE (BC4) to READ (BC4) operation



NOTES:
1. BC4, WL = 5, RL = 5.
2. DIN n = data-in from column n.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:0 = 10] during WRITE command at T0 and READ command at Tn.
5. tWTR controls the write to read delay to the same device and starts with the first rising clock edge after the last write data shown at T7.

TIME BREAK TRANSITIONING DATA Don't Care

Figure 4-44 WRITE (BC4) to Precharge Operation

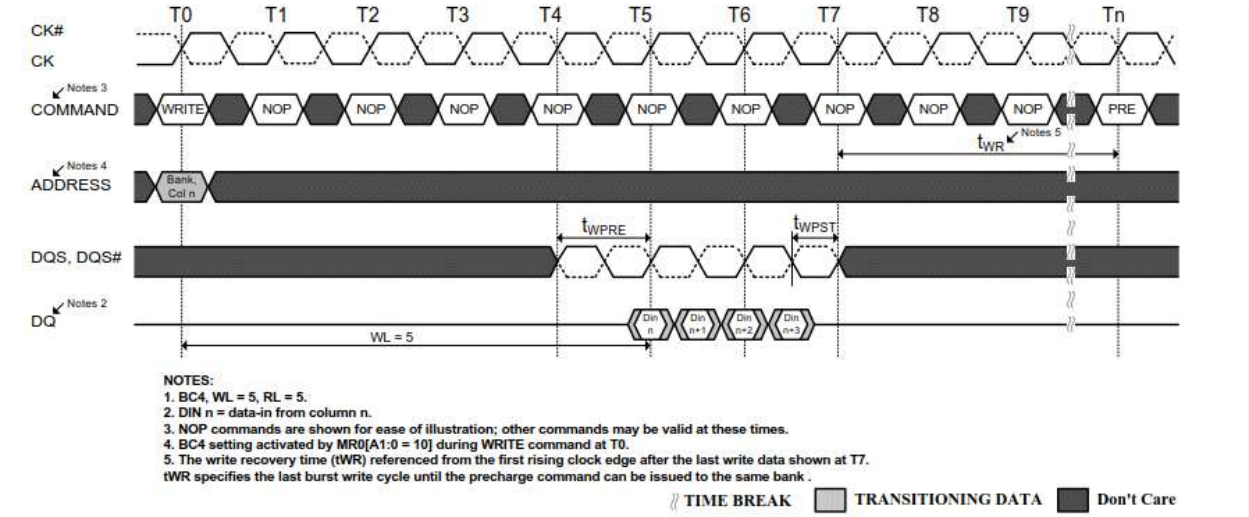


Figure 4-45 WRITE (BC4) OTF to precharge operation

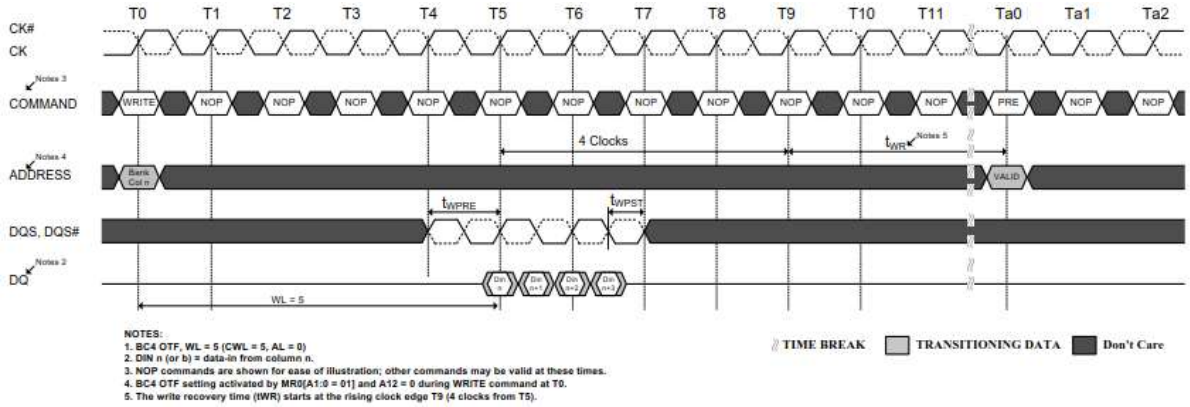


Figure 4-46 WRITE (BC8) to WRITE (BC8)

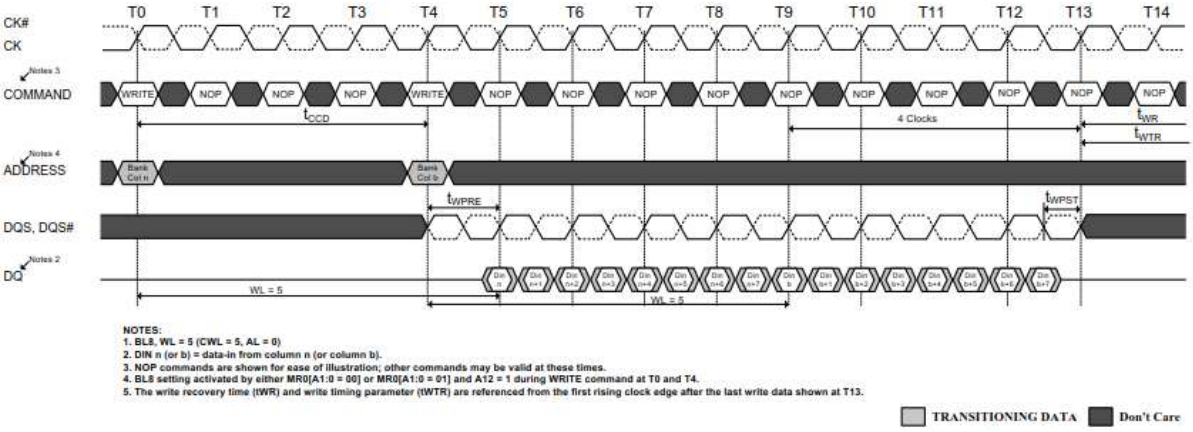


Figure 4-47 WRITE (BC4) to WRITE (BC4) OTF

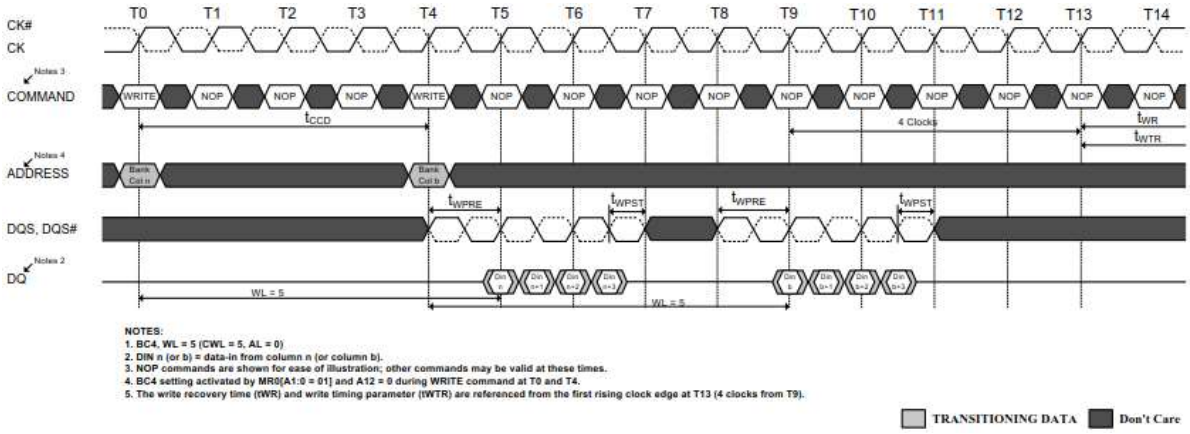


Figure 4-48 WRITE (BC8) to READ (BC4, BC8) OTF

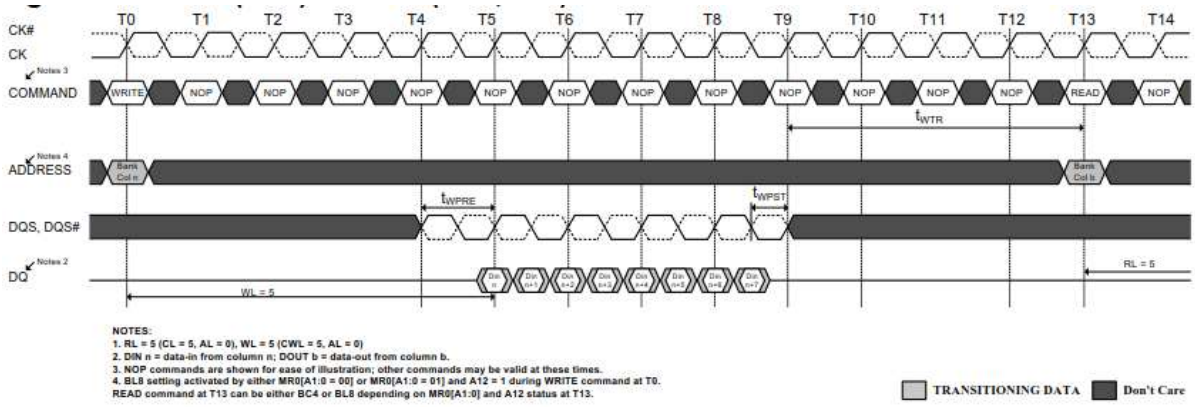


Figure 4-49 WRITE (BC4) to READ (BC4, BC8) OTF

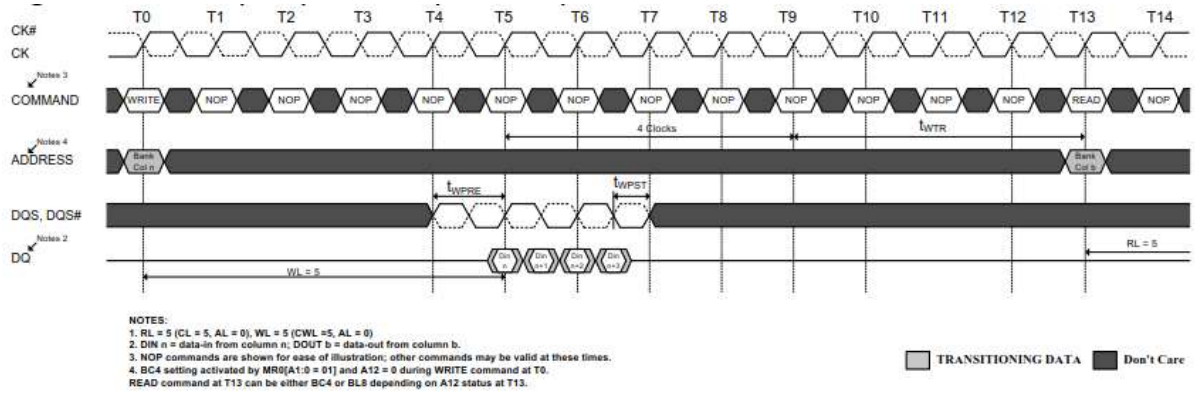


Figure 4-50 WRITE (BC4) to READ (BC4)

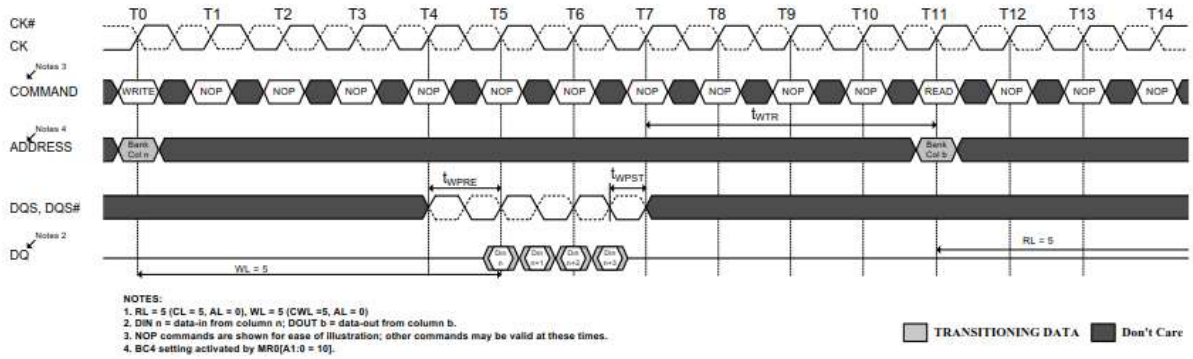


Figure 4-51 WRITE (BC8) to WRITE (BC4) OTF

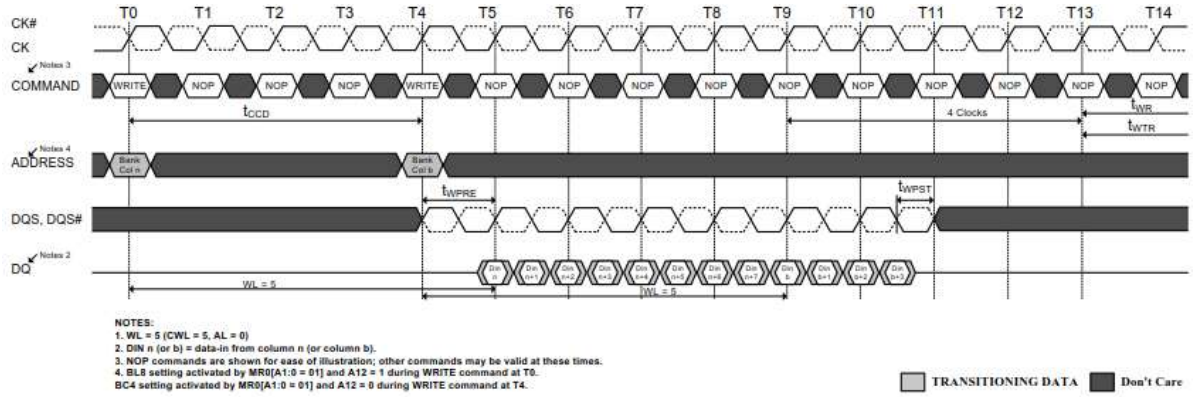


Figure 4-52 WRITE (BC4) to WRITE (BC8) OTF

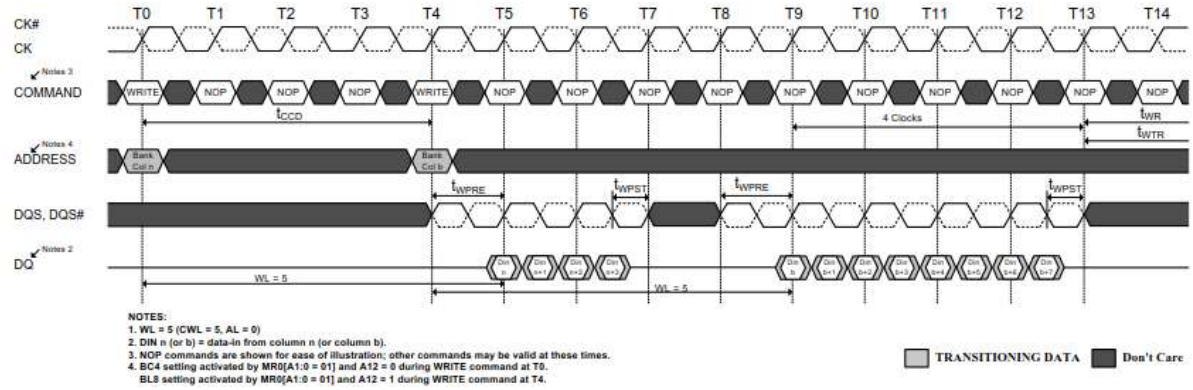


Figure 4-53 Refresh Command Timing

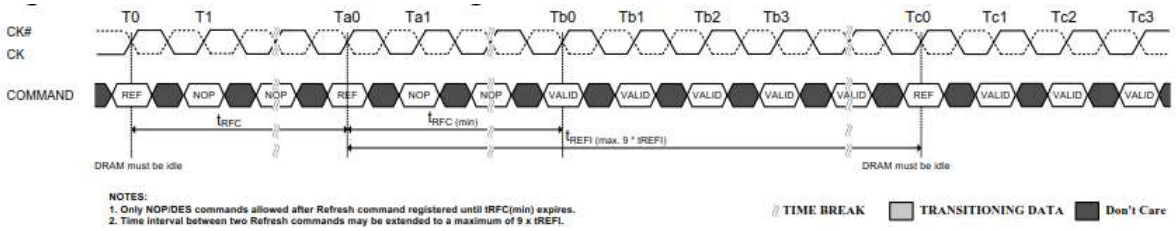


Figure 4-54 Self-Refresh Entry/Exit Timing

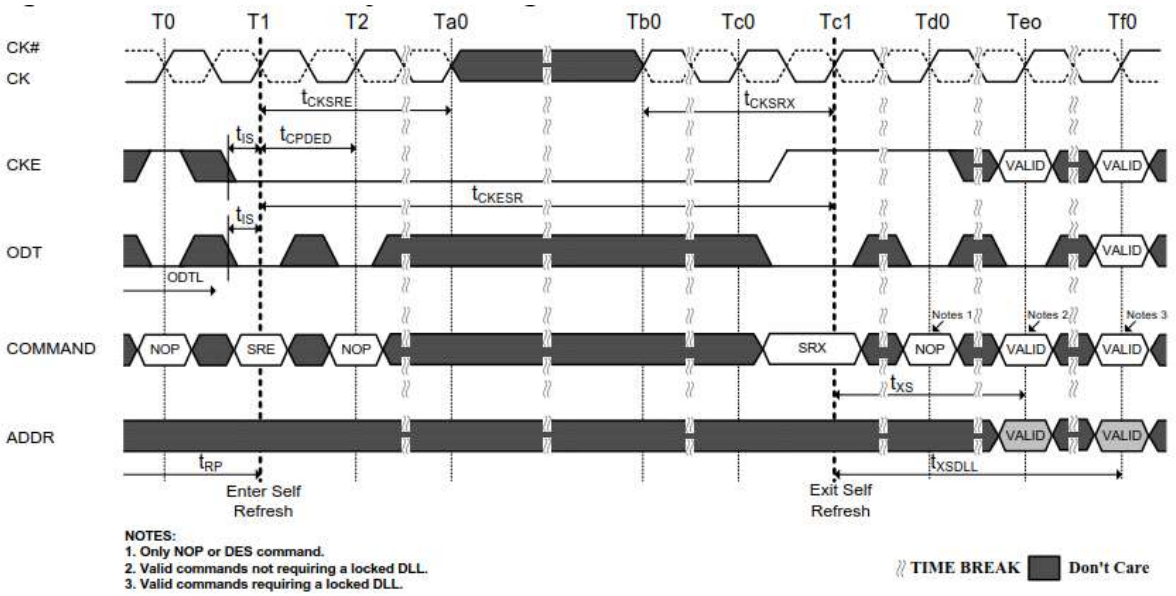


Figure 4-55 Active Power-Down Entry and Exit Timing Diagram

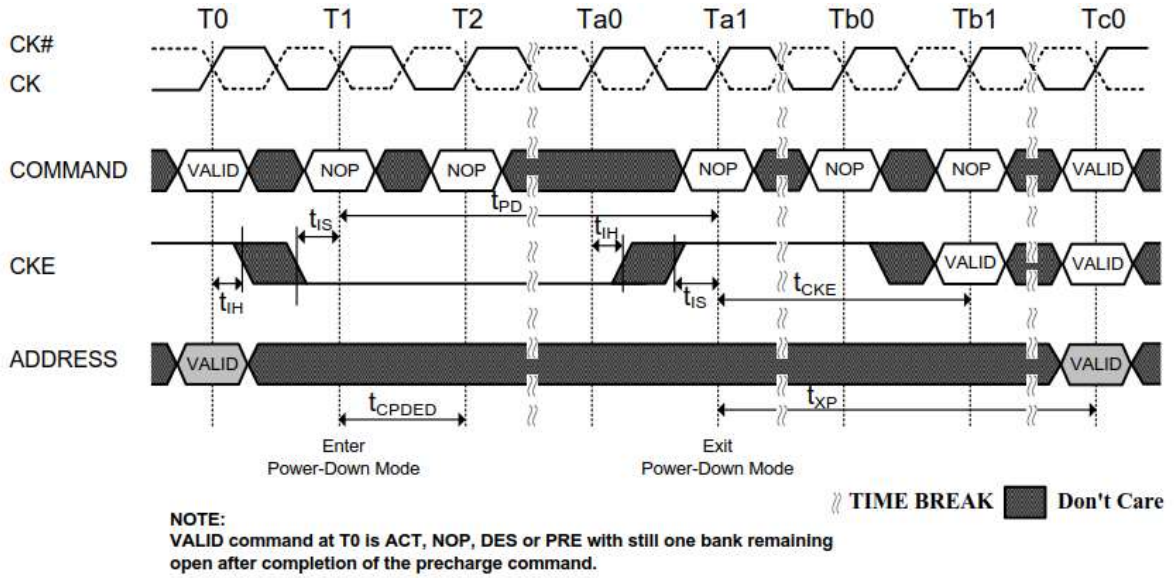


Figure 4-56 Power-Down Entry after Read and Read with Auto Precharge

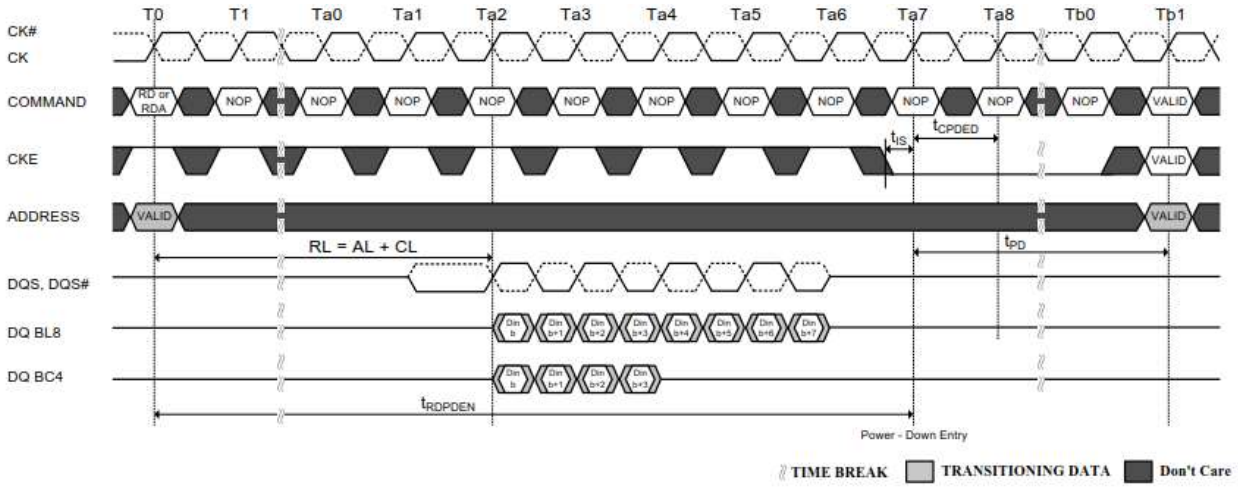


Figure 4-57 Power-Down Entry after Write with Auto Precharge

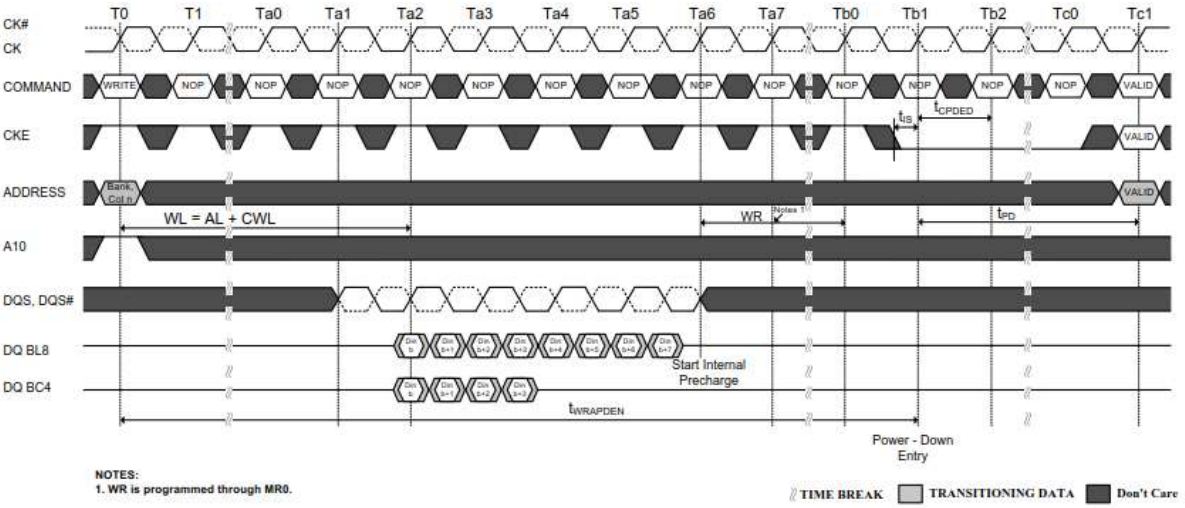


Figure 4-58 Power-Down Entry after Write

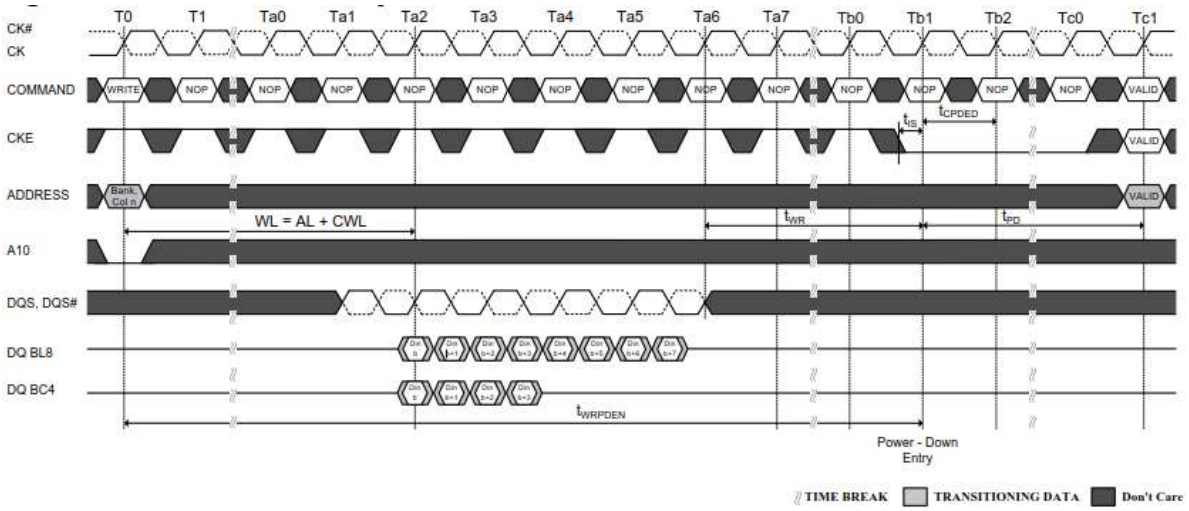


Figure 4-59 Precharge Power-Down (Fast Exit Mode) Entry and Exit

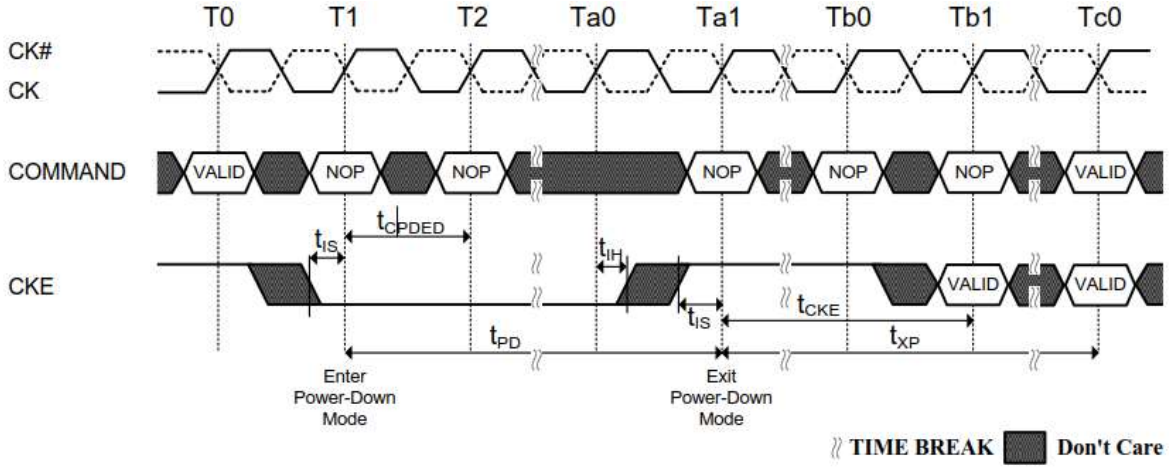


Figure 4-60 Precharge Power-Down (Slow Exit Mode) Entry and Exit

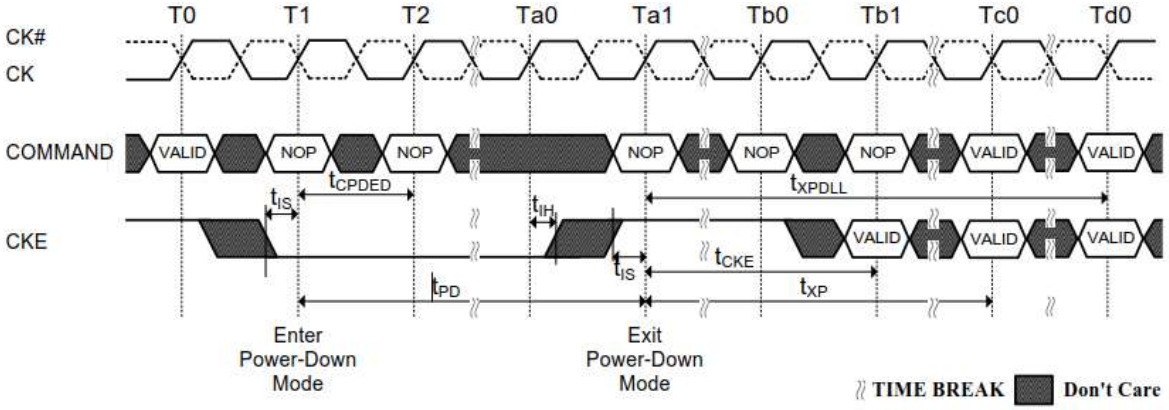


Figure 4-61 Refresh Command to Power-Down Entry

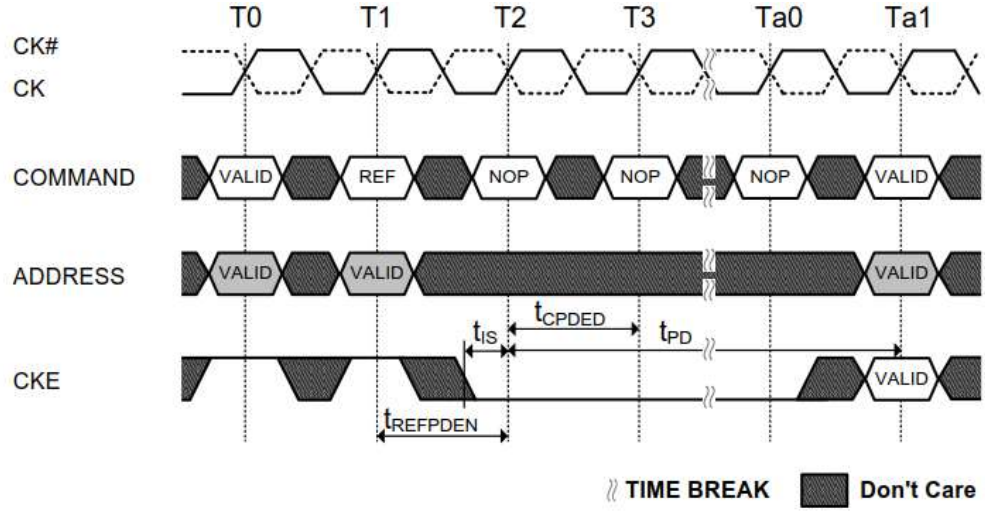


Figure 4-62 Active Command to Power-Down Entry

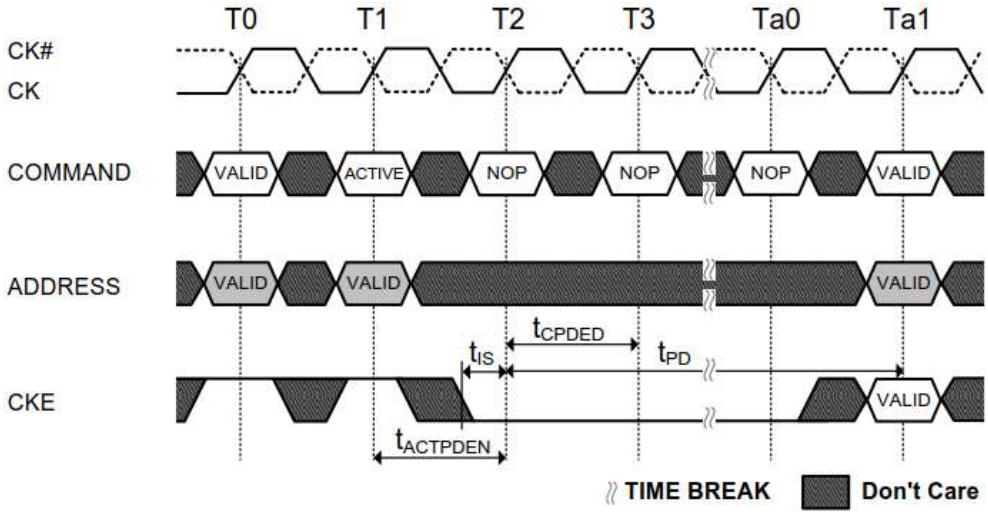


Figure 4-63 Precharge, Precharge all command to Power-Down Entry

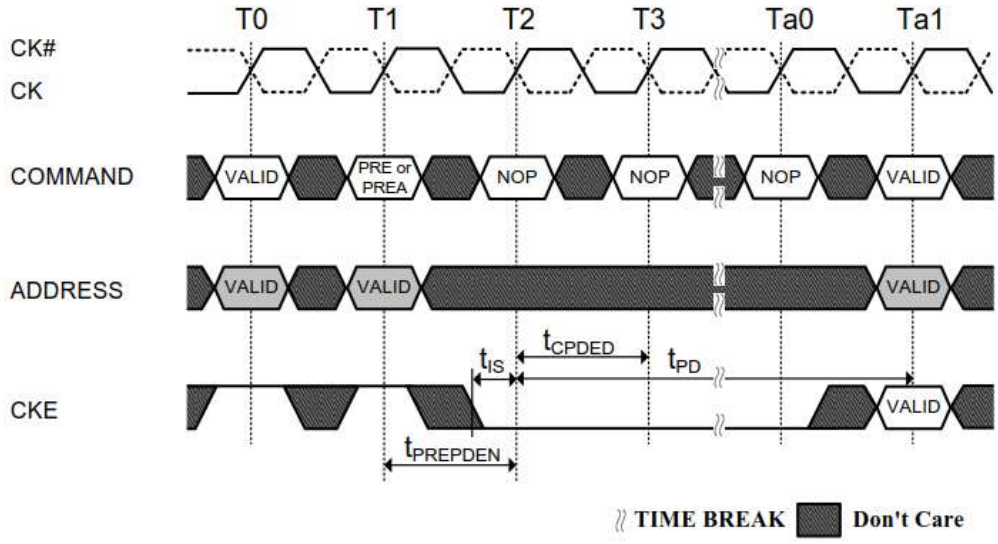


Figure 4-64 MRS Command to Power-Down Entry

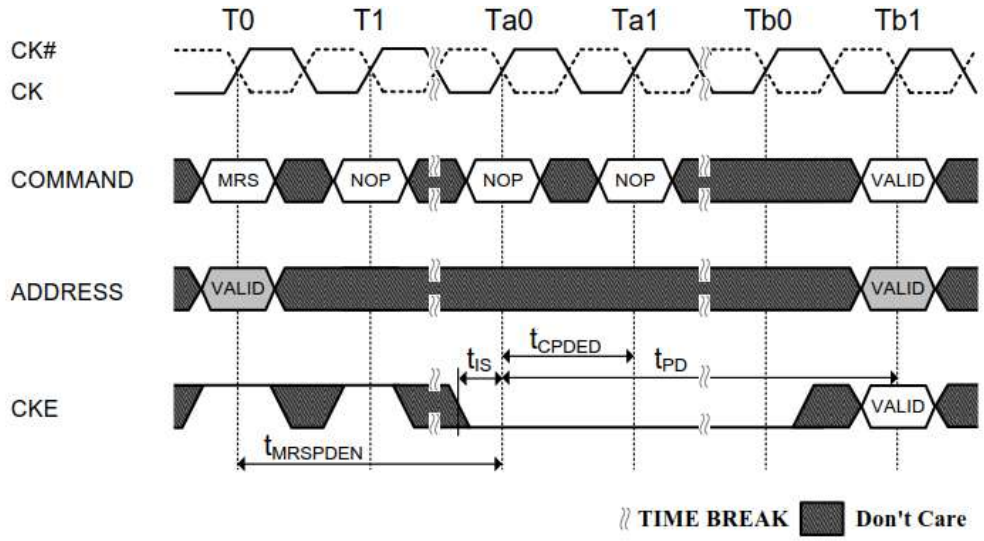


Figure 4-65 Synchronous ODT Timing Example

(AL = 3; CWL = 5; ODTLon = AL + CWL - 2 = 6; ODTLoff = AL + CWL - 2 = 6)

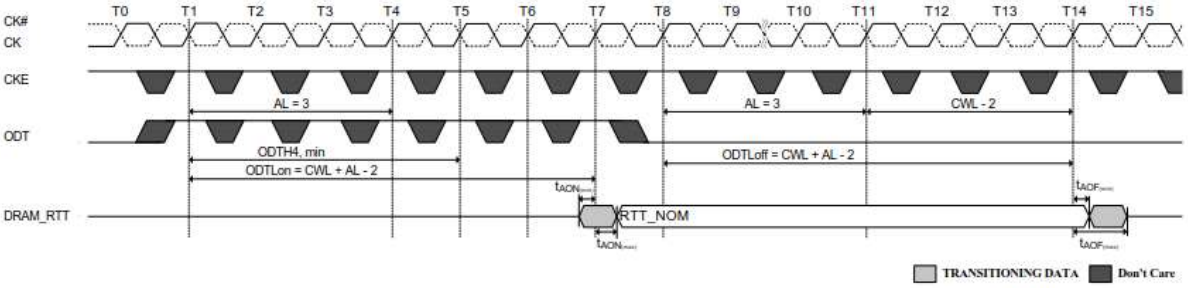


Figure 4-66 Synchronous ODT example with BL = 4, WL = 7

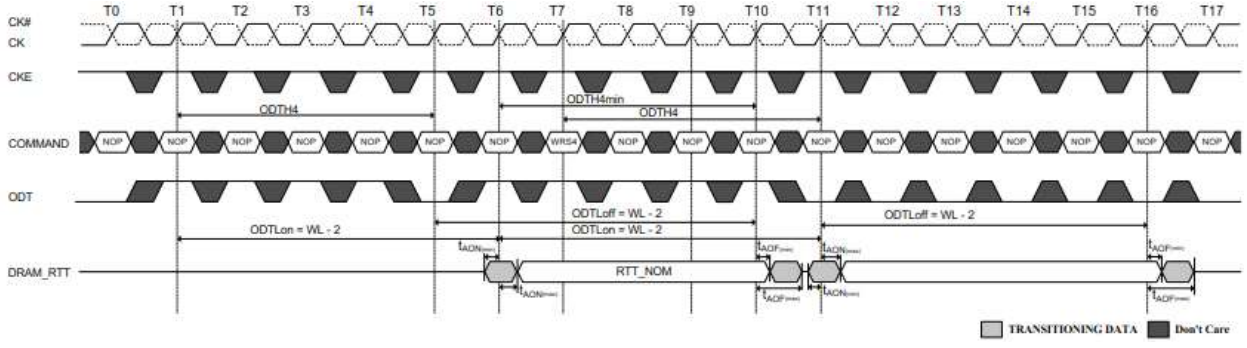
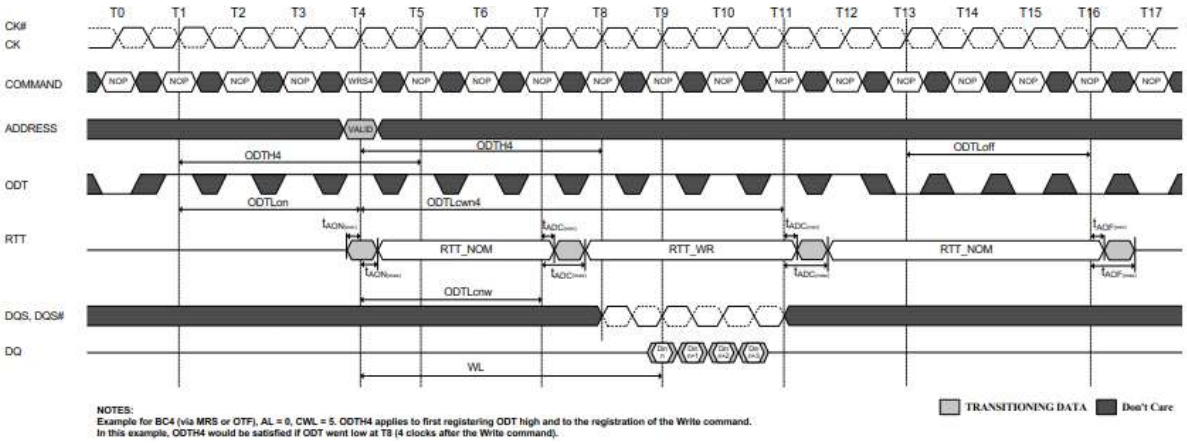
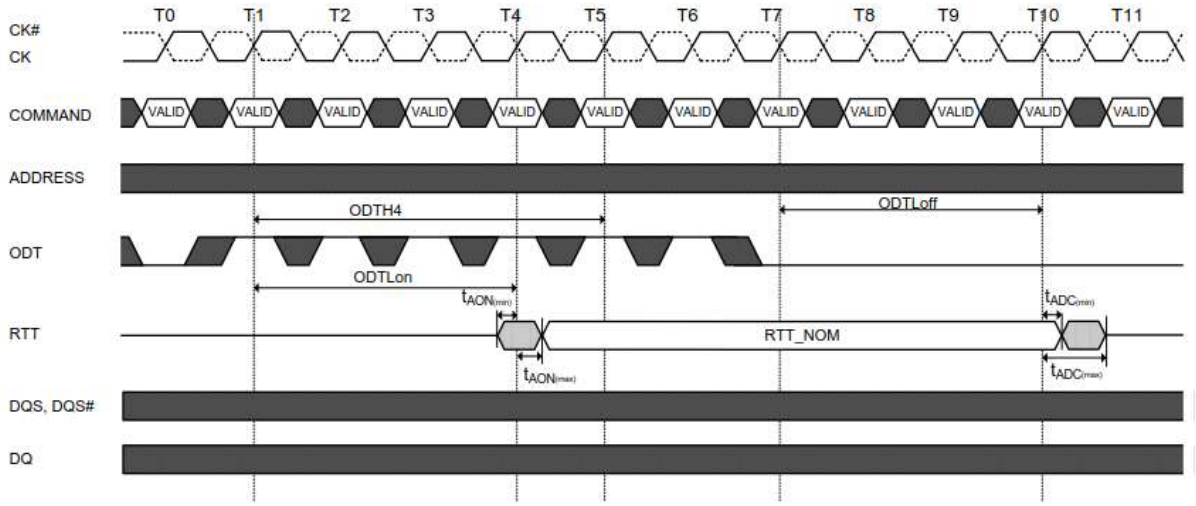


Figure 4-67 Dynamic ODT Behavior with ODT being asseted before and after the write



NOTES:
Example for BC4 (via MRS or OTF), AL = 0, CWL = 5. ODTH4 applies to first registering ODT high and to the registration of the Write command.
In this example, ODTH4 would be satisfied if ODT went low at T8 (4 clocks after the Write command).

Figure 4-68 Dynamic ODT: Behavior without write command, AL = 0, CWL = 5



NOTES:
1. ODTH4 is defined from ODT registered high to ODT registered low, so in this example, ODTH4 is satisfied.
2. ODT registered low at T5 would also be legal.

Figure 4-69 Dynamic ODT: Behavior with ODT pin being asserted together with write command for a duration of 6 clock cycles

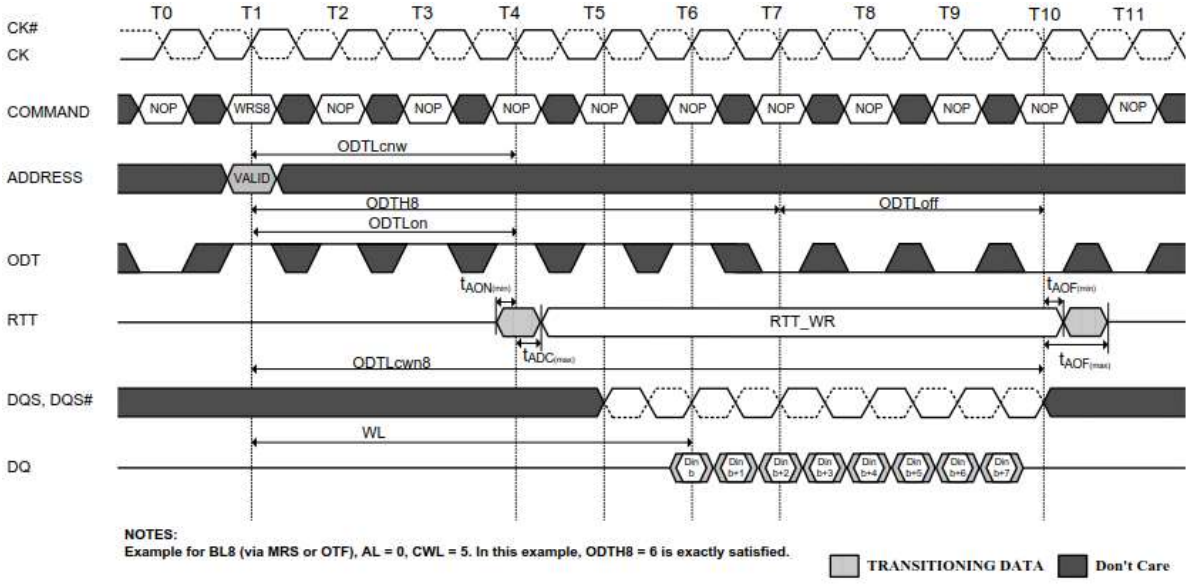


Figure 4-70 Dynamic ODT: Behavior with ODT pin being asserted together with write command for a duration of 6 clock cycles, example for BC4 (via MRS or OTF), AL = 0, CWL = 5

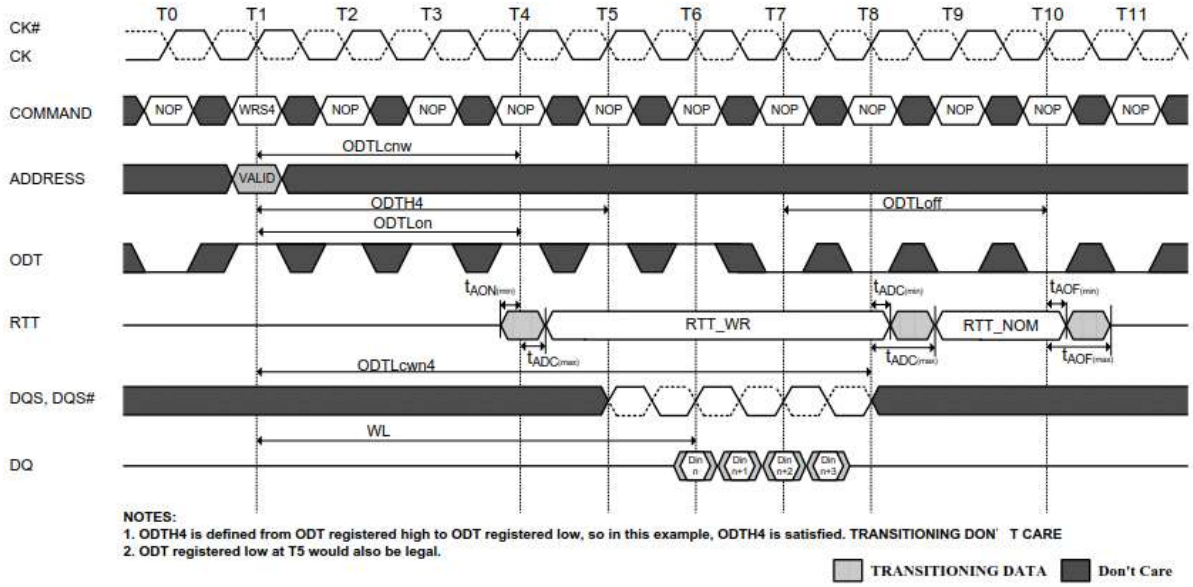


Figure 4-71 Dynamic ODT: Behavior with ODT pin being asserted together with write command for a duration of 4 clock cycles

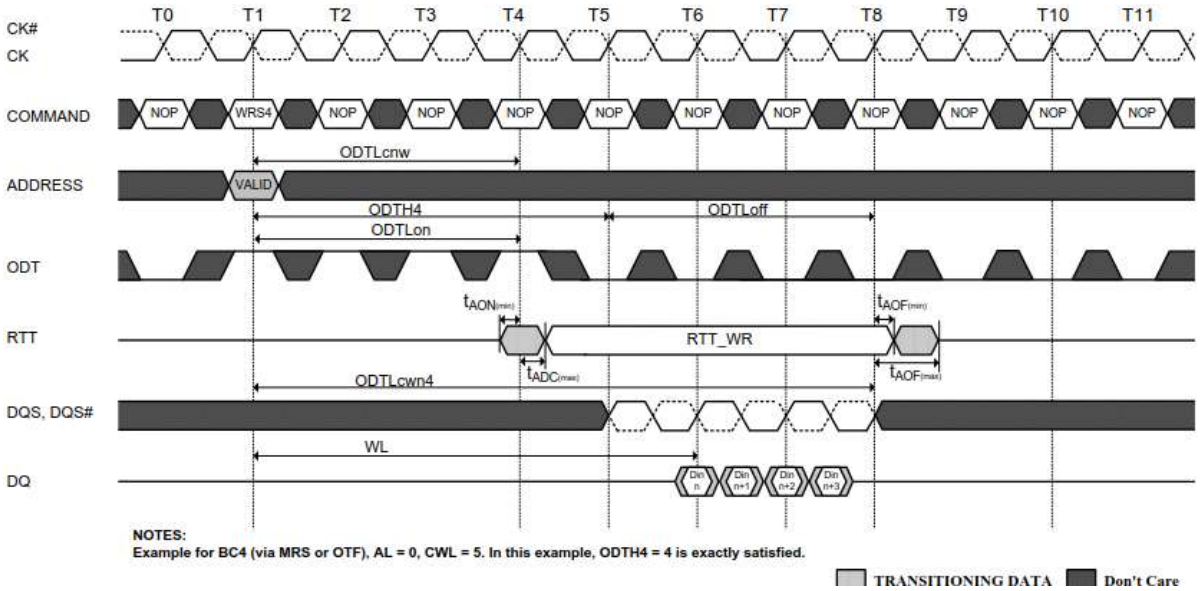


Figure 4-72 Asynchronous ODT Timings on DDR3 SDRAM with fast ODT transition

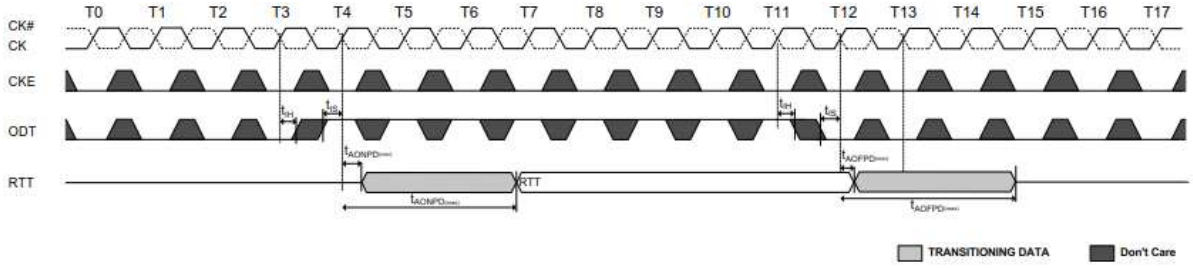


Figure 4-73 Synchronous to asynchronous transition during Precharge Power Down

(with DLL frozen) entry (AL = 0; CWL = 5; tANPD = WL - 1 = 4)

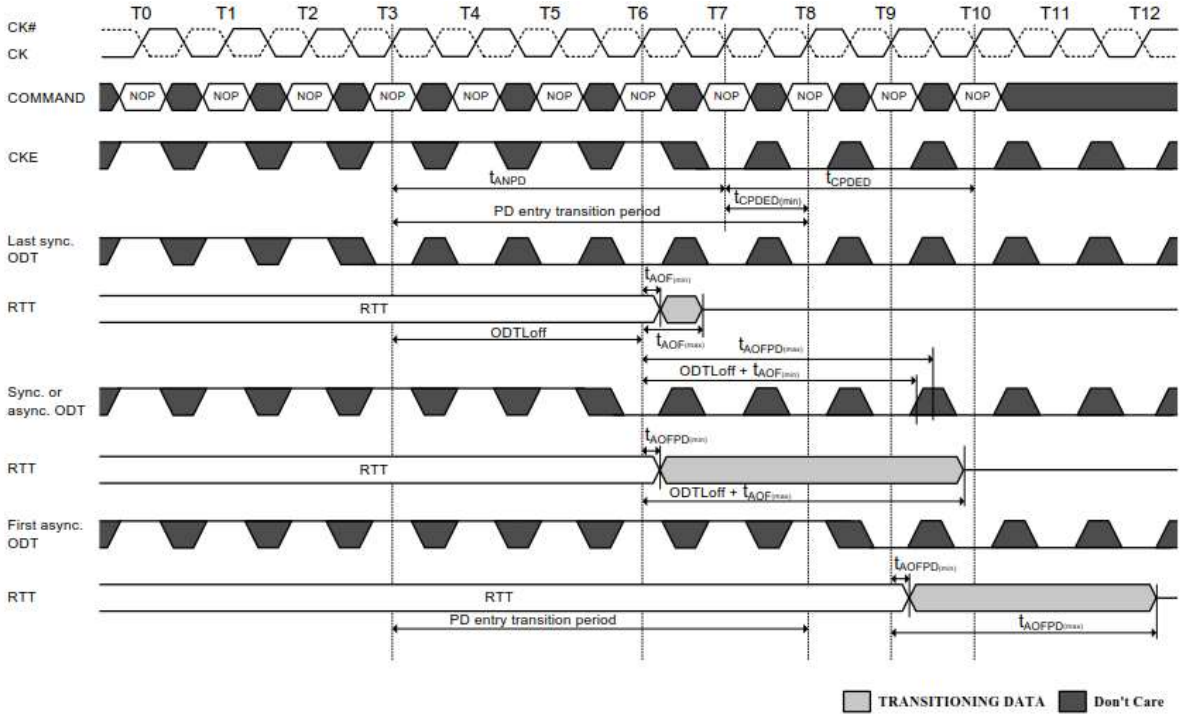


Figure 4-74 Synchronous to asynchronous transition after Refresh command

(AL = 0; CWL = 5; tANPD = WL - 1 = 4)

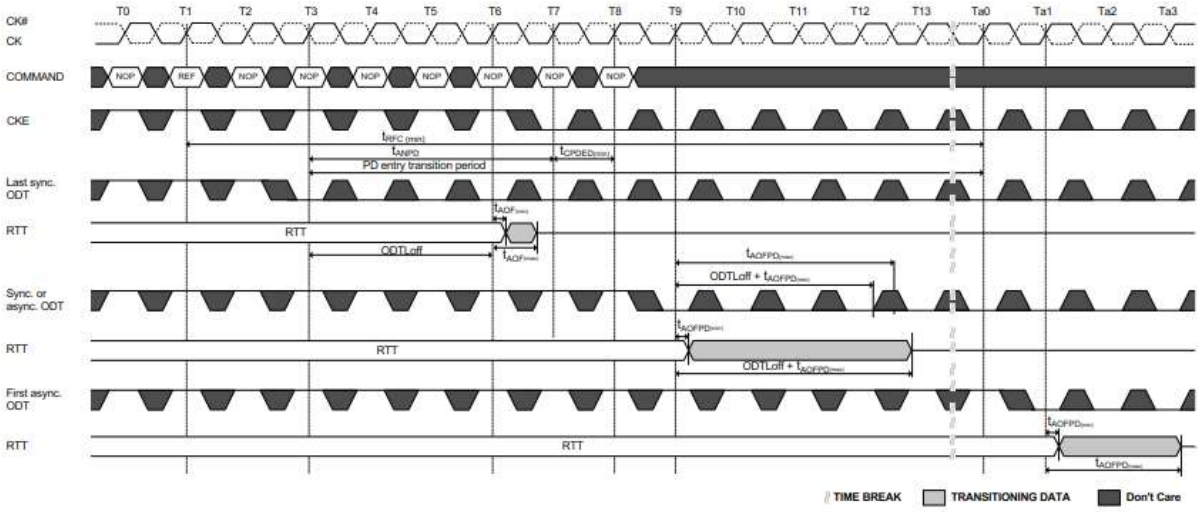


Figure 4-75 Asynchronous to synchronous transition during Precharge Power Down (with DLL frozen) exit (CL = 6; AL = CL - 1; CWL = 5; tANPD = WL - 1 = 9)

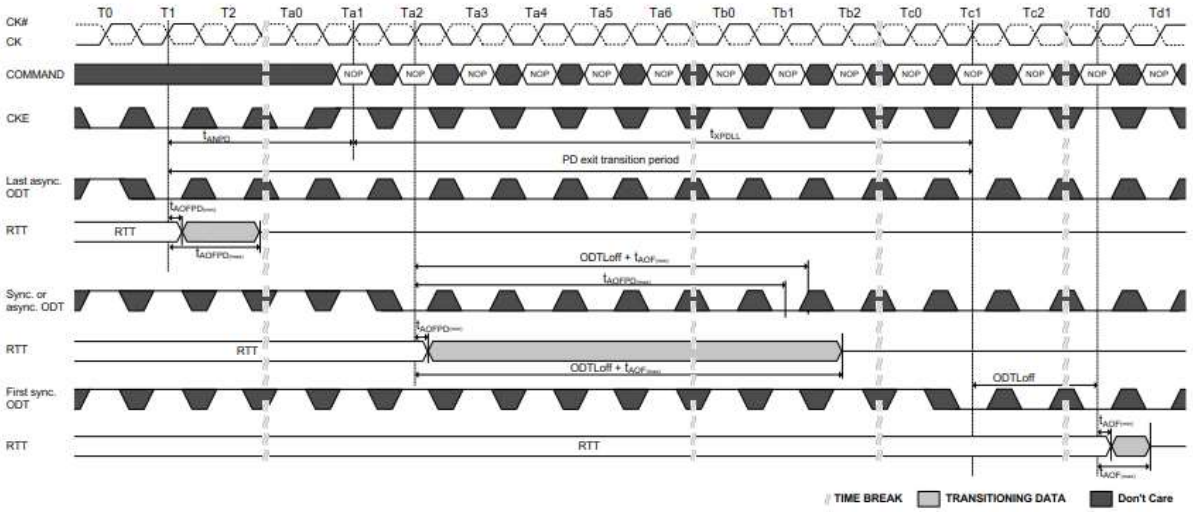


Figure 4-76 Transition period for short CKE cycles, entry and exit period overlapping (AL = 0, WL = 5, tANPD = WL - 1 = 4)

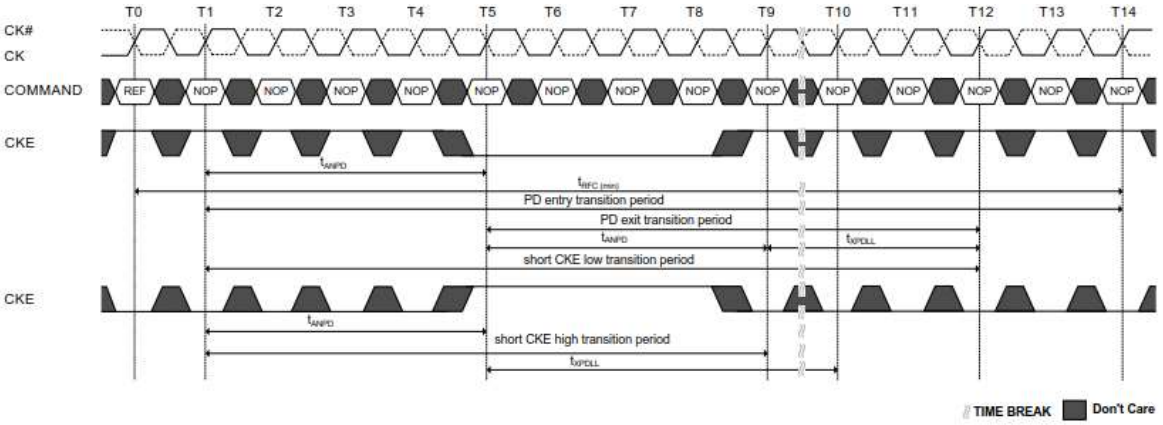


Figure 4-77 Power-Down Entry, Exit Clarifications-Case 1

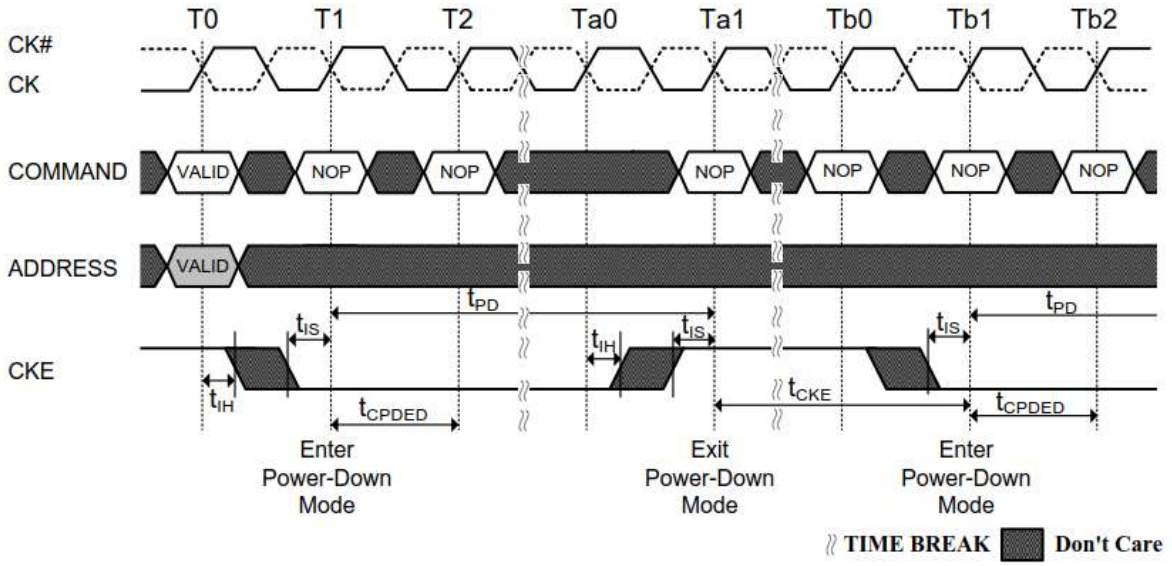


Figure 4-78 Power-Down Entry, Exit Clarifications-Case 2

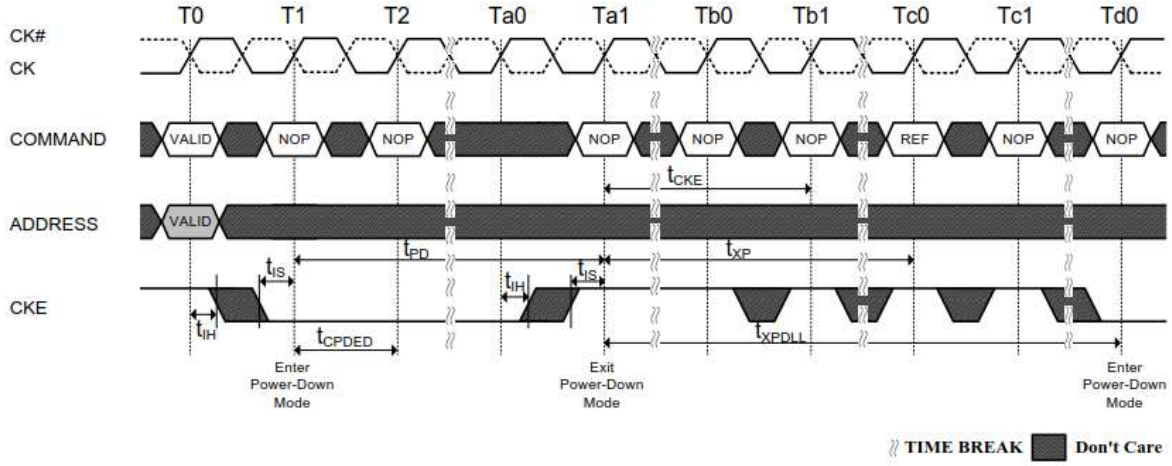
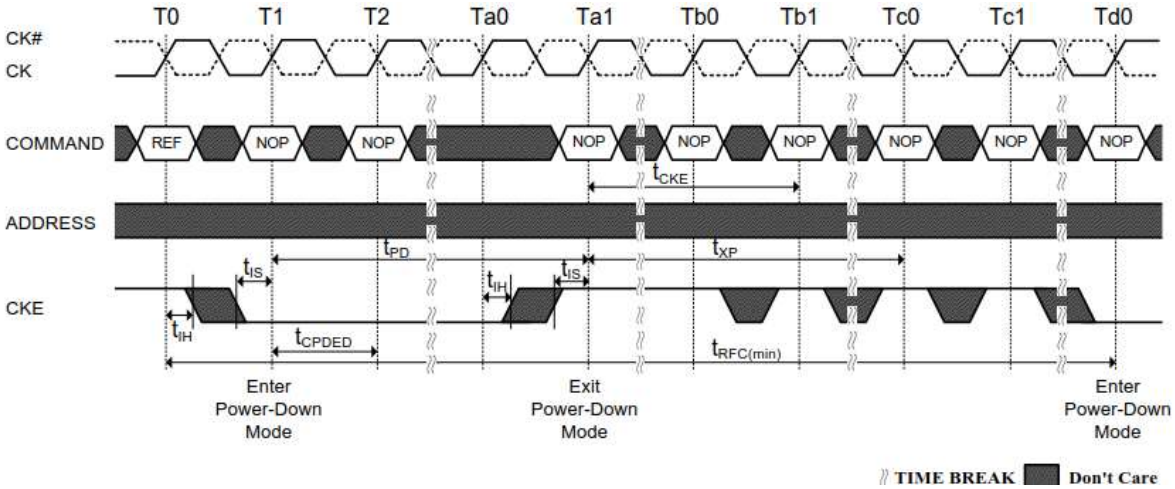
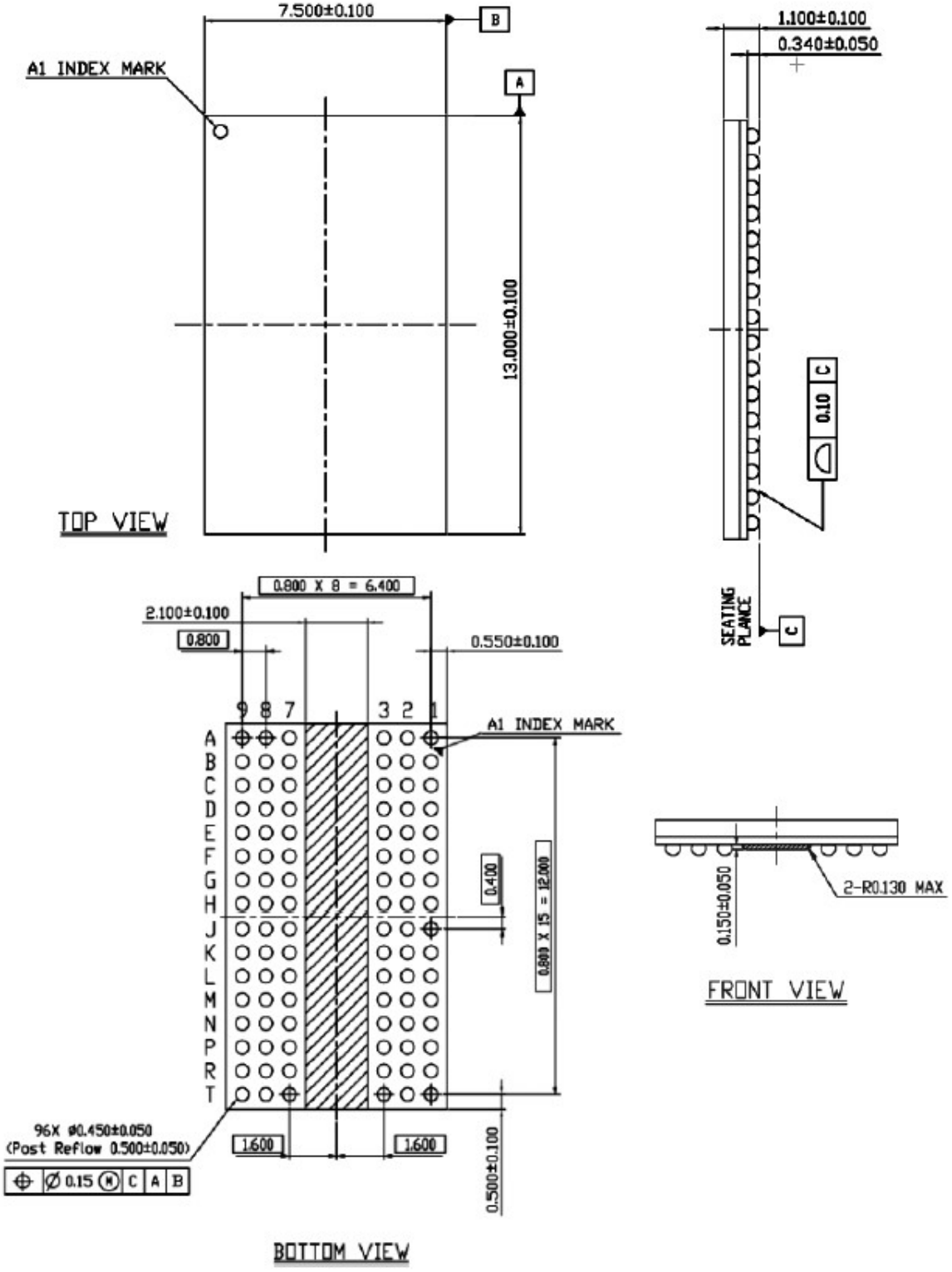


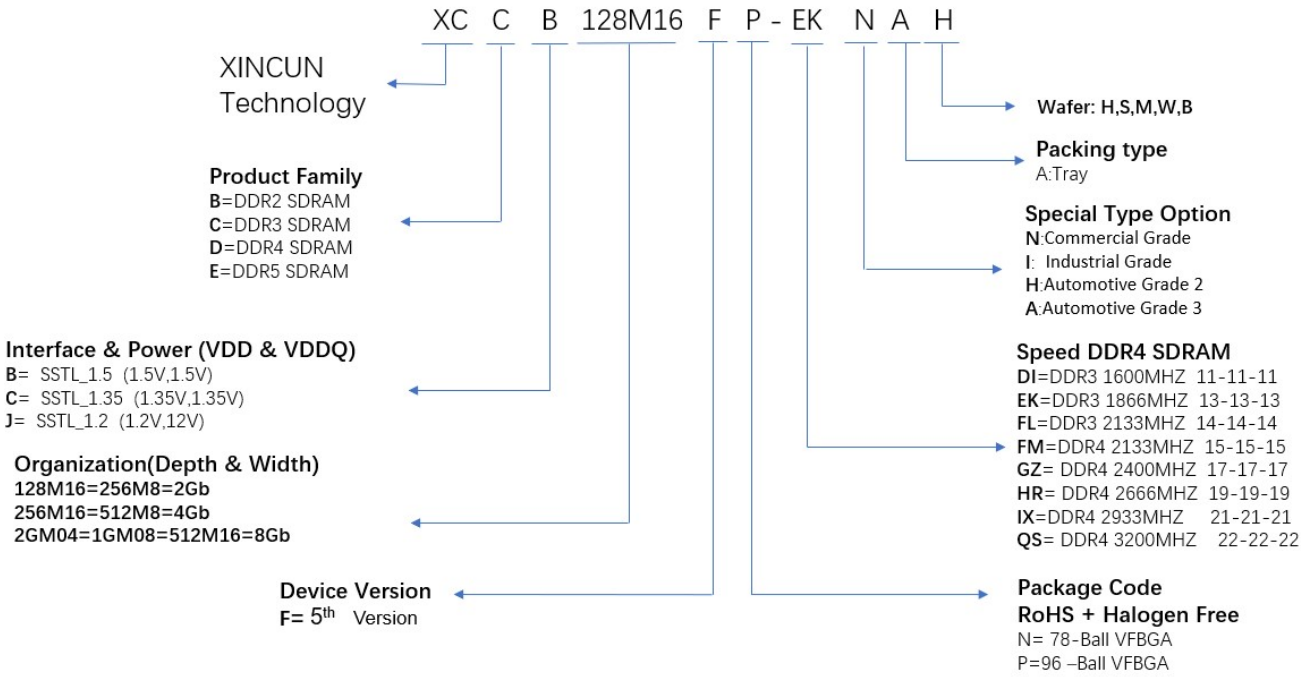
Figure 4-79 Power-Down Entry, Exit Clarifications-Case 3



5. PACKAGE DIMENSION (96Ball FBGA, 7.5x13x1.1mm)



6. PART NUMBER LOGIC



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