SPI NAND Datesheet

XCSP1AAPK-IT

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Product models list:

Specifications	FLASH	VCC	Packaging
XCSP1AAPK-IT	1Gb	3.3V	WSON(8*6mm)-8PIN
XCSP2AAPK-IT	2Gb	3.3V	WSON(8*6mm)-8PIN
XCSP4AAPK-IT	4Gb	3.3V	WSON(8*6mm)-8PIN

Change History:

Rev	Changes	Date	Note
Rev1.0	Initial release	2023.03.03	
Rev1.1	Update logo	2023.05.15	

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1 INTRODUCTION

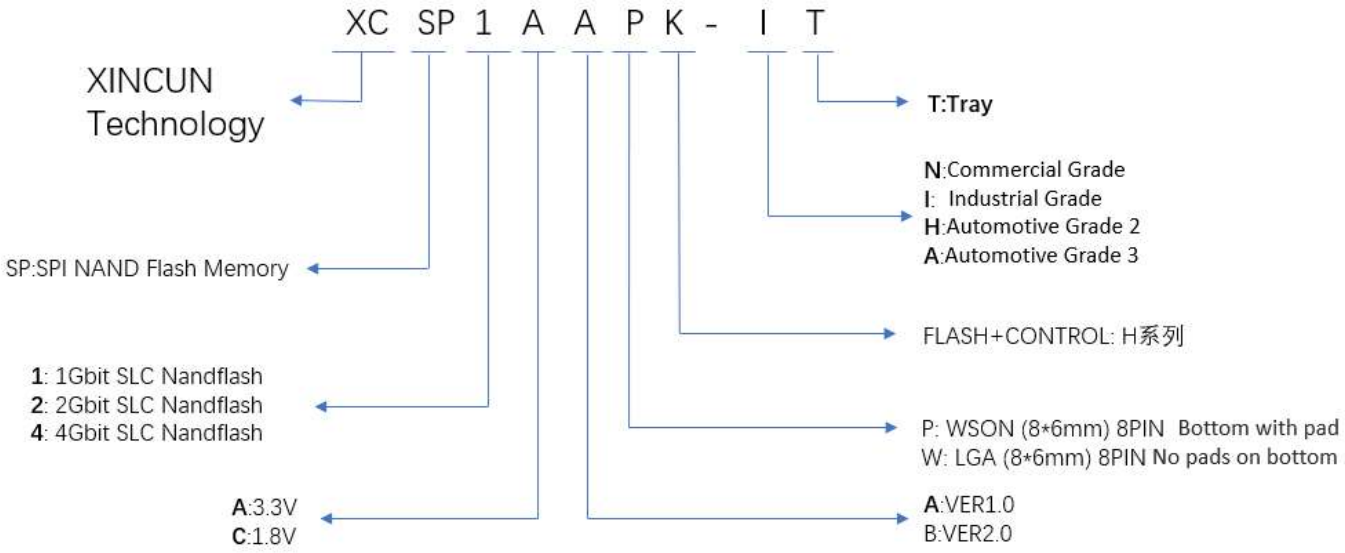
1.1 General Description

The XCSP1AAPK-IT is 1G-bit SPI (Serial Peripheral Interface) NAND Flash memory, with advanced write protection mechanisms. The XCSP1AAPK-IT supports the standred Serial Peripheral interface,Dual/Quad I/O option. The XCSP1AAPK-IT is an optimum solution for large nonvolatile storage applications such as solid state file storage and other portable app.lications requiring non-volatility.

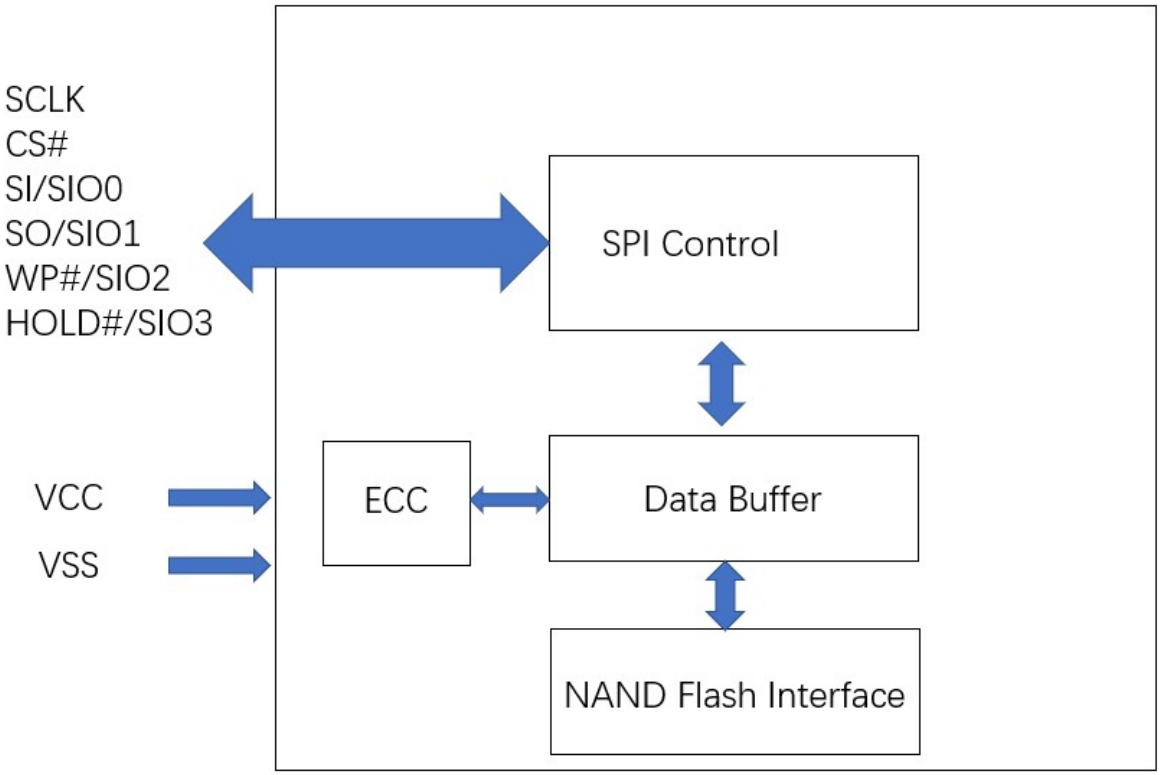
1.2 Features

- **1Gbit NAND Flash memory**
  - single-level cell (SLC) technology
  - Block size : 64pages(128K + 8K bytes)
  - Page Size : 2176 bytes (2048 + 128 bytes)
  - Device : 1Gb (1024 blocks)
- **Read performance**
  - Random access: 45μs(Max.)
  - Sequential access : 20ns(Min.)
- **Write performance**
  - Page program time : 300μs (Typ.)
  - Sequential access : 20ns(Min.)
  - Block erase Time : 2.5ms(Typ.)
  - Page read time: 45μs maximum (w/l ECC).
- **Serial Interface**
  -standard SPI: CLK,CS#,SI,SO,WP#
  -Dual SPI :CLK,CS#,SIO0,SIO1,WP#
  -Quad SPI:CLK,CS#SIO0,SIO1,SIO2,SIO3
- **Operating Temperature**
  -40℃ to 85℃
- **Storage Temperature**
  -55℃ to 125℃
- **8K-Byte OTP**
- **Advanced Security Features**
  -Built in 8bit per sector ECC.
  -Internal data move by page with ECC
- **Supports IDLE and SLEEP power saving modes.**
- **Command/Address/Data Multiplexed I/O Port**
- High Performance
  -104M for fast read.
- 6KV ESD Protection
- Hardware Data Protection.
  - Program/Erase Lockout During Power Transitions.
  -Date protection during data transfer even if unplugged/ power off.
- **Voltage Supply**
  - vcc:3.3V (3.0V-3.6V).
- **Package**
  - 8-pin WSON (8*6mm).
  -All packages are RoHS Compliant and Halogen-free.
- **Data retention: 10 years**
- **Erasure times up to 100,000 times**

2 XINCUN component Part Numbering Guide

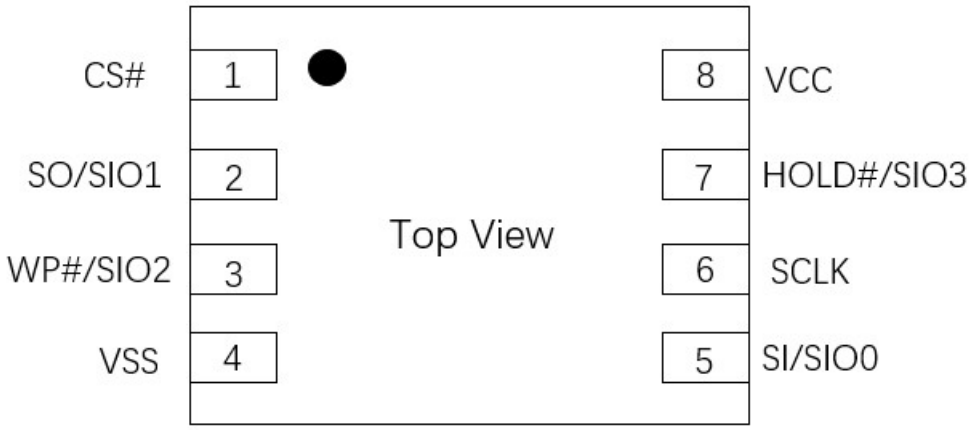


3 Block Diagram



4 Packaging Type and Pin Configurations

4.1 Connection Diagram



8-Pin WSON (8*6mm)

4.2 Pin Description

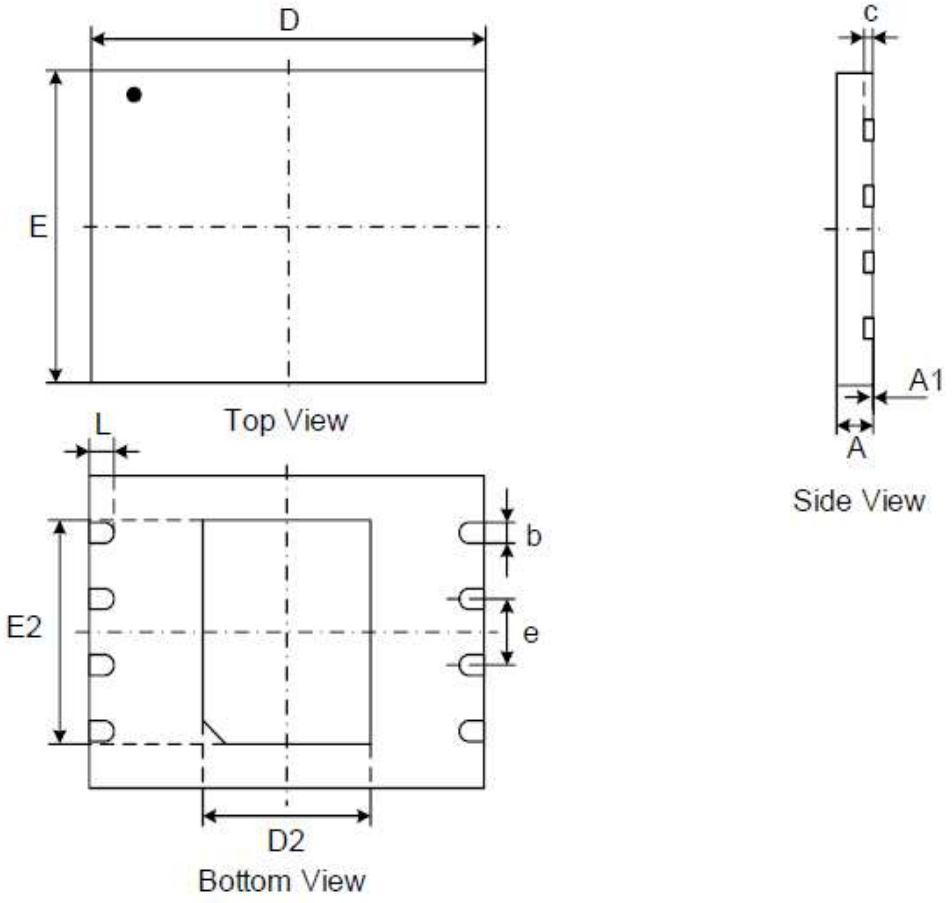
Pin Name	I/O	Description
CS#	**I**	Chip Select input, active low
SO/SIO1	**I/O**	Serial Data Output / Serial Data Input Output 1
WP#/SIO2	**I/O**	Write Protect, active low / Serial Data Input Output 2
VSS	**Ground**	Ground
SI/SIO0	**I/O**	Serial Data Input / Serial Data Input Output 0
SCLK	**I**	Serial Clock input
HOLD#/SIO3	**I/O**	Hold input, active low / Serial Data Input Output3
VCC	**Supply**	Power Supply

Notes:

1. SIO0 and SIO1 are used for Standard and Dual SPI instructions
2. SIO0 – SIO3 are used for Quad SPI instructions, WP# & HOLD# functions are only available for Standard/Dual SPI.

5 PACKAGE INFORMATION

8-Pin WSON8 (8*6mm)



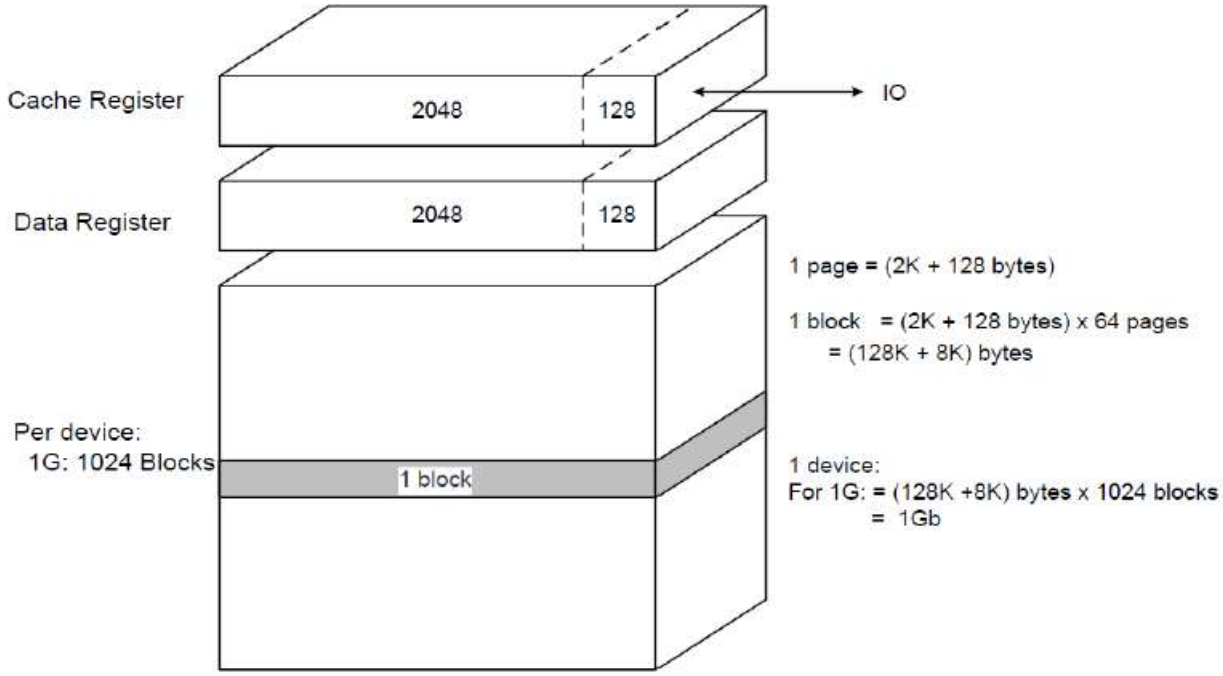
Dimensions

Symbol / Unit		A	A1	c	b	D	D2	E	E2	e	L
mm	Min	0.70	0.00	0.180	0.35	7.90	3.30	5.90	4.20	1.27	0.45
	Nom	0.75	0.02	0.203	0.40	8.00	3.40	6.00	4.30		0.50
	Max	0.80	0.05	0.250	0.45	8.10	3.50	6.05	4.40		0.55
Inch	Min	0.028	0	0.007	0.014	0.311	0.130	0.232	0.165	0.05	0.018
	Nom	0.030	0.001	0.008	0.016	0.315	0.134	0.236	0.169		0.020
	Max	0.032	0.002	0.010	0.018	0.319	0.138	0.238	0.173		0.022

6 ARRAY ORGANIZATION

Each block has	Each page has	
128K+8K	2K+128	bytes
64	-	pages
-	-	blocks

Figure1. Array Organization



7 PIN DESCRIPTIONS

7.1 Chip Select CS#

The SPI Chip Select CS# pin enables and disables device operation. When CS# is high the device is deselected and the Serial Data Output (SO, or SIO0, SIO1, SIO2, SIO3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When CS# is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, CS# must transition from high to low before a new instruction will be accepted. The CS# input must track the VCC supply level at power-up and power-down (see “Write Protection” and Figure30b). If needed, a pull-up resistor on the CS# pin can be used to accomplish this.

7.2 Serial Data Input, Output and IOs (SI, SO and SIO0, SIO1, SIO2, SIO3)

The XCSP1AAPK-IT supports standard SPI, Dual SPI and Quad SPI operation. Standard SPI instructions use the unidirectional **SI** (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional SO (output) to read data or status from the device on the falling edge of CLK.

Dual and Quad SPI instructions use the bidirectional IO pins to serially write instructions, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK.

7.3 Write Protect WP#

The Write Protect WP# pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register’s Block Protect bits BP[3:0] and Status Register Protect SRP bits SRP[1:0], a portion as small as 256K-Byte (2x128KB blocks) or up to the entire memory array can be hardware protected. The WP-E bit in the Protection Register (SR-1) controls the functions of the WP# pin.

When WP-E=0, the device is in the Software Protection mode that only SR-1 can be protected. The WP# pin functions as a data I/O pin for the Quad SPI operations, as well as an active low input pin for the Write Protection function for SR-1. Refer to section Quad SPI for detail information.

When WP-E=1, the device is in the Hardware Protection mode that WP# becomes a dedicated active low input pin for the Write Protection of the entire device. If WP# is tied to GND, all “Write/Program/Erase” functions are disabled. The entire device (including all registers, memory array, OTP pages) will become read-only. Quad SPI read operations are also disabled when WP-E is set to 1.

7.4 HOLD#

During Standard and Dual SPI operations, the HOLD# pin allows the device to be paused while it is actively selected. When HOLD# is brought low, while CS# is low, the SO pin will be at high impedance and signals on the SI and CLK pins will be ignored (don’t care). When HOLD# is brought high, device operation can resume. The HOLD# function can be useful when multiple devices are sharing the same SPI signals. The HOLD# pin is active low.

When a Quad SPI Read/Buffer Load command is issued, HOLD# pin will become a data I/O pin for the Quad operations and no HOLD function is available until the current Quad operation finishes. HOLD#/SIO3 must be driven high by the host, or an external pull-up resistor must be placed on the PCB, in order to avoid allowing the HOLD# input to float.

7.5 Serial Clock CLK

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Operations")

8 Device Operation

8.1 Standard SPI Instructions

The **XCSP1AAPK-IT** is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO). Standard SPI instructions use the SI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The SO output pin is used to read data or status from the device on the falling edge of CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of CS#. For Mode 3, the CLK signal is normally high on the falling and rising edges of CS#.

8.2 Dual SPI Instructions

The **XCSP1AAPK-IT** supports Dual SPI operation when using instructions such as “Fast Read Dual Output (3Bh)” and “Fast Read Dual I/O (BBh)”. These instructions allow data to be transferred to or from the device at two to three times the rate of ordinary Serial Flash devices. The Dual SPI Read instructions are ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed-critical code directly from the SPI bus (XIP). When using Dual SPI instructions, the SI and SO pins become bidirectional I/O pins: SIO0 and SIO1.

8.3 Quad SPI Instructions

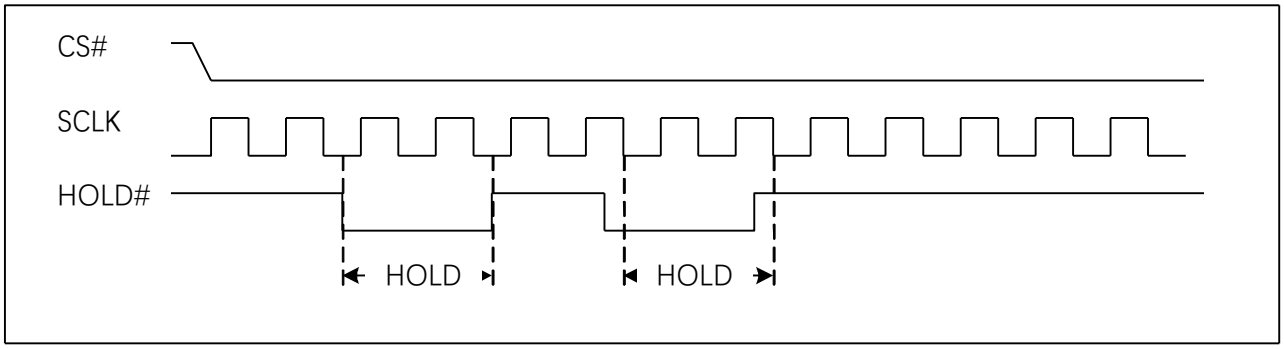
The **XCSP1AAPK-IT** supports Quad SPI operation when using instructions such as “Fast Read Quad Output (6Bh)”, “Fast Read Quad I/O (EBh)” and “Quad Program Data Load (32h/34h)”. These instructions allow data to be transferred to or from the device four to six times the rate of ordinary Serial Flash. The Quad Read instructions offer a significant improvement in continuous and random access transfer rates allowing fast code-shadowing to RAM or execution directly from the SPI bus (XIP). When using Quad SPI instructions the SI and SO pins become bidirectional SIO0 and SIO1, and the WP# and HOLD# pins become SIO2 and SIO3 respectively.

8.4 Hold Function

For Standard SPI and Dual SPI operations, the HOLD# signal allows the **XCSP1AAPK-IT** operation to be paused while it is actively selected (when CS# is low). The HOLD# function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, consider if the page buffer was only partially written when a priority interrupt requires use of the SPI bus. In this case the HOLD# function can save the state of the instruction and the data in the buffer so programming can resume where it left off once the bus is available again. The HOLD# function is only available for standard SPI and Dual SPI operation, not during Quad SPI. When a Quad SPI command is issued, HOLD# pin will act as a dedicated IO pin (SIO3).

To initiate a HOLD# condition, the device must be selected with CS# low. A HOLD# condition will activate on the falling edge of the HOLD# signal if the CLK signal is already low. If the CLK is not already low the HOLD# condition will activate after the next falling edge of CLK. The HOLD# condition will terminate on the rising edge of the HOLD # signal if the CLK signal is already low. If the CLK is not already low the HOLD # condition will terminate after the next falling edge of CLK. During a HOLD # condition, the Serial Data Output (SO) is high impedance, and Serial Data Input (SI) and Serial Clock (CLK) are ignored. The Chip Select (CS #) signal should be kept active (low) for the full duration of the HOLD # operation to avoid resetting the internal logic state of the device.

Hold Condition



8.5 Write Protection

SPI NAND provides Hardware Protection Mode besides the Software Mode. Write Protect (WP#) prevents the block lock bits (BP0, BP1, BP2 and INV, CMP) from being overwritten. If the BRWD bit is set to 1 and WP# is LOW, the block protect bits cannot be altered.

9 COMMANDS DESCRIPTION

Table 1 standard SPI Command set

Command Name	Byte1	Byte2	Byte3	Byte4	Byte5	ByteN
Write Enable	06H					
Write Disable	04H					
Get Features	0FH	A7-A0	(D7-D0)			Wrap
Set Feature	1FH	A7-A0	(D7-D0)	Dummy		
Page Read(to cache)	13H	A23-A16	A15-A8	A7-A0		
Read form Cahe	03H/0BH	A15-A8	A7-A0	dummy	(D7-D0)	Wrap
Read form Cahe x 2	3BH	A15-A8	A7-A0	dummy	(D7-D0)x2	Wrap
Read form Cahe x 4	6BH	A15-A8	A7-A0	dummy	(D7-D0)x4	Wrap
Read form Cahe Dual IO	BBH	A15-A0	dummy	(D7-D0)x2		Wrap
Read form Cahe Quad IO	EBH	A15-A0	(D7-D0)x4			Wrap
Read ID	9FH	A7-A0	MID	DID		Wrap
Program Load	02H	A15-A8	A7-A0	(D7-D0)	Next byte	Byte N
Program Load x 4	32H	A15-A8	A7-A0	(D7-D0)x4	Next byte	Byte N
Program Execute	10H	A23-A16	A15-A8	A7-A0		
Program Load random data	84H	A15-A8	A7-A0	(D7-D0)	Next byte	Byte N
Program Load random data x 4	C4H/34H	A15-A8	A7-A0	(D7-D0)x4	Next byte	Byte N
Program Load random data Quad IO	72H	A15-A0	(D7-D0)x4	Next byte		Byte N
Block Erase	D8H	A23-A16	A15-A8	A7-A0		
Reset	FFH					

Notes:

1. The dummy byte can be inputted or not.
2. The x8 clock = dummy<7:0>.
3. The x8 clock = dummy<7:0>, D7-D0.
4. The x8 clock = dummy<3-0>, A11-A8 or dummy<3-0>, A11-A0.
5. The x8 clock = dummy<3-0>, A11-A0, dummy<7:0>, D7-D0.
6. The x8 clock = dummy<3:0>, A<11:8>.
7. The x8 clock = dummy<3:0>, A<11:0>, D7-D0, D7-D0.
8. MID is Manufacture ID (9Dh for Xincun), DID is Device ID When A7-A0 is 00h, read MID and DID.
9. Reset command:
   - During busy, Reset will reset PAGE READ/PROGRAM/ERASE operation.
   - During idle, Reset will reset status register bits P_FAIL/E_FAIL/ECCS bits.
10. Those commands are only available in Internal Data Move operation.

10 WRITE OPERATIONS

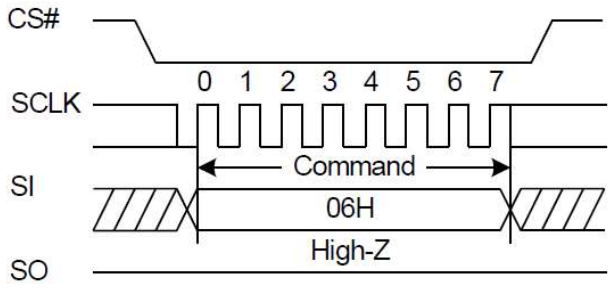
10.1 Write Enable (WREN) (06H)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to following operations that change the contents of the memory array:

- Page program
- OTP program/OTP protection
- Block erase

The WEL bit can be cleared after a reset command.

Write Enable Sequence Diagram

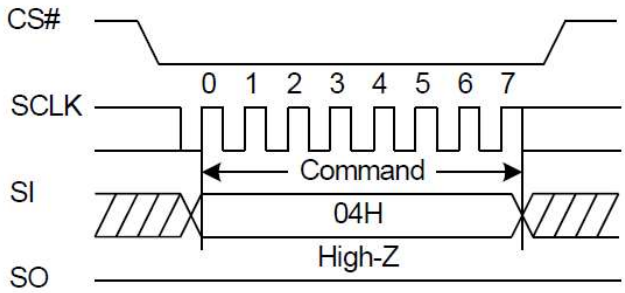


10.2 Write Disable (WRDI) (04H)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit. The WEL bit is reset by following condition:

- Page program
- OTP program/OTP protection
- Block erase

Write Disable Sequence Diagram



11 FEATURE OPERATIONS

Get Features (0FH) and Set Features (1FH)

The GET FEATURES (0FH) and SET FEATURES (1FH) commands are used to monitor the device status and alter the device behavior. These commands use a 1-byte feature address to determine which feature is to be read or modified. Features such as OTP and block locking can be enabled or disabled by setting specific feature bits (shown in the following table). The status register is mostly read, except WEL, which is a writable bit with the WRITE ENABLE (06H) command. When a feature is set, it remains active until the device is power cycled or the feature is written to. Unless otherwise specified in the following table, once the device is set, it remains set, even if a RESET (FFH) command is issued.

Features Settings

Register	Address	7	6	5	4	3	2	1	0
Protection	A0H	BRWD	Reserved	BP2	BP1	BP0	INV	CMP	Reserved
Feature	B0H	OTP_PRT	OTP_EN	Reserved	ECC_EN	Reserved	Reserved	Reserved	QE
Status	C0H	Reserved	Reserved	ECCS1	ECCS0	P_FAIL	E_FAIL	WEL	OIP

Note:

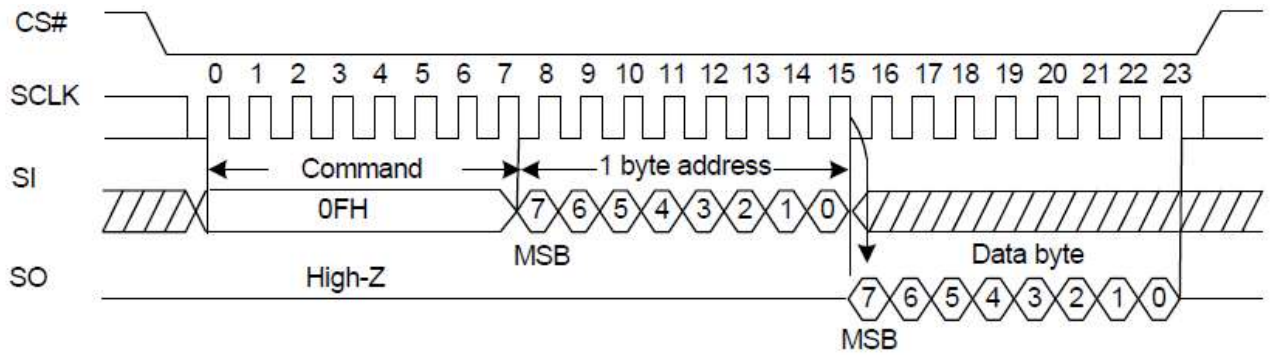
1.If BRWD is enabled and WP# is LOW, then the block lock register cannot be changed.

2.If QE is enabled, the quad IO operations can be executed.

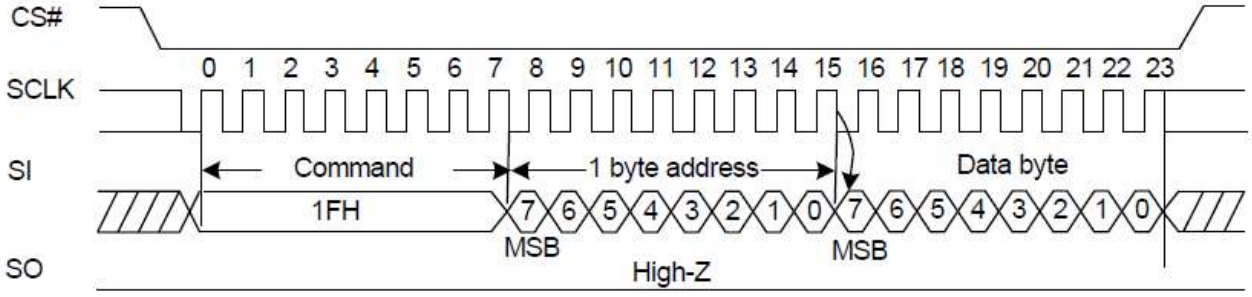
3.All the reserved bits must be held low when the feature is set.

4. 00h is the default data byte value for Output Driver Register after power-up.

Get Features Sequence Diagram



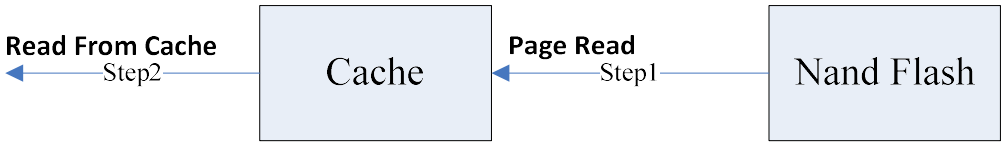
Set Features Sequence Diagram



The set features command supports a dummy byte mode after the data byte as well.The features in the feature byte B0H are all volatileexcept OTP_PRT bit.

12 Read Operations

12.1 Page Read



Reading data from SPI NAND Flash requires three steps:

1. Run the PAGE READ (13H) command to load data pages into Cache.

2. Run the GET FEATURES (0FH) command to query the status register (C0H), wait for the read completion (OIP=0), and read the ECCS1 and ECCS0 after ECC_EN is enabled to check whether the read data is correct.

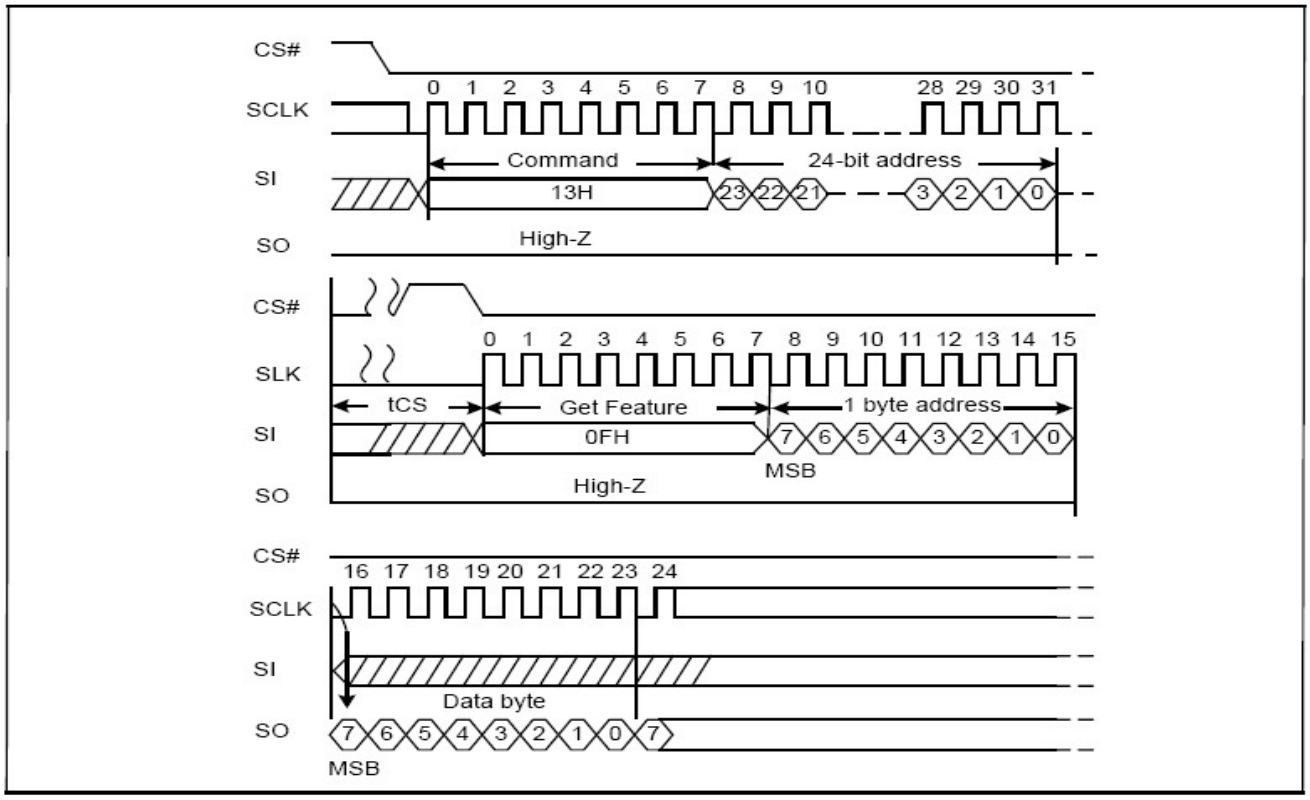
3. Run the Read from cache (03H/0BH/3BH/6BH/BBH/EBH) command to Read data pages from cache.

The Read from cache command address field (16bit) contains a 4-bit Wrap address to indicate the three Wrap modes, and a 12-bit column address to specify the cache start address. The start address of a 12-bit column must range from 0 to 2175. After the Read from cache command is used, the cache outputs data from the specified Column address in sequence. When the wrap (2176/2048/64/16-byte) boundary address is reached, the cache automatically returns to the start address of the region and stops transmission until CS# is high.

Wrap<3>	Wrap<2>	Wrap<1>	Wrap<0>	Wrap Length(byte)
0	0	X	X	2176
0	1	X	X	2048
1	0	X	X	64
1	1	X	X	16

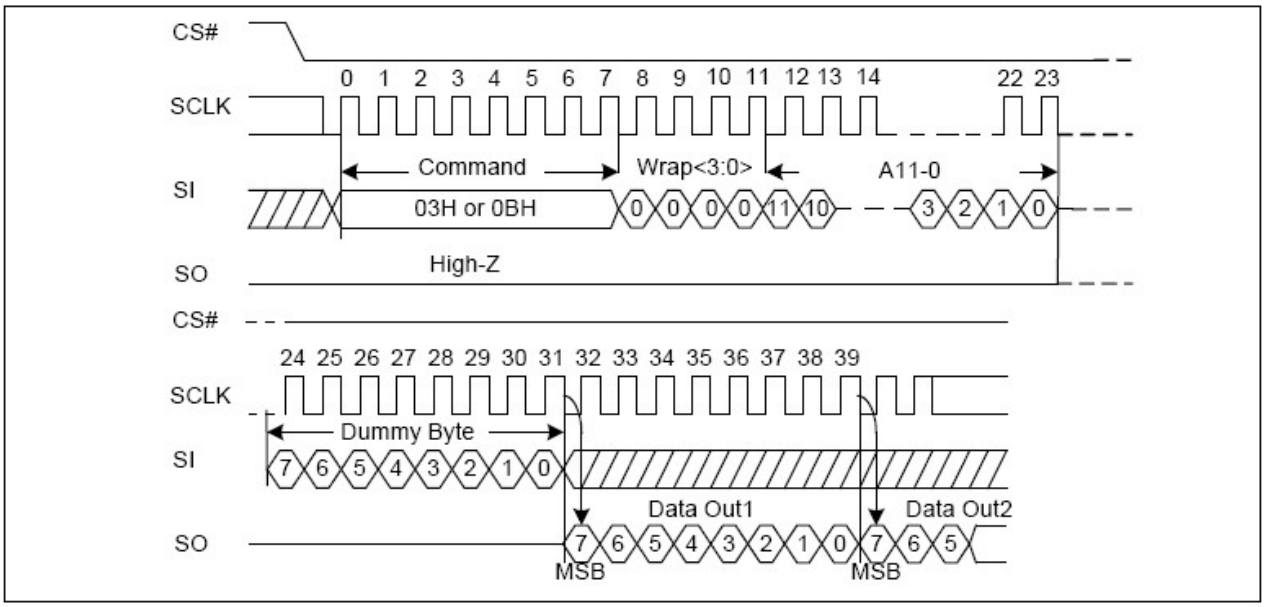
12.2 Page Read to Cache (13H)

The PAGE READ (13H) command is used to READ data from NAND FALSH and load it to the Cache. (If ECC_EN is enabled, data is decoded and corrected by BCH before being loaded to the Cache.) The address field must be 24-bit. The length of the Page/Block address varies with Flash specifications. For details, see Figure 2-3 and Figure 2-4 for RA address descriptions. After the SPI NAND FLASH is addressed successfully, the corresponding NAND FLASH data is loaded to the cache. TRD indicates the loading time. You can run the GET FEATURE (0FH) command to query the OIP status during the loading. (OIP = 0 indicates that the loading is complete.) The data can then be Read from cache (03H/0BH/3BH/6BH/BBH/EBH) command.



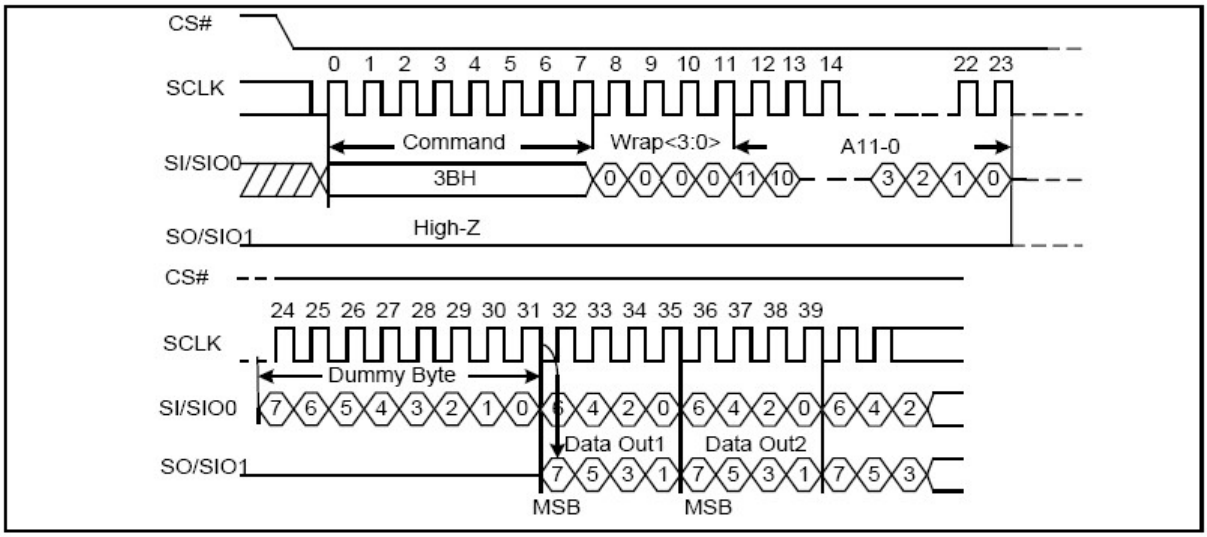
ReadFrom Cache Sequence Diagram

12.3 Read From Cache (0BH or 03H)



ReadFrom Cache Sequence Diagram

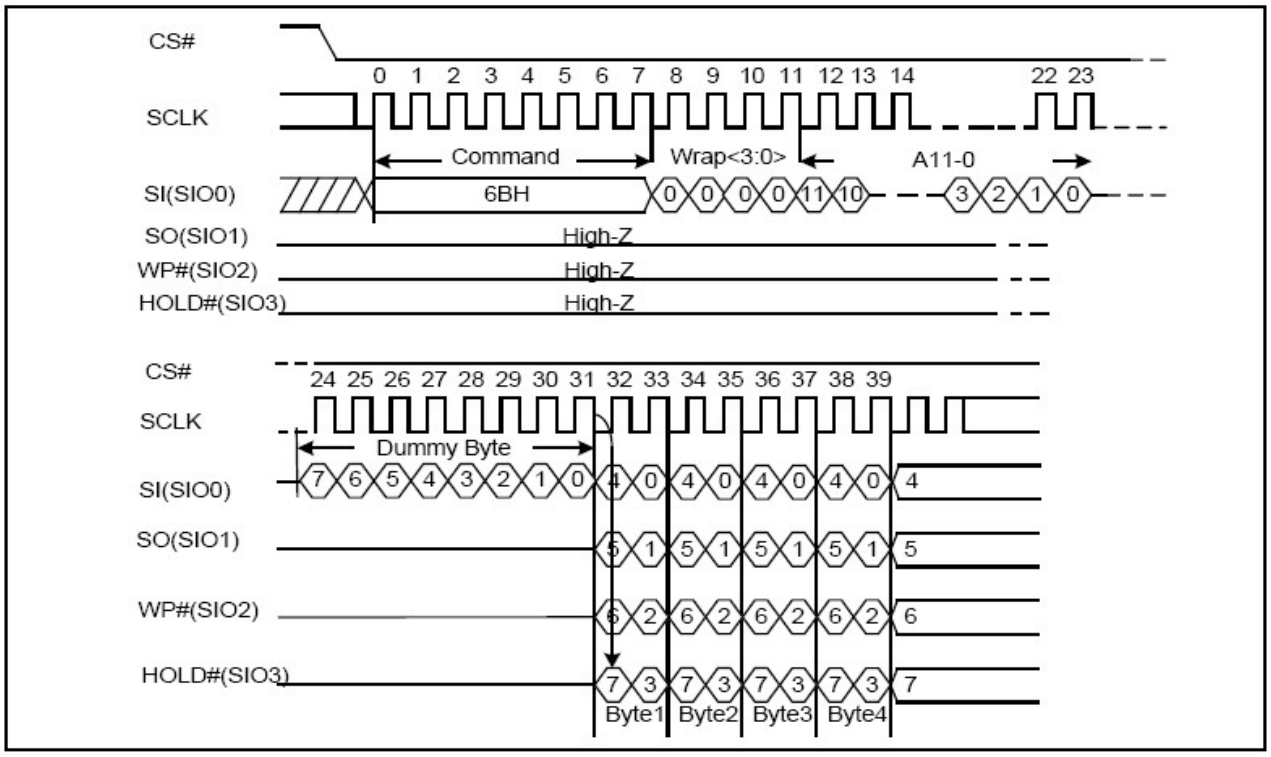
12.4 Read From Cache x2 (3BH)



Read From Cache x2 Sequence Diagram

12.5 Read From Cache x4 (6BH)

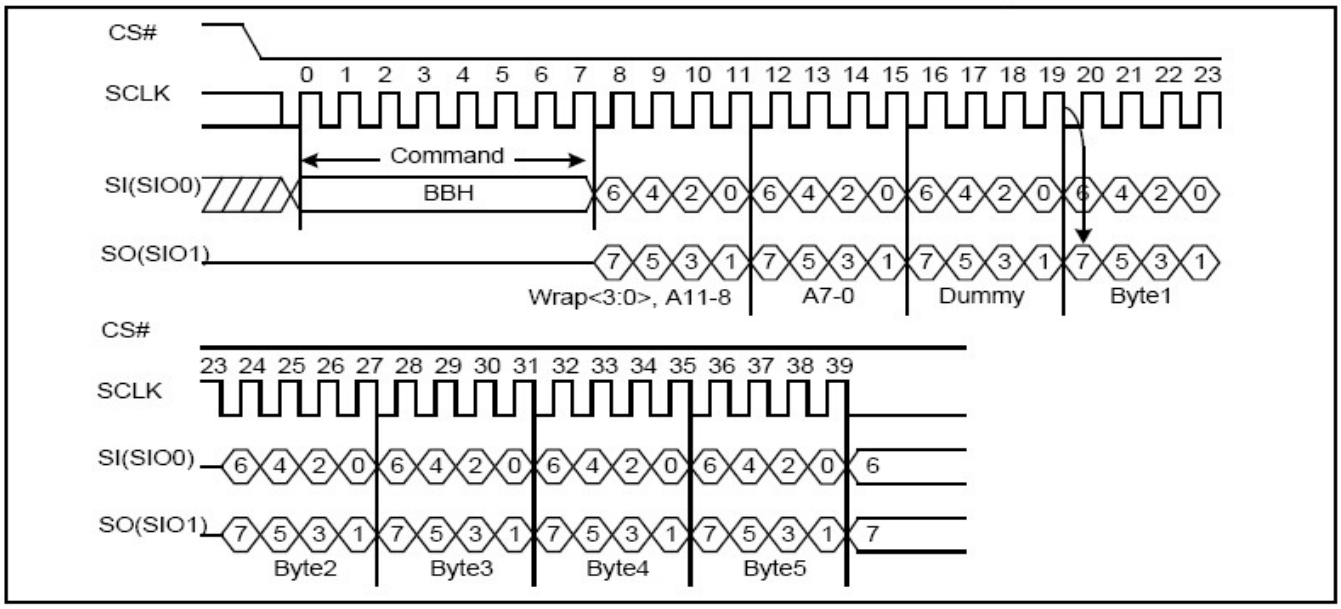
QE must be set to 1 before using the Read From cache x4 command.



Read From Cache x4 Sequence Diagram

12.6 Read From Cache Dual IO (BBH)

The Read From Cache Dual I/O command (BBH) is similar to the Read form Cache x2 command (3BH) except that the address field (WRAP<;3:0>;A11-0) use SIO0.SIO1 for transmission.

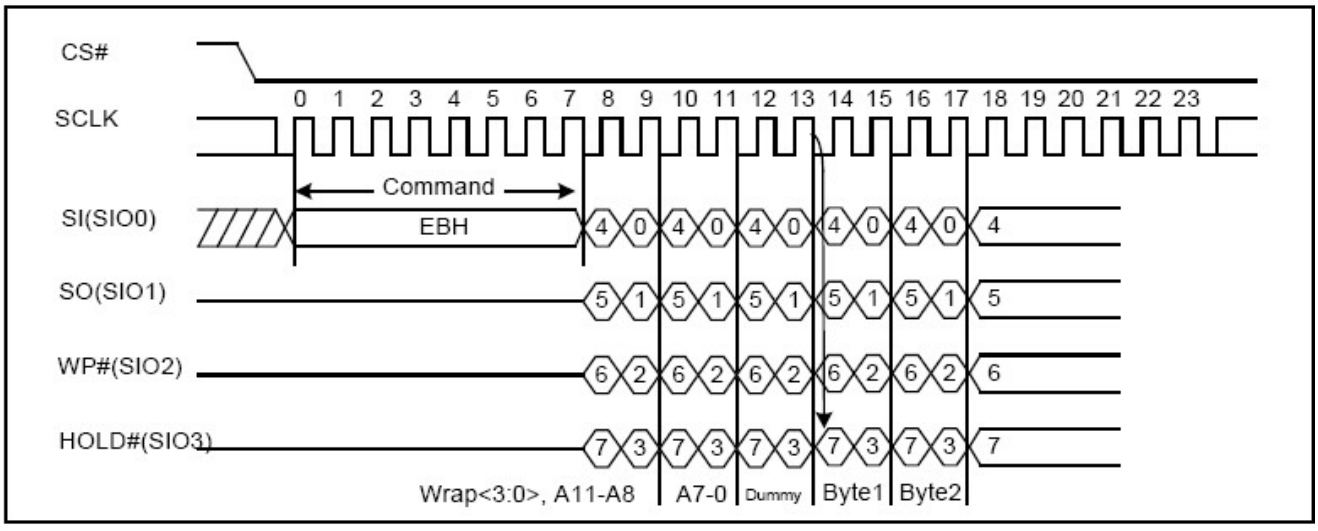


Read From Cache Dual IO Sequence Diagram

12.7 Read From Cache Quad IO (EBH)

The Read From Cache Quad IO Dual I/O command (EBH) is similar to the Read form Cache X4 command (6BH). Before running this command, you must set QE to 1. The difference is in the address field (WRAP< 3:0>; A11-0) use SIO0, SIO1, SIO2 and SIO3 for transmission.

Read From Cache Quad IO Sequence Diagram



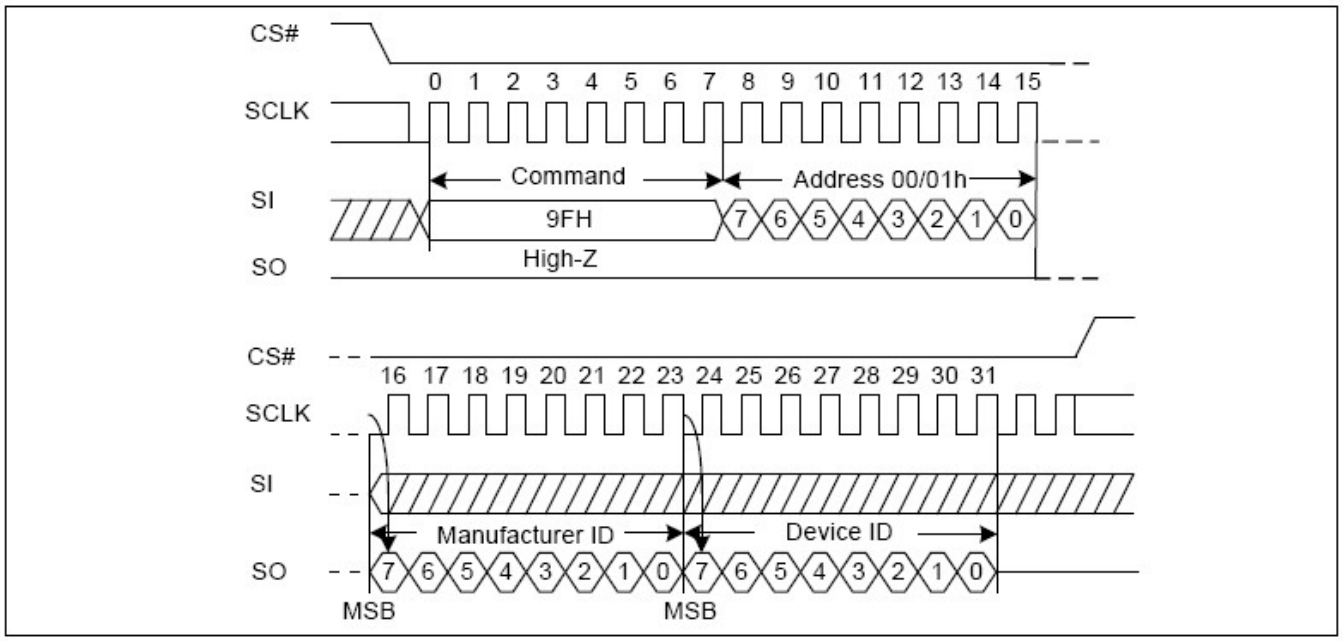
Read From Cache Quad IO Sequence Diagram

12.8 Read ID (9FH)

The READ ID command is used to identify the NAND Flash device.

• With address 00H~01H,the READ ID command outputs the Manufacturer ID and the device ID.

Read ID Sequence Diagram



Read ID Table

Address	Value	Description
Byte 0	8CH	Manufacture XINCUN
Byte 1	01H	Device ID (SPI NAND 1Gbit 3.3V)

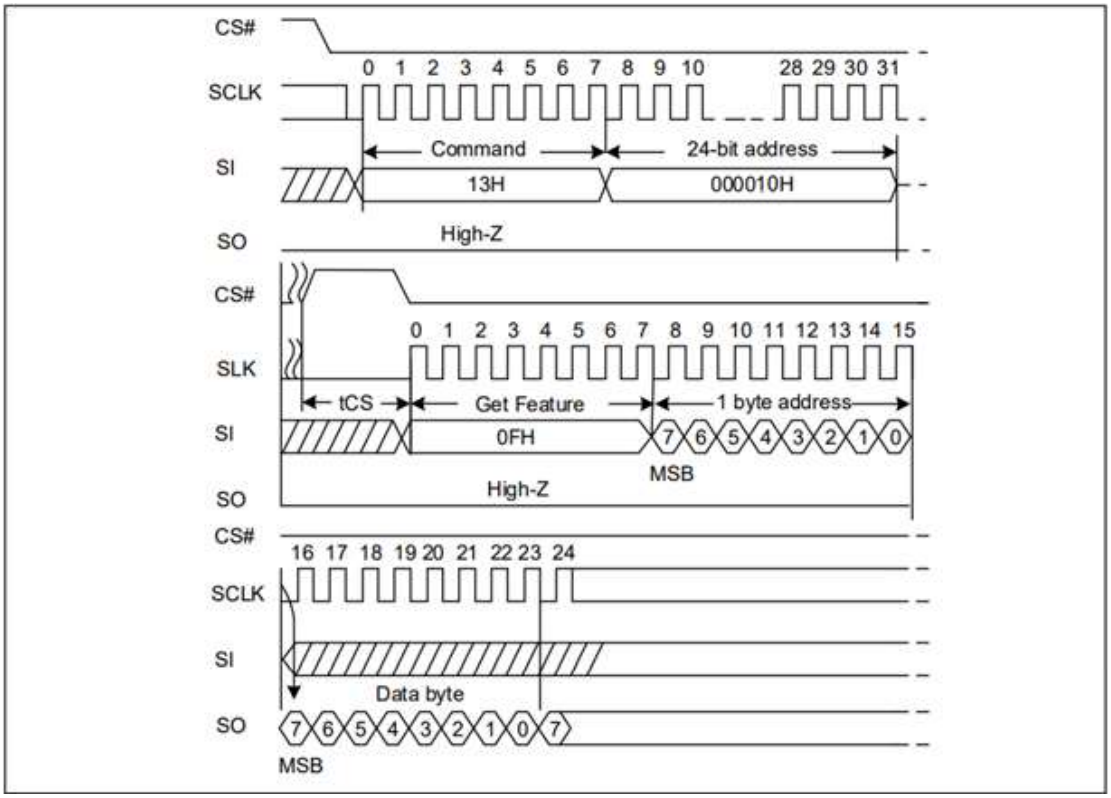
12.9 Read UID (03/0BH)

The read UID function is used to retrieve the unique 16-byte ID of the device. This UID will have a unique relationship with the device manufacturer. The UID data can be stored in the Flash array. In order for the host to check whether there is a UID error, the UID and complement are returned. If both UID and complement are 1 when XOR is used, the UID content is valid. To avoid errors during storage, the second UID and complement are stored at 32-63byte.

Bytes	Value
0 - 15	UID
16 - 31	UID Complement (bit-wise)

Reading a UID from the SPI NAND Flash requires five steps:

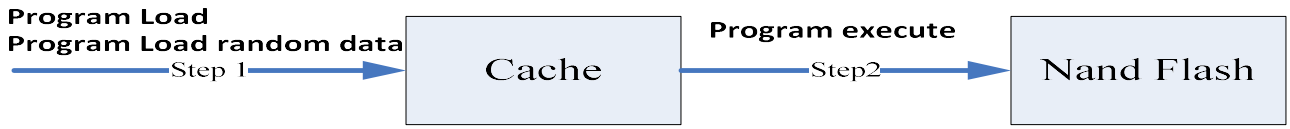
1. Run the Set Feature command to Set register B0 to Set OTP_EN=1.
2. Run the Get Feature command to obtain data from the B0 register and check whether OTP_EN is enabled.
3. Run the Page Read to Cache (13h) command to Read IP address 10H and move the data from the storage array to the Cache.
4. Run the Get Feature command to check whether the read function is complete.
5. Run the Read from cache (03H/0BH) command to Read the UID result from the cache.



Read UID to cache and Get Feature command Timing Diagram

13 PROGRAM OPERATIONS

13.1 Page Program



Page Program Operations Diagram

Writing data to SPI NAND Flash requires four steps:

1. Run the PROGRAM LOAD (02H/32H) command or PROGRAM LOAD RANDOM DATA (84H/C4H/ 34H/72H) command to LOAD the DATA pages to the Cache.

2. WRITE ENABLE (06H)

3. Run the PROGRAM EXECUTE (10H) command to PROGRAM the data page to NAND FLASH.

4. Run the GET FEATURES (0FH) command to query the status register (C0H), wait until the programming is complete (OIP=0), and check P_FAIL to determine whether data programming is successful (P_FAIL= 0 indicates that the programming is successful).According to different application programming requirements, the specific command set and sequence are as follows:

Program Load &Page Program

PROGRAM LOAD is used to PROGRAM 1-2176byte data into the NAND FLASH page. The following is the implementation process of the combined command:

02H (PROGRAM LOAD) /32H (PROGRAM LOAD X4)

06H (WRITE ENABLE)

10H (PROGRAM EXECUTE)

0FH (GET FEATURE)

The address field of the PROGRAM LOAD (02H/32H) command contains 4-bit dummy bits and 12-bit column addresses. Use this command to LOAD data into the cache. If the transmitted data is greater than 2176, the excess data will be ignored. ENABLE WRITE (WEL=1) by using the WRITE ENABLE command (06H). If WEL= 0, subsequent programming operations will be ignored and P_FAIL=0. Next, the PROGRAM EXECUTE command (10H) is used to write the cached data into the corresponding area of NAND FLASH, and GET FEATURE (0FH) is used to query the programming result. OIP = 0 indicates that the programming is finished, P_FAIL= 0 indicates that the programming is successful. If P_FAIL=1, the programming fails. For the cause of the failure, refer to the description of P_FAIL in the status register. Parameter Description MODE.TXT Indicates

Internal Data Move &Page Program

PROGRAM LOAD RANDOM DATA is used to change some or all DATA in the cache. Similar to the NAND FLASH "Copy back" operation, the PROGRAM LOAD RANDOM DATA combination command sequence is as follows:

13H (PAGE READ to cache)

84H/C4H/ 34H (PROGRAM LOAD RANDOM DATA)

84H/C4H/ 34H (PROGRAM LOAD RANDOM DATA)

...

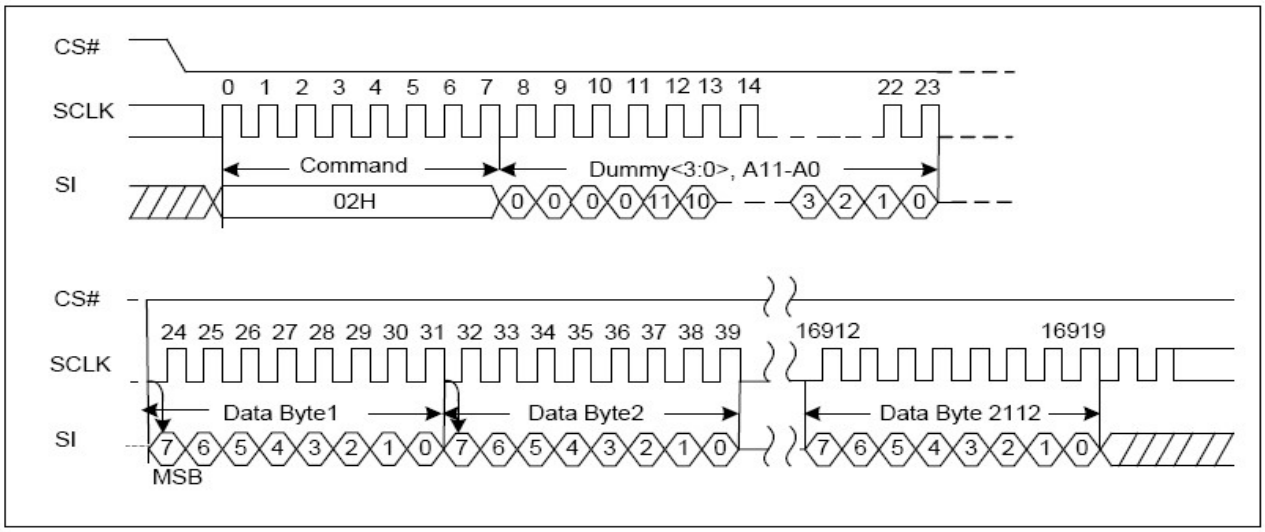
06H (WRITE ENABLE)

10H (PROGRAM EXECUTE)

0FH (GET FEATURE)

13.2 Program Load (PL) (02H)

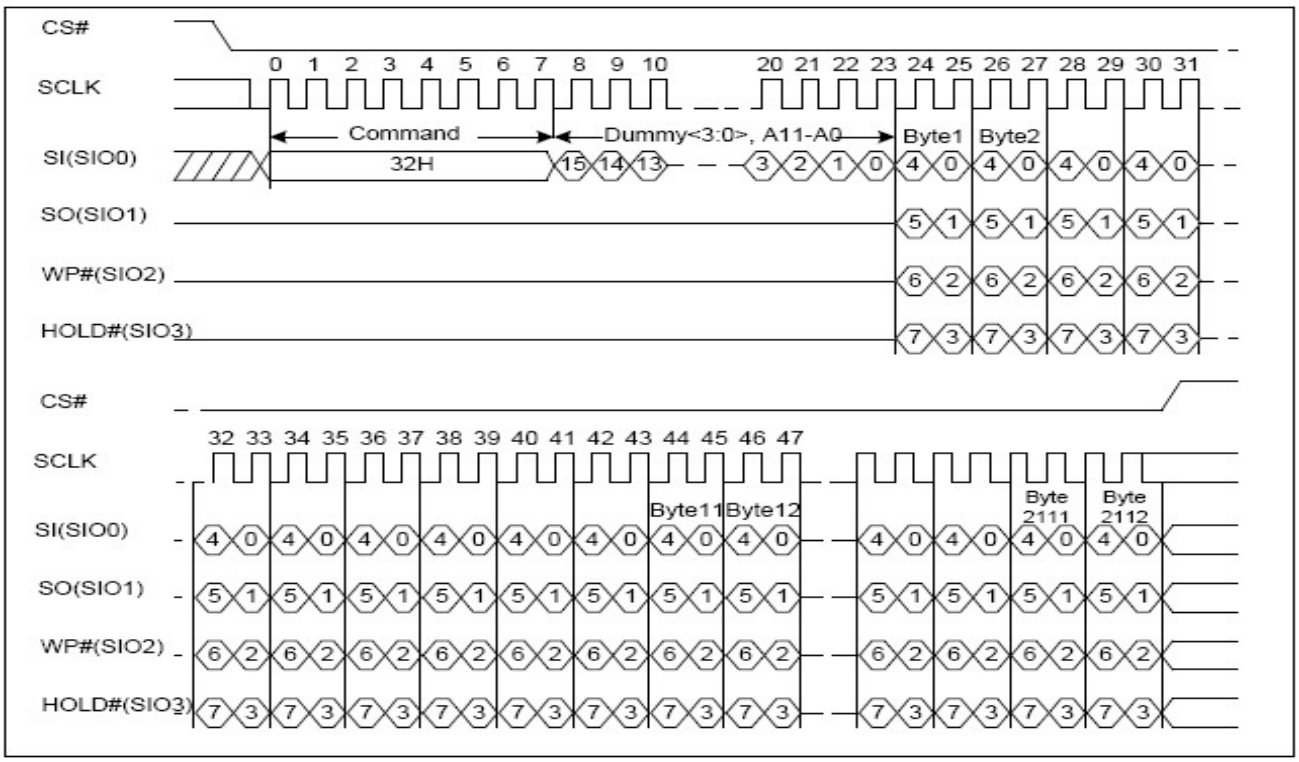
The address field in the PROGRAM LOAD (02H) command contains a 4bit Dummy plus a 12-bit column address. 12-bit column address Locates the start address of the write cache. Input data greater than 2176 will be ignored. Do not raise CS# during data transfer. Otherwise, the operation will be forcibly terminated.



Program Load Sequence Diagram

13.3 Program Load ×4 (PL×4) (32H)

The address field in the PROGRAM LOAD x4 (32H) command contains a 4bit Dummy plus a 12-bit column address. 12-bit column address Locates the start address of the write cache. You must set QE to 1 before using the Program Load x4 command. Input data greater than 2176 will be ignored. C # must not be raised during writing, otherwise the operation will be forced to terminate.

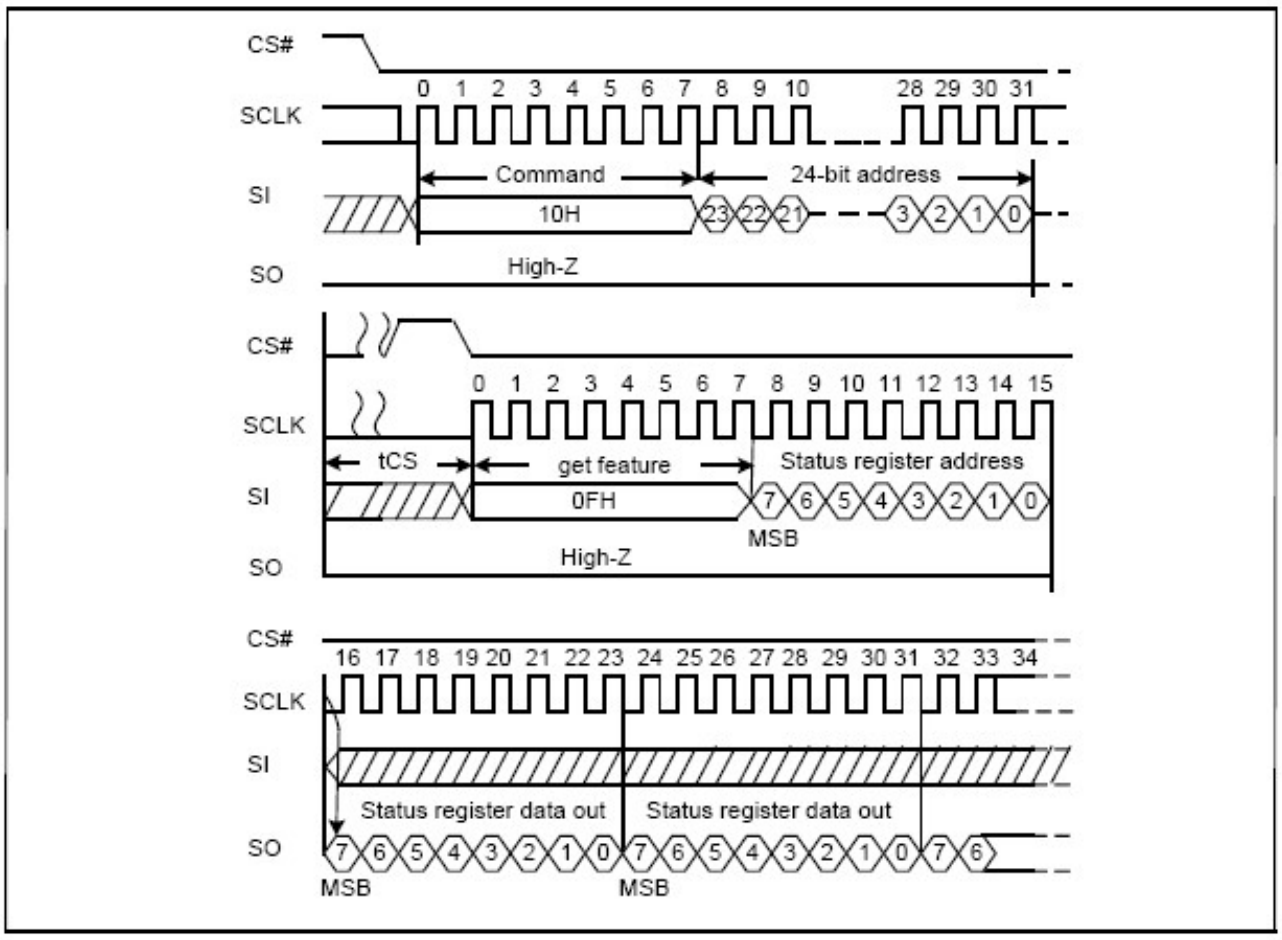


Program Load x4 Sequence Diagram

13.4 Program Execute (PE) (10H)

PROGRAM EXECUTE (10H) is used to PROGRAM cached data into NAND FLASH. The address field must be 24-bit. The length of the Page/Block address varies with Flash specifications. For details, see Figure 2-3 and Figure 2-4 for RA address descriptions. After the address is successfully addressed, the cached data initiates programming, and tPROG indicates the programming time. During the programming process, you can use the GET FEATURE (0FH) command to query the OIP bit (OIP=0 indicates that the programming is complete).

Before running the PROGRAM EXECUTE (10H) command, Load Data to the cache. You can Load Data to the cache in two ways: PROGRAM Load or PROGRAM Load Random Data.



13.5 Internal Data Move

The INTERNAL DATA MOVE command sequence programs or replaces data in a page with existing data. The INTERNAL DATA MOVE command sequence is as follows:

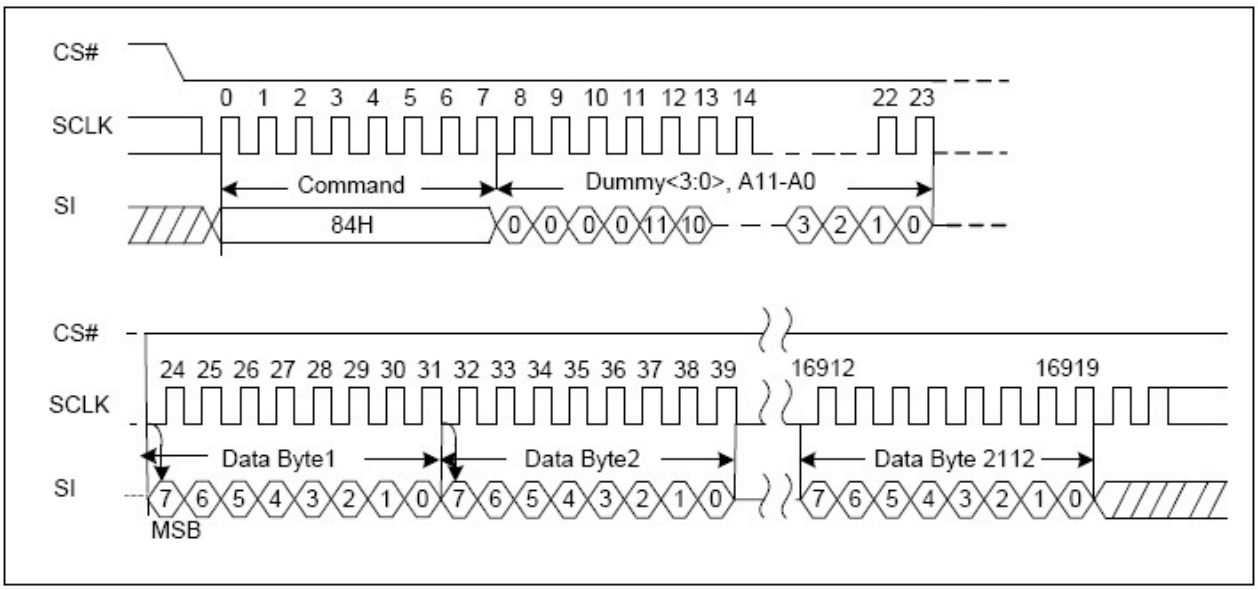
- 13H (PAGE READ to cache)
- Optional 84H/C4H/34H(PROGRAM LOAD RANDOM DATA)
- 06H (WRITE ENABLE)
- 10H (PROGRAM EXECUTE)
- 0FH (GET FEATURE command to read the status)

Prior to performing an internal data move operation, the target page content must be read out into the cache register by issuing a PAGE READ (13H) command. The PROGRAM LOAD RANDOM DATA (84H/C4H/72H) command can be issued, if user wants to update bytes of data in the page.

New data is loaded in the 12-bit column address. If the random data is not sequential, another PROGRAM LOAD RANDOM DATA (84H/C4H/34H/72H) command must be issued with the new column address. After the data is loaded, the WRITE ENABLE command must be issued, and then a PROGRAM EXECUTE (10H) command can be issued to start the programming operation.

13.6 Program Load Random Data (84H)

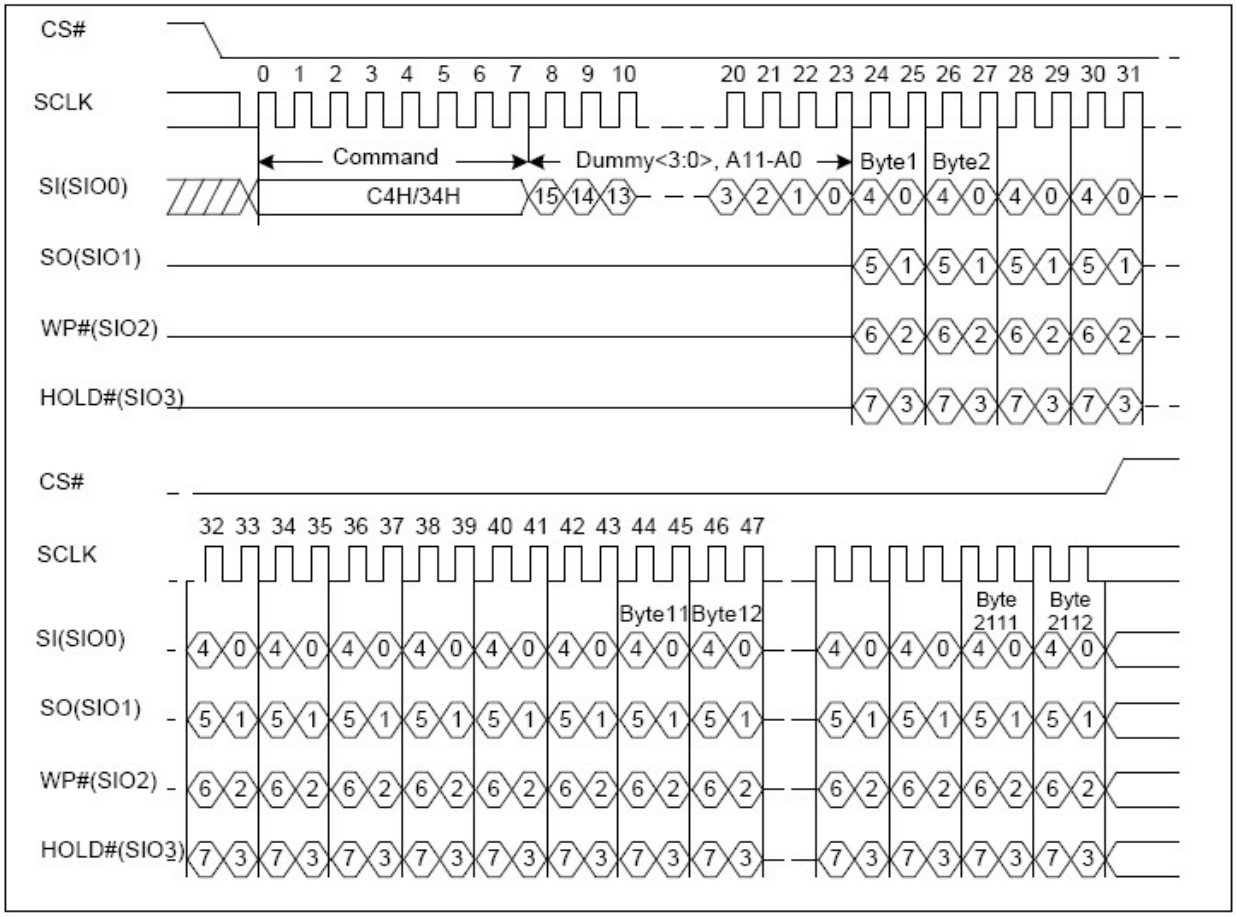
The PROGRAM LOAD RANDOM DATA (84H) command field contains a 4bit Dummy plus a 12-bit column address. 12-bit column address Locates the start address of the write cache. Input data greater than 2176 will be ignored. Do not raise CS# during data transfer. Otherwise, the operation will be forcibly terminated.



Program Load Random Data Sequence Diagram

13.7 Program Load Random Data x4 (C4H/34H)

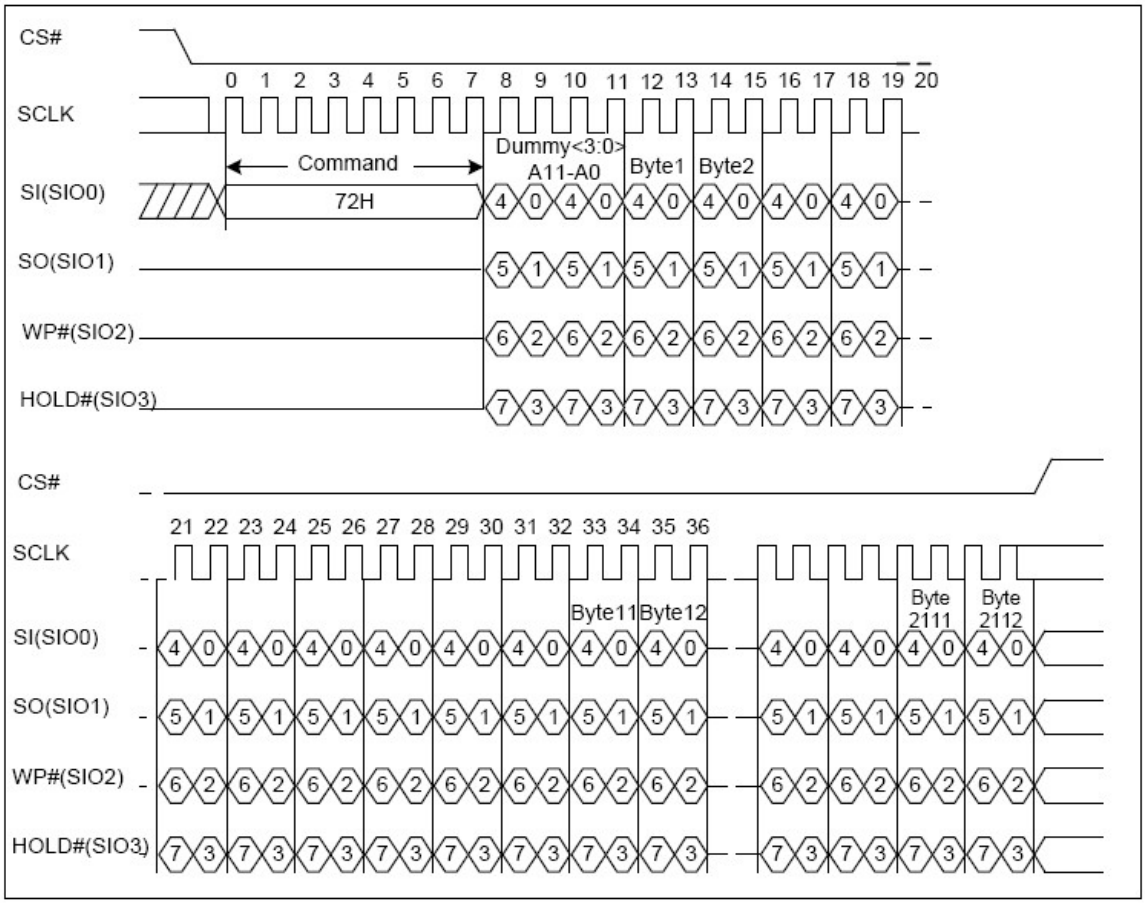
The PROGRAM LOAD RANDOM DATA X4 (C4H/34H) command field contains a 4bit Dummy plus a 12-bit column address. 12-bit column address Locates the start address of the write cache. Input data greater than 2176 will be ignored. Do not raise CS# during data transfer. Otherwise, the operation will be forcibly terminated. QE must be set to 1 before running the PROGRAM LOAD RANDOM DATA X4 (C4H/34H) command.



Program Load Random Data x4 Sequence Diagram

13.8 Program Load Random Data Quad IO (72H)

The Program Load Random Data Quad IO command (EBH) is similar to the Program Load Random Data X4 (C4H/34H) command. Before running this command, you must set QE to 1. The difference is in the address field (Dummy< 3:0> A11-0) use SIO0, SIO1, SIO2 and SIO3 for transmission. Input data greater than 2176 will be ignored. Do not raise CS# during data transfer. Otherwise, the operation will be forcibly terminated.



Program Load Random Data Quad IO Sequence Diagram

14 ERASE OPERATIONS

The BLOCK ERASE (D8H) command erases NAND FLASH blocks. The address field of the BLOCK ERASE (D8H) command contains 24-bit bits. The length of the Page/ BLOCK address varies according to FLASH specifications. After the address is successfully addressed, the erasing is started. TERS indicates the R/B time of erasing. During the erasing process, you can use GET FEATURE (0FH command) to query the OIP bit to monitor the erasing result. For the cause of the failure, see E_FAIL in the status register.

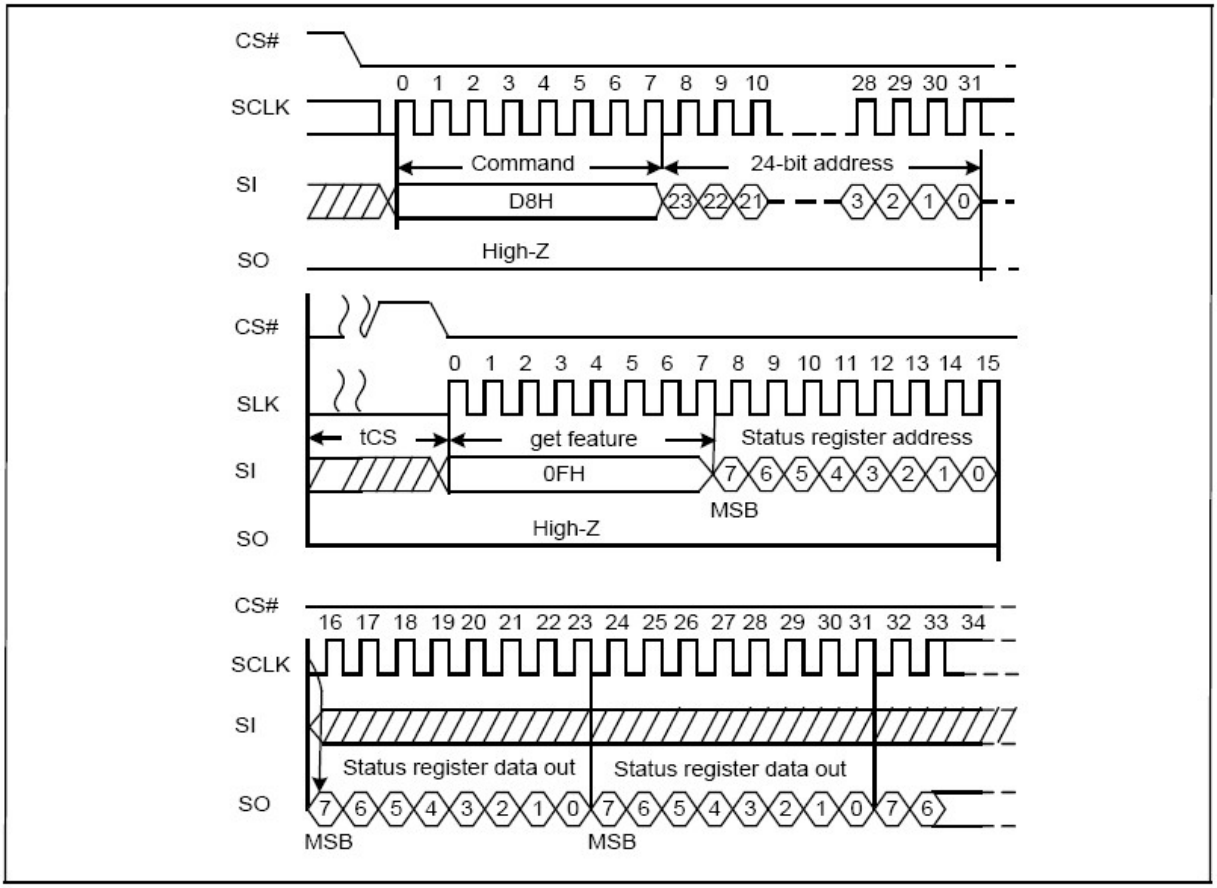
During the execution of BLOCK ERASE (D8H) (OIP = 1), you can run the Read From Cache command (03H/0BH/3BH/6BH/BBH/EBH) to Read the Cache. Alternatively, run the PROGRAM LOAD command (02H/32H/84H/C4H/ 34H/72H) to write data to the Cache.

The command set and sequence are as follows:

06H (WRITE ENABLE)

D8H (BLOCK ERASE)

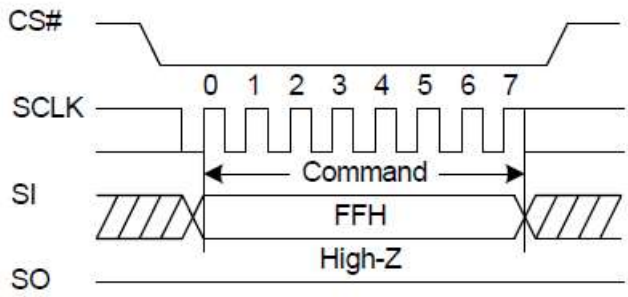
0FH (GET FEATURE)



Block EraseSequence Diagram

15 RESET OPERATIONS

ResetSequence Diagram



The RESET (FFH) command stops all operations. For example, in case of a program or erase or read operation, the reset command can make the device enter the wait state.

During a cache program or cache read, a reset can also stops the previous operation and the pending operation. The OIP status can be read from 300ns after the reset command is sent.

16 ADVANCED FEATURES

16.1 OTP Region

SPI NAND FLASH provides a special OTP area that can only be programmed once. The size of OTP is 4 pages, 2176bytes per page. Users can use this area freely, such as recording serial numbers and placing backup data tables.

register	address	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Feature	B0H	OTP_PRT	OTP_EN	keep	ECC_EN	keep	keep	keep	QE
-	-	Themem ory loss	Read /write	-	Read /write	-	-	-	Read/ write

OTP_PRT = 0 in the factory, users need to use the SET FEATURES command to SET the OTP_EN bit of Feature register when using OTP. Pages 00~03 can be programmed using PROGRAM LOAD (02H/32H) or PROGRAM RANDOM (84H/C4H/34H/72H) plus PROGRAM EXECUTE (10H). PAGE READ (13H) plus READ FROM CACHE (03H/0BH/3BH/6BH/BBH/EBH) can also be used to READ data. To lock the OTP area, run the SET FEATURES command to SET the OTP_EN and OTP_PRT bits of the Feature register, and then run the PROGRAM EXECUTE (10H) command to complete the locking.

OTP_PRT	OTP_EN	State
x	0	Normal operation
0	1	Accessing the OTP region (read, program) Note: OTP_PRT = 0 indicates that the OTP is unlocked. OTP can be programmed more than once, but OTP pages that have already been programmed cannot be programmed more than once, otherwise the result is unknown.
1	1	1. If OTP_PRT = 0 after the SPI NAND is powered on, the user can set OTP_PRT =1,OTP_EN =1, and lock the OTP with PROGRAM_EXECUTE (10H). OTP_PRT is always 1 (no matter the power failure or not). 2. If OTP_PRT = 1 after SPI NAND is powered on, the user can only read the OTP area.

16.2 Access to OTP data

command SET FEATURES (1FH)

Register address B0H

Set the OTP_EN bit

After entering OTP mode, use the command PAGE READ (13H)

Reads data FROM the CACHE using the READ FROM CACHE command (03H/0BH/3BH/6BH/BBH/EBH).

Write data to OTP (only if OTP_PRT=0)

Enter OTP mode

Command WRITE ENABLE (06H)

The command PROGRAM LOAD (02H/32H) or PROGRAM RANDOM (84H/C4H/34H/72H) writes data to the cache command PROGRAM EXECUTE (10H)

The GET FEATURES (0FH) command queries whether is completed (OIP = 0 completed, P_FAIL = 0 successful) Repeat Step 2 and subsequent steps to change the OTP page address

16.3 Protect OTP region

The command SET FEATURES (1FH) sets OTP_EN and OTP_PRT

Command WRITE ENABLE (06H)

command PROGRAM EXECUTE (10H)

After the OTP region is locked, the OTP_PRT bit is permanently placed. After that, the OTP region cannot be erased or reprogrammed.

16.4 Block Protection

register	address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Protection	A0H	BRWD	keep	BP2	BP1	BP0	INV	CMP	keep
—	—	Read /write	—	Read /write	Read /write	Read /write	Read /write	Read /write	Read /write

Access or configure the Protection register using GET FEATURES (0FH) and SET FEATURES (1FH).

SPI NAND provides block write protection for the whole or part of the block area, and all blocks are written protected by default (BP2, BP1, BP0 = 1) after power-on.

BRWD = 1 and WP# is low, all protected state bits cannot be modified by the SET FEATURES (1FH) command.

PROGRAM/ERASE command addressing in a protected area causes an action error (P_FAIL= 1/EFAIL= 1).

Write protected bits (BP0, BP1, BP2, INV, CMP) range of write protected addresses in different capacities (for example, 64 pages per block Flash), as shown in Table

Block Lock Register Block Protect Bits(64 pages per block)

CMP	INV	BP2	BP1	BP0	Protect page Address （1024 Blocks）	Protect page Address （2048 Blocks）	Protect page Address （4096 Blocks）	Protect Rows
X	X	0	0	0	None	None	None	UNLOCK
X	X	1	1	1	0000H-FFFFH	00000H-1FFFFH	0000H-3FFFFH	LOCK
0	0	0	0	1	FC00H-FFFFH	1F800H-1FFFFH	3F000H-3FFFFH	H 1/64
0	0	0	1	0	F800H-FFFFH	1F000H-1FFFFH	3E000H-3FFFFH	H 1/32
0	0	0	1	1	F000H-FFFFH	1E000H-1FFFFH	3C000H-3FFFFH	H 1/16
0	0	1	0	0	E000H-FFFFH	1C000H-1FFFFH	38000H-3FFFFH	H 1/8
0	0	1	0	1	C000H-FFFFH	18000H-1FFFFH	30000H-3FFFFH	H 1/4
0	0	1	1	0	8000H-FFFFH	10000H-1FFFFH	20000H-3FFFFH	H 1/2
0	1	0	0	1	0000H-03FFH	0000H-07FFH	0000H-0FFFH	L 1/64
0	1	0	1	0	0000H-07FFH	0000H-0FFFH	0000H-1FFFH	L 1/32
0	1	0	1	1	0000H-0FFFH	0000H-1FFFH	0000H-3FFFH	L 1/16
0	1	1	0	0	0000H-1FFFH	0000H-3FFFH	0000H-7FFFH	L 1/8
0	1	1	0	1	0000H-3FFFH	0000H-7FFFH	0000H-FFFFH	L 1/4
0	1	1	1	0	0000H-7FFFH	0000H-FFFFH	0000H-1FFFFH	L 1/2
1	0	0	0	1	0000H-FBFFH	0000H-1F7FFH	0000H-3FFFH	L 63/64
1	0	0	1	0	0000H-F7FFH	0000H-1EFFFH	0000H-3DFFFH	L 31/32
1	0	0	1	1	0000H-EFFFH	0000H-1DFFFH	0000H-3BFFFH	L 15/16

CMP	INV	BP2	BP1	BP0	Protect page Address （1024 Blocks）	Protect page Address （2048 Blocks）	Protect page Address （4096 Blocks）	Protect Rows
1	0	1	0	0	0000H-DFFFH	0000H-1BFFFH	0000H-37FFFH	L 7/8
1	0	1	0	1	0000H-BFFFH	0000H-17FFFH	0000H-2FFFFH	L 3/4
1	0	1	1	0	0000H~003FH	0000H~003FH	0000H~0003FH	Block0
0	1	0	0	1	0400H-FFFFH	0800H-1FFFFH	1000H-3FFFFH	H 63/64
0	1	0	1	0	0800H-FFFFH	1000H-1FFFFH	2000H-3FFFFH	H 31/32
0	1	0	1	1	1000H-FFFFH	2000H-1FFFFH	4000H-3FFFFH	H 15/16
0	1	1	0	0	2000H-FFFFH	4000H-1FFFFH	8000H-3FFFFH	H 7/8
0	1	1	0	1	4000H-FFFFH	8000H-1FFFFH	10000H-3FFFFH	H 3/4
0	1	1	1	0	0000H~003FH	0000H~003FH	00000H~0003FH	Block0

16.5 block 0, page 0 is automatically loaded into the cache

To be compatible with booting from the SPI interface, SPI NAND automatically loads block 0, page 0 data into the cache and performs ECC correction upon power-on. The READ FROM CACHE (03H/0BH/3BH/6BH/BBH/EBH) command can be used to READ data FROM the CACHE.

In order to be compatible with some systems the host uses the "soft shutdown" function (SPI NAND has not been powered off). The host will boot the code from block 0, page 0 again after soft boot. SPI NAND FLASH will also load block 0, page 0 data into cache after receiving reset command and perform ECC correction (optional function).

17 Status Register

SPI NAND FLASH has 8-bit status registers to indicate internal operation status, such as ECC error correction result (ECCS1,ECCS0), programming operation result (P_FAIL), operation end (OIP), etc.

The status register value can be obtained by running the GET FEATURES (0FH) + address (C0H) command.

The Status register

register	address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Status	C0H	keep	keep	ECCS1	ECCS0	P_FAIL	E_FAIL	WEL	OIP
—	—	—	—	Read-only	Read-only	Read-only	Read-only	Read-only	Read-only

Description of the status register

Bit	Bit Name	Description
P_FAIL	The programming results	P_FAIL = 0: The programming is OK P_FAIL = 1: The programming fails Note: P_FAIL = 1 May occur under the following conditions: □Programming address out of range □Program the OTP area to be locked and protected Programming protected regions (BP0, BP1, BP2, INV, CMP) □Note: Conditions for clearing 0: □This bit clears 0 after the next programming

Bit	Bit Name	Description
		command is received □This bit clears 0 after receiving the reset command (FFH).
E_FAIL	Erase the results	E_FAIL = 0: The erasing is OK □E_FAIL = 1: erases FAIL □Note: E_FAIL = 1 May occur under the following conditions: □The erasing address is out of range The OTP region is erased Erase protected regions (BP0, BP1, BP2, INV, CMP) Note: Conditions for clearing 0: This bit clears 0 after the next erase command is received This bit clears 0 after receiving the reset command (FFH)
WEL	Write Enable Latch	This bit reflects the result of the WRITE_ENABLE (WEL = 1), WRITE_DISABLE, (WEL = 0) commands □Before using command PROGRAM_EXECUTE (10H) and BLOCK_RASE (D8H), ensure (WEL = 1), otherwise command execution is invalid
OIP	Operation In Progress	When executing PAGE_READ (13H),PROGRAM_EXECUTE (10H), and BLOCK_RASE (D8H), OIP indicates whether the operation is complete. When the RESET (FFH) command is executed after the device is powered on, OIP indicates whether the internal initialization is complete. When the RESET (FFH) command is executed, the OIP indicates whether the interruption is complete Note: OIP = 0 indicates completion, and OIP = 1 indicates execution.
ECCS1,ECSS0	ECC Status	00: indicates that PAGE_READ (13H) executes without error found 01: indicates that an error is found. The error can be corrected. The error is 1 to 4 bits 10: Errors are found, but errors cannot be corrected 11: Errors are found and can be corrected. The error is 5 to 8 bits Note: The condition of being cleared 0 This bit clears 0 the next time it receives the PAGE_READ (13H) command, During power-on reset, this bit reflects the result of block0 and page0 loading. (Reset command (FFH) and power-on will automatically load block0,page0 to cache)

18 Error Management

This NAND Flash device is specified to have the minimum number of valid blocks (NVB) of the total available blocks per die shown in the table below. This means the devices may have blocks that are invalid when shipped from the factory. An invalid block is one that contains at least one page that has more bad bits than can be corrected by the minimum required ECC. Additional bad blocks may develop with use. However, the total number of available blocks will not fall below NVB during the endurance life of the product.

Although NAND Flash memory devices may contain bad blocks, they can be used reliably in systems that provide bad-block management and error-correction algorithms. This ensures data integrity.

Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the NAND Flash array.

NAND Flash devices are shipped from the factory erased. The factory identifies invalid blocks before shipping

by programming the Bad Block Mark (00h) to the first spare area location in each bad block. This method is compliant with ONFI Factory Defect Mapping requirements. See the following table for the bad-block mark.

System software should initially check the first spare area location for non-FFh data on the first page of each block prior to performing any program or erase operations on the NAND Flash device. A bad-block table can then be created, enabling system software to map around these areas. Factory testing is performed under worst-case conditions. Because invalid blocks may be marginal, it may not be possible to recover the bad-block marking if the block is erased.

Error Management Details

Description	Requirement
Minmum number of valid blocks (NVB)	1004
Total available blocks per die	1024
First spare area location	Non FFh

19 Internal ECC

SPI NAND FLASH provides the data error correction protection (ECC) mechanism, which can be enabled by the ECC_EN bit. By default, the ECC_EN is enabled after power-on reset (ECC_EN = 1). Perform the following operations to enable or disable ECC_EN.

using SET FEATURES (1FH)

Enabling ECC: ECC_EN=1, disabling ECC: ECC_EN=0

After ECC is enabled, 2K data in cache is first encoded by BCH and then programmed to NAND FLASH during PROGRAM operation. In the READ operation, the 2K data READ from NAND FLASH is decoded by BCH first, and then stored in cache, and the decoded result is reflected in ECCS1 and ECCS0. ECCS0 =0 for erased but unprogrammed pages regardless of ECC_EN =0/1 when ECCS1 is read. For Flash Flash with Page size of 2176 bytes and 2176 bytes, the ECC has different protection domains for data areas, as shown in Table。

ECC Protection and Spare Area（2176 bytes per page） （version1）

Min Byte Address	MaxByte Address	ECC Protected	Area	Size	Description
000H	1FFH	Yes	Main0	512	User data 0
200H	3FFH	Yes	Main1	512	User data 1
400H	5FFH	Yes	Main2	512	User data 2
600H	7FFH	Yes	Main3	512	User data 3
800H	832H	Yes	OOB	51	User Meta (800H is also for bad block mark)
833H	83FH	Yes	ECC for OOB	13	ECC for OOB
840H	87FH	Yes	Internal ECC	64	ECC for main(0~3) (Not visible to the outside, not accessible)

Note:

1. When ECC is enabled, data written to the ECC for OOB area is ignored
2. No matter whether ECC is enabled or not, the Internal ECC area is invisible and inaccessible

ECC Protection and Spare Area（2176 bytes per page） （version2）

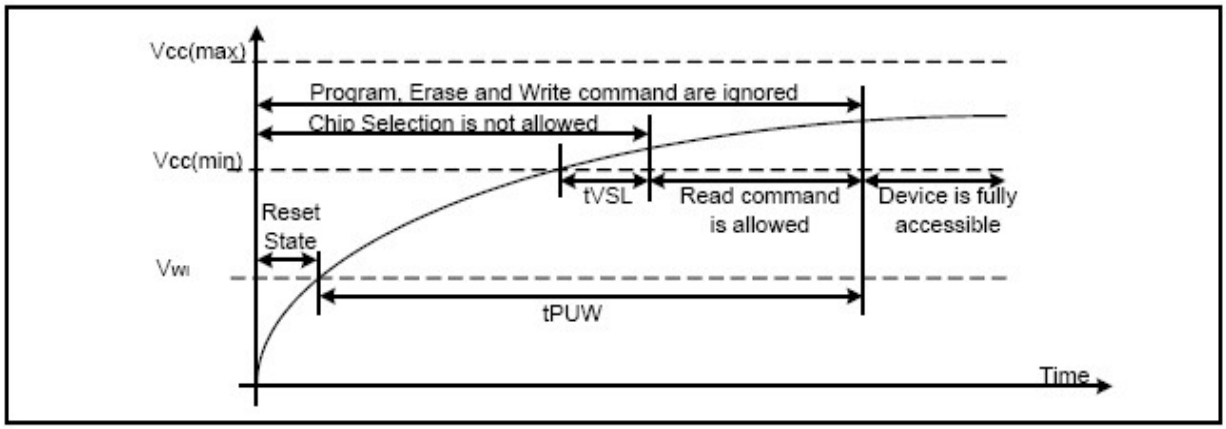
Min Byte Address	MaxByte Address	ECC Protected	Area	Size	Description
000H	1FFH	Yes	Main0	512	User data 0
200H	3FFH	Yes	Main1	512	User data 1
400H	5FFH	Yes	Main2	512	User data 2
600H	7FFH	Yes	Main3	512	User data 3
800H	83FH	No	OOB	64	User Meta (800H is also for bad block mark)
840H	87FH	Yes	Internal ECC	64	ECC for main(0~3) (Not visible to the outside, not accessible)

Note:

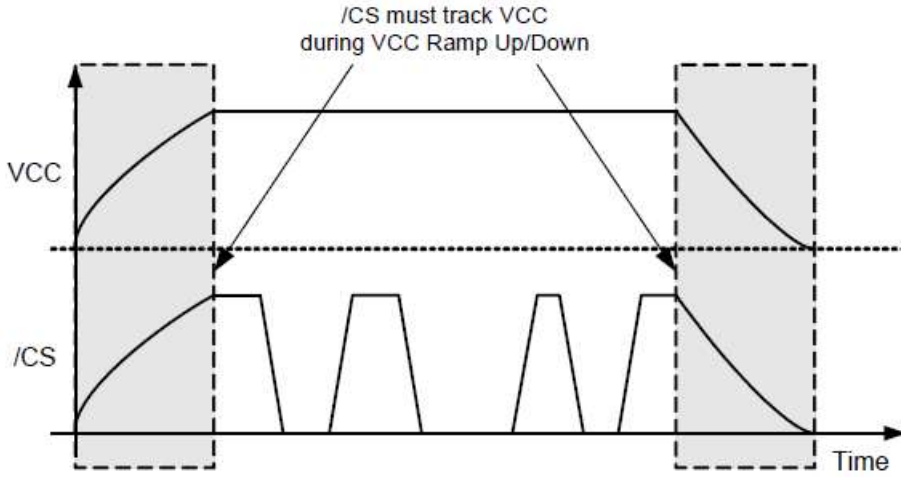
1.No matter whether ECC is enabled or not, the Internal ECC area is invisible and inaccessible

20 POWER ON TIMING

Power on Timing Sequence



Power-up, Power-Down Requirement



Power-On Timing and Write Inhibit Threshold

Symbol	Parameter	Min	Max	Unit
tVSL	VCC(min) To CS# LOW		1	ms
tPUW	Time Delay From $VCC_{(WI)}$ To Write Instruction		1	ms
VWI	Write Inhibit Voltage		2.9	V

21 ABSOLUTE MAXIMUM RATINGS

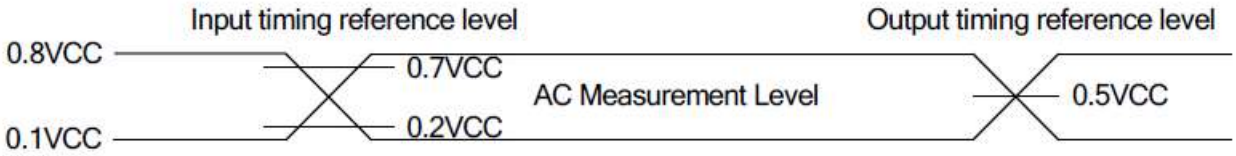
21.1 Absolute Maxmum Ratings

Parameter	Value	Unit
Operating Temperature	-40 to 85	℃
Storage Temperature	-55 to 125	℃
Applied Input/Output Voltage	-0.5 to 4.0V	V
VCC	-0.5 to 4.0V	V

21.2 CAPACITANCE MEASUREMENT CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
CIN	Input Capacitance			6	pF	
COUT	Output Capacitance			10	pF	
C_L	Load Capacitance		30		pF	
	Input Rise And Fall time			5	ns	
	Input Pulse Voltage	0.2VCC to 0.8VCC			V	
	Input Timing Reference Voltage	0.3VCC to 0.7VCC			V	
	Output Timing Reference Voltage	0.5VCC			V	

Input Test Waveform and Measurement Level



Note: Input pulse rise and fall time are<5ns

22 DC CHARACTERISTIC

(T= -40℃~85℃, VCC=1.7~2.0V/3.0~3.6V)

Symbol	Parameter	Test Condition	Min.	Typ	Max.	Unit.
VCC	Supply Voltage		3.0	3.3V	3.6	V
I_{LI}	Input Leakage Current				±2	μA
I_{LO}	Output Leakage Current				±2	μA
I_{CC1}	Standby Current	CS#=VCC, V_{IN}=VCC or VSS			90	μA
I_{CC2}	Operating Current (Read)	CLK=0.1VCC / 0.9VCC at 104MHz, Q=Open(*1,*2,*4 I/O)			30	mA
		CLK=0.1VCC / 0.9VCC at 80MHz, Q=Open(*1,*2,*4 I/O)			25	mA
I_{CC3}	Operation Current (PP)	CS#=VCC			30	mA
I_{CC4}	Operation Current (BE)	CS#=VCC			30	mA
V_{IL}	Input Low Voltage		-0.5		0.3VCC	V
V_{IH}	Input High Voltage		0.7VCC		VCC+0.3	V
V_{OL}	Output Low Voltage	I_{OL} =1.6mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} =-100μA	VCC-0.1			V

23 AC CHARACTERISTICS

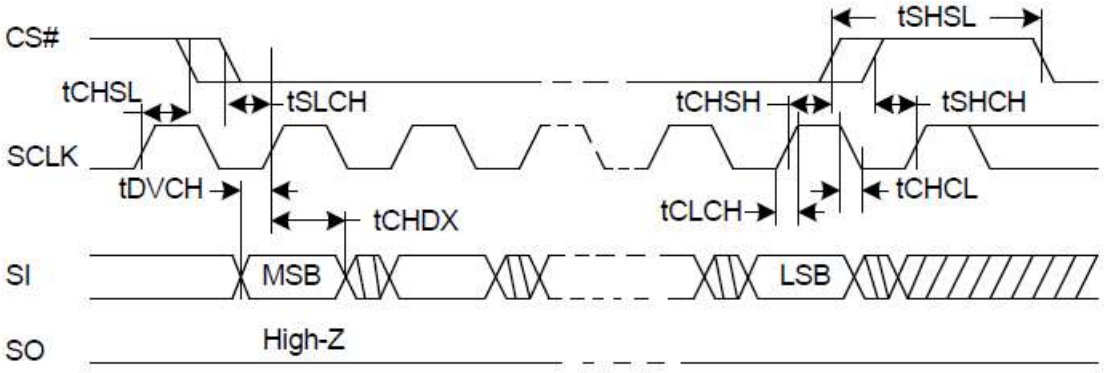
(T= -40℃~85℃, VCC=1.7~2.0V/3.0~3.6V, CL=30pf)

Symbol	Parameter	Min.	Typ.	Max.	Unit.
F_C	Serial Clock Frequency For: all command	DC.		104	MHz
t_{CH}	Serial Clock High Time	5.5			ns
t_{CL}	Serial Clock Low Time	5.5			ns
t_{CLCH}	Serial Clock Rise Time (Slew Rate)	0.5			V/ns
t_{CHCL}	Serial Clock Fall Time (Slew Rate)	0.5			V/ns
t_{SLCH}	CS# Active Setup Time	5			ns
t_{CHSH}	CS# Active Hold Time	5			ns
t_{SHCH}	CS# Not Active Setup Time	5			ns
t_{CHSL}	CS# Not Active Hold Time	5			ns
t_{SHSL}/t_{CS}	CS# High Time	20			ns
t_{SHQZ}	Output Disable Time			10	ns
t_{CLQX}	Output Hold Time	1			ns
t_{DVCH}	Data In Setup Time	3			ns
t_{CHDX}	Data In Hold Time	5			ns
t_{HLCH}	Hold# Low Setup Time (relative to Clock)	5			ns
t_{HHCH}	Hold# High Setup Time (relative to Clock)	5			ns
t_{CHHL}	Hold# High Hold Time (relative to Clock)	5.5			ns
t_{CHHH}	Hold# Low Hold Time (relative to Clock)	5.5			ns
t_{HLQZ}	Hold# Low To High-Z Output			10	ns
t_{HHQX}	Hold# High To Low-Z Output			10	ns
t_{CLQV}	Clock Low To Output Valid			9	ns
t_{WHSL}	WP# Setup Time Before CS# Low	20			ns
t_{SHWL}	WP# Hold Time After CS# High	100			ns

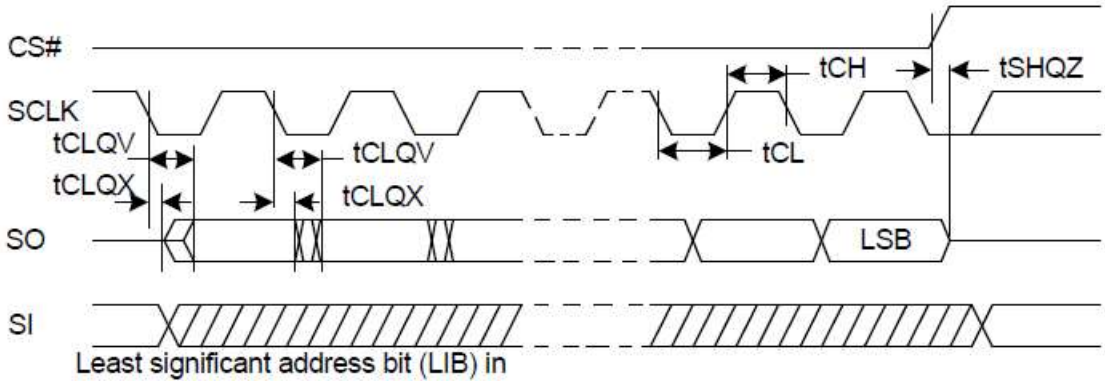
24 PERFORMANCE TIMING

Symbol	Parameter	Min.	Typ.	Max.	Unit.
T_{RST}	CS# High To Next Command After Reset(FFh)			500	μs
t_{RD}	Read From Array		250	400	μs
t_{PROG}	Page Programming Time		0.3	1	ms
t_{BERS}	Block Erase Time		2.5	5	ms

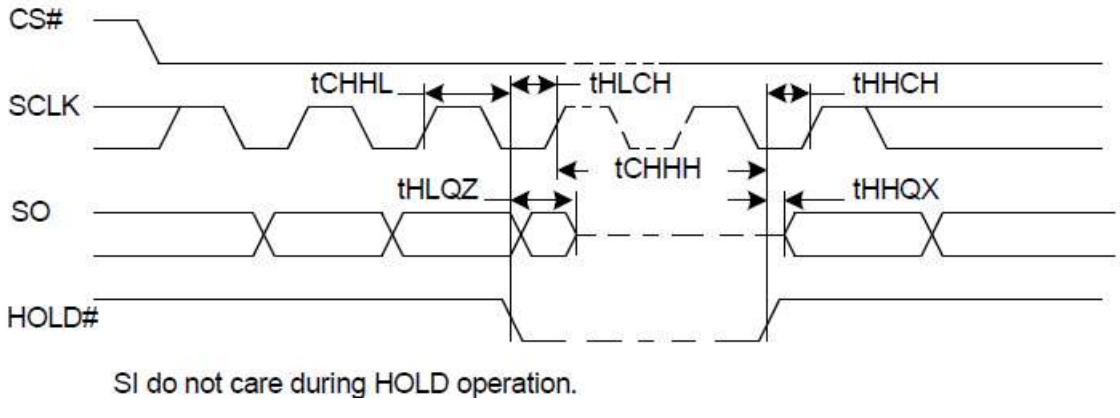
Serial Input Timing



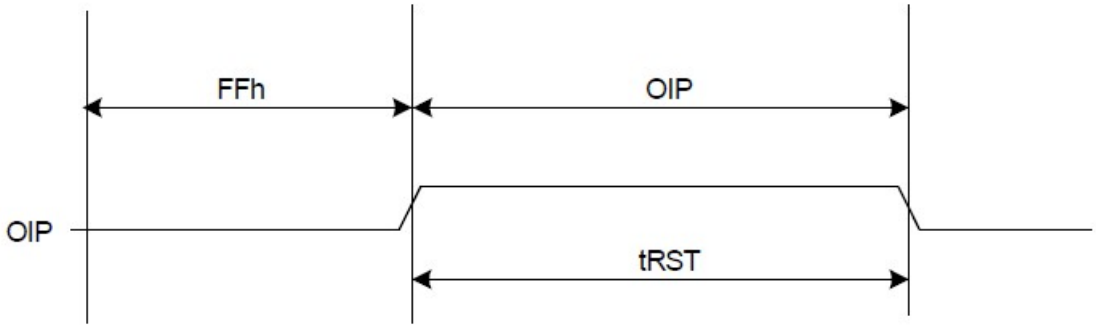
Serial Output Timing



Hold Timing



Reset Timing



Note: The maximum tRST depends on different operations.

Idle: maximum tRST = 5us;

Read: maximum tRST = 5us;

Program: maximum tRST = 10us;

Erase:maximum tRST = 500us;

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